Integrated Load Switch

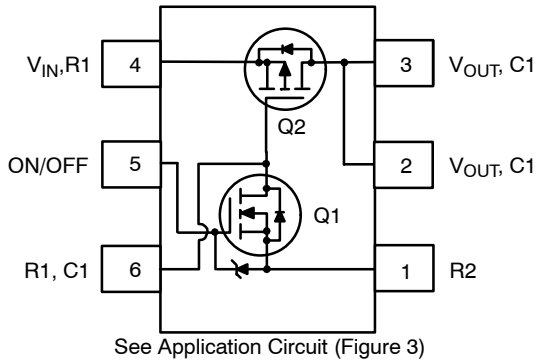
FDC6326L

Description

This device is particularly suited for compact power management in portable electronic equipment where 3 V to 20 V input and 1.8 A output current capability are needed. This load switch integrates a small N−Channel power MOSFET (Q1) which drives a large P−Channel power MOSFET (Q2) in one tiny SUPERSOT™−6 package.

Features

- V_{DROP} = 0.20 V @ V_{IN} = 12 V, I_L = 1.5 A, $R_{DS(on)}$ = 0.125 Ω
- V_{DROP} = 0.20 V @ V_{IN} = 5 V, I_L = 1 A, $R_{DS(on)}$ = 0.20 Ω
- SUPERSOT−6 Package Design Using Copper Lead Frame for Superior Thermal and Electrical Capabilities
- This is a Pb−Free and Halide Free Device



See Application Circuit (Figure 3)

Figure 1.

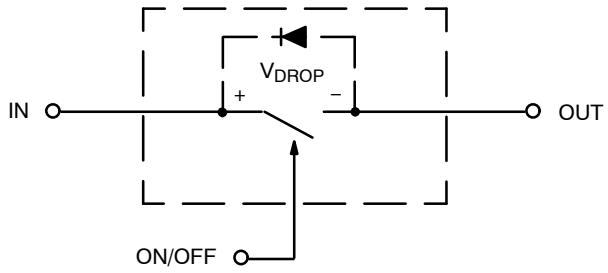


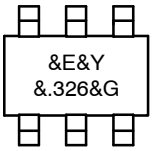
Figure 2. Equivalent Circuit

ON Semiconductor®

www.onsemi.com

TSOT−23−6
CASE 419BL

MARKING DIAGRAM



&E	= Designates Space
&Y	= Binary Calendar Year Coding Scheme
&.	= Pin One Dot
326	= Specific Device Code
&G	= Date Code

ORDERING INFORMATION

Device	Package	Shipping†
FDC6326L	TSOT−23−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

ABSOLUTE MAXIMUM RATINGS T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Unit
V_{IN}	Input Voltage Range	3–20	V
$V_{ON/OFF}$	On/Off Voltage Range	2.5–8	V
I_L	Load Current – Continuous (Note 1)	1.8	A
	Load Current – Pulsed (Note 1, Note 3)	5	
P_D	Maximum Power Dissipation (Note 2)	0.7	W
T_J, T_{STG}	Operating and Storage Temperature Range	–55 to 150	°C
ESD	Electrostatic Discharge Rating MIL–STD–883D Human Body Model (100 pF/1500 Ω)	6	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS T_A = 25°C unless otherwise noted

Symbol	Parameter	Value	Unit
$R_{\theta JA}$	Thermal Resistance, Junction–to–Ambient (Note 2)	180	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction–to–Case (Note 2)	60	°C/W

ELECTRICAL CHARACTERISTICS T_A = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
I_{FL}	Forward Leakage Current	V_{IN} = 20 V, $V_{ON/OFF}$ = 0 V	–	–	1	μA
ON CHARACTERISTICS (Note 3)						
V_{DROP}	Conduction Voltage Drop	V_{IN} = 12 V, $V_{ON/OFF}$ = 3.3 V, I_L = 1.5 A	–	0.15	0.2	V
		V_{IN} = 5 V, $V_{ON/OFF}$ = 3.3 V, I_L = 1 A	–	0.14	0.2	
$R_{DS(on)}$	Q_2 – Static On–Resistance	V_{GS} = –12 V, I_D = –1.9 A	–	0.095	0.125	Ω
		V_{GS} = –5 V, I_D = –1.5 A	–	0.14	0.2	
I_L	Load Current	V_{DROP} = 0.125 V, V_{IN} = 12 V, $V_{ON/OFF}$ = 3.3 V	1	–	–	A
		V_{DROP} = 0.20 V, V_{IN} = 5 V, $V_{ON/OFF}$ = 3.3 V	1	–	–	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:
1. V_{IN} = 20 V, $V_{ON/OFF}$ = 8 V, T_A = 25°C
2. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.
3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

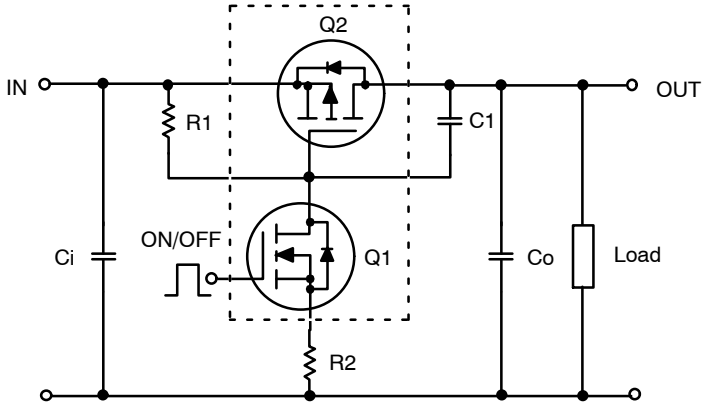


Figure 3. FDC6326L Load Switch Application

External Component Recommendation:

First select R2, 100−1 kΩ, for Slew Rate control.
C1 ≤ 1000 pF can be added in addition to R2 for further In−rush current control.
Then select R1 such that R1/R2 ratio maintains between 10−100. R1 is required to turn Q2 off.
For SPICE simulation, users can download a ″FDC6326L.MOD″ Spice model from ON Semiconductor Web Site at www.onsemi.com

TYPICAL CHARACTERISTICS

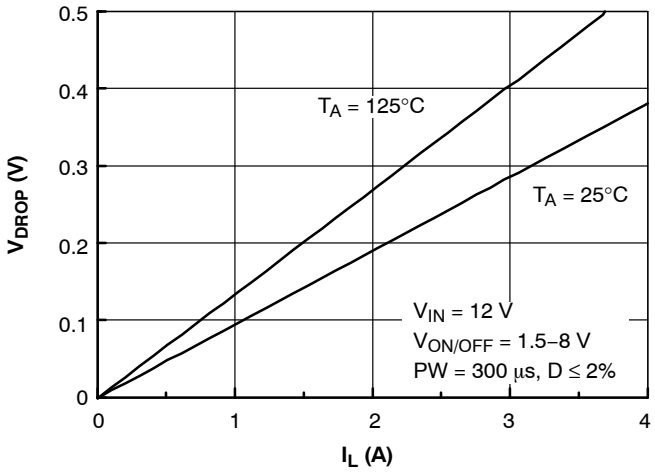


Figure 4. Conduction Voltage Drop Variation with Load Current

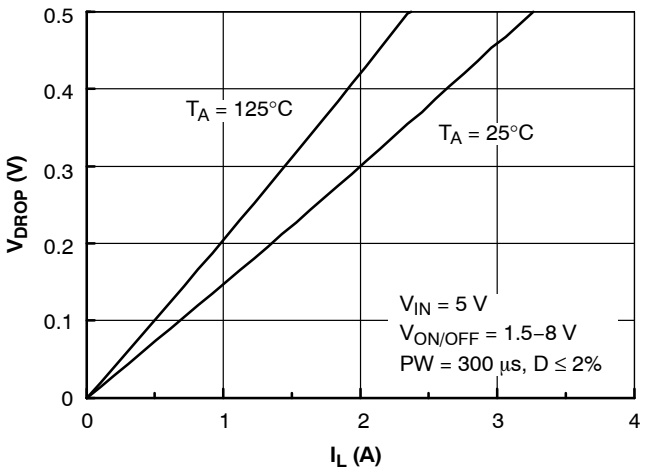


Figure 5. Conduction Voltage Drop Variation with Load Current

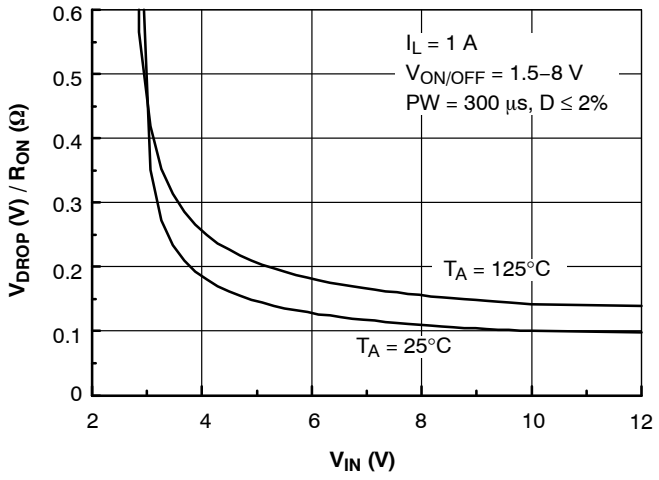


Figure 6. On−Resistance Variation with Input Voltage

TYPICAL CHARACTERISTICS (continued)

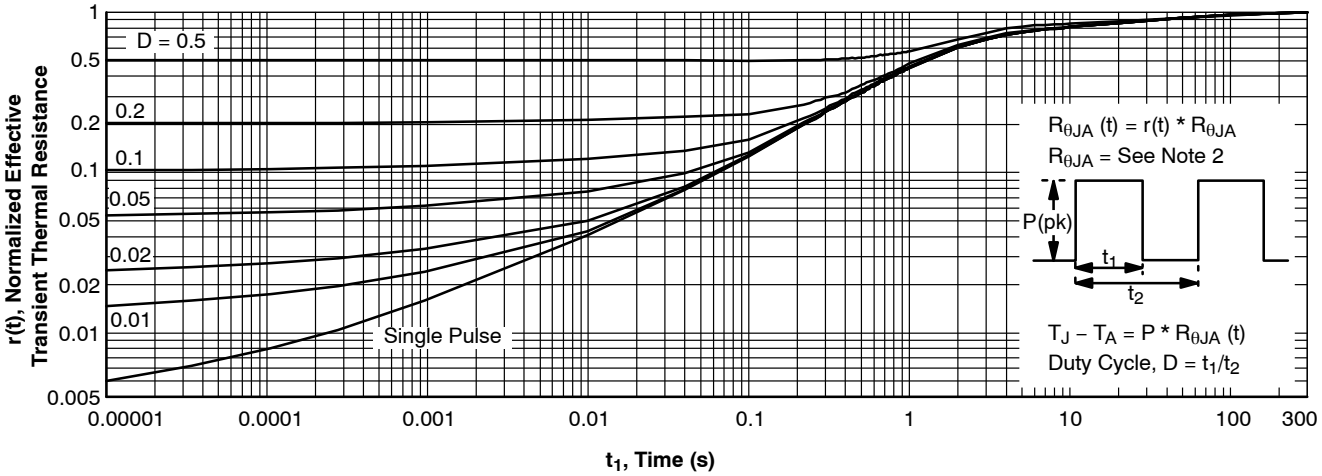


Figure 7. Transient Thermal Response Curve

NOTE: Thermal characterization performed on the conditions described in Note 2.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

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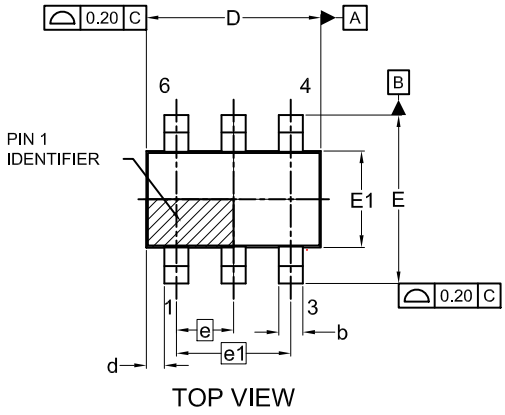
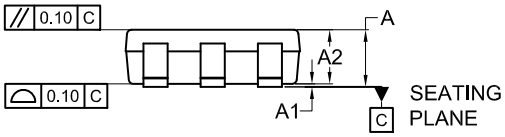
SCALE 2:1

TSOT23 6−Lead
CASE 419BL
ISSUE A

DATE 31 AUG 2020

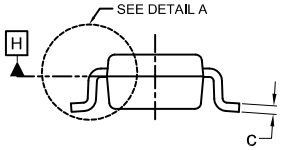


TOP VIEW

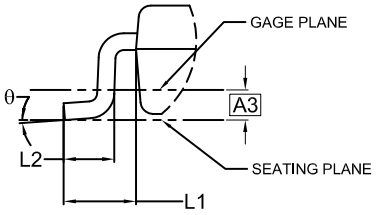


FRONT VIEW

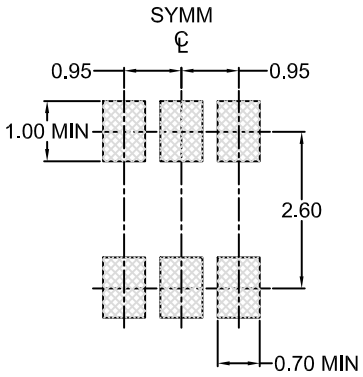
NOTE 4



SIDE VIEW



DETAIL A



LAND PATTERN
RECOMMENDATION

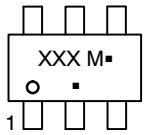
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3		0.25 BSC	
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d		0.30 REF	
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e		0.95 BSC	
e1		1.90 BSC	
L1		0.60 REF	
L2	0.20	0.40	0.60
θ	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSOT23 6−Lead**	**PAGE 1 OF 1**