

# ECOSPARK<sup>®</sup> 2 300 mJ, 400 V, N-Channel Ignition IGBT

## FGB3040G2-F085, FGD3040G2-F085, FGP3040G2-F085, FGI3040G2-F085

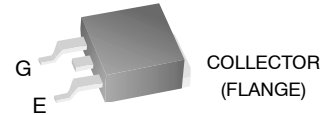
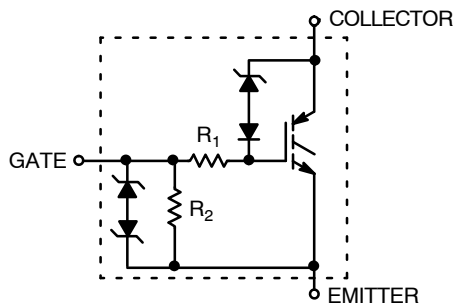
### Features

- SCIS Energy = 300 mJ at T<sub>J</sub> = 25°C
- Logic Level Gate Drive
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free and are RoHS Compliant

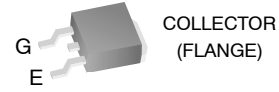
### Applications

- Automotive Ignition Coil Driver Circuits
- Coil On Plug Applications

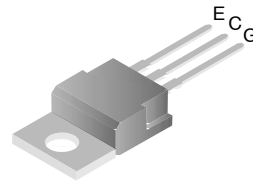
### SYMBOL



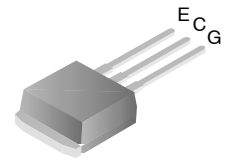
JEDEC TO-263AB  
D<sup>2</sup>PAK-3 (TO-263, 3-LEAD)  
CASE 418AJ



JEDEC TO-263AA  
DPAK3 (TO-252 3 LD)  
CASE 369AS

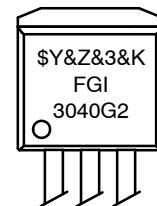
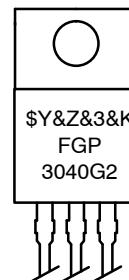
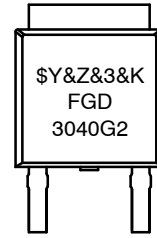
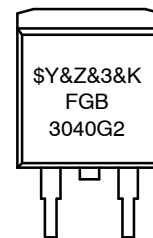


JEDEC TO-220AB  
TO-220-3LD  
CASE 340AT



JEDEC TO-262AA  
I2PAK (TO-262 3 LD)  
CASE 418AV

### MARKING DIAGRAMS



FGx3040G2 = Specific Device Code (x = B/D/P/I)  
 \$Y = onsemi Logo  
 &Z = Assembly Plant Code  
 &3 = 3-Digit Date Code  
 &K = 2-Digits Lot Run Traceability Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

# FGB3040G2-F085, FGD3040G2-F085, FGP3040G2-F085, FGI3040G2-F085

## DEVICE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Rating	Unit
$BV_{CER}$	Collector to Emitter Breakdown Voltage ( $I_C = 1\text{ mA}$ )	400	V
$BV_{ECS}$	Emitter to Collector Voltage - Reverse Battery Condition ( $I_C = 10\text{ mA}$ )	28	V
$E_{SCIS25}$	Self Clamping Inductive Switching Energy (Note 1)	300	mJ
$E_{SCIS150}$	Self Clamping Inductive Switching Energy (Note 2)	170	mJ
$I_{C25}$	Collector Current Continuous, at $V_{GE} = 5.0\text{ V}$ , $T_C = 25^\circ\text{C}$	41	A
$I_{C110}$	Collector Current Continuous, at $V_{GE} = 5.0\text{ V}$ , $T_C = 110^\circ\text{C}$	25.6	A
$V_{GEM}$	Gate to Emitter Voltage Continuous	$\pm 10$	V
$P_D$	Power Dissipation Total, at $T_C = 25^\circ\text{C}$	150	W
	Power Dissipation Derating, for $T_C > 25^\circ\text{C}$	1	W/ $^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to +175	$^\circ\text{C}$
$T_{STG}$	Storage Junction Temperature Range	-55 to +175	$^\circ\text{C}$
$T_L$	Max. Lead Temp. for Soldering (Leads at 1.6 mm from case for 10 s)	300	$^\circ\text{C}$
$T_{PKG}$	Reflow Soldering according to JESD020C	260	$^\circ\text{C}$
ESD	HBM-Electrostatic Discharge Voltage at 100 pF, 1500 $\Omega$	4	kV
	CDM-Electrostatic Discharge Voltage at 1 $\Omega$	2	kV

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Self Clamping Inductive Switching Energy ( $E_{SCIS25}$ ) of 300 mJ is based on the test conditions that starting  $T_J = 25^\circ\text{C}$ ;  $L = 3\text{ mH}$ ,  $I_{SCIS} = 14.2\text{ A}$ ,  $V_{CC} = 100\text{ V}$  during inductor charging and  $V_{CC} = 0\text{ V}$  during the time in clamp.
2. Self Clamping Inductive Switching Energy ( $E_{SCIS150}$ ) of 170 mJ is based on the test conditions that starting  $T_J = 150^\circ\text{C}$ ;  $L = 3\text{ mH}$ ,  $I_{SCIS} = 10.8\text{ A}$ ,  $V_{CC} = 100\text{ V}$  during inductor charging and  $V_{CC} = 0\text{ V}$  during the time in clamp.

# FGB3040G2–F085, FGD3040G2–F085, FGP3040G2–F085, FGI3040G2–F085

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF STATE CHARACTERISTICS

BV <sub>CER</sub>	Collector to Emitter Breakdown Voltage	I <sub>CE</sub> = 2 mA, V <sub>GE</sub> = 0, R <sub>GE</sub> = 1 kΩ, T <sub>J</sub> = -40 to 150°C	370	400	430	V	
BV <sub>CES</sub>	Collector to Emitter Breakdown Voltage	I <sub>CE</sub> = 10 mA, V <sub>GE</sub> = 0 V, R <sub>GE</sub> = 0, T <sub>J</sub> = -40 to 150°C	390	420	450	V	
BV <sub>ECS</sub>	Emitter to Collector Breakdown Voltage	I <sub>CE</sub> = -20 mA, V <sub>GE</sub> = 0 V, T <sub>J</sub> = 25°C	28	–	–	V	
BV <sub>GES</sub>	Gate to Emitter Breakdown Voltage	I <sub>GES</sub> = ±2 mA	±12	±14	–	V	
I <sub>CER</sub>	Collector to Emitter Leakage Current	V <sub>CE</sub> = 250 V, R <sub>GE</sub> = 1 kΩ	T <sub>J</sub> = 25°C	–	–	25	μA
			T <sub>J</sub> = 150°C	–	–	1	mA
I <sub>ECS</sub>	Emitter to Collector Leakage Current	V <sub>EC</sub> = 24 V	T <sub>J</sub> = 25°C	–	–	1	mA
			T <sub>J</sub> = 150°C	–	–	40	
R <sub>1</sub>	Series Gate Resistance		–	120	–	Ω	
R <sub>2</sub>	Gate to Emitter Resistance		10K	–	30K	Ω	

### ON STATE CHARACTERISTICS

V <sub>CE(SAT)</sub>	Collector to Emitter Saturation Voltage	I <sub>CE</sub> = 6 A, V <sub>GE</sub> = 4 V	T <sub>J</sub> = 25°C	–	1.15	1.25	V
V <sub>CE(SAT)</sub>	Collector to Emitter Saturation Voltage	I <sub>CE</sub> = 10 A, V <sub>GE</sub> = 4.5 V	T <sub>J</sub> = 150°C	–	1.35	1.50	V
V <sub>CE(SAT)</sub>	Collector to Emitter Saturation Voltage	I <sub>CE</sub> = 15 A, V <sub>GE</sub> = 4.5 V	T <sub>J</sub> = 150°C	–	1.68	1.85	V
E <sub>SCIS</sub>	Self Clamped Inductive Switching	L = 3.0 mH, R <sub>G</sub> = 1 kΩ, V <sub>GE</sub> = 5 V, (Note 3)	T <sub>J</sub> = 25°C	–	–	300	mJ

### DYNAMIC CHARACTERISTICS

Q <sub>G(ON)</sub>	Gate Charge	I <sub>CE</sub> = 10 A, V <sub>CE</sub> = 12 V, V <sub>GE</sub> = 5 V	–	21	–	nC	
V <sub>GE(TH)</sub>	Gate to Emitter Threshold Voltage	I <sub>CE</sub> = 1 mA, V <sub>CE</sub> = V <sub>GE</sub>	T <sub>J</sub> = 25°C	1.3	1.7	2.2	V
			T <sub>J</sub> = 150°C	0.75	1.2	1.8	
V <sub>GEP</sub>	Gate to Emitter Plateau Voltage	V <sub>CE</sub> = 12 V, I <sub>CE</sub> = 10 A	–	2.8	–	V	

### SWITCHING CHARACTERISTICS

t <sub>d(ON)R</sub>	Current Turn-On Delay Time-Resistive	V <sub>CE</sub> = 14 V, R <sub>L</sub> = 1 kΩ, V <sub>GE</sub> = 5 V, R <sub>G</sub> = 1 kΩ, T <sub>J</sub> = 25°C	–	0.9	4	μs
t <sub>rR</sub>	Current Rise Time-Resistive		–	1.9	7	μs
t <sub>d(OFF)L</sub>	Current Turn-Off Delay Time-Inductive	V <sub>CE</sub> = 300 V, L = 1 mH, V <sub>GE</sub> = 5 V, R <sub>G</sub> = 1 kΩ, I <sub>CE</sub> = 6.5 A, T <sub>J</sub> = 25°C	–	4.8	15	μs
t <sub>fL</sub>	Current Fall Time-Inductive		–	2.0	15	μs

### THERMAL CHARACTERISTICS

R <sub>θJC</sub>	Thermal Resistance Junction to Case	–	–	1	°C/W
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Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- Self Clamping Inductive Switching Energy (E<sub>SCIS25</sub>) of 300 mJ is based on the test conditions that starting T<sub>J</sub> = 25°C; L = 3 mH, I<sub>SCIS</sub> = 14.2 A, V<sub>CC</sub> = 100 V during inductor charging and V<sub>CC</sub> = 0 V during the time in clamp.

TYPICAL PERFORMANCE CURVES

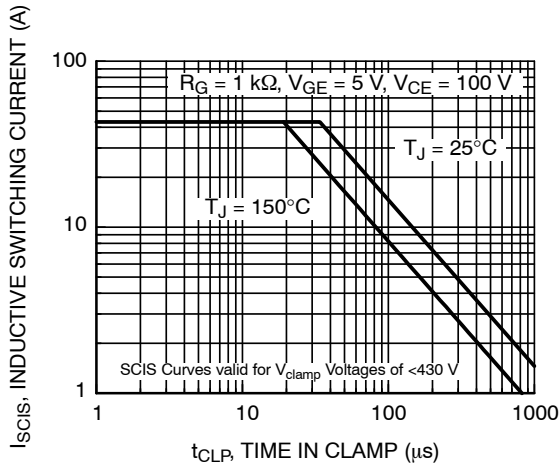


Figure 1. Self Clamped Inductive Switching Current vs. Time in Clamp

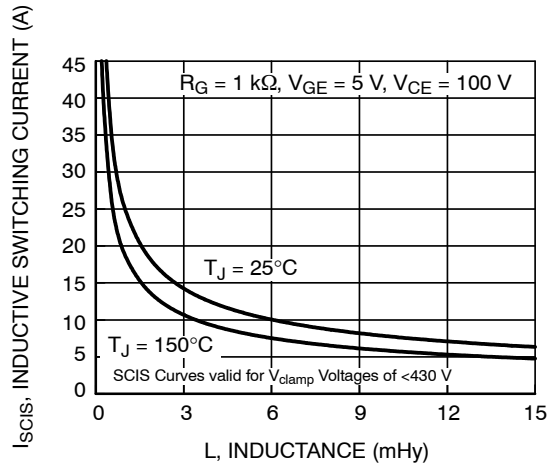


Figure 2. Self Clamped Inductive Switching Current vs. Inductance

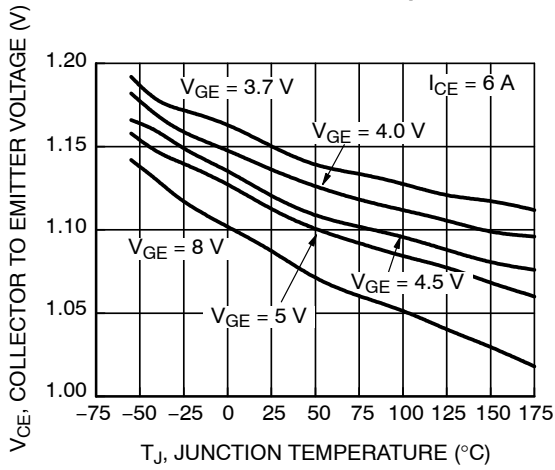


Figure 3. Collector to Emitter On-State Voltage vs. Junction Temperature

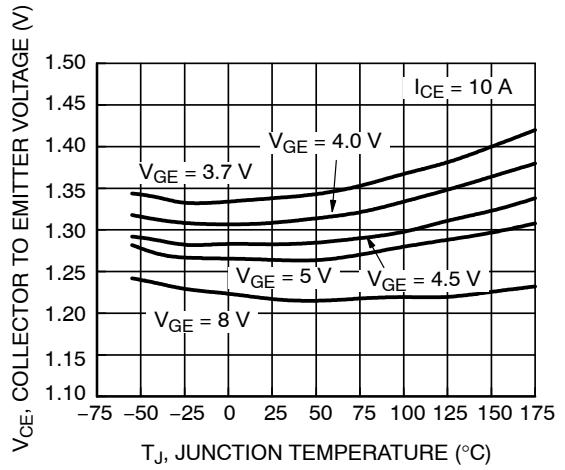


Figure 4. Collector to Emitter On-State Voltage vs. Junction Temperature

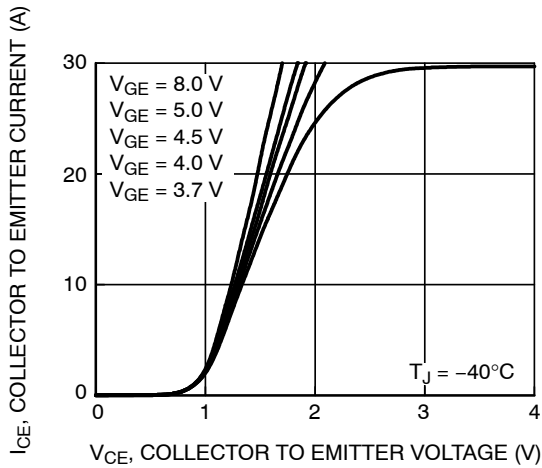


Figure 5. Collector to Emitter On-State Voltage vs. Collector Current

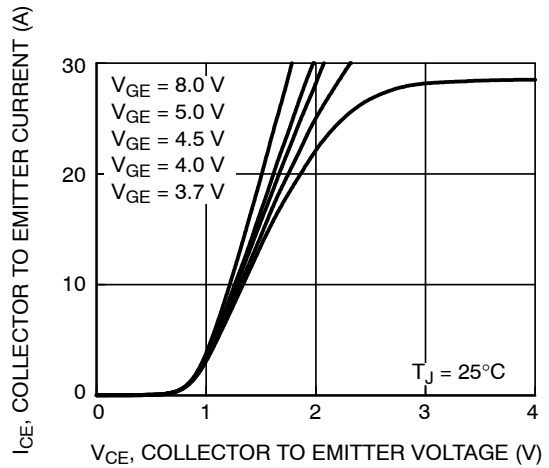


Figure 6. Collector to Emitter On-State Voltage vs. Collector Current

TYPICAL PERFORMANCE CURVES (Continued)

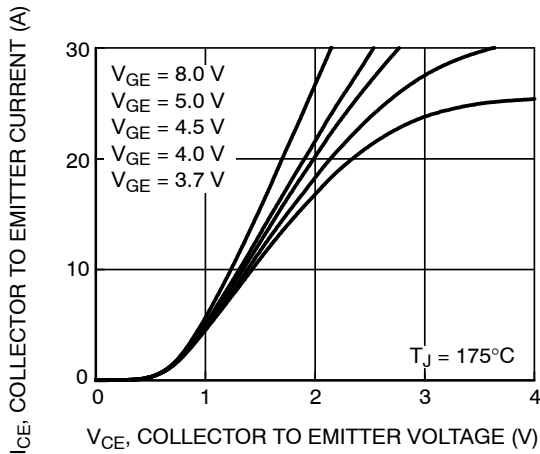


Figure 7. Collector to Emitter On-Stage Voltage vs. Collector Current

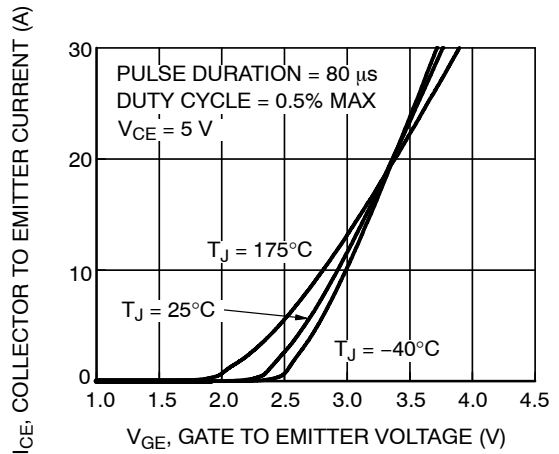


Figure 8. Transfer Characteristics

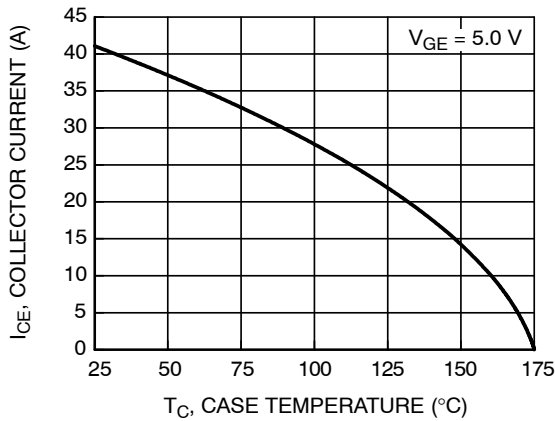


Figure 9. DC Collector Current vs. Case Temperature

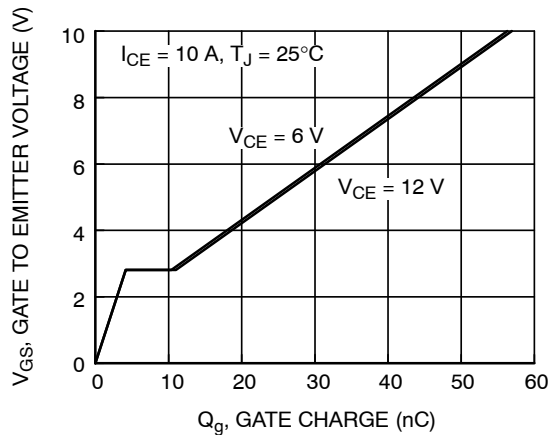


Figure 10. Gate Charge

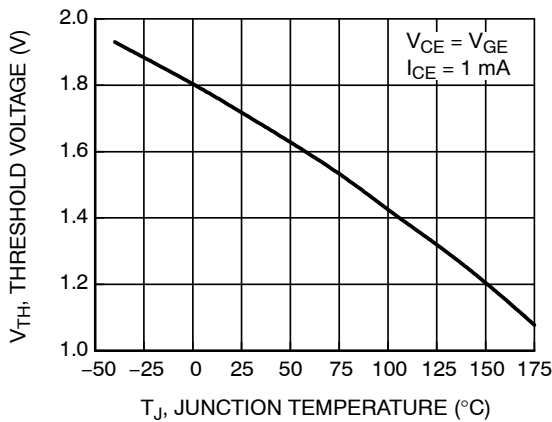


Figure 11. Threshold Voltage vs. Junction Temperature

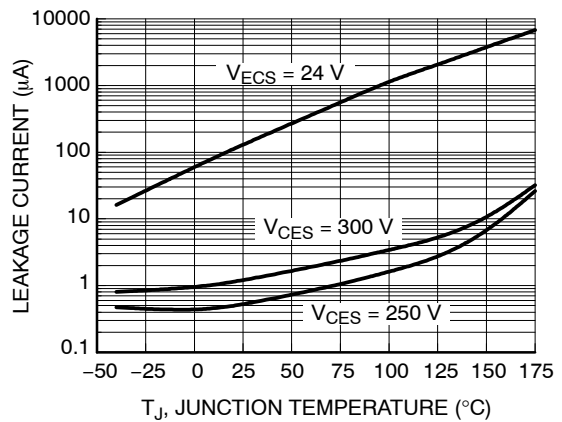


Figure 12. Leakage Current vs. Junction Temperature

TYPICAL PERFORMANCE CURVES (Continued)

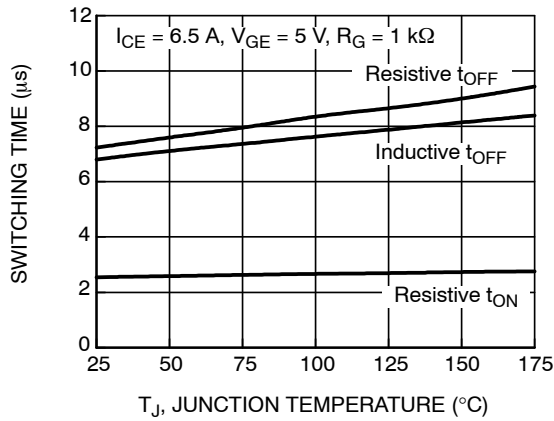


Figure 13. Switching Time vs. Junction Temperature

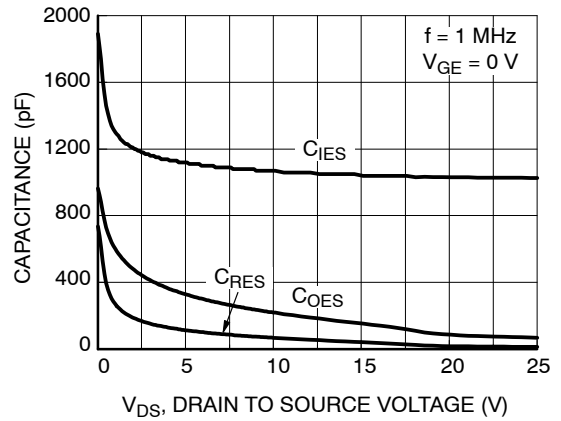


Figure 14. Capacitance vs. Collector to Emitter Voltage

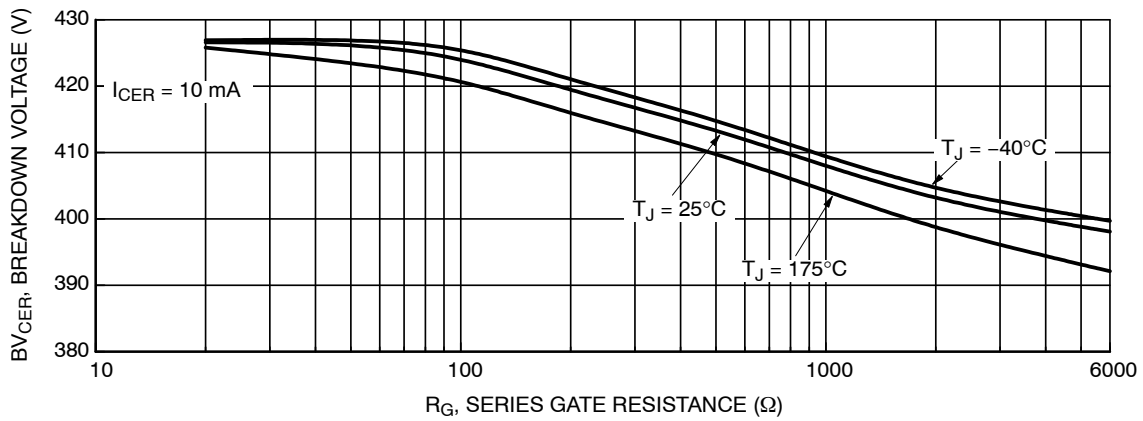


Figure 15. Breakdown Voltage vs. Series Gate Resistance

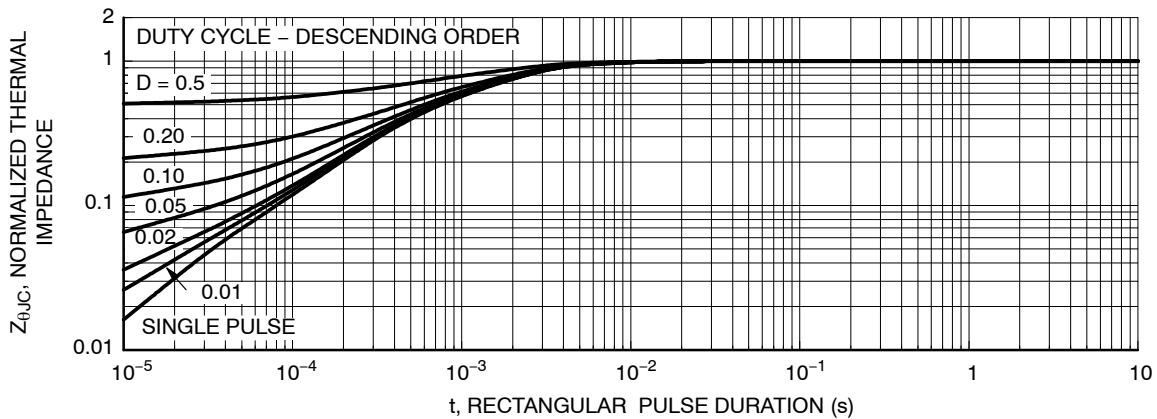


Figure 16. IGBT Normalized Transient Thermal Impedance, Junction to Case

TYPICAL PERFORMANCE CURVES (Continued)

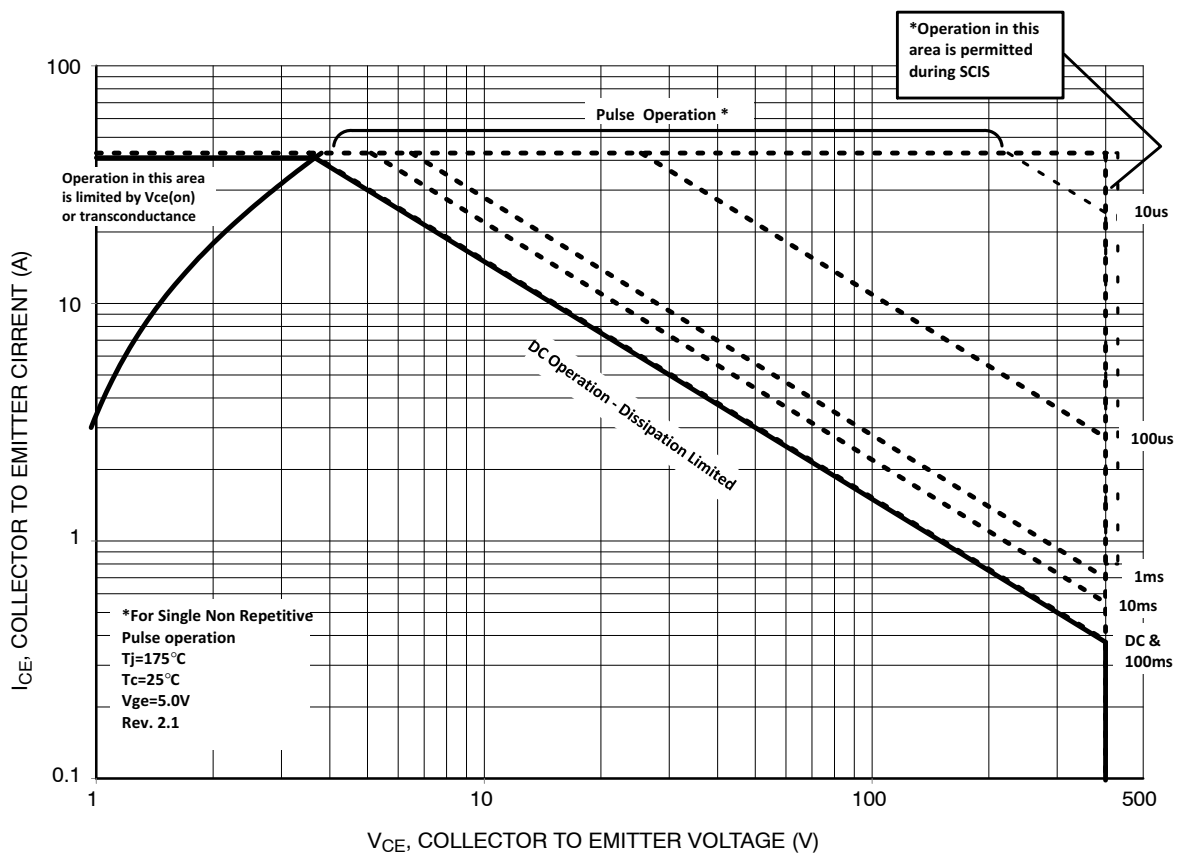


Figure 17. Forward Safe Operating Area

TEST CIRCUIT AND WAVEFORMS

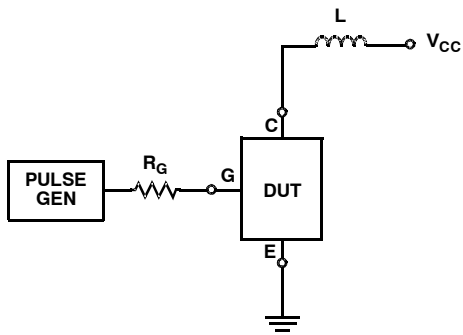


Figure 18. Inductive Switching Test Circuit

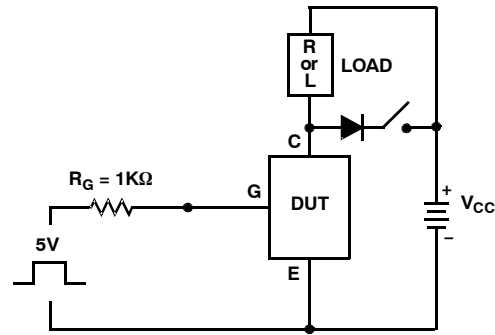


Figure 19.  $t_{ON}$  and  $t_{OFF}$  Switching Test Circuit

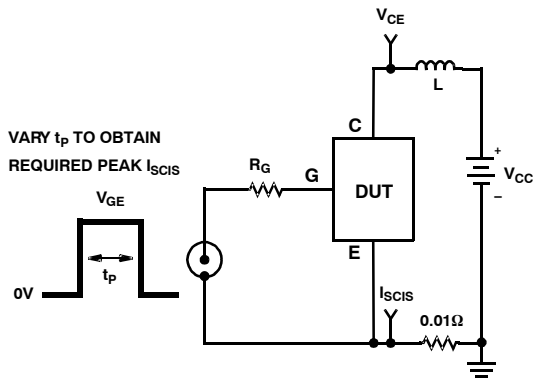


Figure 20. Energy Test Circuit

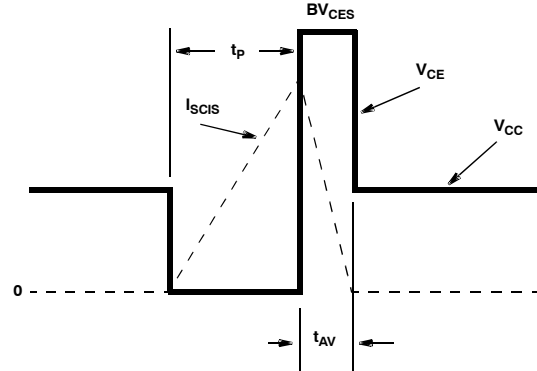


Figure 21. Energy Waveforms

PACKAGE MARKING AND ORDERING INFORMATION

Device	Device Marking	Package	Shipping <sup>†</sup>
FGB3040G2-F085	FGB3040G2	D <sup>2</sup> PAK-3 (TO-263, 3-LEAD) (TO-263AB) (Pb-Free)	800 / Tape & Reel
FGD3040G2-F085	FGD3040G2	DPAK3 (TO-252 3 LD) (TO-252AA) (Pb-Free)	2500 / Tape & Reel
FGP3040G2-F085	FGP3040G2	TO-220-3LD (TO-220AB) (Pb-Free)	400 / Tube
FGI3040G2-F085	FGI3040G2	I2PAK (TO-262 3 LD) (TO-262AA) (Pb-Free)	400 / Tube

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

ON Semiconductor®



Scale 1:1

### TO-220-3LD CASE 340AT ISSUE A

DATE 03 OCT 2017

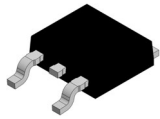


- NOTES:
- A) REFERENCE JEDEC, TO-220, VARIATION AB
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
  - D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
  - E) DOES NOT COMPLY JEDEC STANDARD VALUE.
  - F) "A1" DIMENSIONS AS BELOW:  
 SINGLE GAUGE = 0.51 - 0.61  
 DUAL GAUGE = 1.10 - 1.45
  - G) PRESENCE IS SUPPLIER DEPENDENT
  - H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

<b>DOCUMENT NUMBER:</b>	<b>98AON13818G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>TO-220-3LD</b>	<b>PAGE 1 OF 1</b>

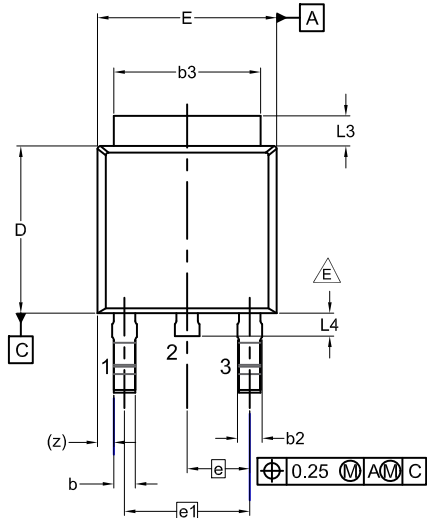
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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

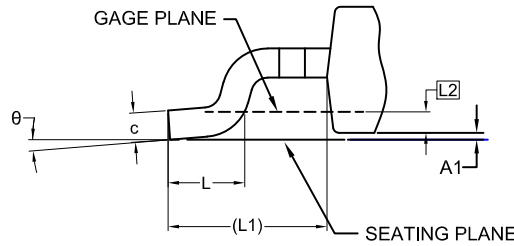


## DPAK3 (TO-252 3 LD) CASE 369AS ISSUE A

DATE 28 SEP 2022



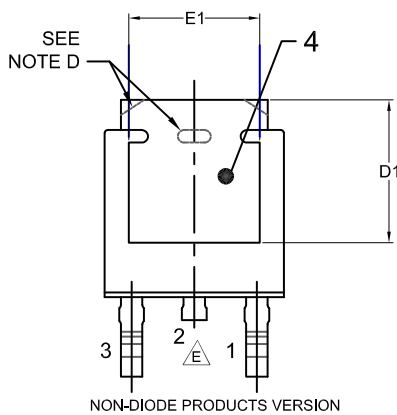
- NOTES: UNLESS OTHERWISE SPECIFIED  
 A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.  
 B) ALL DIMENSIONS ARE IN MILLIMETERS.  
 C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.  
 D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.  
 E) FOR DIODE PRODUCTS, L4 IS 0.25 MM MAX.  
 F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.  
 G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.



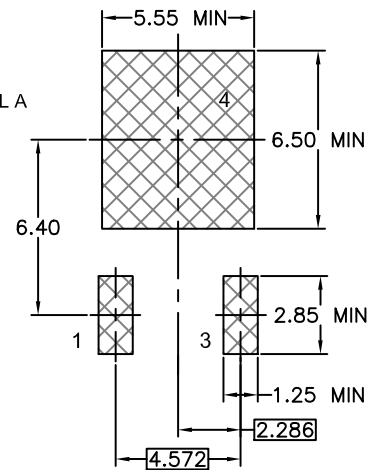
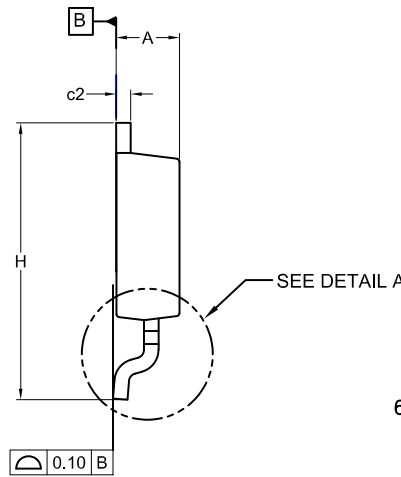
**DETAIL A**  
(ROTATED -90°)  
SCALE: 12X

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.18	2.29	2.39
A1	0.00	-	0.127
b	0.64	0.77	0.89
b2	0.76	0.95	1.14
b3	5.21	5.34	5.46
c	0.45	0.53	0.61
c2	0.45	0.52	0.58
D	5.97	6.10	6.22
D1	5.21	-	-
E	6.35	6.54	6.73
E1	4.32	-	-
e	2.286 BSC		
e1	4.572 BSC		
H	9.40	9.91	10.41
L	1.40	1.59	1.78
L1	2.90 REF		
L2	0.51 BSC		
L3	0.89	1.08	1.27
L4	-	-	1.02
θ	0°	--	10°

NON-DIODE PRODUCTS VERSION



NON-DIODE PRODUCTS VERSION



### LAND PATTERN RECOMMENDATION

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

### GENERIC MARKING DIAGRAM\*



- XXXX = Specific Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

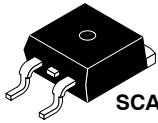
<b>DOCUMENT NUMBER:</b>	<b>98AON13810G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>DPAK3 (TO-252 3 LD)</b>	<b>PAGE 1 OF 1</b>

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# MECHANICAL CASE OUTLINE

## PACKAGE DIMENSIONS

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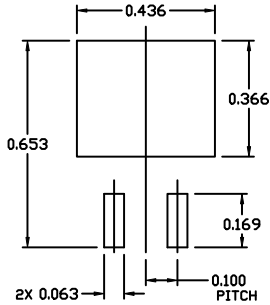
SCALE 1:1

### D<sup>2</sup>PAK-3 (TO-263, 3-LEAD)

#### CASE 418AJ

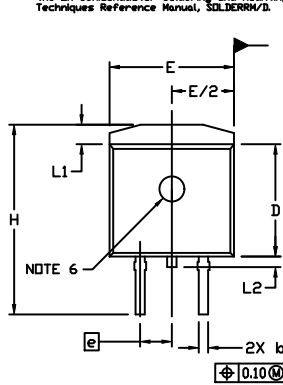
#### ISSUE F

DATE 11 MAR 2021



#### RECOMMENDED MOUNTING FOOTPRINT

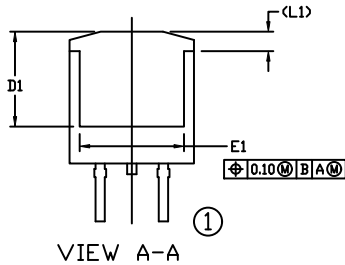
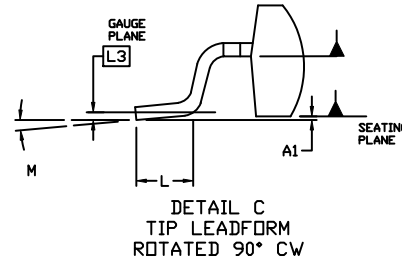
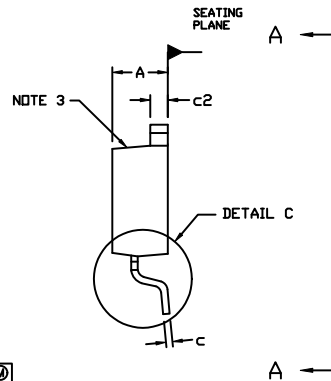
For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



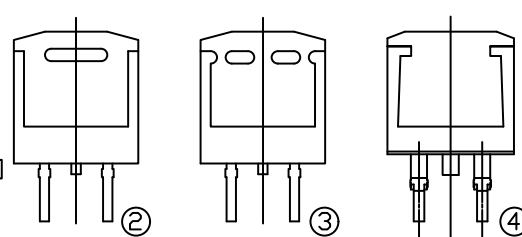
#### NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: INCHES
- CHAMFER OPTIONAL.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
- OPTIONAL MOLD FEATURE.
- ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100	BSC	2.54	BSC
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010	BSC	0.25	BSC
M	0*	8*	0*	8*

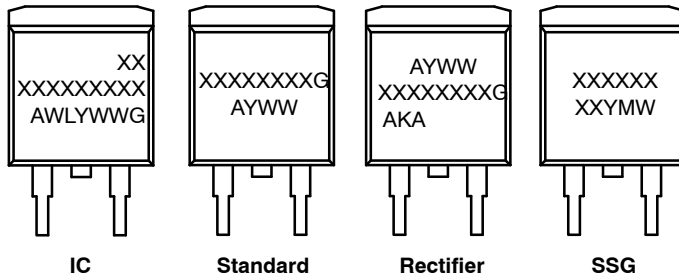


VIEW A-A



VIEW A-A  
OPTIONAL CONSTRUCTIONS

#### GENERIC MARKING DIAGRAMS\*



IC

Standard

Rectifier

SSG

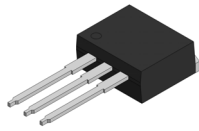
- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- W = Week Code (SSG)
- M = Month Code (SSG)
- G = Pb-Free Package
- AKA = Polarity Indicator

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	D <sup>2</sup> PAK-3 (TO-263, 3-LEAD)	PAGE 1 OF 1

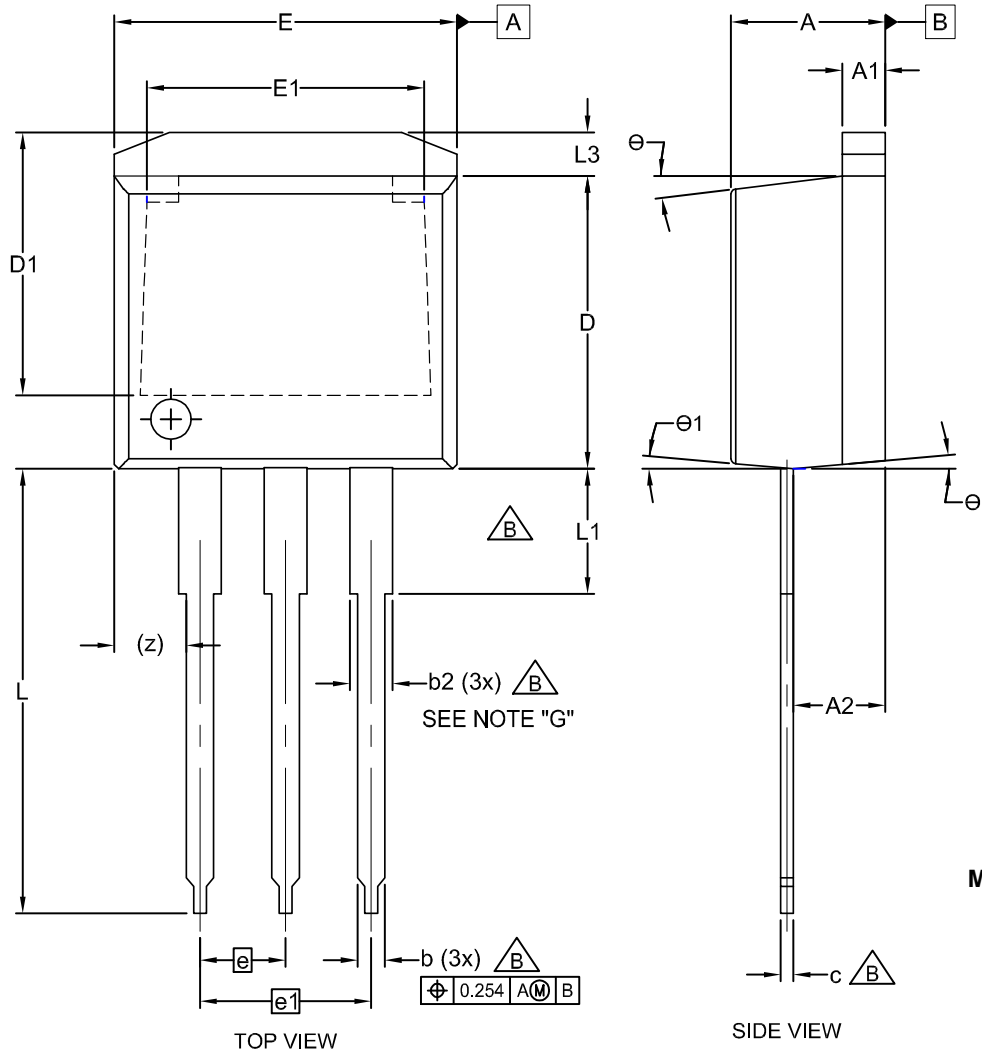
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# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



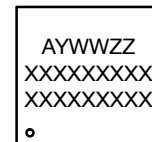
I2PAK (TO-262 3 LD)  
CASE 418AV  
ISSUE A

DATE 30 AUG 2022



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	4.06	4.45	4.83
A1	1.14	1.27	1.40
A2	2.03	2.41	2.79
b	0.64	0.77	0.90
b2	1.14	1.46	1.78
c	0.33	0.49	0.64
D	8.64	9.15	9.65
D1	6.86	7.37	7.88
E	9.65	9.97	10.29
E1	6.22	7.28	8.33
e	2.54 BSC		
e1	5.08 BSC		
L	12.70	13.72	14.73
L1	2.80	3.38	3.96
L3	1.00	1.20	1.40
z	2.13 REF		
θ	0°	--	7°
θ1	0°	--	5°

### GENERIC MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

#### NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO TO262 JEDEC VARIATION AA.
- B. DOES NOT COMPLY JEDEC STD. VALUE.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
- E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.
- F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)
- G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.

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<b>DESCRIPTION:</b>	<b>I2PAK (TO-262 3 LD)</b>	<b>PAGE 1 OF 1</b>

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