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1-Mbit (128K × 8) Serial (I^2C) F-RAM

Features

- 1-Mbit ferroelectric random access memory (F-RAM) logically organized as 128K × 8
  - High-endurance 100 trillion (10^{14}) read/writes
  - 151-year data retention (See Data Retention and Endurance on page 13)
  - NoDelay™ writes
  - Advanced high-reliability ferroelectric process
- Fast two-wire Serial interface (I^2C)
  - Up to 3.4-MHz frequency
  - Direct hardware replacement for serial (I^2C) EEPROM
  - Supports legacy timings for 100 kHz and 400 kHz
- Device ID and Serial Number
  - Manufacturer ID and Product ID
  - Unique Serial Number (FM24VN10)
- Low power consumption
  - 175 µA active current at 100 kHz
  - 90 µA (typ) standby current
  - 5 µA (typ) sleep mode current
- Low-voltage operation: V_{DD} = 2.0 V to 3.6 V
- Industrial temperature: –40 °C to +85 °C
- 8-pin small outline integrated circuit (SOIC) package
- Restriction of hazardous substances (RoHS) compliant

Functional Description

The FM24V10 is a 1-Mbit nonvolatile memory employing an advanced ferroelectric process. A ferroelectric random access memory or F-RAM is nonvolatile and performs reads and writes similar to a RAM. It provides reliable data retention for 151 years while eliminating the complexities, overhead, and system-level reliability problems caused by EEPROM and other nonvolatile memories.

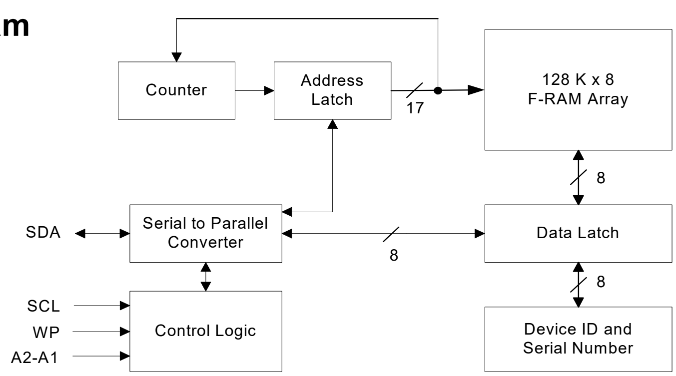
Unlike EEPROM, the FM24V10 performs write operations at bus speed. No write delays are incurred. Data is written to the memory array immediately after each byte is successfully transferred to the device. The next bus cycle can commence without the need for data polling. In addition, the product offers substantial write endurance compared with other nonvolatile memories. Also, F-RAM exhibits much lower power during writes than EEPROM since write operations do not require an internally elevated power supply voltage for write circuits. The FM24V10 is capable of supporting 10^{14} read/write cycles, or 100 million times more write cycles than EEPROM.

These capabilities make the FM24V10 ideal for nonvolatile memory applications, requiring frequent or rapid writes. Examples range from data logging, where the number of write cycles may be critical, to demanding industrial controls where the long write time of EEPROM can cause data loss. The combination of features allows more frequent data writing with less overhead for the system.

The FM24V10 provides substantial benefits to users of serial (I^2C) EEPROM as a hardware drop-in replacement. The FM24VN10 is offered with a unique serial number that is read-only and can be used to identify a board or system. Both devices incorporate a read-only Device ID that allows the host to determine the manufacturer, product density, and product revision. The device specifications are guaranteed over an industrial temperature range of –40 °C to +85 °C.

For a complete list of related documentation, click here.

Logic Block Diagram

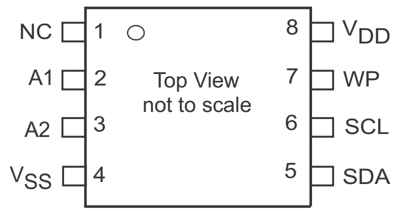


Errata: STOP condition is optional for sleep mode entry. For more information, see Errata on page 19. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability.

Contents

Pinout

Figure 1. 8-pin SOIC pinout



Pin Definitions

Pin Name	I/O Type	Description
A2–A1	Input	**Device Select Address 2–1**. These pins are used to select one of up to 4 devices of the same type on the same I^2C bus. To select the device, the address value on the three pins must match the corresponding bits contained in the slave address. The address pins are pulled down internally.
SDA	Input/Output	**Serial Data/Address**. This is a bi-directional pin for the I^2C interface. It is open-drain and is intended to be wire-AND'd with other devices on the I^2C bus. The input buffer incorporates a Schmitt trigger for noise immunity and the output driver includes slope control for falling edges. An external pull-up resistor is required.
SCL	Input	**Serial Clock**. The serial clock pin for the I^2C interface. Data is clocked out of the device on the falling edge, and into the device on the rising edge. The SCL input also incorporates a Schmitt trigger input for noise immunity.
WP	Input	**Write Protect**. When tied to V_{DD}, addresses in the entire memory map will be write-protected. When WP is connected to ground, all addresses are write enabled. This pin is pulled down internally.
V_{SS}	Power supply	Ground for the device. Must be connected to the ground of the system.
V_{DD}	Power supply	Power supply input to the device.
NC	No connect	No connect. This pin is not connected to the die.

Functional Overview

The FM24V10 is a serial F-RAM memory. The memory array is logically organized as 131,072 × 8 bits and is accessed using an industry-standard I^2C interface. The functional operation of the F-RAM is similar to serial (I^2C) EEPROM. The major difference between the FM24V10 and a serial (I^2C) EEPROM with the same pinout is the F-RAM's superior write performance, high endurance, and low power consumption.

Memory Architecture

When accessing the FM24V10, the user addresses 128K locations of eight data bits each. These eight data bits are shifted in or out serially. The addresses are accessed using the I^2C protocol, which includes a slave address (to distinguish other non-memory devices), a page select bit, and a two-byte address. The 17-bit address consists of a page select bit followed by 16-bits. The complete address of 17-bits specifies each byte address uniquely.

The access time for the memory operation is essentially zero, beyond the time needed for the serial protocol. That is, the memory is read or written at the speed of the I^2C bus. Unlike a serial (I^2C) EEPROM, it is not necessary to poll the device for a ready condition because writes occur at bus speed. By the time a new bus transaction can be shifted into the device, a write operation is complete. This is explained in more detail in the interface section.

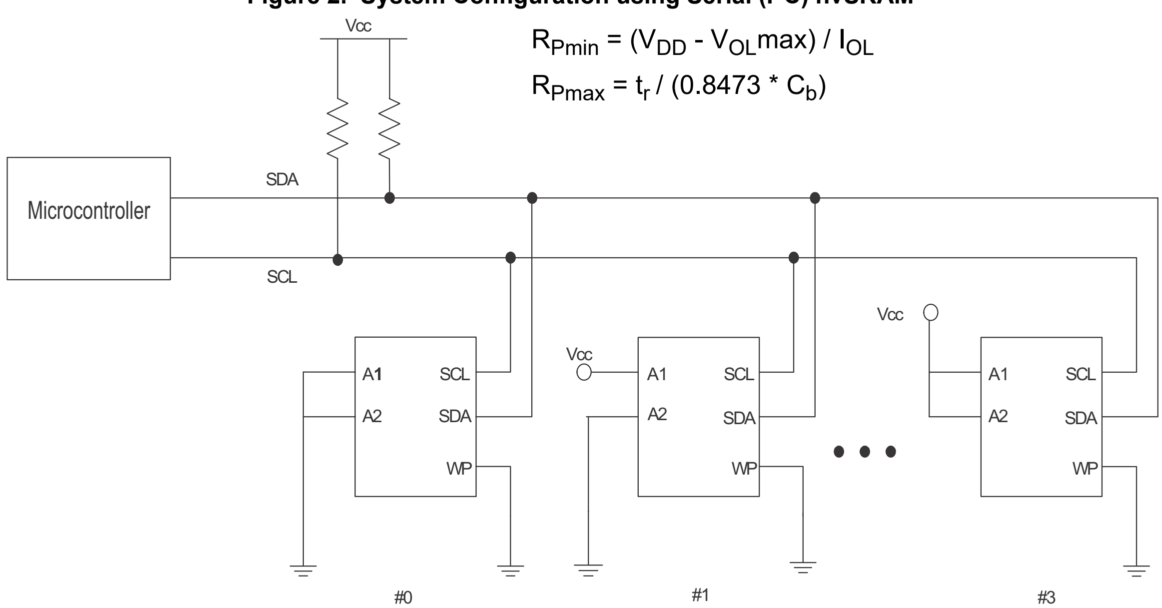
I^2C Interface

The FM24V10 employs a bi-directional I^2C bus protocol using few pins or board space. Figure 2 illustrates a typical system configuration using the FM24V10 in a microcontroller-based system. The industry standard I^2C bus is familiar to many users but is described in this section.

By convention, any device that is sending data onto the bus is the transmitter while the target device for this data is the receiver. The device that is controlling the bus is the master. The master is responsible for generating the clock signal for all operations. Any device on the bus that is being controlled is a slave. The FM24V10 is always a slave device.

The bus protocol is controlled by transition states in the SDA and SCL signals. There are four conditions including START, STOP, data bit, or acknowledge. Figure 3 on page 5 and Figure 4 on page 5 illustrates the signal conditions that specify the four states. Detailed timing diagrams are shown in the electrical specifications section.

Figure 2. System Configuration using Serial (I^2C) nvSRAM



STOP Condition (P)

A STOP condition is indicated when the bus master drives SDA from LOW to HIGH while the SCL signal is HIGH. All operations using the FM24V10 should end with a STOP condition. If an operation is in progress when a STOP is asserted, the operation will be aborted. The master must have control of SDA in order to assert a STOP condition.

START Condition (S)

A START condition is indicated when the bus master drives SDA from HIGH to LOW while the SCL signal is HIGH. All commands should be preceded by a START condition. An operation in progress can be aborted by asserting a START condition at any time. Aborting an operation using the START condition will ready the FM24V10 for a new operation.

If during operation the power supply drops below the specified V_{DD} minimum, the system should issue a START condition prior to performing another operation.

Figure 3. START and STOP Conditions

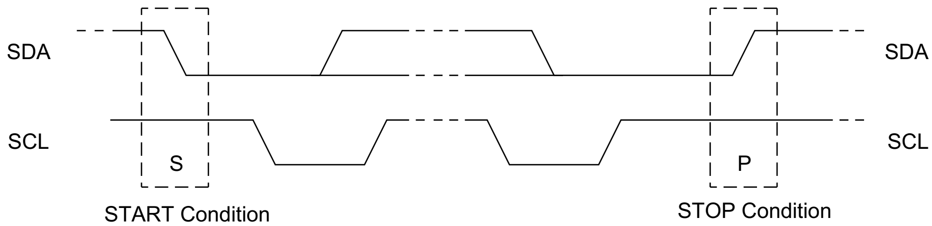
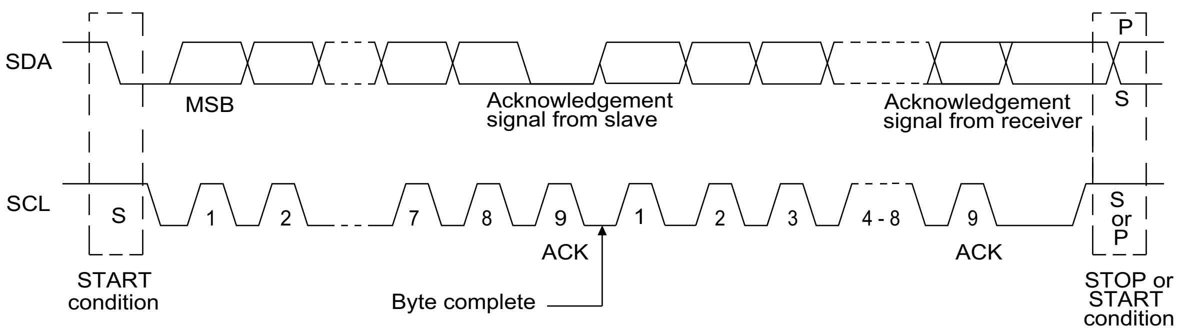


Figure 4. Data Transfer on the I^{2}C Bus



Data/Address Transfer

All data transfers (including addresses) take place while the SCL signal is HIGH. Except under the three conditions described above, the SDA signal should not change while SCL is HIGH.

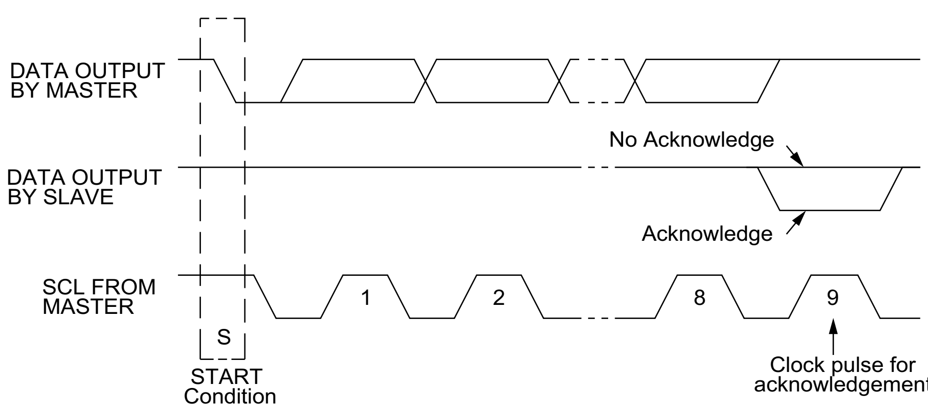
Acknowledge/No-acknowledge

The acknowledge takes place after the 8th data bit has been transferred in any transaction. During this state the transmitter should release the SDA bus to allow the receiver to drive it. The receiver drives the SDA signal LOW to acknowledge receipt of the byte. If the receiver does not drive SDA LOW, the condition is a no-acknowledge and the operation is aborted.

The receiver would fail to acknowledge for two distinct reasons. First is that a byte transfer fails. In this case, the no-acknowledge ceases the current operation so that the device can be addressed again. This allows the last byte to be recovered in the event of a communication error.

Second and most common, the receiver does not acknowledge to deliberately end an operation. For example, during a read operation, the FM24V10 will continue to place data onto the bus as long as the receiver sends acknowledges (and clocks). When a read operation is complete and no more data is needed, the receiver must not acknowledge the last byte. If the receiver acknowledges the last byte, this will cause the FM24V10 to attempt to drive the bus on the next clock while the master is sending a new command such as STOP.

Figure 5. Acknowledge on the I^{2}C Bus

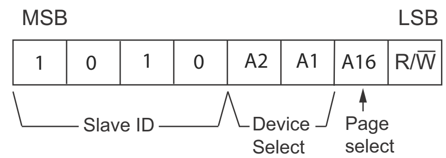


Slave Device Address

The first byte that the FM24V10 expects after a START condition is the slave address. As shown in Figure 6, the slave address contains the device type or slave ID, the device select address bits, a page select bit, and a bit that specifies if the transaction is a read or a write.

Bits 7–4 are the device type (slave ID) and should be set to 1010b for the FM24V10. These bits allow other function types to reside on the I^2C bus within an identical address range. Bits 3–2 are the device select address bits. They must match the corresponding value on the external address pins to select the device. Up to four FM24V10 devices can reside on the same I^2C bus by assigning a different address to each. Bit 1 is the page select bit and is effectively the address MSB, A16. It specifies the 64K-byte block of memory that is targeted for the current operation. Bit 0 is the read/write bit ($R/\overline{W}$). $R/\overline{W}$ = ‘1’ indicates a read operation and $R/\overline{W}$ = ‘0’ indicates a write operation.

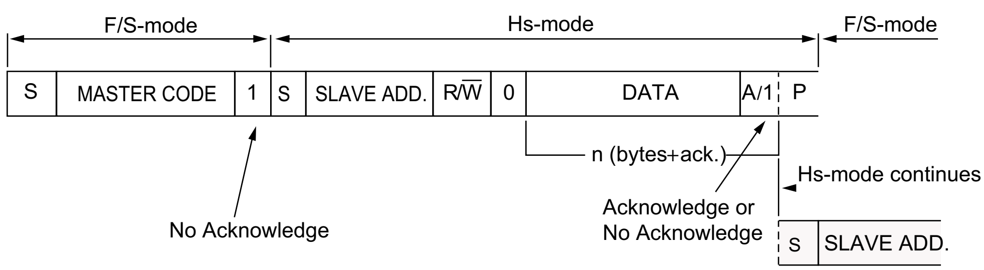
Figure 6. Memory Slave Device Address



High Speed Mode (Hs-mode)

The FM24V10 supports a 3.4-MHz high speed mode. A master code (00001XXXb) must be issued to place the device into high speed mode. Communication between master and slave will then be enabled for speeds up to 3.4-MHz. A STOP condition will exit Hs-mode. Single- and multiple-byte reads and writes are supported.

Figure 7. Data transfer format in Hs-mode



Addressing Overview

After the FM24V10 (as receiver) acknowledges the slave address, the master can place the memory address on the bus for a write operation. The address requires a 1-bit page select and two bytes. Since the device uses 17-bit address, the page select bit is the MSB of the address followed by the remaining 16-bit address. The complete 17-bit address is latched internally. Each access causes the latched address value to be incremented automatically. The current address is the value that is held in the latch; either a newly written value or the address following the last access. The current address will be held for as long as power remains or until a new value is written. Reads always use the current address. A random read address can be loaded by beginning a write operation as explained below.

After transmission of each data byte, just prior to the acknowledge, the FM24V10 increments the internal address latch. This allows the next sequential byte to be accessed with no additional addressing. After the last address (1FFFFh) is reached, the address latch will roll over to 00000h. There is no limit to the number of bytes that can be accessed with a single read or write operation.

Data Transfer

After the address bytes have been transmitted, data transfer between the bus master and the FM24V10 can begin. For a read operation the FM24V10 will place 8 data bits on the bus then wait for an acknowledge from the master. If the acknowledge occurs, the FM24V10 will transfer the next sequential byte. If the acknowledge is not sent, the FM24V10 will end the read operation. For a write operation, the FM24V10 will accept 8 data bits from the master then send an acknowledge. All data transfer occurs MSB (most significant bit) first.

Memory Operation

The FM24V10 is designed to operate in a manner very similar to other I^2C interface memory products. The major differences result from the higher performance write capability of F-RAM technology. These improvements result in some differences between the FM24V10 and a similar configuration EEPROM during writes. The complete operation for both writes and reads is explained below.

Write Operation

All writes begin with a slave address, then a memory address. The bus master indicates a write operation by setting the LSB of the slave address ($R/\overline{W}$ bit) to a ‘0’. After addressing, the bus master sends each byte of data to the memory and the memory generates an acknowledge condition. Any number of sequential bytes may be written. If the end of the address range is reached internally, the address counter will wrap from 1FFFFh to 00000h.

Unlike other nonvolatile memory technologies, there is no effective write delay with F-RAM. Since the read and write access times of the underlying memory are the same, the user experiences no delay through the bus. The entire memory cycle occurs in less time than a single bus clock. Therefore, any operation including read or write can occur immediately following a write. Acknowledge polling, a technique used with EEPROMs to determine if a write is complete is unnecessary and will always return a ready condition.

Internally, an actual memory write occurs after the 8th data bit is transferred. It will be complete before the acknowledge is sent. Therefore, if the user desires to abort a write without altering the memory contents, this should be done using START or STOP condition prior to the 8th data bit. The FM24V10 uses no page buffering.

The memory array can be write-protected using the WP pin. Setting the WP pin to a HIGH condition (V_{DD}) will write-protect all addresses. The FM24V10 will not acknowledge data bytes that are written to protected addresses. In addition, the address counter will not increment if writes are attempted to these addresses. Setting WP to a LOW state (V_{SS}) will disable the write protect. WP is pulled down internally.

Figure 8 and Figure 9 below illustrate a single-byte and multiple-byte write cycles in F/S mode. Figure 10 below illustrate a single-byte write cycles in Hs mode.

Figure 8. Single-Byte Write

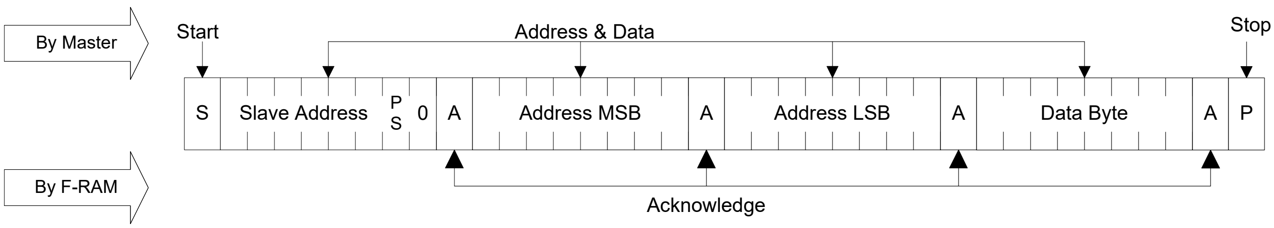


Figure 9. Multi-Byte Write

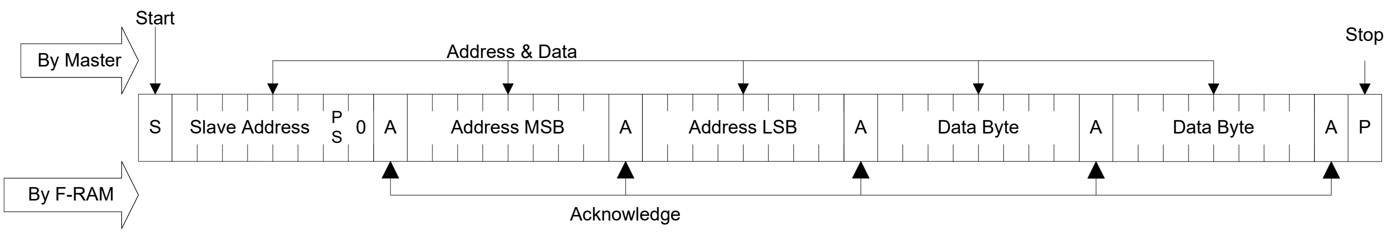
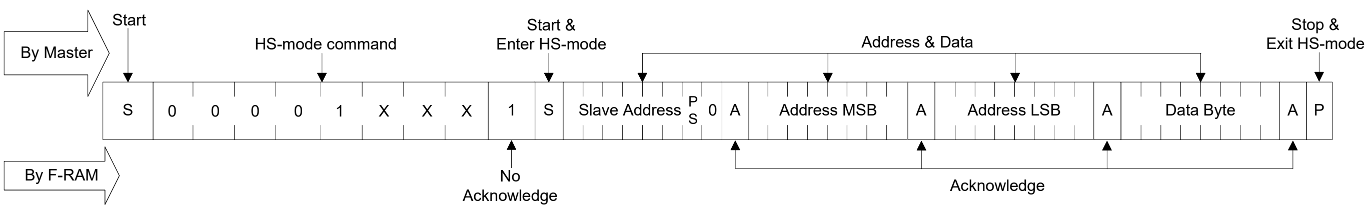


Figure 10. Hs-mode Byte Write



Read Operation

There are two basic types of read operations. They are current address read and selective address read. In a current address read, the FM24V10 uses the internal address latch to supply the address. In a selective read, the user performs a procedure to set the address to a specific value.

Current Address & Sequential Read

As mentioned above the FM24V10 uses an internal latch to supply the address for a read operation. A current address read uses the existing value in the address latch as a starting place for the read operation. The system reads from the address immediately following that of the last operation.

To perform a current address read, the bus master supplies a slave address with the LSB set to a '1'. This indicates that a read operation is requested. After receiving the complete slave address, the FM24V10 will begin shifting out data from the current address on the next clock. The current address is the value held in the internal address latch.

Beginning with the current address, the bus master can read any number of bytes. Thus, a sequential read is simply a current address read with multiple byte transfers. After each byte the internal address counter will be incremented.

Note Each time the bus master acknowledges a byte, this indicates that the FM24V10 should read out the next sequential byte.

There are four ways to properly terminate a read operation. Failing to properly terminate the read will most likely create a bus contention as the FM24V10 attempts to read out additional data onto the bus. The four valid methods are:

1. The bus master issues a no-acknowledge in the 9th clock cycle and a STOP in the 10th clock cycle. This is illustrated in the diagrams below. This is preferred.
2. The bus master issues a no-acknowledge in the 9th clock cycle and a START in the 10th.
3. The bus master issues a STOP in the 9th clock cycle.
4. The bus master issues a START in the 9th clock cycle.

If the internal address reaches 1FFFFh, it will wrap around to 00000h on the next read cycle. Figure 11 and Figure 12 below show the proper operation for current address reads.

Figure 11. Current Address Read

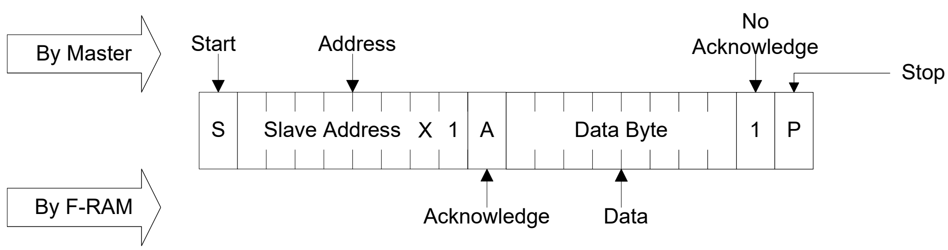


Figure 12. Sequential Read

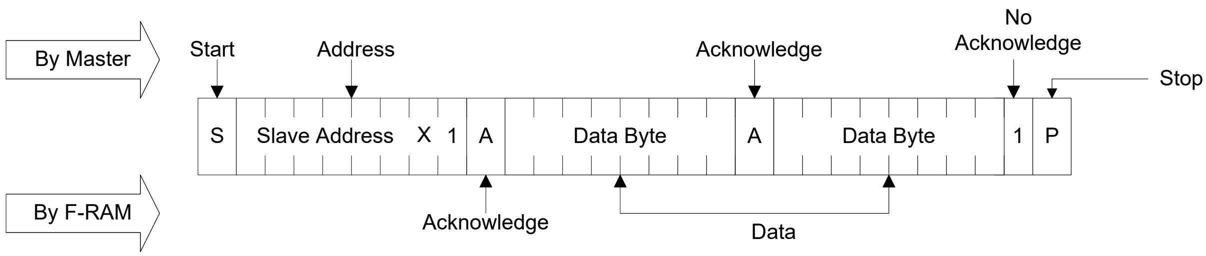
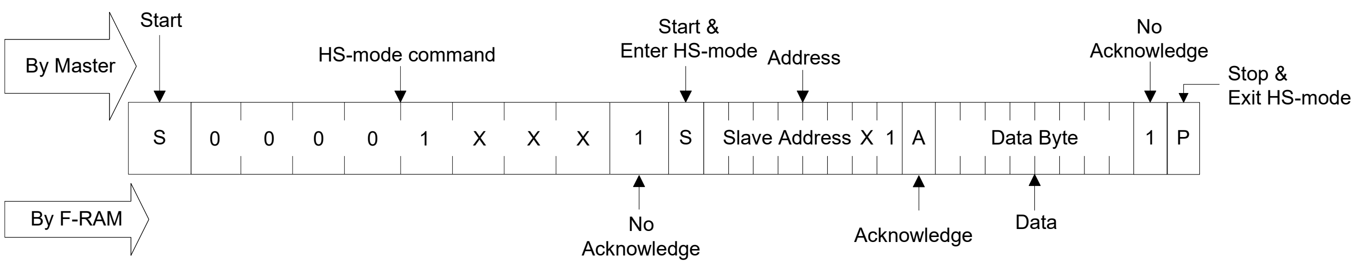


Figure 13. Hs-mode Current Address Read

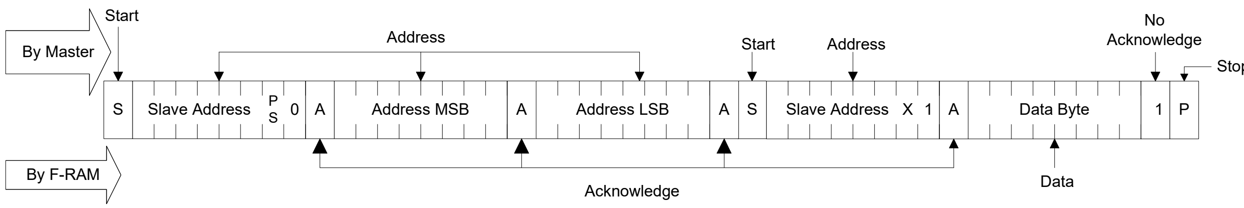


Selective (Random) Read

There is a simple technique that allows a user to select a random address location as the starting point for a read operation. This involves using the first three bytes of a write operation to set the internal address followed by subsequent read operations.

To perform a selective read, the bus master sends out the slave address with the LSB (R/W) set to 0. This specifies a write operation. According to the write protocol, the bus master then sends the address bytes that are loaded into the internal address latch. After the FM24V10 acknowledges the address, the bus master issues a START condition. This simultaneously aborts the write operation and allows the read command to be issued with the slave address LSB set to a '1'. The operation is now a current address read.

Figure 14. Selective (Random) Read



Sleep Mode

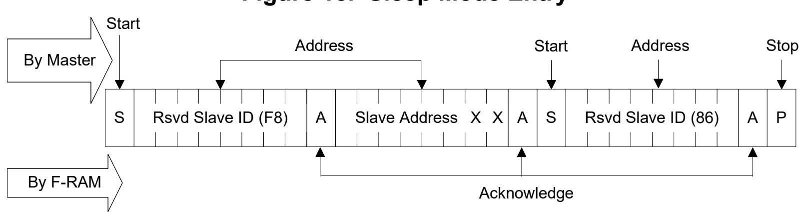
A low power mode called Sleep Mode is implemented on the FM24V10 device. The device will enter this low power state when the Sleep command 86h is clocked-in. Sleep Mode entry can be entered as follows:

1. The master sends a START command.
2. The master sends Reserved Slave ID F8h.
3. The FM24V10 sends an ACK.
4. The master sends the I^2C-bus slave address of the slave device it needs to identify. The last bit is a 'Don't care' value (page select and R/W bits). Only one device must acknowledge this byte (the one that has the I^2C-bus slave address).
5. The FM24V10 sends an ACK.
6. The master sends a Re-START command.
7. The master sends Reserved Slave ID 86h.
8. The FM24V10 sends an ACK.
9. The master sends STOP to ensure the device enters sleep mode.

Note Errata: Step 9 - Sending STOP is an optional step for FM24V10. The FM24V10 starts entering the Sleep mode from step 8 and releases the SDA line when in the Sleep mode. The LOW to HIGH transition on the SDA line when I^2C clock is HIGH generates an unintended STOP. For more information, see Errata on page 19.

Once in sleep mode, the device draws I_{ZZ} current, but the device continues to monitor the I^2C pins. Once the master sends a Slave Address that the FM24V10 identifies, it will "wakeup" and be ready for normal operation within t_{REC} time. As an alternative method of determining when the device is ready, the master can send read or write commands and look for an ACK. While the device is waking up, it will NACK the master until it is ready.

Figure 15. Sleep Mode Entry



Device ID

The FM24V10 device incorporates a means of identifying the device by providing three bytes of data, which are manufacturer ID, product ID, and die revision. The Device ID is read-only. It can be accessed as follows:

1. The master sends a START command.
2. The master sends Reserved Slave ID F8h.
3. The FM24V10 sends an ACK.
4. The master sends the I^2C-bus slave address of the slave device it needs to identify. The last bit is a 'Don't care' value (page select and R/W bits). Only one device must acknowledge this byte (the one that has the I^2C-bus slave address).
5. The FM24V10 sends an ACK.
6. The master sends a Re-START command.
7. The master sends Reserved Slave ID F9h.
8. The FM24V10 sends an ACK.
9. The Device ID Read can be done, starting with the 12 manufacturer bits, followed by the 9 device identification bits, and then the 3 die revision bits.
10. The master ends the Device ID read sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

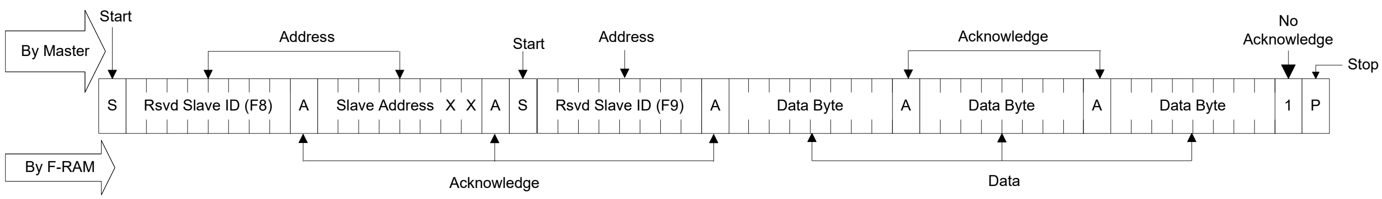
Note The reading of the Device ID can be stopped anytime by sending a NACK command.

Table 1. Device ID

Device	Device ID (3 bytes)	Device ID Description			
		23–12 (12 bits)	11–8 (4 bits)	7–3 (5 bits)	2–0 (3 bits)
		Manufacturer ID	Product ID		
			Density	Variation	Die Rev
FM24V10	004400h	000000000100	0100	N0000	000
FM24VN10	004480h	000000000100	0100	10000	000

Note Product ID bit 4 = S/N, Product ID bit 0 = reserved.

Figure 16. Read Device ID



Unique Serial Number (FM24VN10 only)

The FM24VN10 device also incorporates a read-only 8-byte serial number. It can be used to uniquely identify a pc board or system. The serial number includes a 40-bit unique number, an 8-bit CRC, and a 16-bit number that can be defined upon request by the customer. If a customer-specific number is not requested, the 16-bit Customer Identifier is 0000h. The 8 bytes of data are accessed via a slave address sequence similar to the Device ID. The serial number can be read by the system as follows:

1. The master sends a START command
2. The master sends Reserved Slave ID F8h
3. The FM24VN10 sends an ACK.
4. The master sends the I²C-bus slave address of the slave device it needs to identify. The last two bits are 'Don't care' values. Only one device must acknowledge this byte (the one that has the I²C-bus slave address).
5. The FM24VN10 sends an ACK.
6. The master sends a Re-START command
7. The master sends Reserved Slave ID CDh to read the serial number.
8. The FM24VN10 sends an ACK.
9. The master ends the serial number read sequence by NACKing the last byte, thus resetting the slave device state machine and allowing the master to send the STOP command.

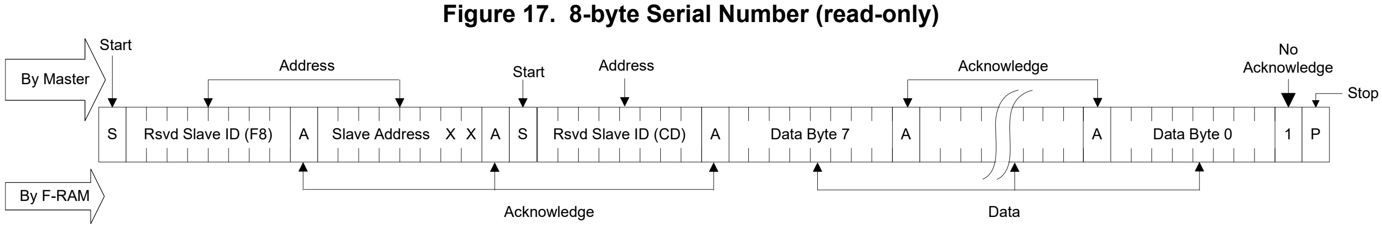
The 8-bit CRC value can be used to compare to the value calculated by the controller. If the two values match, then the communication between slave and master was performed without errors. The function (shown in Function to Calculate CRC on page 11) is used to calculate the CRC value. To perform the calculation, 7 bytes of data are filled into a memory buffer in the same order as they are read from the part - i.e. byte7, byte6, byte5, byte4, byte3, byte2, byte1 of the serial number. The calculation is performed on the 7 bytes, and the result should match the final byte out from the part which is byte0, the 8-bit CRC value.

Table 2. 8-Byte Serial Number (read-only)

Customer IDENTIFIER		40-bit UNIQUE NUMBER					8-bit CRC
SN(63–56)	SN(55–48)	SN(47–40)	SN(39–32)	SN(31–24)	SN(23–16)	SN(15–8)	SN(7–0)

Note Contact factory for requesting a customer identifier number.

Figure 17. 8-byte Serial Number (read-only)



Function to Calculate CRC

```
BYTE calcCRC8( BYTE* pData, int nBytes )
{
  static BYTE crctable[256] = {
        0x00, 0x07, 0x0E, 0x09, 0x1C, 0x1B, 0x12, 0x15,
        0x38, 0x3F, 0x36, 0x31, 0x24, 0x23, 0x2A, 0x2D,
        0x70, 0x77, 0x7E, 0x79, 0x6C, 0x6B, 0x62, 0x65,
        0x48, 0x4F, 0x46, 0x41, 0x54, 0x53, 0x5A, 0x5D,
        0xE0, 0xE7, 0xEE, 0xE9, 0xFC, 0xFB, 0xF2, 0xF5,
        0xD8, 0xDF, 0xD6, 0xD1, 0xC4, 0xC3, 0xCA, 0xCD,
        0x90, 0x97, 0x9E, 0x99, 0x8C, 0x8B, 0x82, 0x85,
        0xA8, 0xAF, 0xA6, 0xA1, 0xB4, 0xB3, 0xBA, 0xBD,
        0xC7, 0xC0, 0xC9, 0xCE, 0xDB, 0xDC, 0xD5, 0xD2,
        0xFF, 0xF8, 0xF1, 0xF6, 0xE3, 0xE4, 0xED, 0xEA,
        0xB7, 0xB0, 0xB9, 0xBE, 0xAB, 0xAC, 0xA5, 0xA2,
        0x8F, 0x88, 0x81, 0x86, 0x93, 0x94, 0x9D, 0x9A,
        0x27, 0x20, 0x29, 0x2E, 0x3B, 0x3C, 0x35, 0x32,
        0x1F, 0x18, 0x11, 0x16, 0x03, 0x04, 0x0D, 0x0A,
        0x57, 0x50, 0x59, 0x5E, 0x4B, 0x4C, 0x45, 0x42,
        0x6F, 0x68, 0x61, 0x66, 0x73, 0x74, 0x7D, 0x7A,
        0x89, 0x8E, 0x87, 0x80, 0x95, 0x92, 0x9B, 0x9C,
        0xB1, 0xB6, 0xBF, 0xB8, 0xAD, 0xAA, 0xA3, 0xA4,
        0xF9, 0xFE, 0xF7, 0xF0, 0xE5, 0xE2, 0xEB, 0xEC,
        0xC1, 0xC6, 0xCF, 0xC8, 0xDD, 0xDA, 0xD3, 0xD4,
        0x69, 0x6E, 0x67, 0x60, 0x75, 0x72, 0x7B, 0x7C,
        0x51, 0x56, 0x5F, 0x58, 0x4D, 0x4A, 0x43, 0x44,
        0x19, 0x1E, 0x17, 0x10, 0x05, 0x02, 0x0B, 0x0C,
        0x21, 0x26, 0x2F, 0x28, 0x3D, 0x3A, 0x33, 0x34,
        0x4E, 0x49, 0x40, 0x47, 0x52, 0x55, 0x5C, 0x5B,
        0x76, 0x71, 0x78, 0x7F, 0x6A, 0x6D, 0x64, 0x63,
        0x3E, 0x39, 0x30, 0x37, 0x22, 0x25, 0x2C, 0x2B,
        0x06, 0x01, 0x08, 0x0F, 0x1A, 0x1D, 0x14, 0x13,
        0xAE, 0xA9, 0xA0, 0xA7, 0xB2, 0xB5, 0xBC, 0xBB,
        0x96, 0x91, 0x98, 0x9F, 0x8A, 0x8D, 0x84, 0x83,
        0xDE, 0xD9, 0xD0, 0xD7, 0xC2, 0xC5, 0xCC, 0xCB,
        0xE6, 0xE1, 0xE8, 0xEF, 0xFA, 0xFD, 0xF4, 0xF3

 };
BYTE crc = 0;
.................... while( nBytes-- ) crc = crctable[crc ^ *pData++];
  return crc;
}
```

Maximum Ratings

Exceeding maximum ratings may shorten the useful life of the device. These user guidelines are not tested.

Storage temperature .... –65 °C to +125 °C

Maximum accumulated storage time
At 125 °C ambient temperature .... 1000 h
At 85 °C ambient temperature .... 10 Years

Ambient temperature
with power applied .... –55 °C to +125 °C

Supply voltage on V_{DD} relative to V_{SS} ....–1.0 V to +4.5 V

Input voltage .... –1.0 V to + 4.5 V and $V_{IN} < V_{DD}$ + 1.0 V

DC voltage applied to outputs
in High-Z state ....–0.5 V to V_{DD} + 0.5 V

Transient voltage (< 20 ns)
on any pin to ground potential ....–2.0 V to V_{DD} + 2.0 V

Package power dissipation capability
(T_A = 25 °C) .... 1.0 W

Surface mount lead soldering temperature
(10 seconds) .... +260 °C

Electrostatic Discharge Voltage
Human Body Model (AEC-Q100-002 Rev. E) .... 2.5 kV
Charged Device Model (AEC-Q100-011 Rev. B) .... 1.25 kV
Machine Model (AEC-Q100-003 Rev. E) .... 200 V

Latch-up current .... > 140 mA

* Exception: The "$V_{IN} < V_{DD}$ + 1.0 V" restriction does not apply to the SCL and SDA inputs.

Operating Range

Range	Ambient Temperature (T_A)	V_{DD}
Industrial	–40 °C to +85 °C	2.0 V to 3.6 V

DC Electrical Characteristics

Over the Operating Range

Parameter	Description	Test Conditions		Min	Typ [1]	Max	Unit
V_{DD}	Power supply			2.0	3.3	3.6	V
I_{DD}	Average V_{DD} current	SCL toggling between V_{DD} – 0.2 V and V_{SS}, other inputs V_{SS} or V_{DD} – 0.2 V.	f_{SCL} = 100 kHz	–	–	175	µA
			f_{SCL} = 1 MHz	–	–	400	µA
			f_{SCL} = 3.4 MHz	–	–	1000	µA
I_{SB}	Standby current	SCL = SDA = V_{DD}. All other inputs V_{SS} or V_{DD}. Stop command issued.		–	90	150	µA
I_{ZZ}	Sleep mode current	SCL = SDA = V_{DD}. All other inputs V_{SS} or V_{DD}. Stop command issued.		–	5	8	µA
I_{LI}	Input leakage current (Except WP and A2–A1)	$V_{SS} \le V_{IN} \le V_{DD}$		–1	–	+1	µA
	Input leakage current (for WP and A2–A1)	$V_{SS} \le V_{IN} \le V_{DD}$		–1	–	+100	µA
I_{LO}	Output leakage current	$V_{SS} \le V_{IN} \le V_{DD}$		–1	–	+1	µA
V_{IH}	Input HIGH voltage			0.7 × V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input LOW voltage			–0.3	–	0.3 × V_{DD}	V
V_{OL1}	Output LOW voltage	I_{OL} = 2 mA, $V_{DD} \ge$ 2.7 V		–	–	0.4	V
V_{OL2}	Output LOW voltage	I_{OL} = 150 µA		–	–	0.2	V
R_{in} [2]	Input resistance (WP, A2–A1)	For $V_{IN} = V_{IL\ (Max)}$		50	–	–	kΩ
		For $V_{IN} = V_{IH\ (Min)}$		1	–	–	MΩ

Notes
1. Typical values are at 25 °C, V_{DD} = V_{DD} (typ). Not 100% tested.
2. The input pull-down circuit is strong (50 kΩ) when the input voltage is below V_{IL} and weak (1 MΩ) when the input voltage is above V_{IH}.

Data Retention and Endurance

Parameter	Description	Test condition	Min	Max	Unit
T_{DR}	Data retention	T_A = 85 °C	10	–	Years
		T_A = 75 °C	38	–	
		T_A = 65 °C	151	–	
NV_C	Endurance	Over operating temperature	10^{14}	–	Cycles

Capacitance

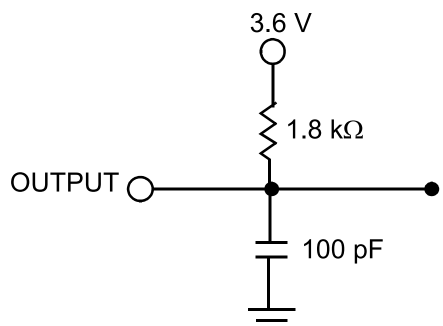
Parameter [3]	Description	Test Conditions	Max	Unit
C_O	Output pin capacitance (SDA)	T_A = 25 °C, f = 1 MHz, V_{DD} = V_{DD}(typ)	8	pF
C_I	Input pin capacitance		6	pF

Thermal Resistance

Parameter [3]	Description	Test Conditions	8-pin SOIC	Unit
Θ_{JA}	Thermal resistance (junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	138	°C/W
Θ_{JC}	Thermal resistance (junction to case)		40	°C/W

AC Test Loads and Waveforms

Figure 18. AC Test Loads and Waveforms



AC Test Conditions

Input pulse levels ....10% and 90% of V_{DD}
Input rise and fall times ....10 ns
Input and output timing reference levels ....0.5 × V_{DD}
Output load capacitance .... 100 pF

Note
3. These parameters are guaranteed by design and are not tested.

AC Switching Characteristics

Over the Operating Range

Parameter [4]		Description	F/S-mode [5]		Hs-mode[5]		Unit
Cypress Parameter	Alt. Parameter		Min	Max	Min	Max	
f_{SCL}[6]		SCL clock frequency	–	1.0	–	3.4	MHz
$t_{SU; STA}$		Start condition setup for repeated Start	260	–	160	–	ns
$t_{HD;STA}$		Start condition hold time	260	–	160	–	ns
t_{LOW}		Clock LOW period	500	–	160	–	ns
t_{HIGH}		Clock HIGH period	260	–	60	–	ns
$t_{SU;DAT}$[7]	$t_{SU;DATA}$	Data in setup	50	–	10	–	ns
$t_{HD;DAT}$	$t_{HD;DATA}$	Data in hold	0	–	0	–	ns
t_{DH}		Data output hold (from SCL @ V_{IL})	0	–	0	–	ns
t_R[8]	t_r	Input rise time	–	120	–	80	ns
t_F[8]	t_f	Input fall time	–	120	–	80	ns
$t_{SU;STO}$		STOP condition setup	260	–	160	–	ns
t_{AA}	$t_{VD;DATA}$	SCL LOW to SDA Data Out Valid	–	450	–	130	ns
t_{BUF}		Bus free before new transmission	500	–	300	–	ns
t_{SP}		Noise suppression time constant on SCL, SDA	–	50	–	5	ns

Figure 19. Read Bus Timing Diagram

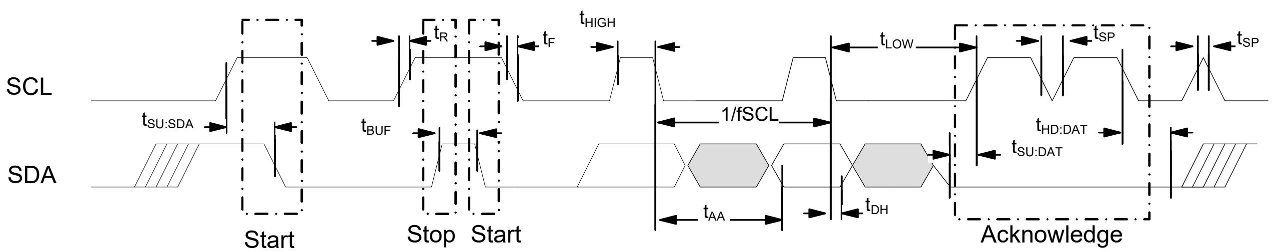
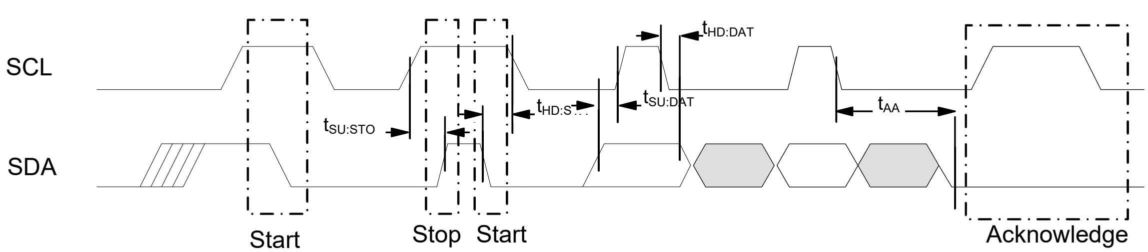


Figure 20. Write Bus Timing Diagram



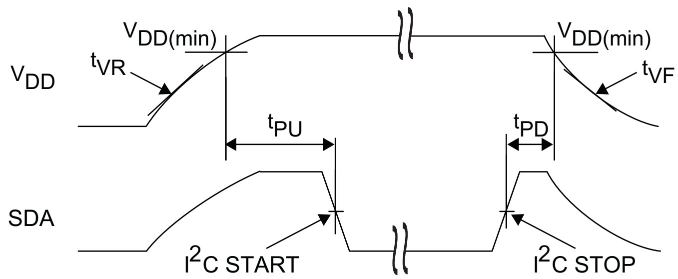
Notes
4. Test conditions assume signal transition time of 10 ns or less, timing reference levels of $V_{DD}/2$, input pulse levels of 0 to V_{DD}(typ), and output loading of the specified I_{OL} and load capacitance shown in Figure 18 on page 13.
5. Bus Load (Cb) considerations; Cb < 500 pF for I[2]C clock frequency (SCL) 1 MHz; Cb < 100 pF for SCL at 3.4 MHz.
6. The speed-related specifications are guaranteed characteristic points along a continuous curve of operation from DC to f_{SCL} (max).
7. In Hs-mode and V_{DD} < 2.7 V, the $t_{SU:DAT}$ (min.) spec is 15 ns.
8. These parameters are guaranteed by design and are not tested.

Power Cycle Timing

Over the Operating Range

Parameter	Description	Min	Max	Unit
t_{PU}	Power-up V_{DD}(min) to first access (START condition)	250	–	µs
t_{PD}	Last access (STOP condition) to power-down (V_{DD}(min))	0	–	µs
t_{VR} [9, 10]	V_{DD} power-up ramp rate	50	–	µs/V
t_{VF} [9, 10]	V_{DD} power-down ramp rate	100	–	µs/V
t_{REC} [10]	Recovery time from sleep mode	–	400	µs

Figure 21. Power Cycle Timing



Notes
9. Slope measured at any point on the V_{DD} waveform.
10. Guaranteed by design.

Ordering Information

Ordering Code	Package Diagram	Package Type	Operating Range
FM24V10-G	51-85066	8-pin SOIC	Industrial
FM24V10-GTR			
FM24VN10-G		8-pin SOIC, Serial Number	
FM24VN10-GTR			

All these parts are Pb-free. Contact your local Cypress sales representative for availability of these parts.

Ordering Code Definitions

FM 24 V N 10 - G X

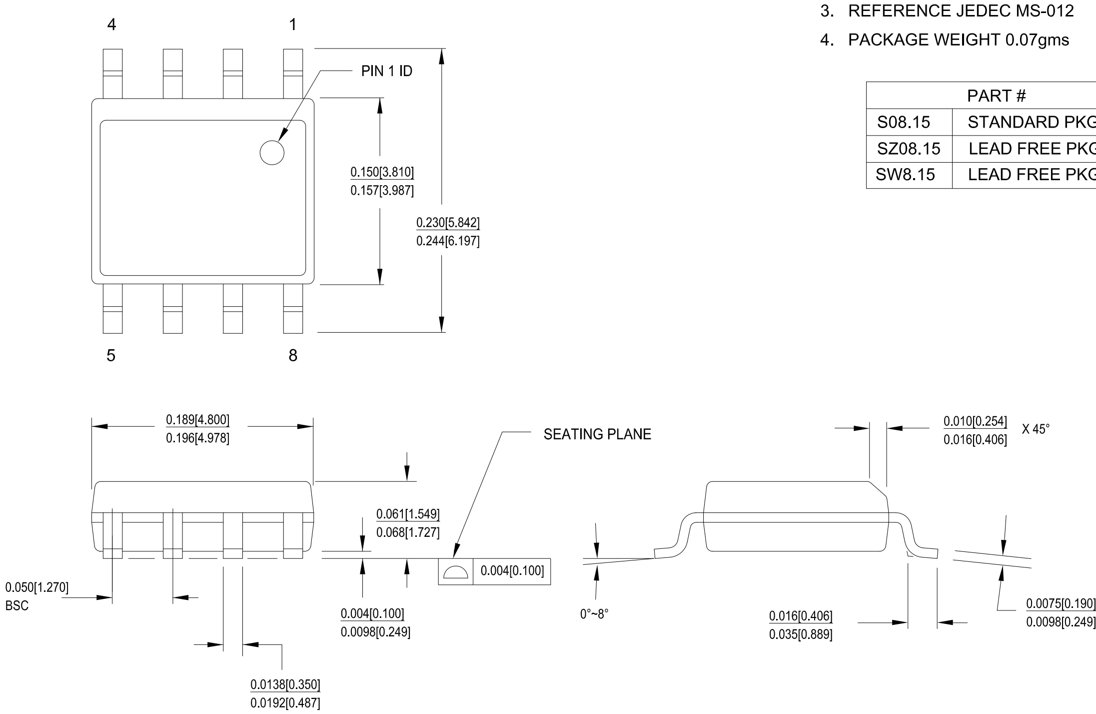
- X — Option: X = Blank or TR
  Blank = Standard; TR = Tape and Reel
- G — Package Type:
  G = 8-pin SOIC
- 10 — Density: 10 = 1-Mbit
- N — N = Serial Number
- V — Voltage: V = 2.0 V to 3.6 V
- 24 — I^2C F-RAM
- FM — Cypress

Package Diagram

Figure 22. 8-pin SOIC (150 Mils) Package Outline, 51-85066

1. DIMENSIONS IN INCHES[MM] MIN. / MAX.
2. PIN 1 ID IS OPTIONAL, ROUND ON SINGLE LEADFRAME RECTANGULAR ON MATRIX LEADFRAME
3. REFERENCE JEDEC MS-012
4. PACKAGE WEIGHT 0.07gms

PART #	
S08.15	STANDARD PKG
SZ08.15	LEAD FREE PKG
SW8.15	LEAD FREE PKG



51-85066 *I

Acronyms

Acronym	Description
ACK	Acknowledge
CMOS	Complementary Metal Oxide Semiconductor
EIA	Electronic Industries Alliance
I^2C	Inter-Integrated Circuit
I/O	Input/Output
JEDEC	Joint Electron Devices Engineering Council
LSB	Least Significant Bit
MSB	Most Significant Bit
NACK	No Acknowledge
RoHS	Restriction of Hazardous Substances
$R/\overline{W}$	Read/Write
SCL	Serial Clock Line
SDA	Serial Data Access
SOIC	Small Outline Integrated Circuit
WP	Write Protect

Document Conventions

Units of Measure

Symbol	Unit of Measure
°C	degree Celsius
Hz	hertz
Kb	1024 bit
kHz	kilohertz
kΩ	kilohm
MHz	megahertz
MΩ	megaohm
µA	microampere
µs	microsecond
mA	milliampere
ms	millisecond
ns	nanosecond
Ω	ohm
%	percent
pF	picofarad
V	volt
W	watt

Errata

This document describes the errata for the serial I^{2}C F-RAM FM24V10/FM24VN10 (1-Mbit) product. Details include errata trigger conditions, scope of impact, available workarounds, and silicon revision applicability. Compare this document to the device's datasheet for a complete functional description.

Contact your local Cypress Sales Representative if you have questions. You can also send your related queries directly to cypressfram@cypress.com.

Part Numbers Affected

Part Number	Device Characteristics
FM24V10	1-Mbit (128K × 8) Serial (I^{2}C) F-RAM with Device ID, 2.0 V to 3.6 V, Industrial temperature
FM24VN10	1-Mbit (128K × 8) Serial (I^{2}C) F-RAM with Device ID and Unique Serial Number, 2.0 V to 3.6 V, Industrial temperature

FM24V10/FM24VN10 I^{2}C F-RAM Qualification Status

Production parts.

FM24V10/FM25VN10 Errata Summary

The following table defines the errata applicability to available FM24V10/FM24VN10 devices.

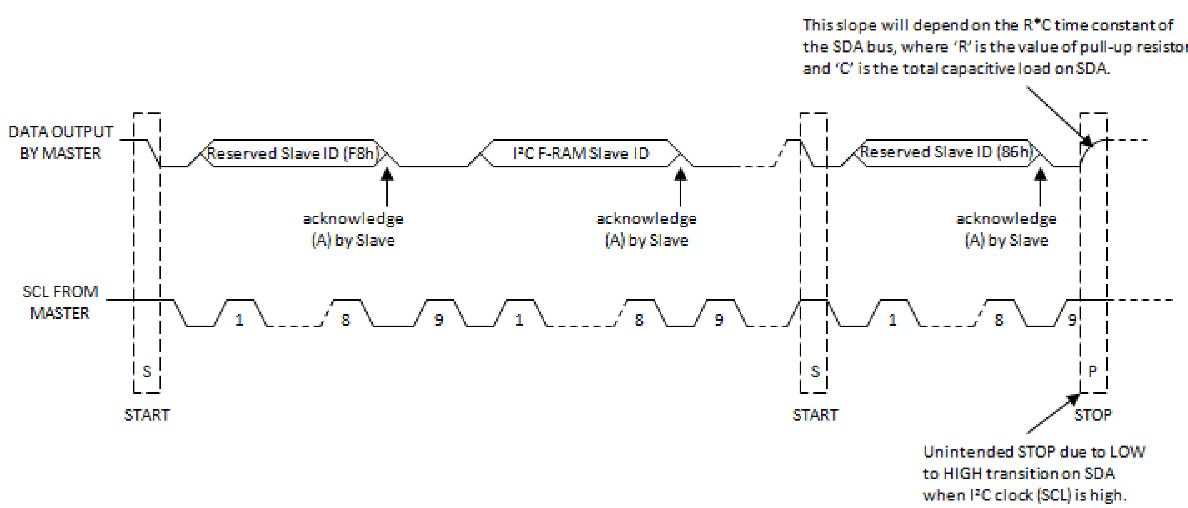
Items	Part Number	Silicon Revision	Fix Status
1. The I2C F-RAM enters Sleep mode without the STOP condition	FM24V10-G FM24V10-GTR FM24VN10-G FM24VN10-GTR	Rev A	None.

1. The I^{2}C F-RAM enters Sleep mode without the STOP condition

■ **Problem Definition**

When the I^{2}C master sends the last Reserved Slave ID (86h) of the Sleep command sequence, as shown in Figure 23, the I^{2}C F-RAM returns an acknowledgement (ACK) and releases the SDA line after the rising edge of the 9th clock. If this LOW to HIGH transition on the SDA line happens when the I^{2}C clock is HIGH, it artificially generates an unintended STOP.

Figure 23. I^{2}C F-RAM Sleep Cycle



- **Parameters Affected**

  None of the existing parameters are affected.

- **Trigger Condition(S)**

  The I^2C master sends the last Reserved Slave ID (86h) of the Sleep command and receives an ACK from the I^2C F-RAM. The I^2C F-RAM starts entering the Sleep mode from the 9th rising edge of the I^2C clock and releases the SDA line when in the Sleep mode. The LOW to HIGH transition on the SDA line when I^2C clock is HIGH generates an unintended STOP.

- **Scope of Impact**

  The ongoing I^2C communication can be disrupted due to unintended STOP generated by the I^2C F-RAM slave.

- **Workaround**

  This issue can be mitigated by implementing one of the following two methods:
  - The I^2C master ignores any unintended STOP generated by the I^2C F-RAM slave.
  - The I^2C master latches the ACK on the 9th rising edge of the I^2C clock and starts driving the SDA line LOW. This will ensure when the I^2C F-RAM enters Sleep and releases the SDA line; it still remains LOW driven by the I^2C master. This will prevent unintended LOW to HIGH transition when SCL is LOW.

- **Fix Status**

  This issue is applicable to all the existing I^2C F-RAM parts shown in this errata. The existing parts are in production status and will continue serving with errata. There is no plan to fix this issue in the existing silicon.

Document History Page

Document Title: FM24V10, 1-Mbit (128K × 8) Serial (I^2C) F-RAM Document Number: 001-84463				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	3902204	GVCH	02/25/2013	New spec
*A	3996669	GVCH	05/13/2013	Added Appendix A - Errata for FM24V10 and FM24VN10
*B	4045469	GVCH	06/30/2013	All errata items are fixed and the errata is removed.
*C	4283424	GVCH	02/18/2014	Updated Maximum Ratings: Added “Maximum junction temperature” and its corresponding details. Added “DC voltage applied to outputs in High-Z state” and its corresponding details. Added “Transient voltage (< 20 ns) on any pin to ground potential” and its corresponding details. Added “Package power dissipation capability (T_A = 25 °C)” and its corresponding details. Removed “Package Moisture Sensitivity Level (MSL)” and its corresponding details. Added “Latch-up current” and its corresponding details. Updated DC Electrical Characteristics: Removed existing details of I_{LI} parameter and splitted I_{LI} parameter into two rows namely “Input leakage current (Except WP and A2–A1)” and “Input leakage current (for WP and A2–A1)” and added corresponding values. Updated Data Retention and Endurance: Removed existing details of T_{DR} parameter. Added details of T_{DR} parameter corresponding to “T_A = 85 °C”, “T_A = 75 °C” and “T_A = 65 °C”. Added NV_C parameter and its corresponding details. Added Thermal Resistance. Updated Package Diagram: Removed Package Marking Scheme (top mark). Removed “Ramtron Revision History”. Updated to Cypress template. Completing Sunset Review.
*D	4564960	GVCH	11/10/2014	Updated Functional Description: Added “For a complete list of related documentation, click here.” at the end.
*E	4700243	GVCH	03/26/2015	Updated Package Diagram: spec 51-85066 – Changed revision from *F to *G. Added Errata.
*F	4781095	GVCH	05/29/2015	Updated Ordering Information: No change in part numbers. Fixed Typo (Replaced “001-85066” with “51-85066” in “Package Diagram” column). Updated to new template.
*G	4874648	ZSK / PSR	08/06/2015	Updated Maximum Ratings: Removed “Maximum junction temperature” and its corresponding details. Added “Maximum accumulated storage time” and its corresponding details. Added “Ambient temperature with power applied” and its corresponding details.

Document History Page (continued)

Document Title: FM24V10, 1-Mbit (128K × 8) Serial (I^2C) F-RAM Document Number: 001-84463				
Rev.	**ECN No.**	**Orig. of Change**	**Submission Date**	**Description of Change**
*H	5366088	GVCH	07/22/2016	Updated Pin Definitions: Added details corresponding to “NC” pin. Updated Package Diagram: spec 51-85066 – Changed revision from *G to *H. Updated to new template.
*I	5738855	GNKK	05/16/2017	Updated Cypress logo and copyright.
*J	6422002	GVCH	12/26/2018	Updated Maximum Ratings: Replaced “–55 °C to +125 °C” with “–65 °C to +125 °C” in ratings corresponding to “Storage temperature”. Updated Package Diagram: spec 51-85066 – Changed revision from *H to *I. Updated to new template. Completing Sunset Review.