

Gate Drive Optocoupler, High Noise Immunity, 2.5 A Output Current

FOD3120

Description

The FOD3120 is a 2.5 A Output Current Gate Drive Optocoupler, capable of driving most medium power IGBT/MOSFET. It is ideally suited for fast switching driving of power IGBT and MOSFETs used in motor control inverter applications, and high performance power system.

It utilizes onsemi's coplanar packaging technology, OPTOPLANAR[®], and optimized IC design to achieve high noise immunity, characterized by high common mode rejection.

It consists of a gallium aluminum arsenide (AlGaAs) light emitting diode optically coupled to an integrated circuit with a high-speed driver for push-pull MOSFET output stage.

Features

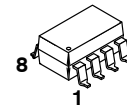
- High Noise Immunity Characterized by 35 kV/μs Minimum Common Mode Rejection
- 2.5 A Peak Output Current Driving Capability for Most 1200 V/20 A IGBT
- Use of P-Channel MOSFETs at Output Stage Enables Output Voltage Swing Close to the Supply Rail
- Wide Supply Voltage Range from 15 V to 30 V
- Fast Switching Speed
 - ◆ 400 ns maximum Propagation Delay
 - ◆ 100 ns maximum Pulse Width Distortion
- Under Voltage LockOut (UVLO) with Hysteresis
- Extended Industrial Temperature Range, -40°C to 100°C Temperature Range
- Safety and Regulatory Approvals
 - ◆ UL1577, 5000 V_{RMS} for 1 min.
 - ◆ DIN EN/IEC60747-5-5
- R_{DS(ON)} of 1 Ω (typ.) Offers Lower Power Dissipation
- >8.0 mm Clearance and Creepage Distance (Option 'T' or 'TS')
- 1414 V Peak Working Insulation Voltage (V_{IORM})
- This is a Pb-Free Device

Applications

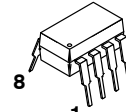
- Industrial Inverter
- Uninterruptible Power Supply
- Induction Heating
- Isolated IGBT/Power MOSFET Gate Drive

Related Resources

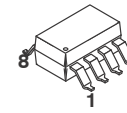
- FOD3150, 1 A Output Current, Gate Drive Optocoupler Datasheet
- <https://www.onsemi.com/products/optoelectronics/>



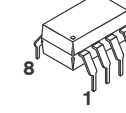
PDIP8 GW
CASE 709AC



PDIP8 9.655x6.6, 2.54P
CASE 646CQ

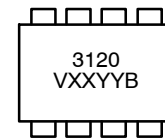


PDIP8 GW
CASE 709AD



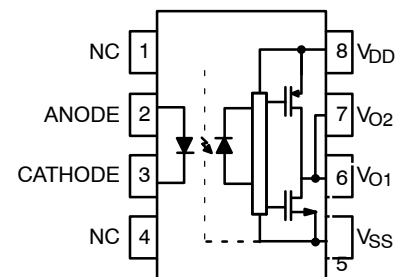
PDIP8 6.6x3.81, 2.54P
CASE 646BW

MARKING DIAGRAM



- 3120 = Device Number
- V = DIN_EN/IEC60747-5-5 Option (only appears on component ordered with this option)
- XX = Two Digit Year Code
- YY = Two Digit Work Week
- B = Assembly Package Code

FUNCTIONAL BLOCK DIAGRAM



Note: A 0.1 μF bypass capacitor must be connected between pins 5 and 8.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

FOD3120

Table 1. TRUTH TABLE

LED	V _{DD} – V _{SS} “Positive Going” (Turn-on)	V _{DD} – V _{SS} “Negative Going” (Turn-off)	V _O
Off	0 V to 30 V	0 V to 30 V	Low
On	0 V to 11.5 V	0 V to 10 V	Low
On	11.5 V to 13.5 V	10 V to 12 V	Transition
On	13.5 V to 30 V	12 V to 30 V	High

Table 2. PIN DEFINITIONS

Pin #	Name	Description
1	NC	Not Connected
2	Anode	LED Anode
3	Cathode	LED Cathode
4	NC	Not Connected
5	V _{SS}	Negative Supply Voltage
6	V _{O2}	Output Voltage 2 (internally connected to V _{O1})
7	V _{O1}	Output Voltage 1
8	V _{DD}	Positive Supply Voltage

Table 3. SAFETY AND INSULATION RATINGS

As per DIN EN/IEC 60747-5-5. This optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	< 150 V _{RMS}	I-IV		
		< 300 V _{RMS}	I-IV		
		< 450 V _{RMS}	I-III		
		< 600 V _{RMS}	I-III		
		< 1000 V _{RMS} (Option T, TS)	I-III		
	Climatic Classification		40/100/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
V _{PR}	Input to Output Test Voltage, Method A, V _{IORM} × 1.6 = V _{PR} , Type and Sample Test with t _m = 10 s, Partial Discharge < 5 pC	2262			V _{peak}
	Input to Output Test Voltage, Method B, V _{IORM} × 1.875 = V _{PR} , 100% Production Test with t _m = 1 s, Partial Discharge < 5 pC	2651			V _{peak}
V _{IORM}	Maximum Working Insulation Voltage	1414			V _{peak}
V _{IOTM}	Highest Allowable Over Voltage	6000			V _{peak}
	External Creepage	8.0			mm
	External Clearance	7.4			mm
	External Clearance (for Option T or TS, 0.4” Lead Spacing)	10.16			mm
DTI	Distance Through Insulation (Insulation Thickness)	0.5			mm
T _S	Case Temperature (Note 1)	175			°C
I _{S,INPUT}	Input Current (Note 1)	400			mA
P _{S,OUTPUT}	Output Power (Duty Factor ≤ 2.7 %) (Note 1)	700			mW
R _{IO}	Insulation Resistance at T _S , V _{IO} = 500 V (Note 1)	10 ⁹			Ω

1. Safety limit value – maximum values allowed in the event of a failure.

FOD3120

Table 4. ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise specified.)

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	-55 to +125	$^\circ\text{C}$
T_{OPR}	Operating Temperature	-40 to +100	$^\circ\text{C}$
T_J	Junction Temperature	-40 to +125	$^\circ\text{C}$
T_{SOL}	Lead Wave Solder Temperature (refer to page 13 for reflow solder profile)	260 for 10 s	$^\circ\text{C}$
$I_{F(AVG)}$	Average Input Current	25	mA
$I_{F(PEAK)}$	Peak Transient Forward Current (Note 2)	1	A
f	Operating Frequency (Note 3)	50	kHz
V_R	Reverse Input Voltage	5	V
$I_{O(PEAK)}$	Peak Output Current (Note 4)	3.0	A
$V_{DD} - V_{SS}$	Supply Voltage		V
		$T_A \geq 90^\circ\text{C}$	
$V_{O(PEAK)}$	Peak Output Voltage	0 to V_{DD}	V
$t_{R(IN)}, t_{F(IN)}$	Input Signal Rise and Fall Time	500	ns
PD_I	Input Power Dissipation (Note 5, Note 7)	45	mW
PD_O	Output Power Dissipation (Note 6, Note 7)	250	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Pulse Width, $PW \leq 1 \mu\text{s}$, 300 pps
- Exponential Waveform, $I_{O(PEAK)} \leq |2.5 \text{ A}| (\leq 0.3 \mu\text{s})$
- Maximum pulse width = 10 μs , maximum duty cycle = 1.1%
- Derate linearly above 87°C , free air temperature at a rate of 0.77 mW/ $^\circ\text{C}$
- No derating required across temperature range.
- Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

Table 5. RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Units
T_A	Ambient Operating Temperature	-40 to +100	$^\circ\text{C}$
$V_{DD} - V_{SS}$	Power Supply	15 to 30	V
$I_{F(ON)}$	Input Current (ON)	7 to 16	mA
$V_{F(OFF)}$	Input Voltage (OFF)	0 to 0.8	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

Table 6. ISOLATION CHARACTERISTICS

Apply over all recommended conditions, typical value is measured at $T_A = 25^\circ\text{C}$

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ISO}	Input-Output Isolation Voltage	$T_A = 25^\circ\text{C}$, R.H. < 50 %, $t = 1.0 \text{ min.}$, $I_{I-O} \leq 10 \mu\text{A}$, 50 Hz (Note 8, Note 9)	5000			V_{RMS}
R_{ISO}	Isolation Resistance	$V_{I-O} = 500 \text{ V}$ (Note 8)		10^{11}		Ω
C_{ISO}	Isolation Capacitance	$V_{I-O} = 0 \text{ V}$, Frequency = 1.0 MHz (Note 8)		1		pF

- Device is considered a two terminal device: pins 2 and 3 are shorted together and pins 5, 6, 7 and 8 are shorted together.
- 5000 V_{RMS} for 1 minute duration is equivalent to 6000 V_{ACRMS} for 1 second duration.

FOD3120

Table 7. ELECTRICAL CHARACTERISTICS

Apply over all recommended conditions, typical value is measured at $V_{DD} = 30\text{ V}$, $V_{SS} = \text{Ground}$, $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_F	Input Forward Voltage	$I_F = 10\text{ mA}$	1.2	1.5	1.8	V
$\Delta(V_F/T_A)$	Temperature Coefficient of Forward Voltage			-1.8		mV/°C
BV_R	Input Reverse Breakdown Voltage	$I_R = 10\text{ }\mu\text{A}$	5			V
C_{IN}	Input Capacitance	$f = 1\text{ MHz}$, $V_F = 0\text{ V}$		60		pF
I_{OH}	High Level Output Current (Note 3)	$V_O = V_{DD} - 3\text{ V}$	-1.0	-2.0	-2.5	A
		$V_O = V_{DD} - 6\text{ V}$	-2.0		-2.5	
I_{OL}	Low Level Output Current (Note 3)	$V_O = V_{SS} + 3\text{ V}$	1.0	2.0	2.5	A
		$V_O = V_{SS} + 6\text{ V}$	2.0		2.5	
V_{OH}	High Level Output Voltage	$I_F = 10\text{ mA}$, $I_O = -2.5\text{ A}$	$V_{DD} - 6.25\text{ V}$	$V_{DD} - 2.5\text{ V}$		V
		$I_F = 10\text{ mA}$, $I_O = -100\text{ mA}$	$V_{DD} - 0.25\text{ V}$	$V_{DD} - 0.1\text{ V}$		
V_{OL}	Low Level Output Voltage	$I_F = 0\text{ mA}$, $I_O = 2.5\text{ A}$		$V_{SS} + 2.5\text{ V}$	$V_{SS} + 6.25\text{ V}$	V
		$I_F = 0\text{ mA}$, $I_O = 100\text{ mA}$		$V_{SS} + 0.1\text{ V}$	$V_{SS} + 0.25\text{ V}$	
I_{DDH}	High Level Supply Current	$V_O = \text{Open}$, $I_F = 7\text{ to }16\text{ mA}$		2.8	3.8	mA
I_{DDL}	Low Level Supply Current	$V_O = \text{Open}$, $V_F = 0\text{ to }0.8\text{ V}$		2.8	3.8	mA
I_{FLH}	Threshold Input Current Low to High	$I_O = 0\text{ mA}$, $V_O > 5\text{ V}$		2.3	5.0	mA
V_{FHL}	Threshold Input Voltage High to Low	$I_O = 0\text{ mA}$, $V_O < 5\text{ V}$	0.8			V
V_{UVLO+}	Under Voltage Lockout Threshold	$I_F = 10\text{ mA}$, $V_O > 5\text{ V}$	11.5	12.7	13.5	V
V_{UVLO-}		$I_F = 10\text{ mA}$, $V_O < 5\text{ V}$	10.0	11.2	12.0	V
$UVLO_{HYS}$	Under Voltage Lockout Threshold Hysteresis			1.5		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Table 8. SWITCHING CHARACTERISTICS

Apply over all recommended conditions, typical value is measured at $V_{DD} = 30\text{ V}$, $V_{SS} = \text{Ground}$, $T_A = 25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
t_{PHL}	Propagation Delay Time to Logic Low Output	$I_F = 7\text{ mA to }16\text{ mA}$, $R_g = 10\text{ }\Omega$, $C_g = 10\text{ nF}$, $f = 10\text{ kHz}$, Duty Cycle = 50 %	150	275	400	ns
t_{PLH}	Propagation Delay Time to Logic High Output		150	255	400	ns
PWD	Pulse Width Distortion, $ t_{PHL} - t_{PLH} $			20	100	ns
PDD (Skew)	Propagation Delay Difference Between Any Two Parts or Channels, $(t_{PHL} - t_{PLH})$ (Note 10)			-250	250	ns
t_R	Output Rise Time (10% – 90%)				60	ns
t_F	Output Fall Time (90% – 10%)				60	ns
$t_{UVLO\text{ ON}}$	UVLO Turn On Delay		$I_F = 10\text{ mA}$, $V_O > 5\text{ V}$		1.6	
$t_{UVLO\text{ OFF}}$	UVLO Turn Off Delay	$I_F = 10\text{ mA}$, $V_O < 5\text{ V}$		0.4		μs
$ CM_H $	Common Mode Transient Immunity at Output High	$T_A = 25^\circ\text{C}$, $V_{DD} = 30\text{ V}$, $I_F = 7\text{ to }16\text{ mA}$, $V_{CM} = 2000\text{ V}$ (Note 11)	35	50		kV/ μs
$ CM_L $	Common Mode Transient Immunity at Output Low	$T_A = 25^\circ\text{C}$, $V_{DD} = 30\text{ V}$, $V_F = 0\text{ V}$, $V_{CM} = 2000\text{ V}$ (Note 12)	35	50		kV/ μs

10. The difference between t_{PHL} and t_{PLH} between any two FOD3120 parts under same test conditions.

11. Common mode transient immunity at output high is the maximum tolerable negative dV_{cm}/dt on the trailing edge of the common mode impulse signal, V_{cm} , to assure that the output will remain high (i.e., $V_O > 15.0\text{ V}$).

12. Common mode transient immunity at output low is the maximum tolerable positive dV_{cm}/dt on the leading edge of the common pulse signal, V_{cm} , to assure that the output will remain low (i.e., $V_O < 1.0\text{ V}$).

TYPICAL PERFORMANCE CHARACTERISTICS

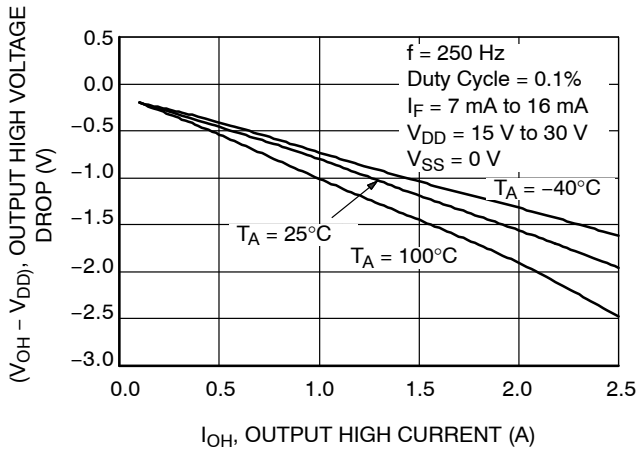


Figure 1. Output High Voltage Drop vs. Output High Current

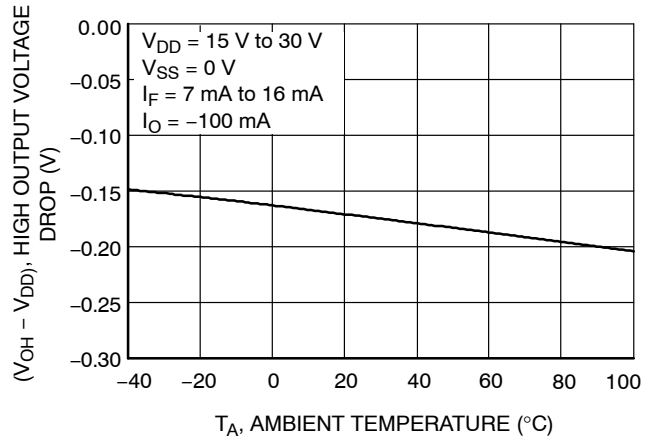


Figure 2. Output High Voltage Drop vs. Ambient Temperature

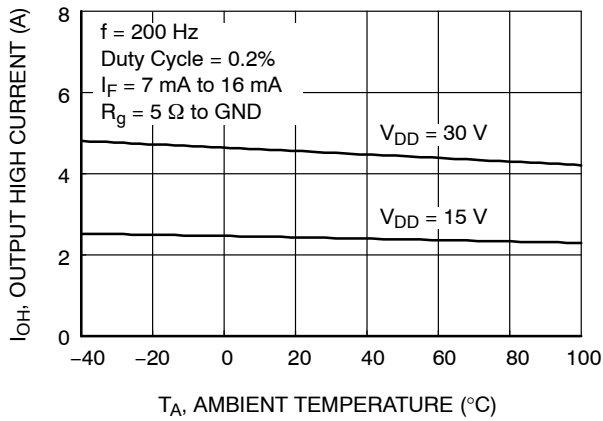


Figure 3. Output High Current vs. Ambient Temperature

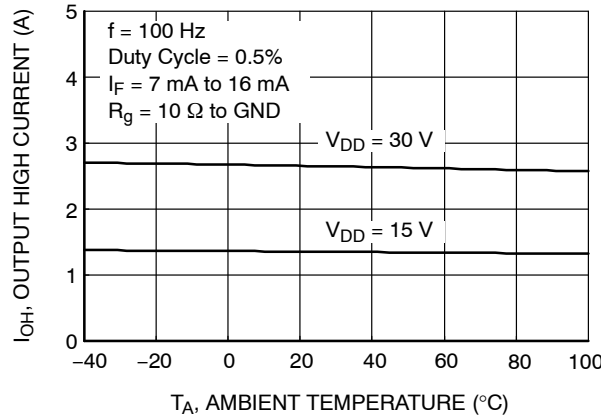


Figure 4. Output High Current vs. Ambient Temperature

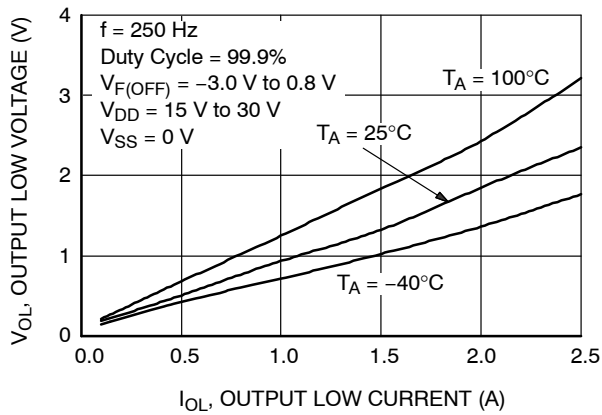


Figure 5. Output Low Voltage vs. Output Low Current

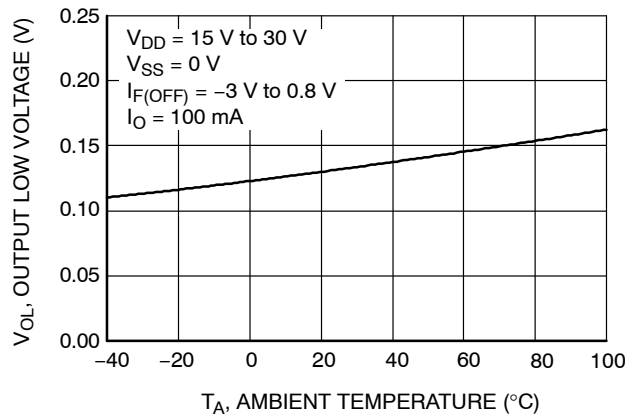


Figure 6. Output Low Voltage vs. Ambient Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

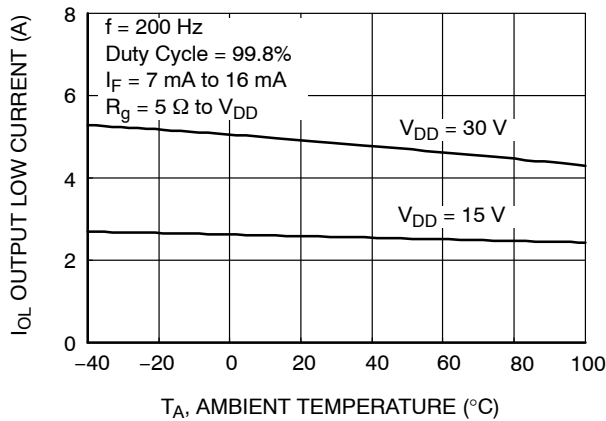


Figure 7. Output Low Current vs. Ambient Temperature

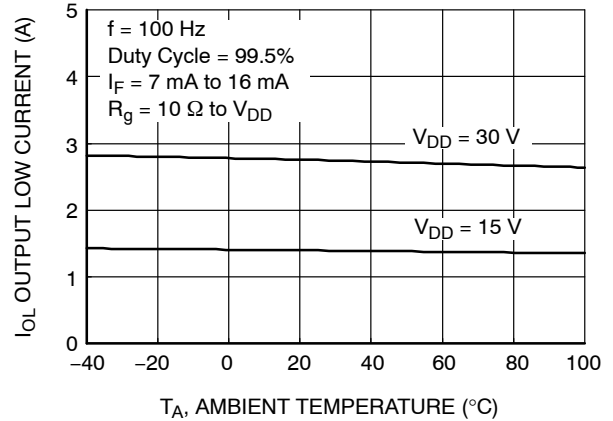


Figure 8. Output Low Current vs. Ambient Temperature

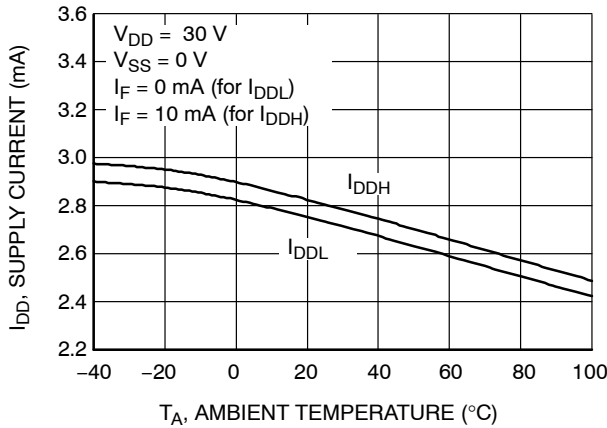


Figure 9. Supply Current vs. Ambient Temperature

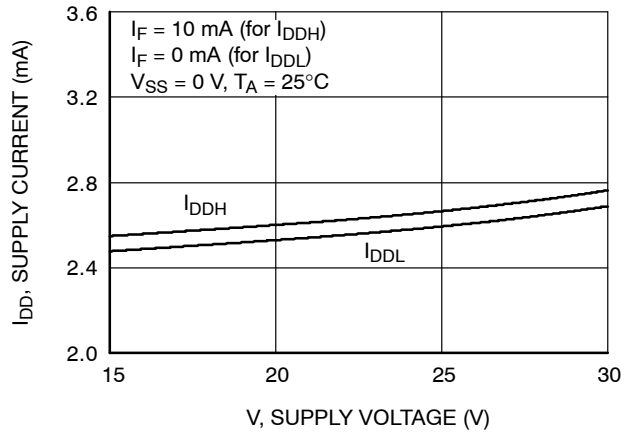


Figure 10. Supply Current vs. Supply Voltage

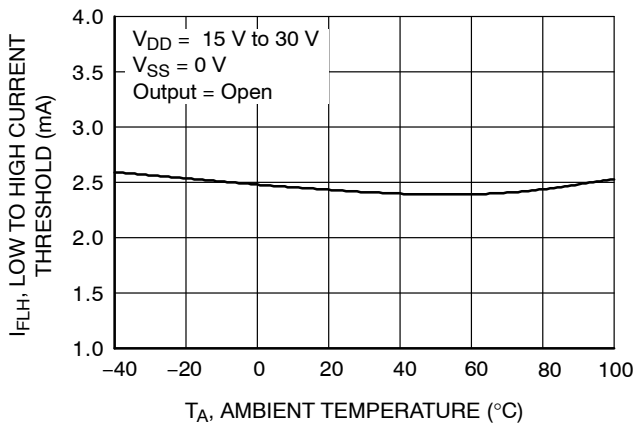


Figure 11. Low to High Input Current Threshold vs. Ambient Temperature

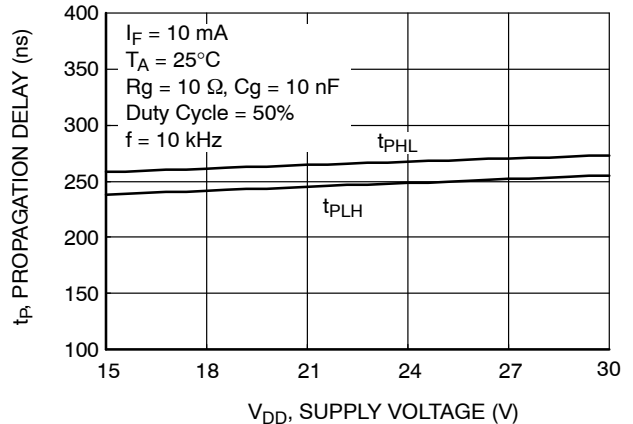


Figure 12. Propagation Delay vs. Supply Voltage

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

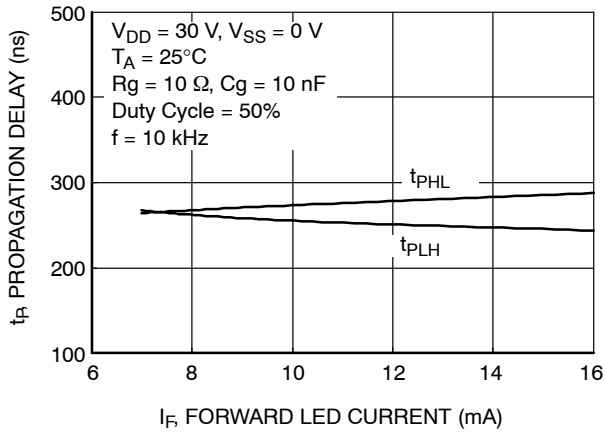


Figure 13. Propagation Delay vs. LED Forward Current

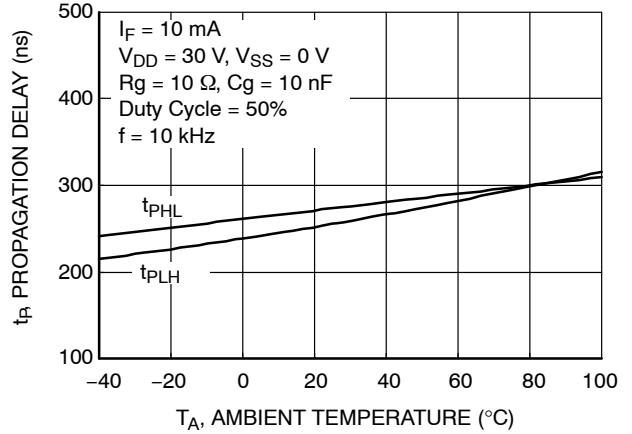


Figure 14. Propagation Delay vs. Ambient Temperature

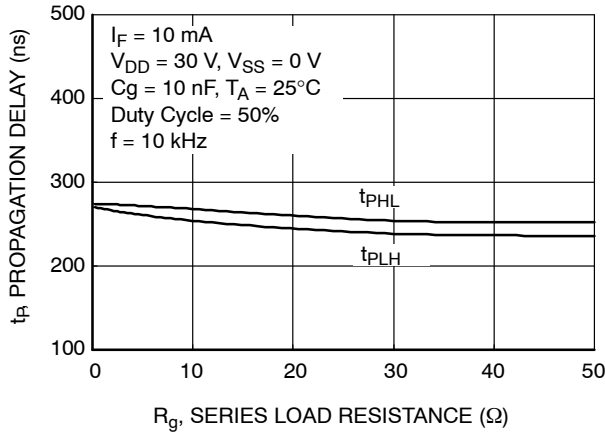


Figure 15. Propagation Delay vs. Series Load Resistance

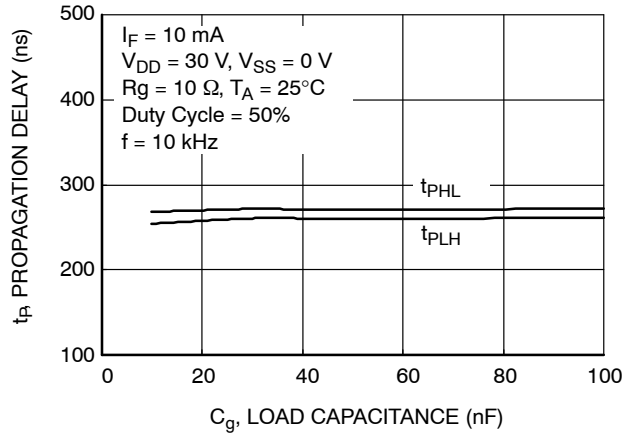


Figure 16. Propagation Delay vs. Load Capacitance

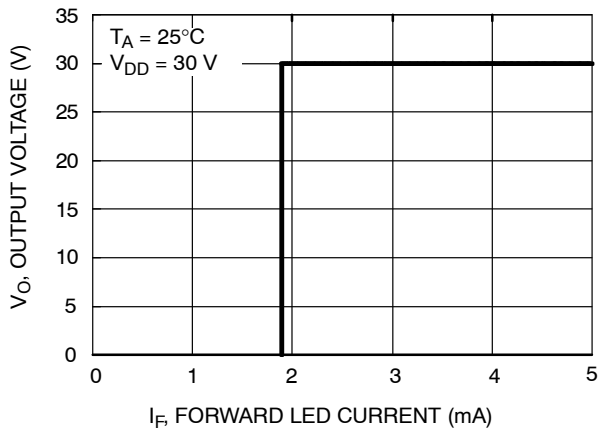


Figure 17. Transfer Characteristics

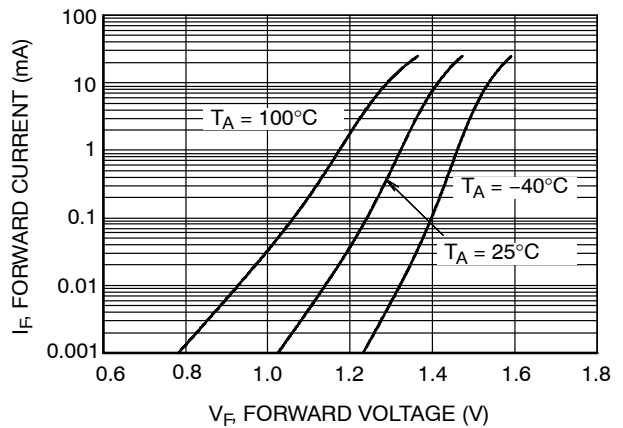


Figure 18. Input Forward Current vs. Forward Voltage

FOD3120

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

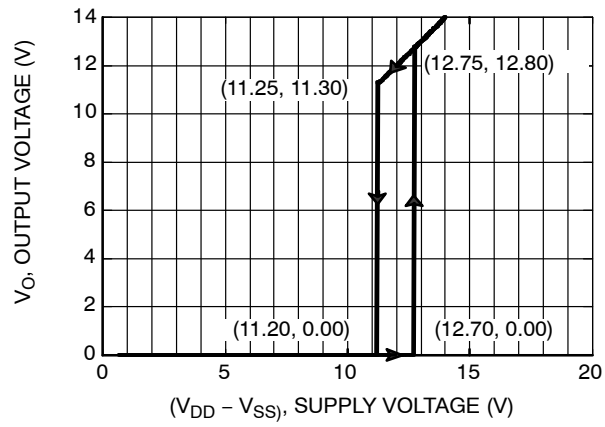


Figure 19. Under Voltage Lockout

FOD3120

TEST CIRCUIT

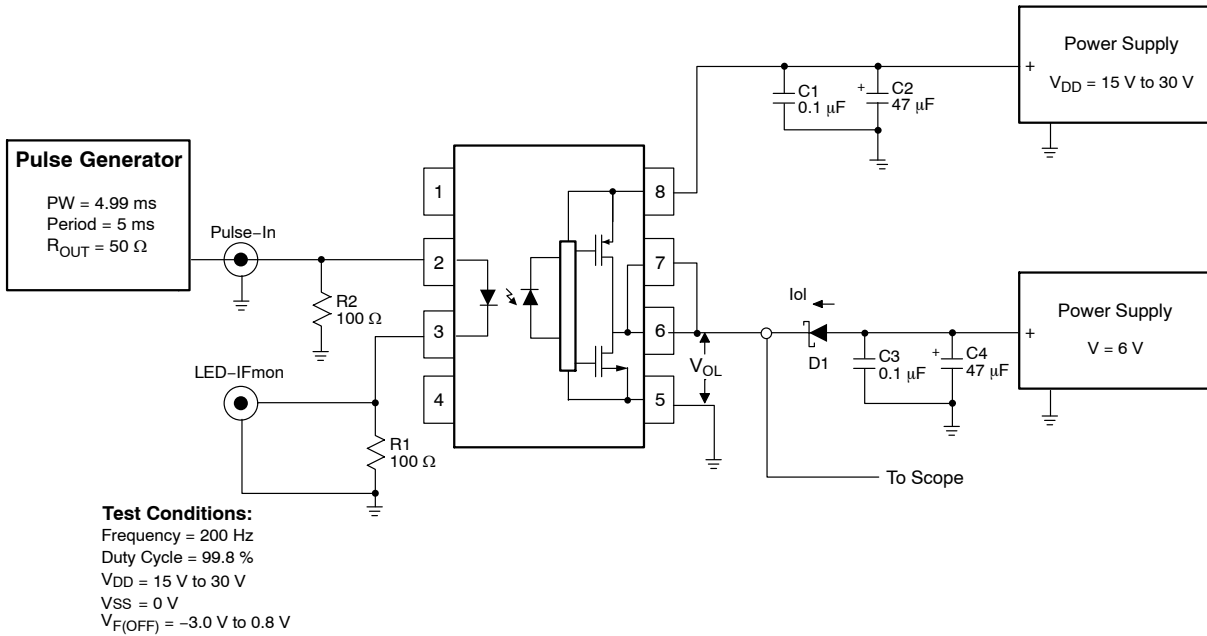


Figure 20. I_{OL} Test Circuit

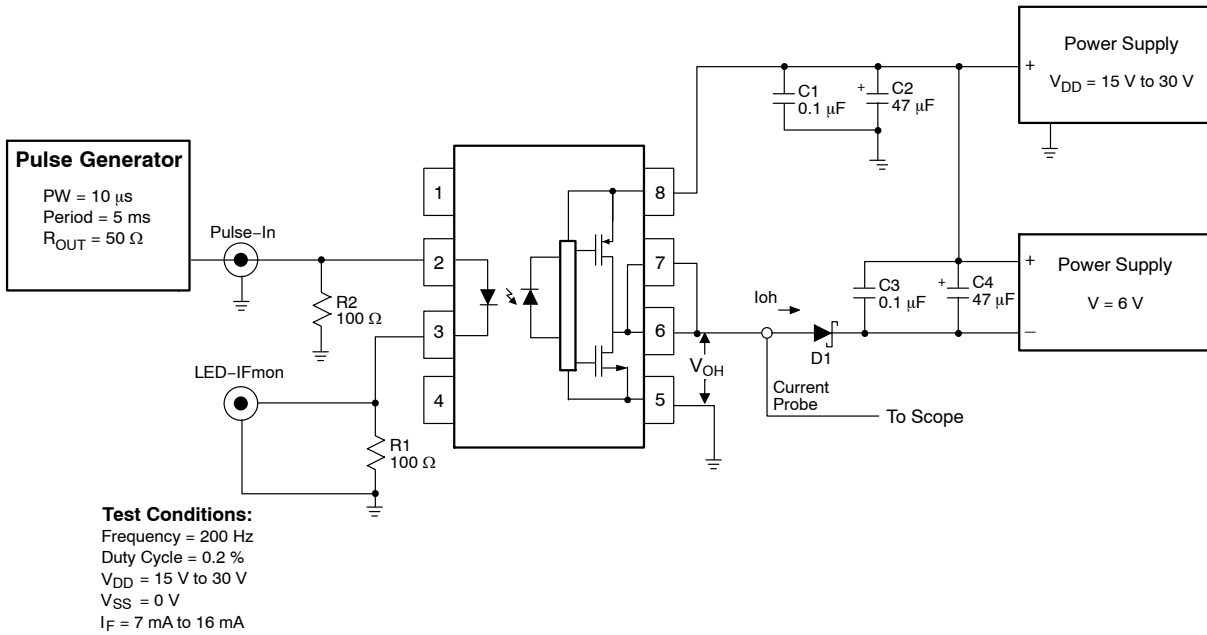


Figure 21. I_{OH} Test Circuit

FOD3120

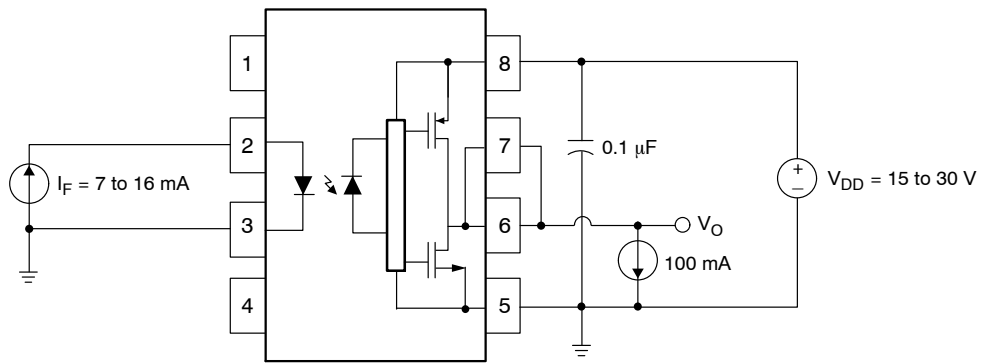


Figure 22. V_{OH} Test Circuit

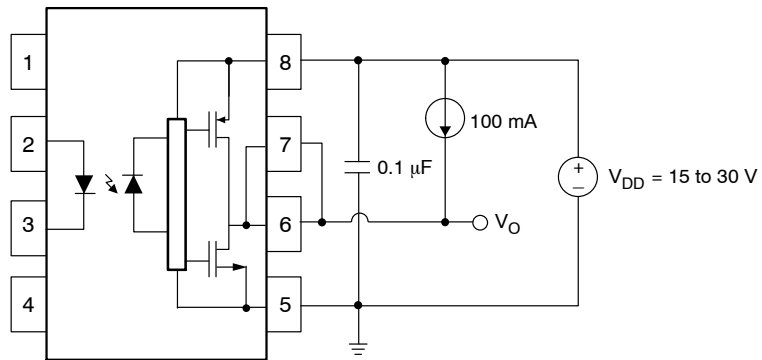


Figure 23. V_{OL} Test Circuit

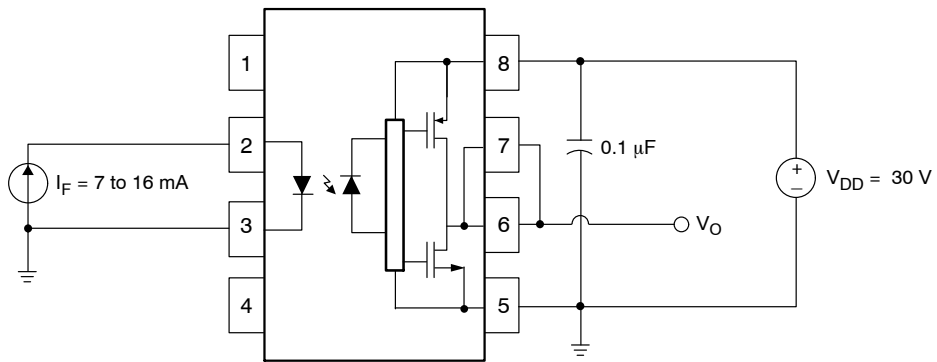


Figure 24. I_{DDH} Test Circuit

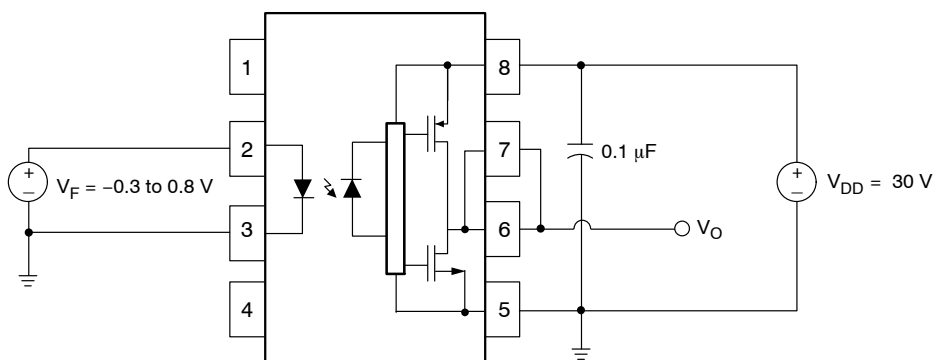


Figure 25. I_{DDL} Test Circuit

FOD3120

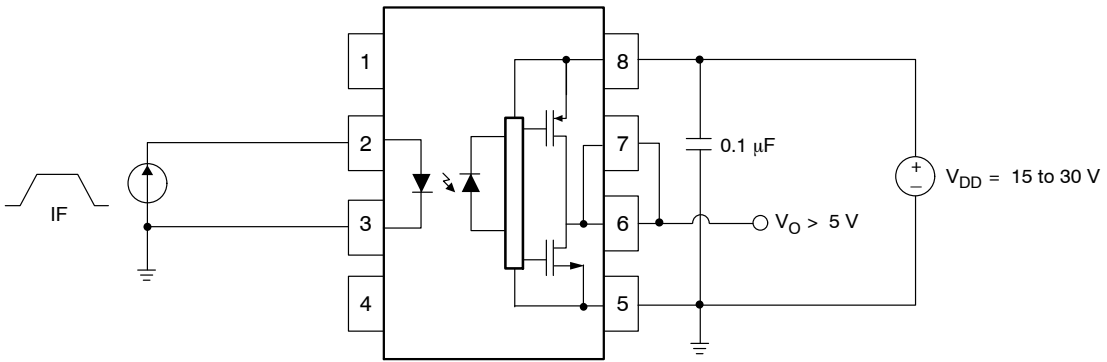


Figure 26. I_{FLH} Test Circuit

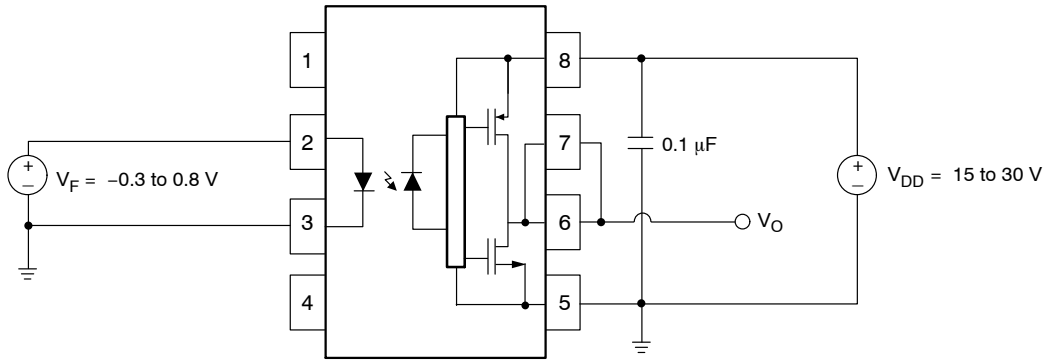


Figure 27. V_{FHL} Test Circuit

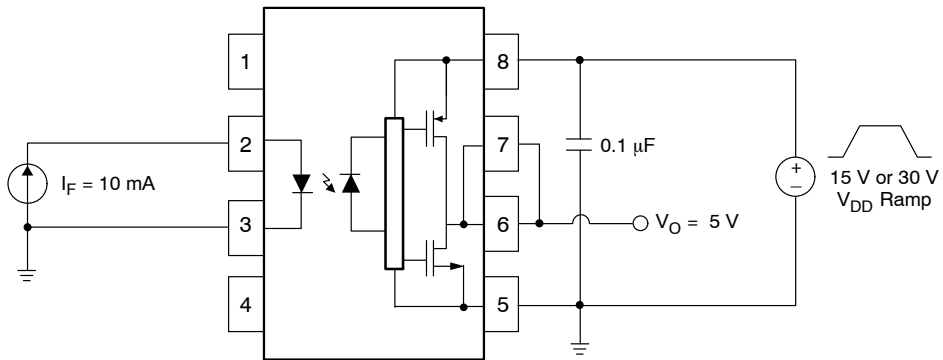


Figure 28. UVLO Test Circuit

FOD3120

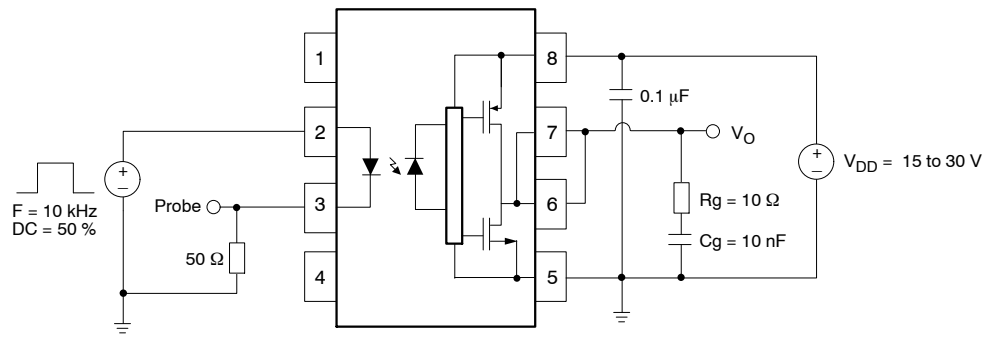


Figure 29. t_{PHL} , t_{PLH} , t_R and t_F Test Circuit and Waveforms

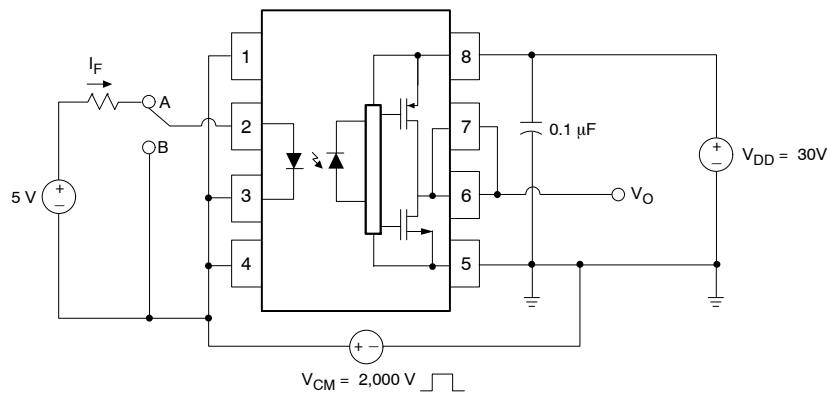


Figure 30. CMR Test Circuit and Waveforms

FOD3120

REFLOW PROFILE

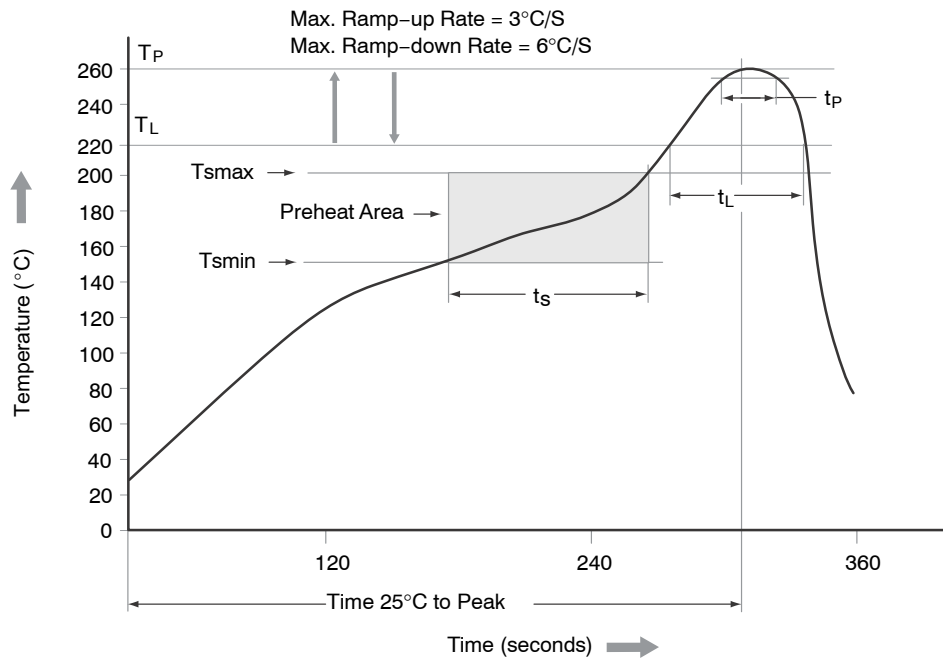


Figure 31. Reflow Profile

Table 9. REFLOW PROFILE

Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmmin)	150°C
Temperature Max. (Tsmmax)	200°C
Time (ts) from (Tsmmin to Tsmmax)	60-120 s
Ramp-up Rate (tL to tp)	3°C/s max.
Liquidous Temperature (TL)	217°C
Time (tL) Maintained Above (TL)	60-150 s
Peak Body Package Temperature	260°C +0°C / -5°C
Time (tp) within 5°C of 260°C	30 s
Ramp-down Rate (TP to TL)	6°C/s max.
Time 25°C to Peak Temperature	8 min. max.

FOD3120

ORDERING INFORMATION

Part Number	Package	Shipping†
FOD3120	DIP 8-Pin	50 / Tube
FOD3120S	SMT 8-Pin (Lead Bend)	50 / Tube
FOD3120SD	SMT 8-Pin (Lead Bend)	1000 / Tape & Reel
FOD3120V	DIP 8-Pin, DIN EN/IEC60747-5-5 option	50 / Tube
FOD3120SV	SMT 8-Pin (Lead Bend), DIN EN/IEC60747-5-5 option	50 / Tube
FOD3120SDV	SMT 8-Pin (Lead Bend), DIN EN/IEC60747-5-5 option	1000 / Tape & Reel
FOD3120TV	DIP 8-Pin, 0.4" Lead Spacing, DIN EN/IEC60747-5-5 option	50 / Tube
FOD3120TSV	SMT 8-Pin, 0.4" Lead Spacing, DIN EN/IEC60747-5-5 option	50 / Tube
FOD3120TSR2V	SMT 8-Pin, 0.4" Lead Spacing, DIN EN/IEC60747-5-5 option	700 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

OPTOPLANAR is a registered trademark of Semiconductor Components Industries, LLC dba "onsemi" or its affiliates and/or subsidiaries in the United States and/or other countries.

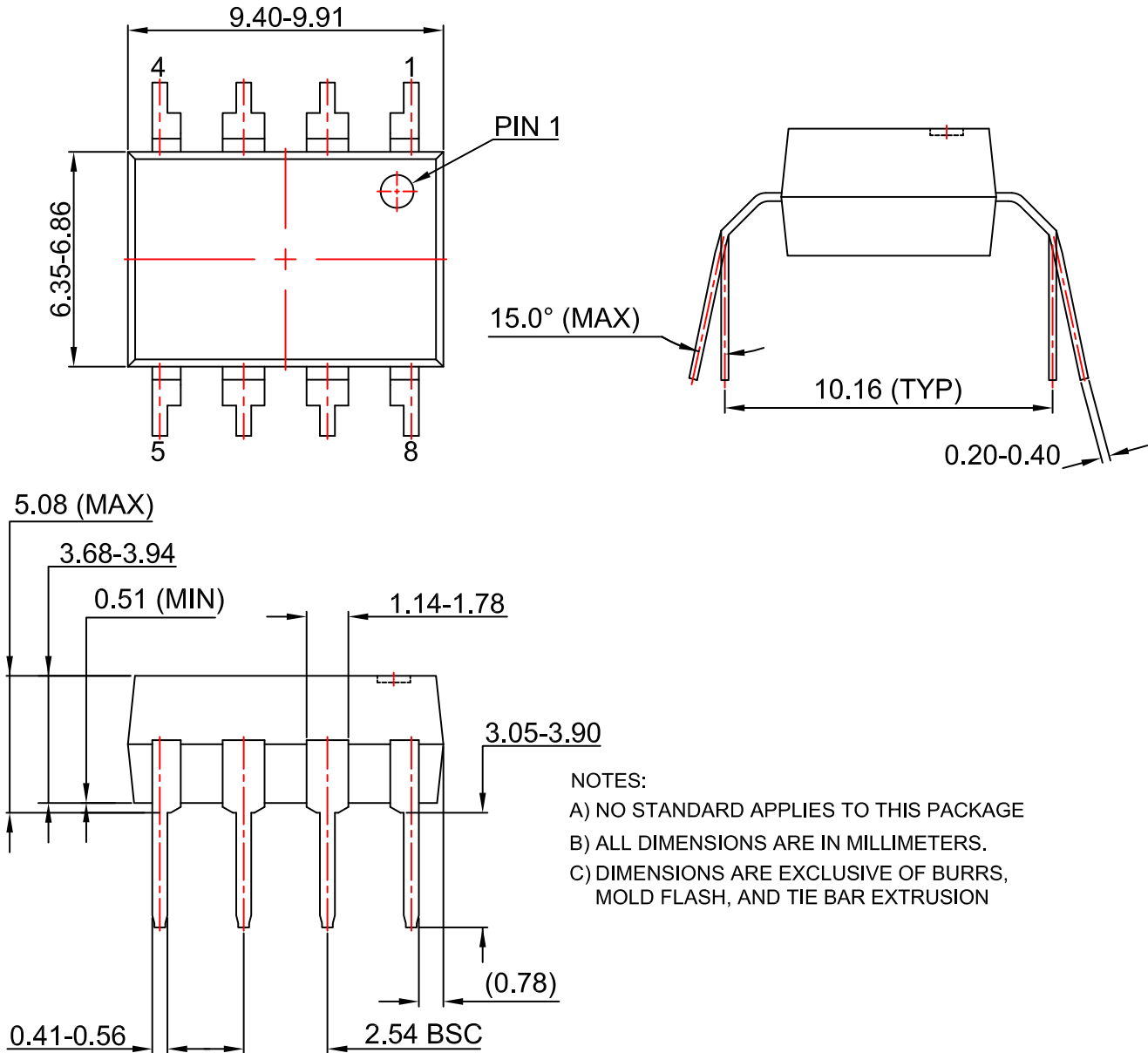
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



PDIP8 6.6x3.81, 2.54P
CASE 646BW
ISSUE O

DATE 31 JUL 2016



- NOTES:
A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

DOCUMENT NUMBER:	98AON13445G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PDIP8 6.6X3.81, 2.54P	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

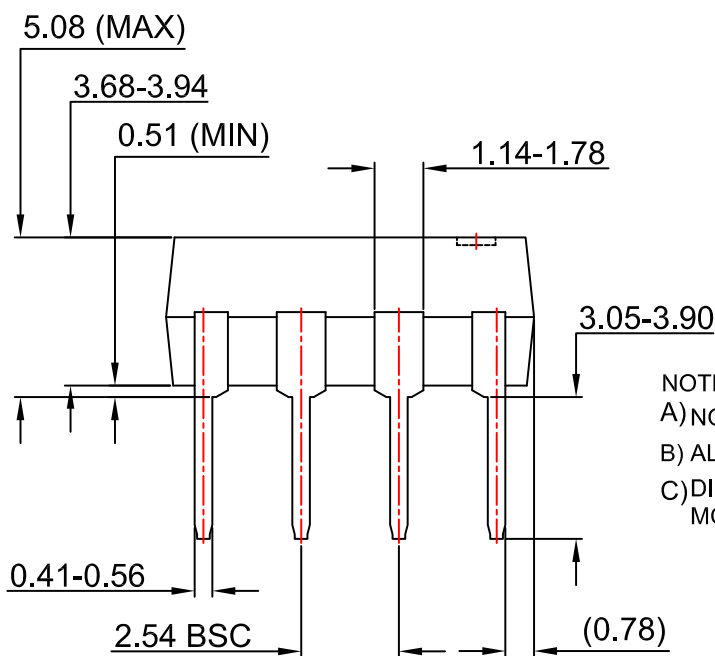
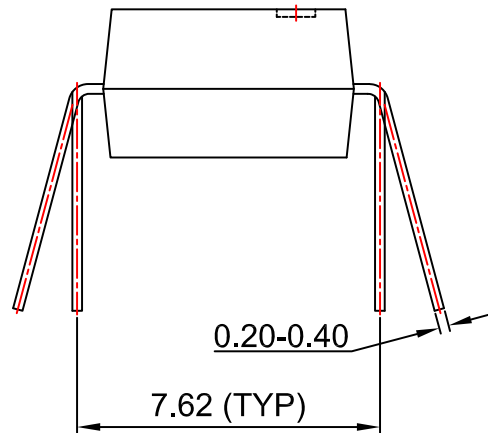
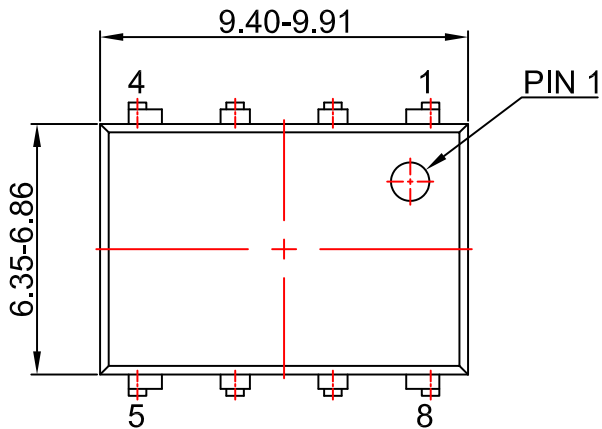
PACKAGE DIMENSIONS

ON Semiconductor®



PDIP8 9.655x6.6, 2.54P
CASE 646CQ
ISSUE O

DATE 18 SEP 2017



NOTES:
A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

DOCUMENT NUMBER:	98AON13446G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PDIP8 9.655X6.6, 2.54P	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

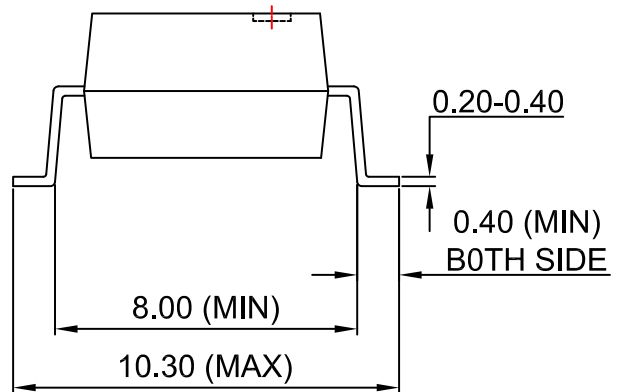
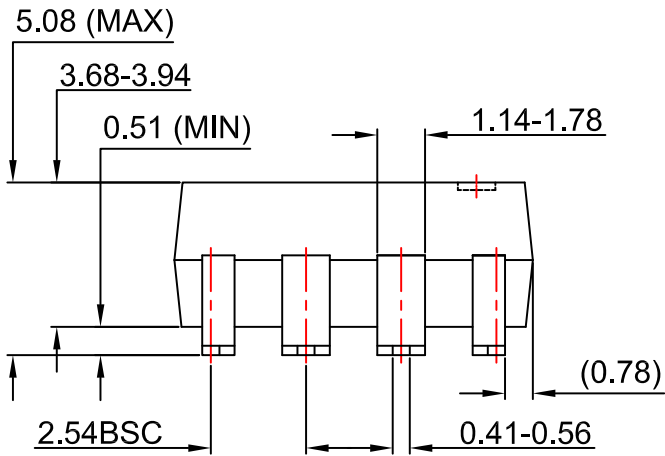


PDIP8 GW
CASE 709AC
ISSUE O

DATE 31 JUL 2016



LAND PATTERN RECOMMENDATION



NOTES:

- A) NO STANDARD APPLIES TO THIS PACKAGE
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

DOCUMENT NUMBER:	98AON13447G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PDIP8 GW	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

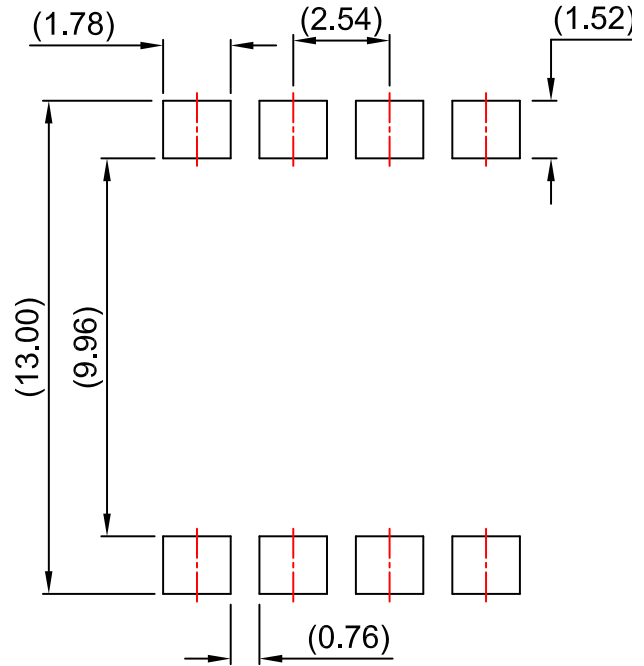
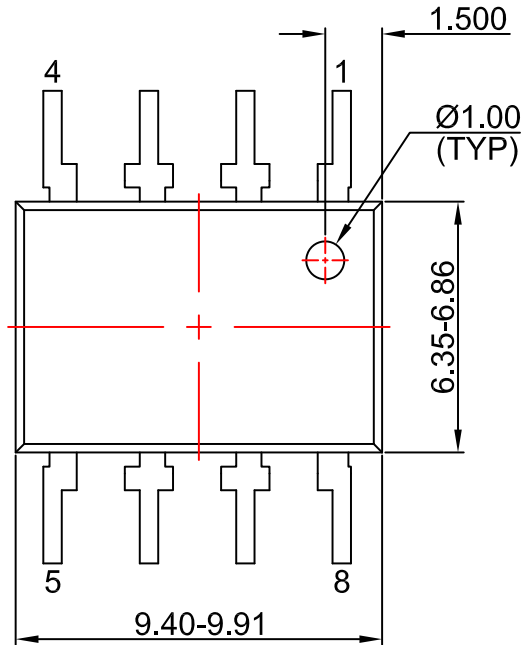
PACKAGE DIMENSIONS

ON Semiconductor®

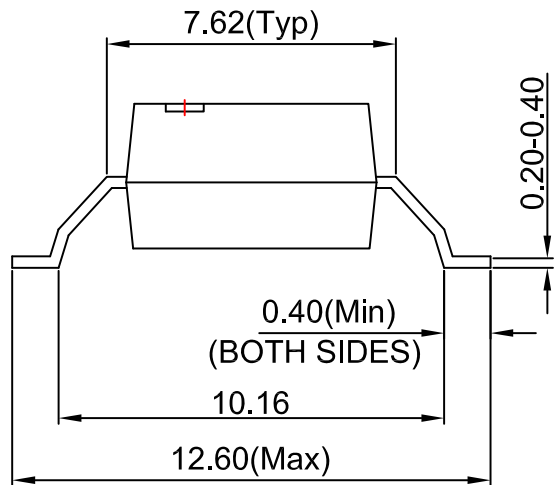
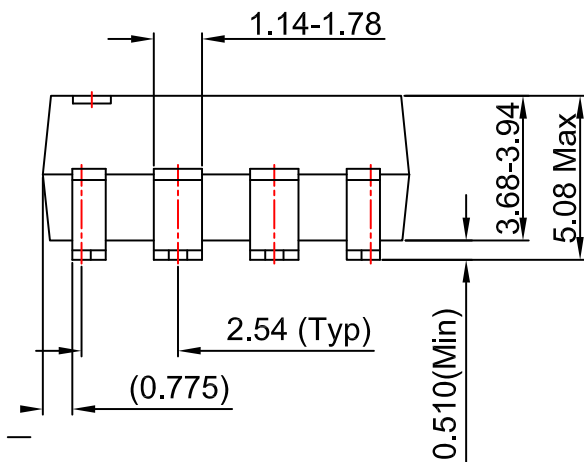


PDIP8 GW
CASE 709AD
ISSUE O

DATE 31 JUL 2016



LAND PATTERN RECOMMENDATION



NOTES:

- A) NO STANDARD APPLIES TO THIS PACKAGE
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

DOCUMENT NUMBER:	98AON13448G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PDIP8 GW	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.