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March 2016

# FOD8163, FOD8163T

## 3.3 V / 5 V, 10 Mbit/sec, Logic Gate Optocoupler in Stretched Body SOP 6-Pin

### Features

- 8 mm Creepage and Clearance Distance, and 0.4 mm Insulation Distance to Achieve Reliable and High Voltage Insulation
- High Noise Immunity Characterized by Common Mode Transient Immunity (CMTI)
  - 20 kV/ $\mu$ s Minimum CMTI
- Specifications Guaranteed Over 3 V to 5.5 V Supply Voltage and -40°C to 100°C Extended Industrial Temperature Range
- High-Speed, 10 Mbit/s Data Rate (NRZ)
- Safety and Regulatory Approvals
  - UL1577, 5,000 VAC<sub>RMS</sub> for 1 Minute
  - DIN-EN/IEC60747-5-5, 1,140 V Peak Working Immunity Insulation Voltage

### Applications

- Isolating Intelligent Power Module
- Isolating Industrial Communication Interface

### Related Resources

- [www.fairchildsemi.com/products/optoelectronics/](http://www.fairchildsemi.com/products/optoelectronics/)
- [www.fairchildsemi.com/pf/FO/FOD8160.html](http://www.fairchildsemi.com/pf/FO/FOD8160.html)
- [www.fairchildsemi.com/pf/FO/FODM8061.html](http://www.fairchildsemi.com/pf/FO/FODM8061.html)
- [www.fairchildsemi.com/pf/FO/FODM611.html](http://www.fairchildsemi.com/pf/FO/FODM611.html)

### Description

The FOD8163 series is a 3.3 V / 5 V high-speed logic gate optocoupler with open-collector output, which supports isolated communications allowing digital signals to communicate between systems without conducting ground loops or hazardous voltages.

The FOD8163 series utilizes stretched body package to achieve 8 mm creepage and clearance distances (FOD8163T), and optimized IC design to achieve reliably high-insulation voltage and high-noise immunity.

The FOD8163 series consists of an aluminium gallium arsenide (AlGaAs) light emitting diode and an integrated high-speed photodetector. The output of the detector IC is an open collector schottky-clamped transistor. The electrical and switching characteristics are guaranteed over the extended industrial temperature range of -40°C to 100°C and a  $V_{CC}$  range of 3 V to 5.5 V.

### Functional Schematic

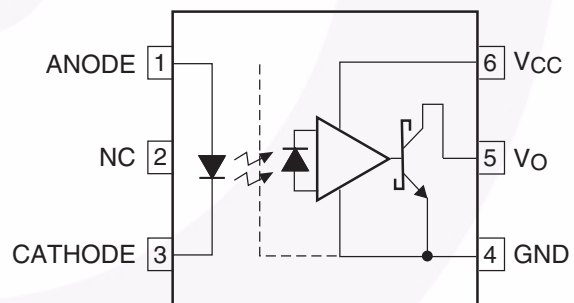


Figure 1. Functional Schematic

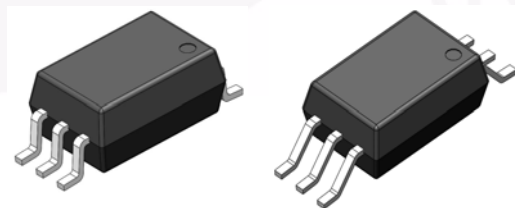


Figure 2. Package Outline

FOD8163, FOD8163T — 3.3 V / 5 V, 10 Mbit/sec, Logic Gate Optocoupler in Stretched Body SOP 6-Pin

### Truth Table

LED	$V_O$
Off	HIGH
On	LOW

### Pin Definitions

Pin #	Name	Description
1	ANODE	Anode
2	NC	Not Connected
3	CATHODE	Cathode
4	GND	Output Ground
5	$V_O$	Output Voltage
6	$V_{CC}$	Output Supply Voltage

### Pin Configuration



Figure 3. Pin Configuration

## Safety and Insulation Ratings

As per DIN EN/IEC60747-5-5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Parameter		Characteristics	
		FOD8163	FOD8163T
Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	< 150 V <sub>RMS</sub>	I-IV	I-IV
	< 300 V <sub>RMS</sub>	I-IV	I-IV
	< 450 V <sub>RMS</sub>	I-III	I-IV
	< 600 V <sub>RMS</sub>	I-III	I-III
Climatic Classification		40/100/21	40/100/21
Pollution Degree (DIN VDE 0110/1.89)		2	2
Comparative Tracking Index		175	175

Symbol	Parameter	Value		Unit
		FOD8163	FOD8163T	
V <sub>PR</sub>	Input-to-Output Test Voltage, Method B, V <sub>IORM</sub> × 1.875 = V <sub>PR</sub> , 100% Production Test with t <sub>m</sub> = 1 s, Partial Discharge < 5 pC	1,671	2,137	V <sub>peak</sub>
	Input-to-Output Test Voltage, Method A, V <sub>IORM</sub> × 1.6 = V <sub>PR</sub> , Type and Sample Test with t <sub>m</sub> = 10 s, Partial Discharge < 5 pC	1,426	1,824	V <sub>peak</sub>
V <sub>IORM</sub>	Maximum Working Insulation Voltage	891	1,140	V <sub>peak</sub>
V <sub>IOTM</sub>	Highest Allowable Over-Voltage	6,000	8,000	V <sub>peak</sub>
	External Creepage	≥ 8.0	≥ 8.0	mm
	External Clearance	≥ 7.0	≥ 8.0	mm
DTI	Distance Through Insulation (Insulation Thickness)	≥ 0.4	≥ 0.4	mm
T <sub>S</sub>	Safety Limit Values – Maximum Values Allowed in the Event of a Failure, Case Temperature	150	150	°C
I <sub>S,INPUT</sub>	Input Current	200	200	mA
P <sub>S,OUTPUT</sub>	Output Power	600	600	mW
R <sub>IO</sub>	Insulation Resistance at T <sub>S</sub> , V <sub>IO</sub> = 500 V	10 <sup>9</sup>	10 <sup>9</sup>	Ω

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $T_A = 25^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Value	Unit
$T_{\text{STG}}$	Storage Temperature	-40 to +125	$^\circ\text{C}$
$T_{\text{OPR}}$	Operating Temperature	-40 to +100	$^\circ\text{C}$
$T_J$	Junction Temperature	-40 to +125	$^\circ\text{C}$
$T_{\text{SOL}}$	Lead Solder Temperature (Refer to Reflow Temperature Profile)	260 for 10 sec	$^\circ\text{C}$
<b>Input Characteristics</b>			
$I_F$	Average Forward Input Current	25	mA
$V_R$	Reverse Input Voltage	5.0	V
$PD_I$	Input Power Dissipation <sup>(1)</sup>	45	mW
<b>Output Characteristics</b>			
$V_{\text{CC}}$	Supply Voltage	0 to 7.0	V
$V_O$	Output Voltage	-0.5 to $V_{\text{CC}} + 0.5$	V
$I_O$	Average Output Current	50	mA
$PD_O$	Output Power Dissipation <sup>(1)</sup>	85	mW

**Note:**

1. No derating required up to  $100^\circ\text{C}$ .

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
$T_A$	Ambient Operating Temperature	-40	+100	$^\circ\text{C}$
$V_{\text{CC}}$	Supply Voltages <sup>(2)</sup>	3.0	5.5	V
$V_{\text{FL}}$	Logic Low Input Voltage	0	0.8	V
$I_{\text{FL}}$	Logic Low Input Current		250	$\mu\text{A}$
$I_{\text{FH}}$	Logic High Input Current	6.0	15	mA
N	Fan Out (at $R_L = 1\text{ k}\Omega$ )		5	TTL loads
$R_L$	Output Pull-up Resistor	330	4000	$\Omega$

**Note:**

2.  $0.1\ \mu\text{F}$  bypass capacitor must be connected between pins 4 and 6.

## Isolation Characteristics

Apply over all recommended conditions, typical value is measured at  $T_A = 25^\circ\text{C}$ .

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{\text{ISO}}$	Input-Output Isolation Voltage	$T_A = 25^\circ\text{C}$ , R.H. < 50%, $t = 1.0$ min, $I_{\text{I-O}} \leq 20 \mu\text{A}$ <sup>(3)(4)</sup>	5,000			$\text{VAC}_{\text{RMS}}$
$R_{\text{ISO}}$	Isolation Resistance	$V_{\text{I-O}} = 500 \text{ V}$ <sup>(3)</sup>		$10^{11}$		$\Omega$
$C_{\text{ISO}}$	Isolation Capacitance	$V_{\text{I-O}} = 0 \text{ V}$ , frequency = 1.0 MHz <sup>(3)</sup>		1.0		pF

### Notes:

- Device is considered a two-terminal device: pins 1, 2 and 3 are shorted together and pins 4, 5, and 6 are shorted together.
- 5,000  $\text{VAC}_{\text{RMS}}$  for 1-minute duration is equivalent to 6,000  $\text{VAC}_{\text{RMS}}$  for 1-second duration.

## Electrical Characteristics

Apply over all recommended conditions;  $T_A = -40^\circ\text{C}$  to  $+100^\circ\text{C}$ ,  $3.0 \text{ V} \leq V_{\text{CC}} \leq 5.5 \text{ V}$ ; unless otherwise specified. Typical value is measured at  $T_A = 25^\circ\text{C}$  and  $V_{\text{CC}} = 3.3 \text{ V}$  or  $V_{\text{CC}} = 5 \text{ V}$ .

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	Figure
<b>Input Characteristics</b>							
$V_F$	Forward Voltage	$I_F = 10 \text{ mA}$	1.05	1.45	1.80	V	4
$\Delta(V_F / T_A)$	Temperature Coefficient of Forward Voltage			-1.8		mV/°C	
$BV_R$	Input Reverse Breakdown Voltage	$I_R = 10 \mu\text{A}$	5.0			V	
$I_{\text{FHL}}$	Threshold Input Current	$V_O = 0.6 \text{ V}$ , $I_{\text{OL}}(\text{sink}) = 13 \text{ mA}$		2.0	6.0	mA	5
<b>Output Characteristics</b>							
$V_{\text{OL}}$	Logic Low Output Voltage	$I_F = \text{rated } I_{\text{FHL}}$ , $I_{\text{OL}}(\text{sink}) = 13 \text{ mA}$		0.4	0.6	V	6
$I_{\text{OH}}$	Logic High Output Current	$I_F = 250 \mu\text{A}$ , $V_O = 3.3 \text{ V}$		8.0	50.0	$\mu\text{A}$	7
		$I_F = 250 \mu\text{A}$ , $V_O = 5.0 \text{ V}$		3.0	40.0	$\mu\text{A}$	7
$I_{\text{CCL}}$	Logic Low Output Supply Current	$I_F = 10 \text{ mA}$ , $V_{\text{CC}} = 3.3 \text{ V}$		5.3	8.5	mA	8, 10
		$I_F = 10 \text{ mA}$ , $V_{\text{CC}} = 5.0 \text{ V}$		7.1	10.0	mA	8, 10
$I_{\text{CCH}}$	Logic High Output Supply Current	$I_F = 0 \text{ mA}$ , $V_{\text{CC}} = 3.3 \text{ V}$		3.5	7.0	mA	9, 10
		$I_F = 0 \text{ mA}$ , $V_{\text{CC}} = 5.0 \text{ V}$		5.3	9.0	mA	9, 10

## Switching Characteristics

Apply over all recommended conditions;  $T_A = -40^\circ\text{C}$  to  $+100^\circ\text{C}$ ,  $3.3\text{ V} \leq V_{CC} \leq 5\text{ V}$ ,  $I_F = 6.0\text{ mA}$ ; unless otherwise specified. Typical value is measured at  $T_A = 25^\circ\text{C}$  and  $V_{CC} = 3.3\text{ V}$ .

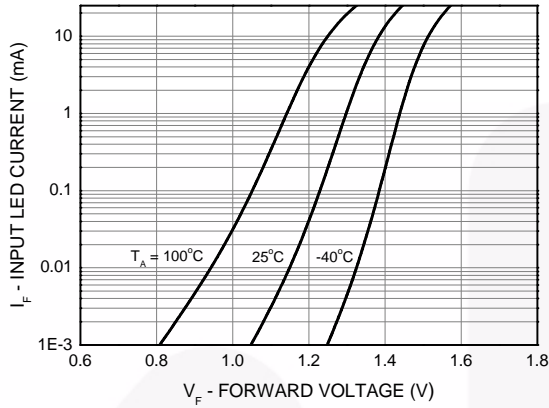
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	Figure
Data Rate		$R_L = 350\ \Omega$			10	Mbit/sec	
$t_{PHL}$	Propagation Delay to Logic Low Output	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$		42	80	ns	11, 13, 16
$t_{PLH}$	Propagation Delay to Logic High Output	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$		53	90	ns	11, 13, 16
PWD	Pulse Width Distortion, $ t_{PHL} - t_{PLH} $	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$		11	35	ns	12, 14, 16
$t_{PSK}$	Propagation Delay Skew	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$ <sup>(5)</sup>			40	ns	
$t_R$	Output Rise Time (10% to 90%)	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$		20		ns	15, 16
$t_F$	Output Fall Time (90% to 10%)	$R_L = 350\ \Omega$ , $C_L = 15\text{ pF}$		10		ns	15, 16
$ CM_H $	Common-Mode Transient Immunity at Output High	$I_F = 0\text{ mA}$ , $V_O > 2\text{ V}$ , $V_{CM} = 1500\text{ V}$ <sup>(6)</sup>	20	40		kV/ $\mu\text{s}$	17
$ CM_L $	Common-Mode Transient Immunity at Output Low	$I_F = 6.0\text{ mA}$ , $V_O < 0.8\text{ V}$ , $V_{CM} = 1500\text{ V}$ <sup>(6)</sup>	20	40		kV/ $\mu\text{s}$	17

### Notes:

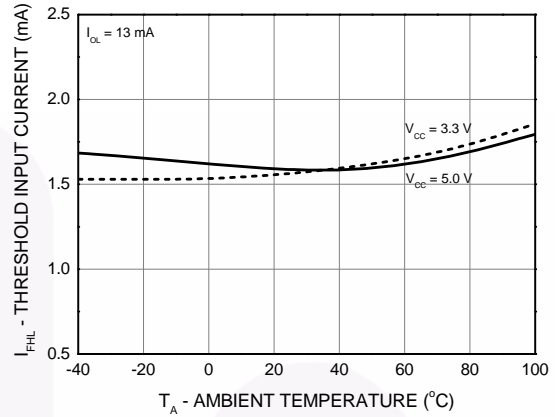
- $t_{PSK}$  is equal to the magnitude of the worst-case difference in  $t_{PHL}$  and/or  $t_{PLH}$  between any two units from the same manufacturing date code that are operated at same case temperature ( $\pm 5^\circ\text{C}$ ), at same operating conditions, with equal loads ( $R_L = 350\ \Omega$ ,  $C_L = 15\text{ pF}$ ), and with an input rise time less than 5 ns.
- Common-mode transient immunity at output HIGH is the maximum tolerable positive  $dV_{cm}/dt$  on the leading edge of the common-mode impulse signal,  $V_{CM}$ , to assure that the output remains HIGH. Common-mode transient immunity at output LOW is the maximum tolerable negative  $dV_{cm}/dt$  on the trailing edge of the common pulse signal,  $V_{CM}$ , to assure that the output remains LOW.



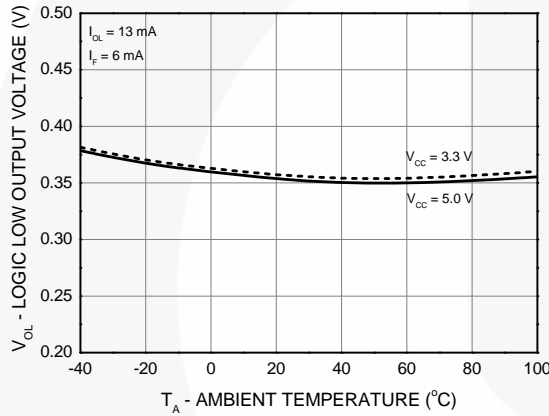
## Typical Performance Characteristics



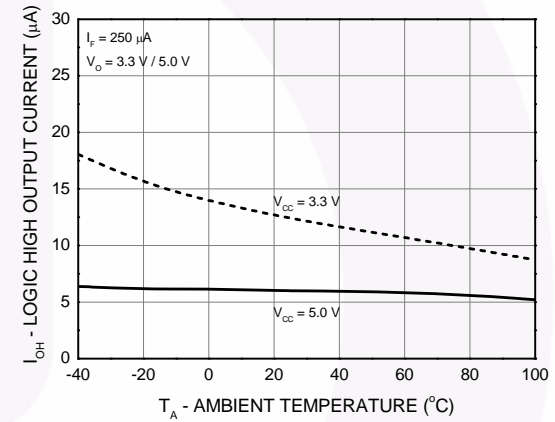
**Figure 4. Input LED Current vs. Forward Voltage**



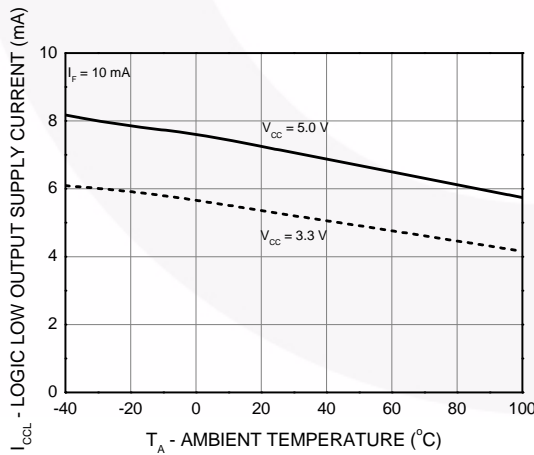
**Figure 5. Threshold Input Current vs. Ambient Temperature**



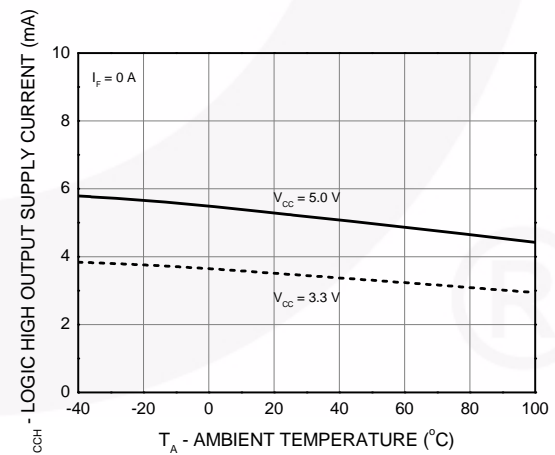
**Figure 6. Logic Low Output Voltage vs. Ambient Temperature**



**Figure 7. Logic High Output Current vs. Ambient Temperature**

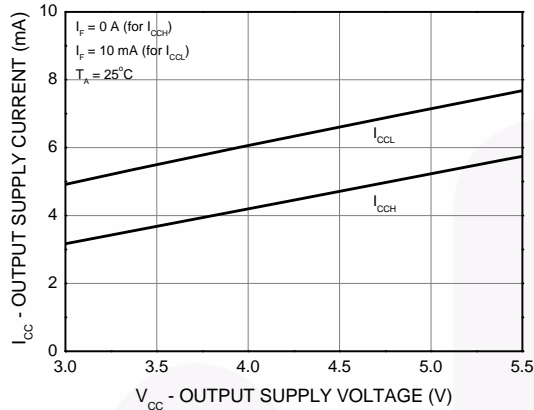


**Figure 8. Logic Low Output Supply Current vs. Ambient Temperature**

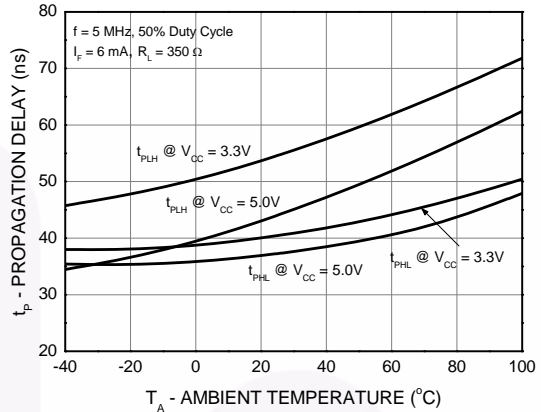


**Figure 9. Logic High Output Supply Current vs. Ambient Temperature**

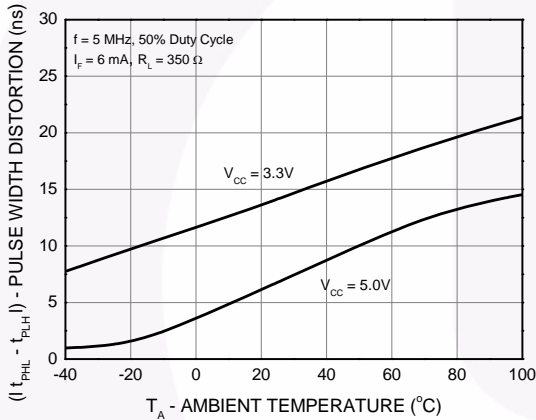
### Typical Performance Characteristics (Continued)



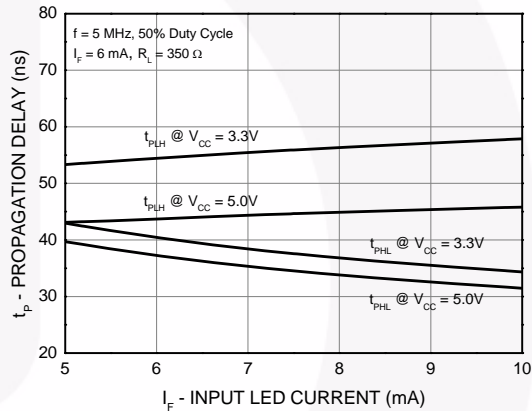
**Figure 10. Output Supply Current vs. Output Supply Voltage**



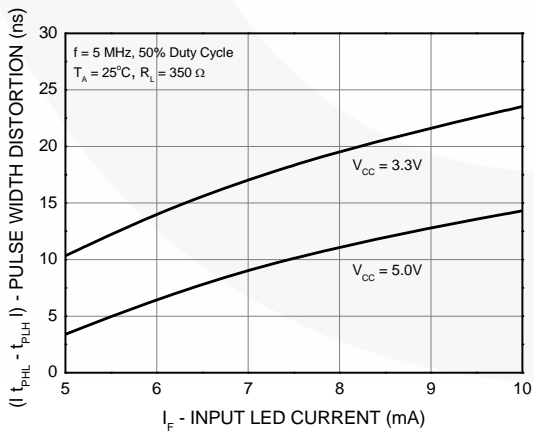
**Figure 11. Propagation Delay vs. Ambient Temperature**



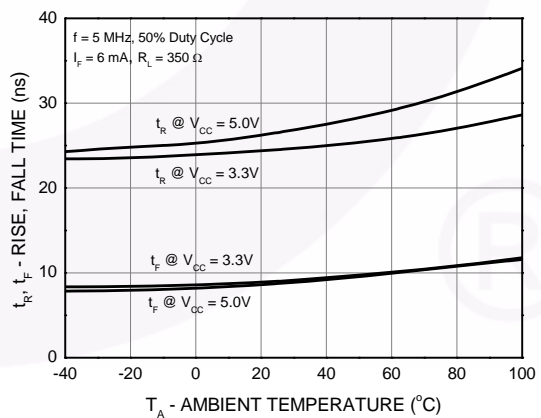
**Figure 12. Pulse Width Distortion vs. Ambient Temperature**



**Figure 13. Propagation Delay vs. Input LED Current**

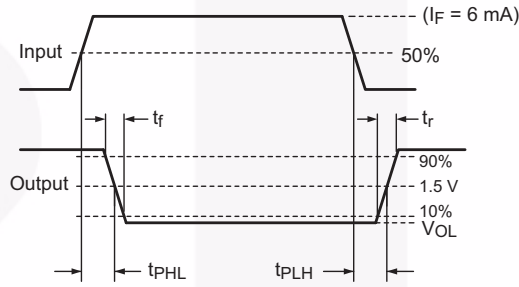
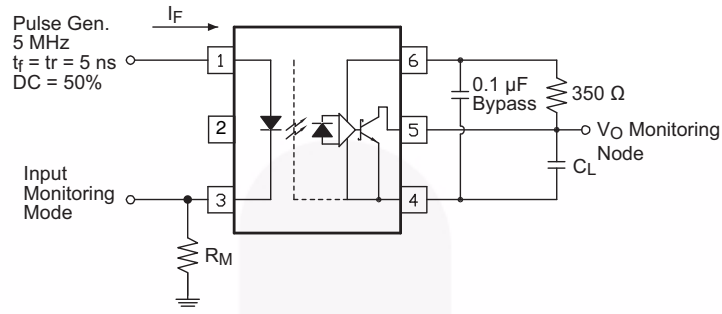


**Figure 14. Pulse Width Distortion vs. Input LED Current**

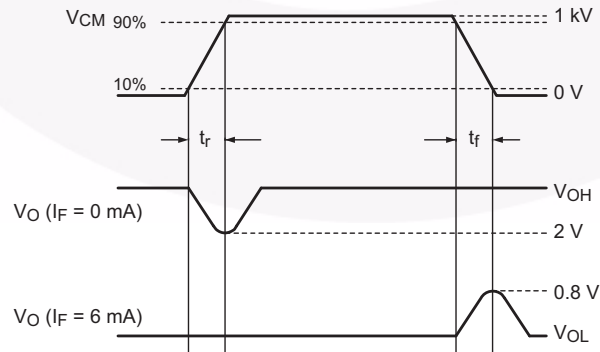
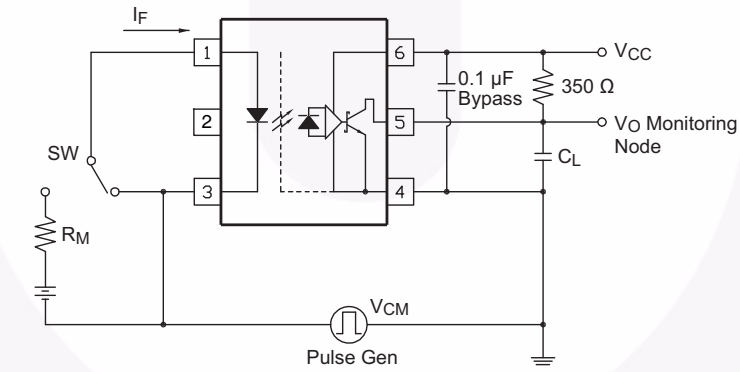


**Figure 15. Rise Time and Fall Time vs. Ambient Temperature**

### Test Circuit

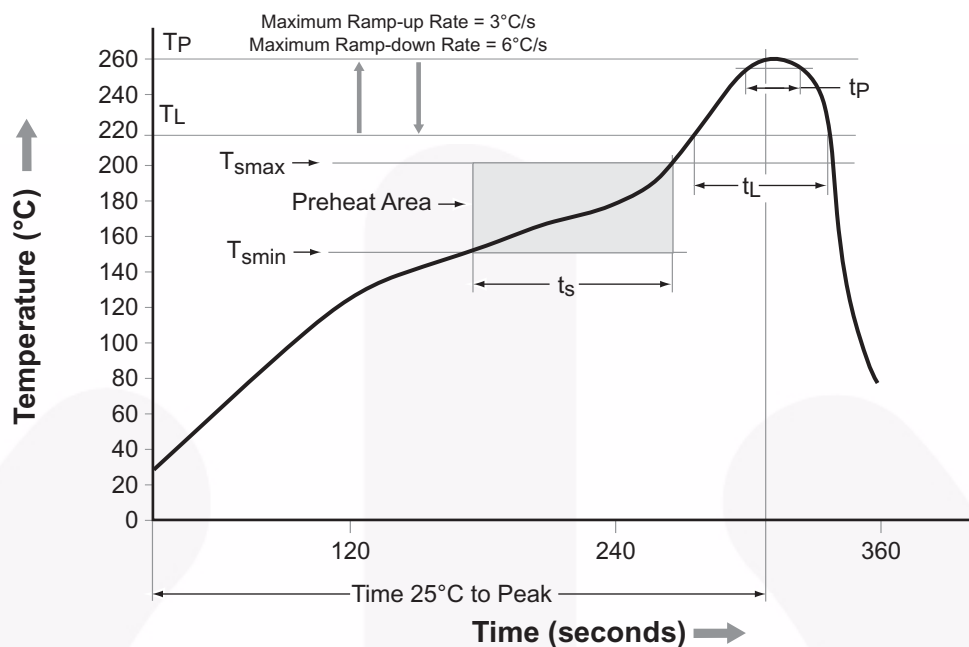


**Figure 16. Test Circuit for Propagation Delay, Rise Time, and Fall Time**



**Figure 17. Test Circuit for Instantaneous Common-Mode Rejection Voltage**

## Reflow Profile




Profile Feature	Pb-Free Assembly Profile
Temperature Minimum ( $T_{smin}$ )	150°C
Temperature Maximum ( $T_{smax}$ )	200°C
Time ( $t_s$ ) from ( $T_{smin}$ to $T_{smax}$ )	60 s to 120 s
Ramp-up Rate ( $t_L$ to $t_P$ )	3°C/second maximum
Liquidous Temperature ( $T_L$ )	217°C
Time ( $t_L$ ) Maintained Above ( $T_L$ )	60 s to 150 s
Peak Body Package Temperature	260°C +0°C / -5°C
Time ( $t_p$ ) within 5°C of 260°C	30 s
Ramp-Down Rate ( $T_P$ to $T_L$ )	6°C/s maximum
Time 25°C to Peak Temperature	8 minutes maximum

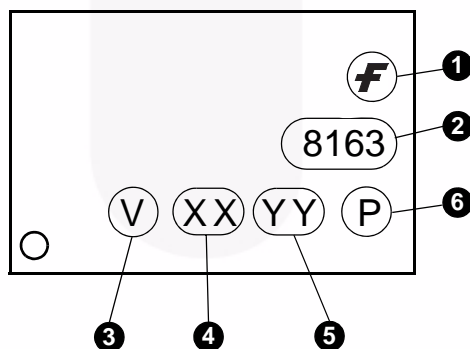
Figure 18. Reflow Profile

## Ordering Information

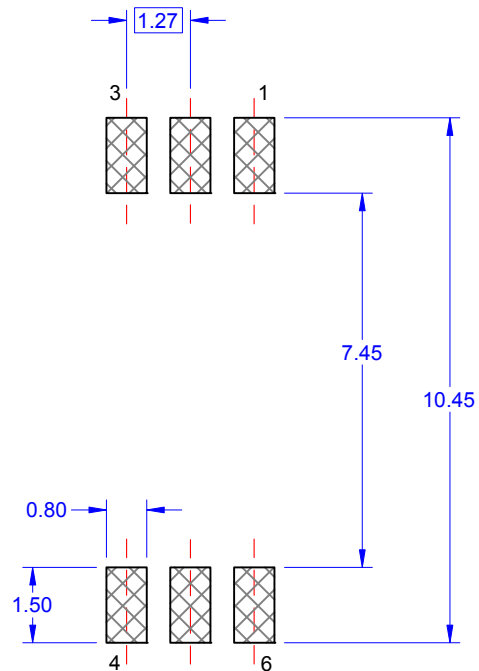
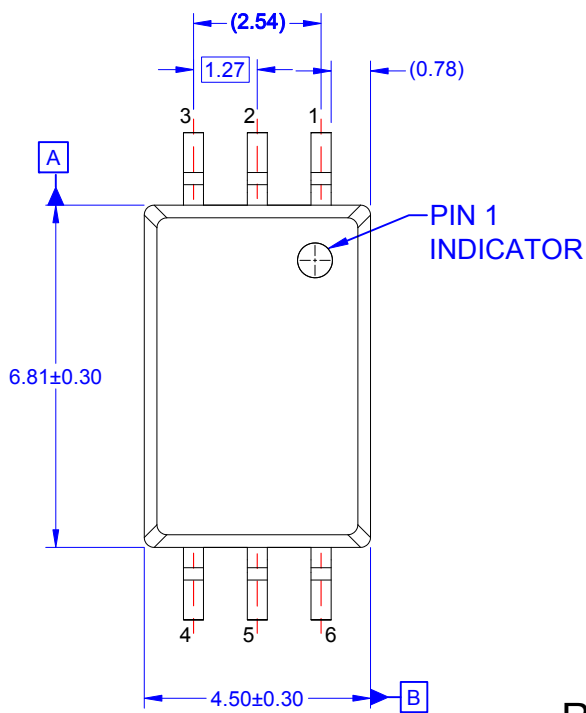
Part Number	Package	Packing Method
FOD8163	Stretched Body SOP 6-Pin	Tube (100 units per tube)
FOD8163R2	Stretched Body SOP 6-Pin	Tape and Reel (1,000 units per reel)
FOD8163V	Stretched Body SOP 6-Pin, DIN EN/IEC60747-5-5 Option	Tube (100 units per tube)
FOD8163R2V	Stretched Body SOP 6-Pin, DIN EN/IEC60747-5-5 Option	Tape and Reel (1,000 units per reel)
FOD8163T	Stretched Body SOP 6-Pin, Wide Lead	Tube (100 units per tube)
FOD8163TR2	Stretched Body SOP 6-Pin, Wide Lead	Tape and Reel (1,000 units per reel)
FOD8163TV	Stretched Body SOP 6-Pin, Wide Lead, DIN EN/IEC60747-5-5 Option	Tube (100 units per tube)
FOD8163TR2V	Stretched Body SOP 6-Pin, Wide Lead, DIN EN/IEC60747-5-5 Option	Tape and Reel (1,000 units per reel)

 All packages are lead free per JEDEC: J-STD-020B standard.

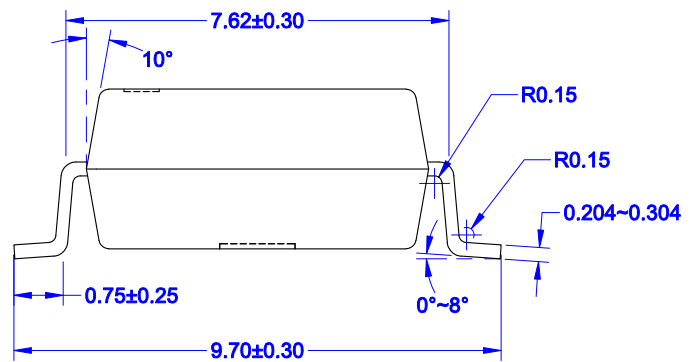
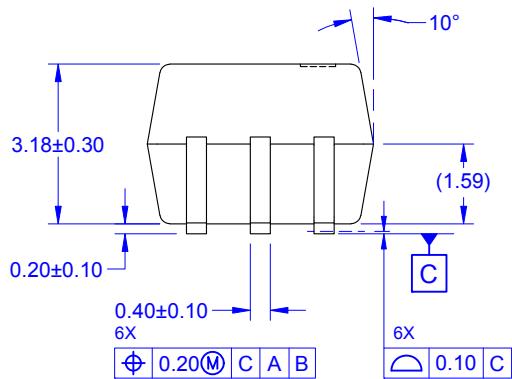
## Marking Information



Definitions	
1	Fairchild Logo
2	Device Number, e.g. 8163
3	DIN EN/IEC60747-5-5 Option (only appears on component ordered with this option)
4	One Digit Year Code, e.g. '5'
5	Two Digit Work Week Ranging from '01' to '53'
6	Assembly Package Code

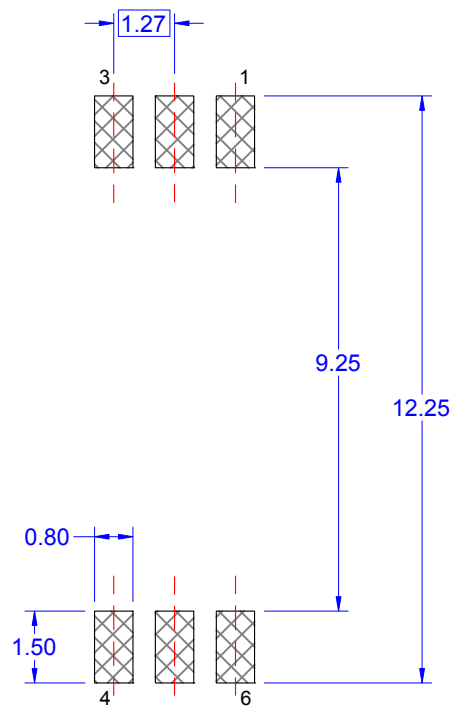
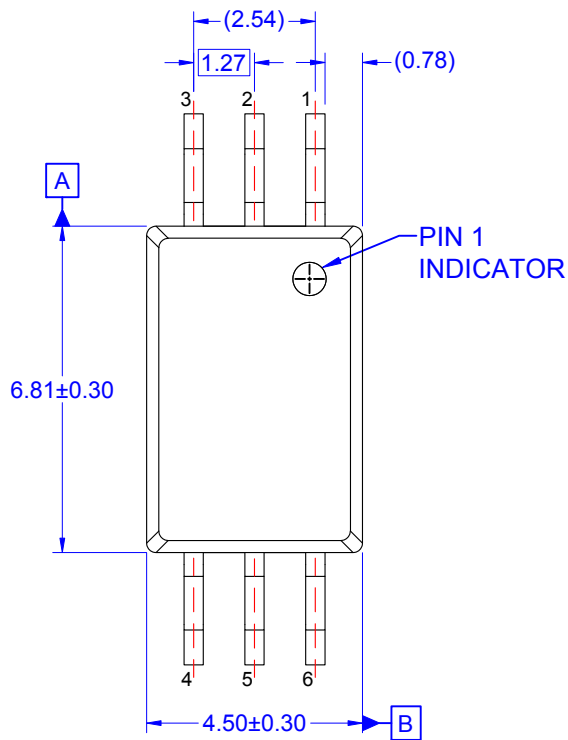


## RECOMMENDED LAND PATTERN

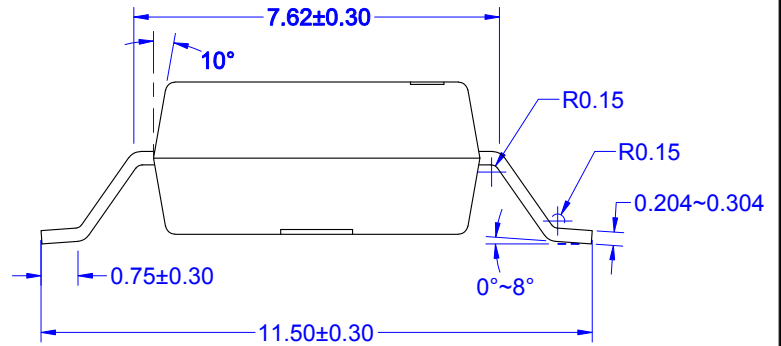
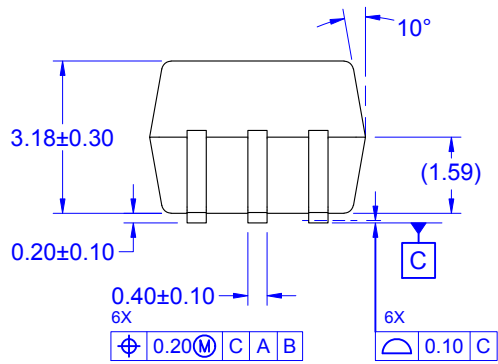


- NOTES: UNLESS OTHERWISE SPECIFIED
- A) NO STANDARD APPLIES TO THIS PACKAGE
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH, AND TIE BAR EXTRUSION.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - E) DRAWING FILE NAME: MKT-M06BREV1





### RECOMMENDED LAND PATTERN



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) NO STANDARD APPLIES TO THIS PACKAGE
  - B) ALL DIMENSIONS ARE IN MILLIMETERS.
  - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH, AND TIE BAR EXTRUSION.
  - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
  - E) DRAWING FILE NAME: MKT-M06CREV1

