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Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

March 2016

FOD8163, FOD8163T
3.3 V / 5 V, 10 Mbit/sec, Logic Gate Optocoupler in Stretched Body SOP 6-Pin

Features

- 8 mm Creepage and Clearance Distance, and 0.4 mm Insulation Distance to Achieve Reliable and High Voltage Insulation
- High Noise Immunity Characterized by Common Mode Transient Immunity (CMTI)
  - 20 kV/μs Minimum CMTI
- Specifications Guaranteed Over 3 V to 5.5 V Supply Voltage and -40°C to 100°C Extended Industrial Temperature Range
- High-Speed, 10 Mbit/s Data Rate (NRZ)
- Safety and Regulatory Approvals
  - UL1577, 5,000 VAC_{RMS} for 1 Minute
  - DIN-EN/IEC60747-5-5, 1,140 V Peak Working Immunity Insulation Voltage

Applications

- Isolating Intelligent Power Module
- Isolating Industrial Communication Interface

Related Resources

- www.fairchildsemi.com/products/optoelectronics/
- www.fairchildsemi.com/pf/FO/FOD8160.html
- www.fairchildsemi.com/pf/FO/FODM8061.html
- www.fairchildsemi.com/pf/FO/FODM611.html

Description

The FOD8163 series is a 3.3 V / 5 V high-speed logic gate optocoupler with open-collector output, which supports isolated communications allowing digital signals to communicate between systems without conducting ground loops or hazardous voltages.

The FOD8163 series utilizes stretched body package to achieve 8 mm creepage and clearance distances (FOD8163T), and optimized IC design to achieve reliably high-insulation voltage and high-noise immunity.

The FOD8163 series consists of an aluminium gallium arsenide (AlGaAs) light emitting diode and an integrated high-speed photodetector. The output of the detector IC is an open collector schottky-clamped transistor. The electrical and switching characteristics are guaranteed over the extended industrial temperature range of -40°C to 100°C and a V_{CC} range of 3 V to 5.5 V.

Functional Schematic

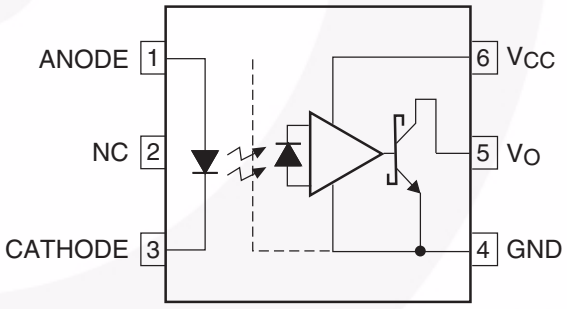


Figure 1. Functional Schematic

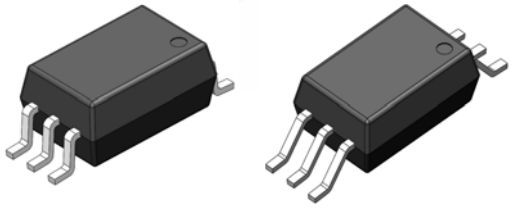


Figure 2. Package Outline

Truth Table

LED	V_O
Off	HIGH
On	LOW

Pin Definitions

Pin #	Name	Description
1	ANODE	Anode
2	NC	Not Connected
3	CATHODE	Cathode
4	GND	Output Ground
5	V_O	Output Voltage
6	V_{CC}	Output Supply Voltage

Pin Configuration

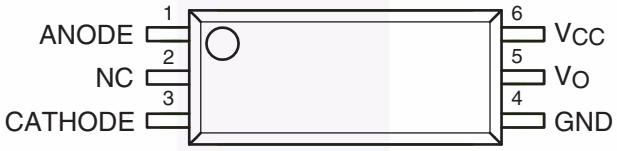


Figure 3. Pin Configuration

Safety and Insulation Ratings

As per DIN EN/IEC60747-5-5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Parameter		Characteristics	
		FOD8163	FOD8163T
Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	< 150 V_{RMS}	I–IV	I–IV
	< 300 V_{RMS}	I–IV	I–IV
	< 450 V_{RMS}	I–III	I–IV
	< 600 V_{RMS}	I–III	I–III
Climatic Classification		40/100/21	40/100/21
Pollution Degree (DIN VDE 0110/1.89)		2	2
Comparative Tracking Index		175	175

Symbol	Parameter	Value		Unit
		FOD8163	FOD8163T	
V_{PR}	Input-to-Output Test Voltage, Method B, V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC	1,671	2,137	V_{peak}
	Input-to-Output Test Voltage, Method A, V_{IORM} x 1.6 = V_{PR}, Type and Sample Test with t_m = 10 s, Partial Discharge < 5 pC	1,426	1,824	V_{peak}
V_{IORM}	Maximum Working Insulation Voltage	891	1,140	V_{peak}
V_{IOTM}	Highest Allowable Over-Voltage	6,000	8,000	V_{peak}
	External Creepage	≥ 8.0	≥ 8.0	mm
	External Clearance	≥ 7.0	≥ 8.0	mm
DTI	Distance Through Insulation (Insulation Thickness)	≥ 0.4	≥ 0.4	mm
	Safety Limit Values – Maximum Values Allowed in the Event of a Failure,			
T_S	Case Temperature	150	150	°C
$I_{S,INPUT}$	Input Current	200	200	mA
$P_{S,OUTPUT}$	Output Power	600	600	mW
R_{IO}	Insulation Resistance at T_S, V_{IO} = 500 V	10^9	10^9	Ω

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A = 25°C unless otherwise specified.

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	-40 to +125	°C
T_{OPR}	Operating Temperature	-40 to +100	°C
T_J	Junction Temperature	-40 to +125	°C
T_{SOL}	Lead Solder Temperature *(Refer to Reflow Temperature Profile)*	260 for 10 sec	°C
Input Characteristics			
I_F	Average Forward Input Current	25	mA
V_R	Reverse Input Voltage	5.0	V
PD_I	Input Power Dissipation(1)	45	mW
Output Characteristics			
V_{CC}	Supply Voltage	0 to 7.0	V
V_O	Output Voltage	-0.5 to V_{CC} + 0.5	V
I_O	Average Output Current	50	mA
PD_O	Output Power Dissipation(1)	85	mW

Note:

1. No derating required up to 100°C.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient Operating Temperature	-40	+100	ºC
V_{CC}	Supply Voltages(2)	3.0	5.5	V
V_{FL}	Logic Low Input Voltage	0	0.8	V
I_{FL}	Logic Low Input Current		250	μA
I_{FH}	Logic High Input Current	6.0	15	mA
N	Fan Out (at R_L = 1 kΩ)		5	TTL loads
R_L	Output Pull-up Resistor	330	4000	Ω

Note:

2. 0.1 μF bypass capacitor must be connected between pins 4 and 6.

Isolation Characteristics

Apply over all recommended conditions, typical value is measured at T_A = 25°C.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
V_{ISO}	Input-Output Isolation Voltage	T_A = 25°C, R.H. < 50%, t = 1.0 min, $I_{I-O} \le 20\ \mu A$[3][4]	5,000			VAC_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500 V[3]		10^{11}		Ω
C_{ISO}	Isolation Capacitance	V_{I-O} = 0 V, frequency = 1.0 MHz[3]		1.0		pF

Notes:

3. Device is considered a two-terminal device: pins 1, 2 and 3 are shorted together and pins 4, 5, and 6 are shorted together.
4. 5,000 VAC_{RMS} for 1-minute duration is equivalent to 6,000 VAC_{RMS} for 1-second duration.

Electrical Characteristics

Apply over all recommended conditions; T_A = -40°C to +100°C, 3.0 V ≤ V_{CC} ≤ 5.5 V; unless otherwise specified. Typical value is measured at T_A = 25°C and V_{CC} = 3.3 V or V_{CC} = 5 V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	Figure
Input Characteristics							
V_F	Forward Voltage	I_F = 10 mA	1.05	1.45	1.80	V	4
$\Delta(V_F / T_A)$	Temperature Coefficient of Forward Voltage			-1.8		mV/°C	
BV_R	Input Reverse Breakdown Voltage	I_R = 10 μA	5.0			V	
I_{FHL}	Threshold Input Current	V_O = 0.6 V, I_{OL}(sink) = 13 mA		2.0	6.0	mA	5
Output Characteristics							
V_{OL}	Logic Low Output Voltage	I_F = rated I_{FHL}, I_{OL}(sink) = 13 mA		0.4	0.6	V	6
I_{OH}	Logic High Output Current	I_F = 250 μA, V_O = 3.3 V		8.0	50.0	μA	7
		I_F = 250 μA, V_O = 5.0 V		3.0	40.0	μA	7
I_{CCL}	Logic Low Output Supply Current	I_F = 10 mA, V_{CC} = 3.3 V		5.3	8.5	mA	8, 10
		I_F = 10 mA, V_{CC} = 5.0 V		7.1	10.0	mA	8, 10
I_{CCH}	Logic High Output Supply Current	I_F = 0 mA, V_{CC} = 3.3 V		3.5	7.0	mA	9, 10
		I_F = 0 mA, V_{CC} = 5.0 V		5.3	9.0	mA	9, 10

Switching Characteristics

Apply over all recommended conditions; T_A = -40°C to +100°C, 3.3 V ≤ V_{CC} ≤ 5 V, I_F = 6.0 mA; unless otherwise specified. Typical value is measured at T_A = 25°C and V_{CC} = 3.3 V.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit	Figure
Data Rate		R_L = 350 Ω			10	Mbit/sec	
t_{PHL}	Propagation Delay to Logic Low Output	R_L = 350 Ω, C_L = 15 pF		42	80	ns	11, 13, 16
t_{PLH}	Propagation Delay to Logic High Output	R_L = 350 Ω, C_L = 15 pF		53	90	ns	11, 13, 16
PWD	Pulse Width Distortion, $\lvert t_{PHL} - t_{PLH} \rvert$	R_L = 350 Ω, C_L = 15 pF		11	35	ns	12, 14, 16
t_{PSK}	Propagation Delay Skew	R_L = 350 Ω, C_L = 15 pF (5)			40	ns	
t_R	Output Rise Time (10% to 90%)	R_L = 350 Ω, C_L = 15 pF		20		ns	15, 16
t_F	Output Fall Time (90% to 10%)	R_L = 350 Ω, C_L = 15 pF		10		ns	15, 16
$\lvert CM_H \rvert$	Common-Mode Transient Immunity at Output High	I_F = 0 mA, V_O > 2 V, V_{CM} = 1500 V(6)	20	40		kV/µs	17
$\lvert CM_L \rvert$	Common-Mode Transient Immunity at Output Low	I_F = 6.0 mA, V_O < 0.8 V, V_{CM} = 1500 V(6)	20	40		kV/µs	17

Notes:

5. t_{PSK} is equal to the magnitude of the worst-case difference in t_{PHL} and/or t_{PLH} between any two units from the same manufacturing date code that are operated at same case temperature (±5°C), at same operating conditions, with equal loads (R_L = 350 Ω, C_L = 15 pF), and with an input rise time less than 5 ns.
6. Common-mode transient immunity at output HIGH is the maximum tolerable positive dVcm/dt on the leading edge of the common-mode impulse signal, V_{CM}, to assure that the output remains HIGH. Common-mode transient immunity at output LOW is the maximum tolerable negative dVcm/dt on the trailing edge of the common pulse signal, V_{CM}, to assure that the output remains LOW.

Typical Performance Characteristics

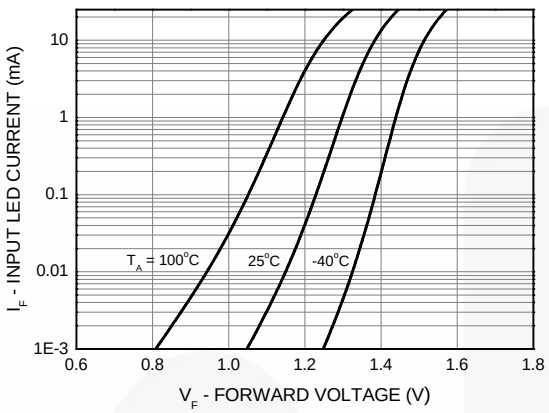


Figure 4. Input LED Current vs. Forward Voltage

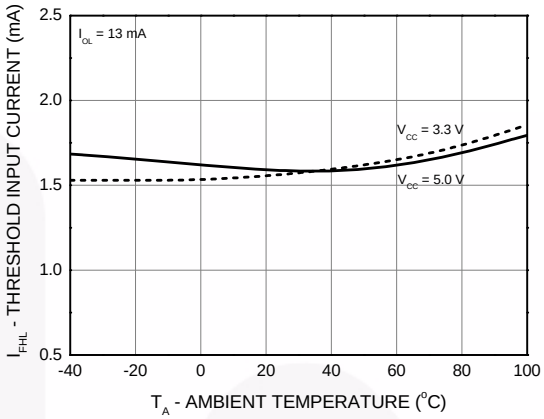


Figure 5. Threshold Input Current vs. Ambient Temperature

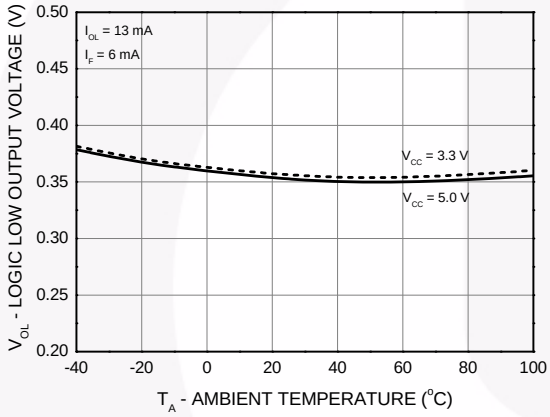


Figure 6. Logic Low Output Voltage vs. Ambient Temperature

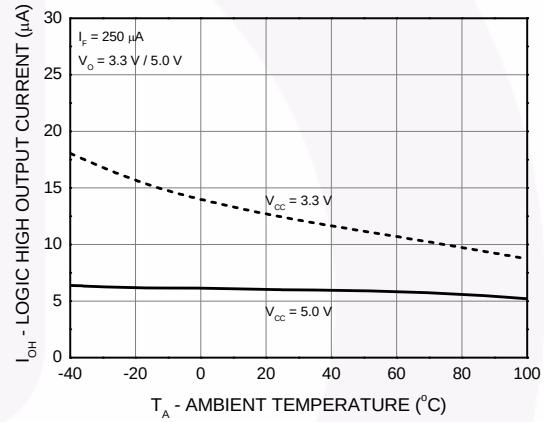


Figure 7. Logic High Output Current vs. Ambient Temperature

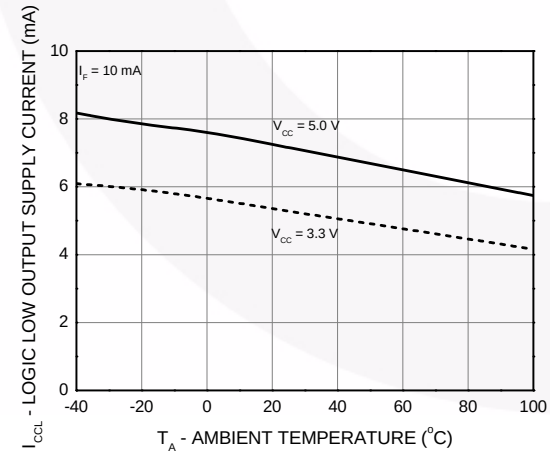


Figure 8. Logic Low Output Supply Current vs. Ambient Temperature

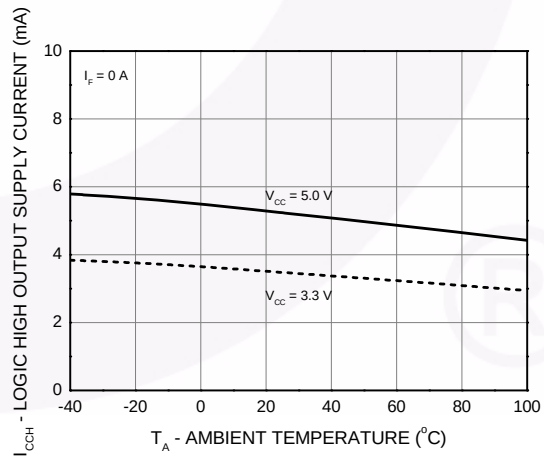


Figure 9. Logic High Output Supply Current vs. Ambient Temperature

Typical Performance Characteristics (Continued)

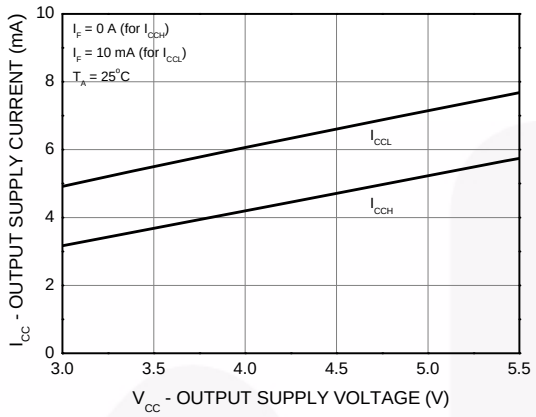


Figure 10. Output Supply Current vs. Output Supply Voltage

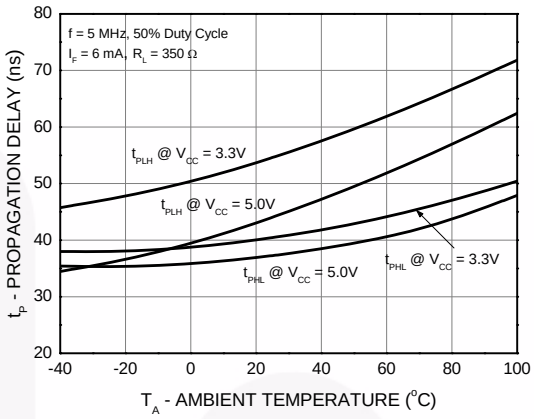


Figure 11. Propagation Delay vs. Ambient Temperature

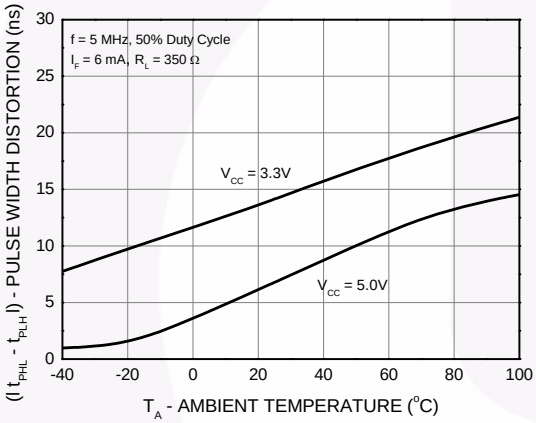


Figure 12. Pulse Width Distortion vs. Ambient Temperature

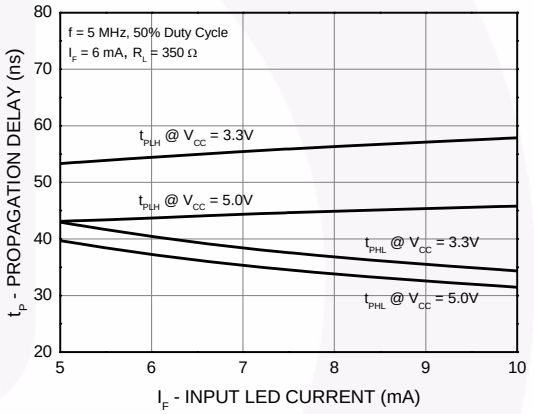


Figure 13. Propagation Delay vs. Input LED Current

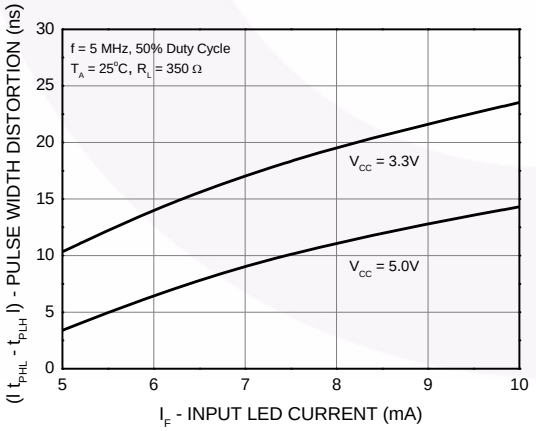


Figure 14. Pulse Width Distortion vs. Input LED Current

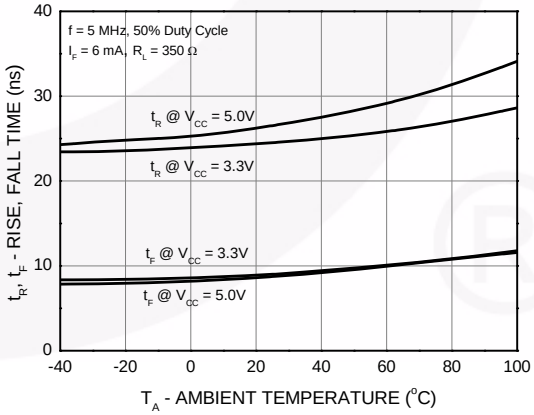


Figure 15. Rise Time and Fall Time vs. Ambient Temperature

Test Circuit

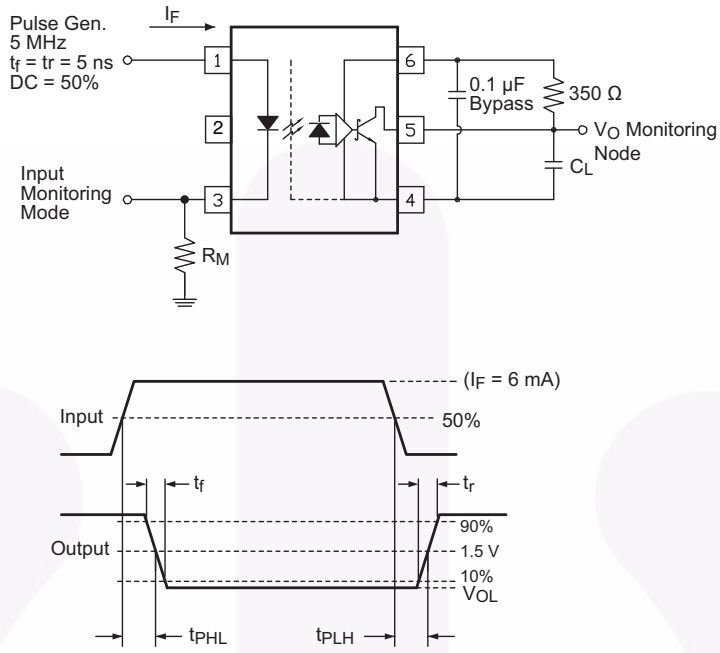


Figure 16. Test Circuit for Propagation Delay, Rise Time, and Fall Time

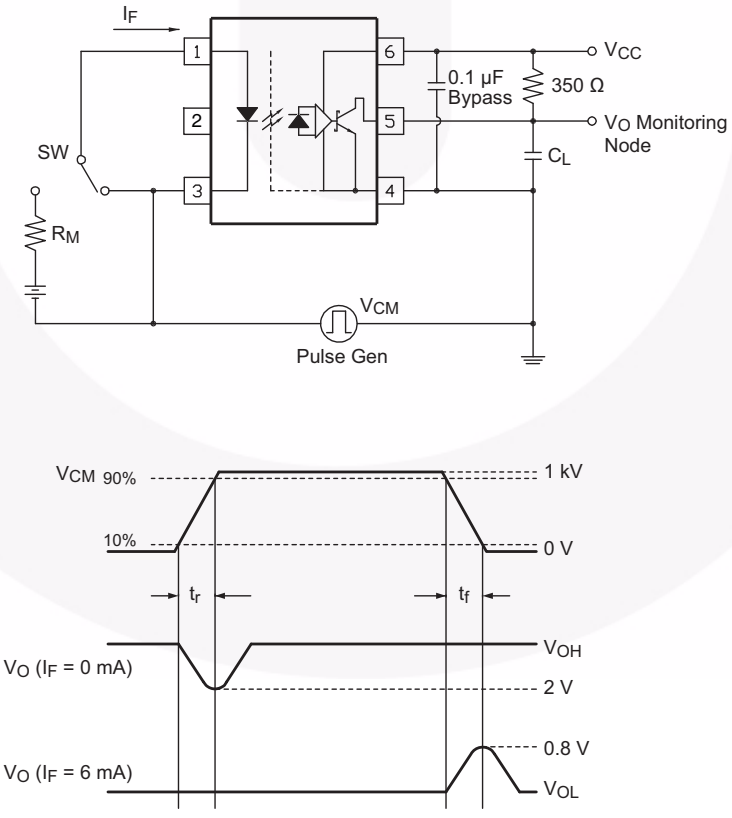
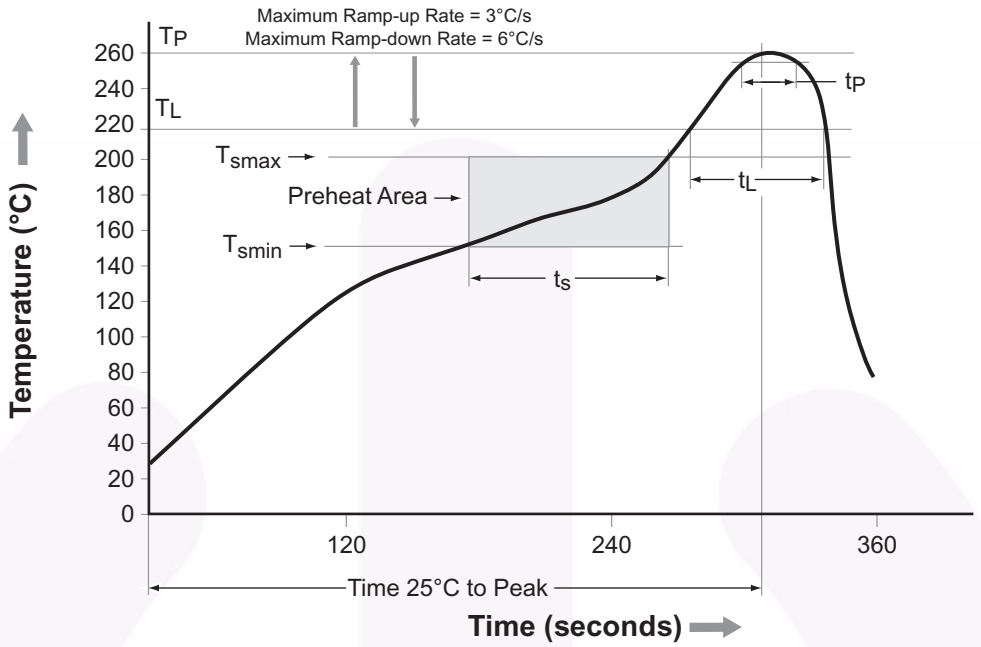


Figure 17. Test Circuit for Instantaneous Common-Mode Rejection Voltage

Reflow Profile



Profile Freature	Pb-Free Assembly Profile
Temperature Minimum (T_{smin})	150°C
Temperature Maximum (T_{smax})	200°C
Time (t_S) from (T_{smin} to T_{smax})	60 s to 120 s
Ramp-up Rate (t_L to t_P)	3°C/second maximum
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60 s to 150 s
Peak Body Package Temperature	260°C +0°C / –5°C
Time (t_P) within 5°C of 260°C	30 s
Ramp-Down Rate (T_P to T_L)	6°C/s maximum
Time 25°C to Peak Temperature	8 minutes maximum

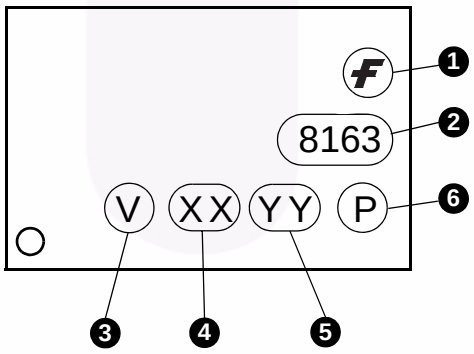
Figure 18. Reflow Profile

Ordering Information

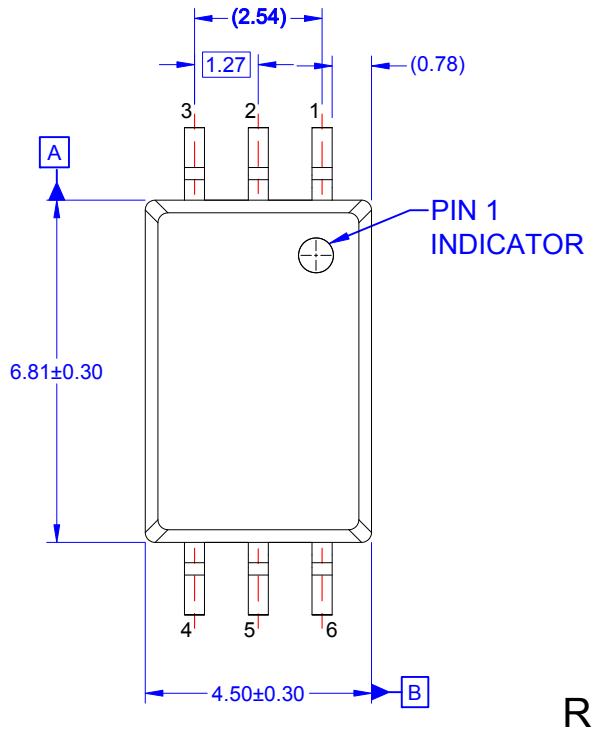
Part Number	Package	Packing Method
FOD8163	Stretched Body SOP 6-Pin	Tube (100 units per tube)
FOD8163R2	Stretched Body SOP 6-Pin	Tape and Reel (1,000 units per reel)
FOD8163V	Stretched Body SOP 6-Pin, DIN EN/IEC60747-5-5 Option	Tube (100 units per tube)
FOD8163R2V	Stretched Body SOP 6-Pin, DIN EN/IEC60747-5-5 Option	Tape and Reel (1,000 units per reel)
FOD8163T	Stretched Body SOP 6-Pin, Wide Lead	Tube (100 units per tube)
FOD8163TR2	Stretched Body SOP 6-Pin, Wide Lead	Tape and Reel (1,000 units per reel)
FOD8163TV	Stretched Body SOP 6-Pin, Wide Lead, DIN EN/IEC60747-5-5 Option	Tube (100 units per tube)
FOD8163TR2V	Stretched Body SOP 6-Pin, Wide Lead, DIN EN/IEC60747-5-5 Option	Tape and Reel (1,000 units per reel)

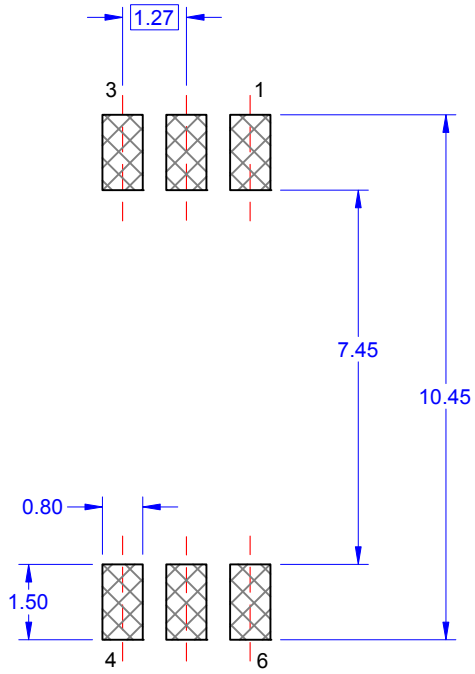
All packages are lead free per JEDEC: J-STD-020B standard.

Marking Information

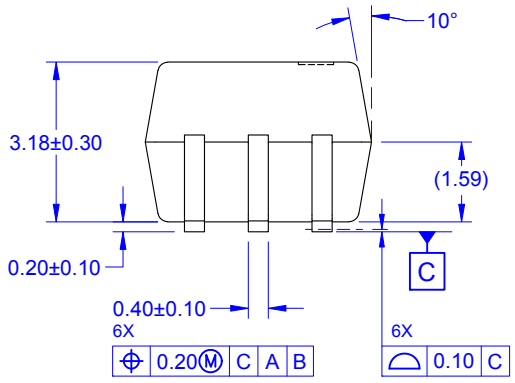


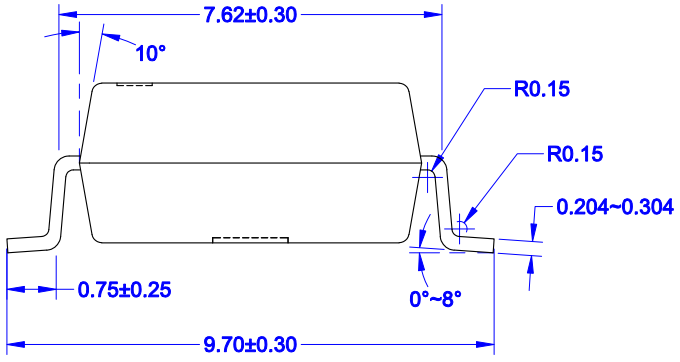
Definitions	
1	Fairchild Logo
2	Device Number, e.g. 8163
3	DIN EN/IEC60747-5-5 Option (only appears on component ordered with this option)
4	One Digit Year Code, e.g. ‘5’
5	Two Digit Work Week Ranging from ‘01’ to ‘53’
6	Assembly Package Code





RECOMMENDED LAND PATTERN

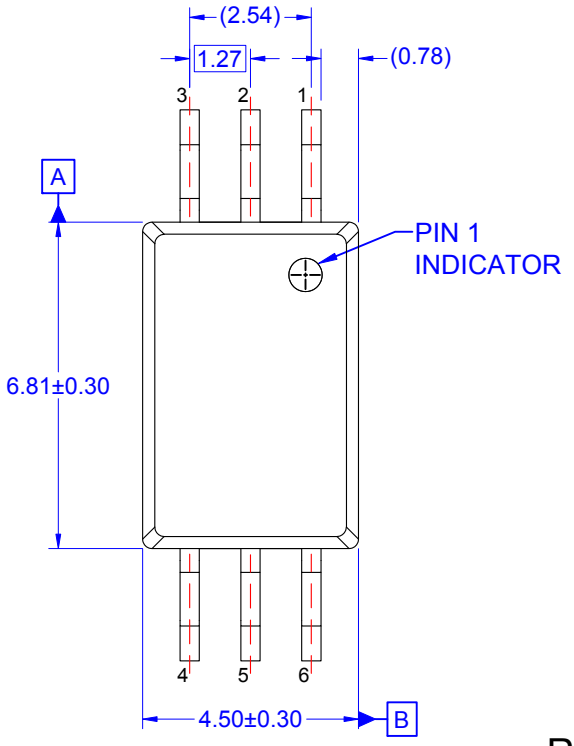


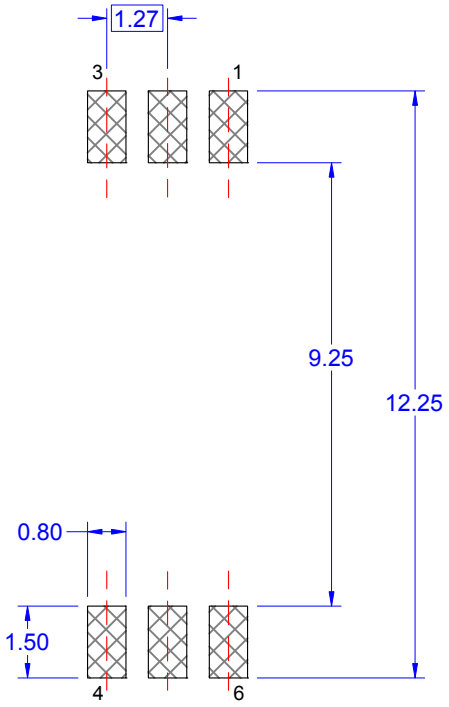


NOTES: UNLESS OTHERWISE SPECIFIED

A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH, AND TIE BAR EXTRUSION.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E) DRAWING FILE NAME: MKT-M06BREV1

FAIRCHILD™





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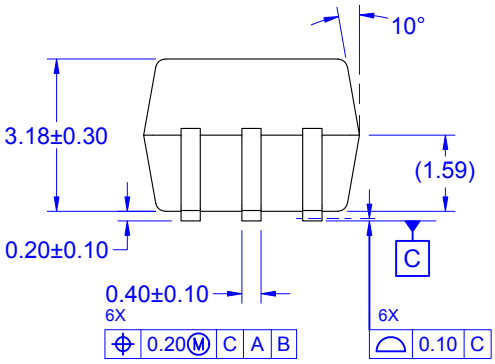

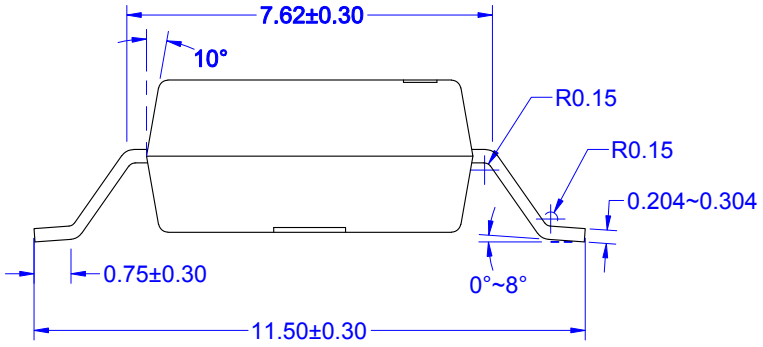

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B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH, AND TIE BAR EXTRUSION.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E) DRAWING FILE NAME: MKT-M06CREV1

FAIRCHILD™