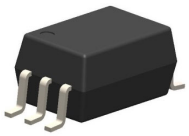
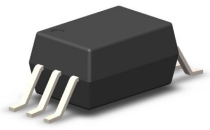
# 3.0 A Output Current, High Speed Gate Drive Optocoupler in Stretched Body SOP 6-Pin

# FOD8342, FOD8342T



SOIC6
CASE 751EL



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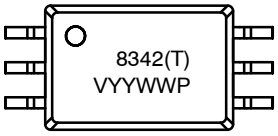
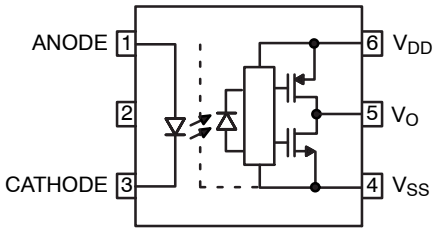
## MARKING DIAGRAM




8342(T) = Specific Device Number
V = DIN EN/IEC60747−5−5 Option
YY = Two Digit Year Code
WW = Two Digit Work Week
P = Assembly Package Code

## FUNCTIONAL SCHEMATIC




## ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 18 of this data sheet.

### Description

The FOD8342 series is a 3.0 A output current gate drive optocoupler, capable of driving medium−power IGBT/ MOSFETs. It is ideally suited for fast−switching driving of power IGBT and MOSFET used in motor−control inverter applications, and high−performance power systems.

The FOD8342 series utilizes stretched body package to achieve 8 mm creepage and clearance distances (FOD8342T), and optimized IC design to achieve reliably high−insulation voltage and high−noise immunity.

The FOD8342 series consists of an Aluminum Gallium Arsenide (AlGaAs) Light−Emitting Diode (LED) optically coupled to an integrated circuit with a high−speed driver for push−pull MOSFET output stage. The device is housed in a stretched body, 6−pin, small outline, plastic package.

### Features

- FOD8342T − 8 mm Creepage and Clearance Distance, and 0.4 mm Insulation Distance to Achieve Reliable and High−Voltage Insulation
- 3.0 A Peak Output Current Driving Capability for Medium− Power IGBT/MOSFET
  - Use of P−Channel MOSFETs at Output Stage Enables Output Voltage Swing Close to Supply Rail
- 20 kV/μs Minimum Common Mode Rejection
- Wide Supply Voltage Range: 10 V to 30 V
- Fast Switching Speed Over Full Operating Temperature Range
  - 210 ns Maximum Propagation Delay
  - 65 ns Maximum Pulse Width Distortion
- Under−Voltage Lockout (UVLO) with Hysteresis
- Extended Industrial Temperate Range: −40°C to 100°C
- Safety and Regulatory Approvals:
  - UL1577, 5,000 $V_{RMS}$ for 1 Minute
  - DIN EN/IEC60747−5−5, 1,140V Peak Working Insulation Voltage

### Applications

- AC and Brushless DC Motor Drives
- Industrial Inverter
- Uninterruptible Power Supply
- Induction Heating
- Isolated IGBT/Power MOSFET Gate Drive

### Related Resources

- FOD3182, 3 A Output Current, High Speed MOSFET Gate Drive Optocoupler
- FOD8314, FOD8314T, 1.0 A Output Current, Gate Drive Optocoupler in Stretched Body SOP 6−Pin
- www.onsemi.com

**Table 1. TRUTH TABLE**

| LED | $V_{DD}$ – $V_{SS}$ "Positive Going" (Turn–On) | $V_{DD}$ – $V_{SS}$ "Negative Going" (Turn–Off) | $V_O$ |
|---|---|---|---|
| Off | 0 V to 30 V | 0 V to 30 V | LOW |
| On | 0 V to 7 V | 0 V to 6.5 V | LOW |
| On | 7 V to 9.5 V | 6.5 V to 9 V | Transition |
| On | 9.5 V to 30 V | 9 V to 30 V | HIGH |

**Table 2. PIN DESCRIPTION**

| Pin No. | Name | Description |
|---|---|---|
| 1 | ANODE | LED Anode |
| 2 | N.C | Not Connection |
| 3 | CATHODE | LED Cathode |
| 4 | $V_{SS}$ | Negative Supply Voltage |
| 5 | $V_O$ | Output Voltage |
| 6 | $V_{DD}$ | Positive Supply Voltage |

## Pin Configuration

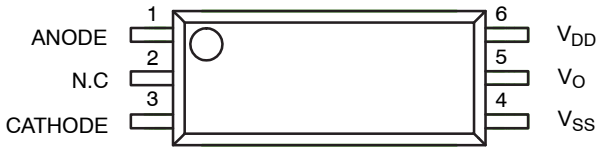



**Figure 1. Pin Configuration**

**Table 3. SAFETY AND INSULATION RATINGS**
As per DIN_EN/IEC60747−5−5. This optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

| Parameter | | Symbol | FOD8342 | FOD8342T | Unit |
|---|---|---|---|---|---|
| Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Main Voltage | <150 Vrms | | I−IV | I−IV | |
| | <300 Vrms | | I−IV | I−IV | |
| | <450 Vrms | | I−III | I−IV | |
| | <600 Vrms | | I−III | I−III | |
| Climatic Classification | | | 40/100/21 | 40/100/21 | |
| Pollution Degree (DIN VDE 0110/1.89) | | | 2 | 2 | |
| Comparative Tracking Index | | CTI | 175 | 175 | |
| Input to Output Test Voltage, Method B, $V_{IORM}$ x 1.875 = $V_{PR}$, 100% Production Test with $t_m$ = 1 sec, Partial Discharge <5 pC | | $V_{PR}$ | 1,671 | 2,137 | $V_{peak}$ |
| Input to Output Test Voltage, Method A, $V_{IORM}$ x 1.6 = $V_{PR}$, Type and Sample Test with $t_m$ = 10 sec, Partial Discharge <5 pC | | | 1,426 | 1,824 | $V_{peak}$ |
| Max Working Insulation Voltage | | $V_{IORM}$ | 891 | 1,140 | $V_{peak}$ |
| Highest Allowable Over Voltage | | $V_{IOTM}$ | 6,000 | 8,000 | $V_{peak}$ |
| External Creepage | | | ≥8.0 | ≥8.0 | mm |
| External Clearance | | | ≥7.0 | ≥8.0 | mm |
| Distance Through Insulation (Insulation Thickness) | | DTI | ≥0.4 | ≥0.4 | mm |
| Safety Limit Values− Maximum Values Allowed in the Event of a Failure, | | | | | |
| Case Temperature | | $T_S$ | 150 | 150 | °C |
| Input Current | | $I_{S,INPUT}$ | 200 | 200 | mA |
| Output Power | | $P_{S,OUTPUT}$ | 600 | 600 | mW |
| Insulation Resistance at $T_S$, $V_{IO}$ = 500 V | | $R_{IO}$ | $10^9$ | $10^9$ | Ω |

**Table 4. ABSOLUTE MAXIMUM RATINGS** ($T_A$ = 25°C unless otherwise specified)

| Symbol | Parameter | Value | Units |
|---|---|---|---|
| $T_{STG}$ | Storage Temperature | −40 to +125 | °C |
| $T_{OPR}$ | Operating Temperature | −40 to +100 | °C |
| $T_J$ | Junction Temperature | −40 to +125 | °C |
| $T_{SOL}$ | Lead Solder Temperature *(Refer to Reflow Temperature Profile)* | 260 for 10 s | °C |
| $I_{F(AVG)}$ | Average Input Current | 25 | mA |
| $V_R$ | Reverse Input Voltage | 5.0 | V |
| $I_{O(PEAK)}$ | Peak Input Voltage (Note 1) | 3 | A |
| $V_{DD}$ | Supply Voltage | −0.5 to 35 | V |
| $V_{O(PEAK)}$ | Peak Output Voltage | 0 to $V_{DD}$ | V |
| $t_{R(IN)}$, $t_{F(IN)}$ | Input Signal Rise and Fall Time | 250 | ns |
| $PD_I$ | Input Power Dissipation (Notes 2, 4) | 45 | mW |
| $PD_O$ | Output Power Dissipation (Notes 3, 4) | 500 | mW |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Maximum pulse width = 10 μs, maximum duty cycle = 0.2%.
2. No derating required across operating temperature range.
3. Derate linearly from 25°C at a rate of 5.2 mW/°C.
4. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

**Table 5. RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $T_A$ | Ambient Operating Temperature | −40 | +100 | °C |
| $V_{DD}$ − $V_{SS}$ | Supply Voltages | 10 | 30 | V |
| $I_{F(ON)}$ | Input Current (ON) | 10 | 16 | mA |
| $V_{F(OFF)}$ | Input Voltage (OFF) | −3.0 | 0.8 | V |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 6. ISOLATION CHARACTERISTICS** (Apply over all recommended conditions, typical value is measured at $T_A$ = 25°C)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{ISO}$ | Input−Output Isolation Voltage | $T_A$ = 25°C, R.H. < 50%, t = 1.0 min, $I_{I-O} \le$ 20 μA (Notes 5, 6) | 5000 | | | $VAC_{RMS}$ |
| $R_{ISO}$ | Isolation Resistance | $V_{I-O}$ = 500 V (Note 5) | | $10^{11}$ | | Ω |
| $C_{ISO}$ | Isolation Capacitance | $V_{I-O}$ = 0 V, freq = 1.0 MHz (Note 5) | | 1 | | pF |

5. Device is considered a two terminal device: Pins 1, 2 and 3 are shorted together and Pins 4, 5, and 6 are shorted together.
6. 5,000 $VAC_{RMS}$ for 1 minute duration is equivalent to 6,000 $VAC_{RMS}$ for 1 second duration.

**Table 7. ELECTRICAL CHARACTERISTICS** (Apply over all recommended conditions, $T_A$ = −40°C to +100°C, 4.5 V ≤ $V_{DD}$ ≤ 30 V, FOD8480: $I_{F(ON)}$ = 6 mA to 10 mA, FOD8482: $I_{F(ON)}$ = 4 mA to 7 mA, $V_{F(OFF)}$ = 0 to 0.8 V, unless otherwise specified. Typical value is measured at $T_A$ = 25°C and $V_{DD}$ = 5 V.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_F$ | Input Forward Voltage | $I_F$ = 10 mA | 1.1 | 1.5 | 1.8 | V |
| $\Delta V_F/\Delta T_A$ | Temperature Coefficient of Forward Voltage | | | −1.8 | | mV/°C |
| $BV_R$ | Input Reverse Breakdown Voltage | $I_R$ = 10 μA | 5.0 | | | V |
| $C_{IN}$ | Input Capacitance | $V_F$ = 0 V, f = 1 MHz | | 20 | | pF |
| $I_{OH}$ | High Level Output Current (Note 1) | $V_{OH}$ = $V_{DD}$ − 3 V | 1.0 | | | A |
| | | $V_{OH}$ = $V_{DD}$ − 6 V | 2.5 | | | |
| $I_{OL}$ | Low Level Output Current (Note 1) | $V_{OL}$ = $V_{SS}$ + 3 V | 1.0 | | | A |
| | | $V_{OL}$ = $V_{SS}$ + 6 V | 2.5 | | | |
| $V_{OH}$ | High Level Output Voltage (Notes 7, 8) | $I_F$ = 10 mA, $I_O$ = −100 mA | $V_{DD}$ − 0.5 | $V_{DD}$ − 0.1 | | V |
| $V_{OL}$ | Low Level Output Voltage (Notes 7, 8) | $I_F$ = 0 mA, $I_O$ = 100 mA | | $V_{SS}$ + 0.1 | $V_{SS}$ + 0.5 | |
| $I_{DDH}$ | High Output Supply Current | $V_O$ = Open, $I_F$ = 10 to 16 mA | | 2.9 | 4.0 | mA |
| $I_{DDL}$ | Low Output Supply Current | $V_O$ = Open, $V_F$ = −3.0 to 0.8 V | | 2.8 | 4.0 | mA |
| $I_{FLH}$ | Threshold Input Current Low to High | $I_O$ = 0 mA, $V_O$ > 5 V | | 2.0 | 7.5 | mA |
| $V_{FHL}$ | Threshold Input Voltage High to Low | $I_O$ = 0 mA, $V_O$ < 5 V | 0.8 | | | V |
| $V_{UVLO+}$ | Under Voltage Lockout Threshold | $I_F$ = 10 mA, $V_O$ > 5 V | 7.0 | 8.3 | 9.5 | V |
| $V_{UVLO-}$ | | $I_F$ = 10 mA, $V_O$ < 5 V | 6.5 | 7.7 | 9.0 | |
| $UVLO_{HYS}$ | Under Voltage Lockout Threshold Hysteresis | | | 0.6 | | V |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. In this test, $V_{OH}$ is measured with a dc load current of 100 mA. When driving capacitive load $V_{OH}$ will approach $V_{DD}$ as $I_{OH}$ approaches 0 A.
8. Maximum pulse width = 1 ms, maximum duty cycle = 20%.

**Table 8. SWITCHING CHARACTERISTICS** (Apply over all recommended conditions, typical value is measured at $T_A$ = 25°C, $V_{SS}$ = Ground and $V_{DD}$ = 30 V, unless otherwise specified.)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $t_{PHL}$ | Propagation Delay Time to Logic Low Output (Note 9) | $I_F$ = 10 mA, $R_g$ = 10 Ω, $C_g$ = 10 nF, f = 250 kHz, Duty Cycle = 50% | 50 | 145 | 210 | ns |
| $t_{PLH}$ | Propagation Delay Time to Logic High Output (Note 10) | | 50 | 120 | 210 | ns |
| PWD | Pulse Width Distortion, $\|t_{PHL} - t_{PLH}\|$ (Note 11) | | | 35 | 65 | ns |
| PDD (Skew) | Propagation Delay Difference Between Any Two Parts (Note 12) | | −90 | | 90 | |
| $t_R$ | Output Rise Time (10% to 90%) | | | 38 | | ns |
| $t_F$ | Output Fall Time (90% to 10%) | | | 24 | | ns |
| $t_{UVLO\ ON}$ | ULVO Turn On Delay | $I_F$ = 10 mA, $V_O$ > 5 V | | 2.0 | | μs |
| $t_{UVLO\ OFF}$ | ULVO Turn Off Delay | $I_F$ = 10 mA, $V_O$ < 5 V | | 0.3 | | μs |
| $\|CM_H\|$ | Common Mode Transient Immunity at Output High | $V_{DD}$ = 30 V, $I_F$ = 10 mA to 16 mA, $V_{CM}$ = 2000 V, $T_A$ = 25°C (Note 13) | 20 | 50 | | kV/μs |
| $\|CM_L\|$ | Common Mode Transient Immunity at Output Low | $V_{DD}$ = 30 V, $V_F$ = 0 V, $V_{CM}$ = 2000 V, $T_A$ = 25°C (Note 14) | 20 | 50 | | kV/μs |

9. Propagation delay $t_{PHL}$ is measured from the 50% level on the falling edge of the input pulse to the 50% level of the falling edge of the $V_O$ signal.
10. Propagation delay $t_{PLH}$ is measured from the 50% level on the rising edge of the input pulse to the 50% level of the rising edge of the $V_O$ signal.
11. PWD is defined as $|t_{PHL} - t_{PLH}|$ for any given device.
12. The difference between $t_{PHL}$ and $t_{PLH}$ between any two FOD8342 parts under the same operating conditions, with equal loads.
13. Common mode transient immunity at output high is the maximum tolerable negative dVcm/dt on the trailing edge of the common mode impulse signal, $V_{CM}$, to ensure that the output remains high (i.e., $V_O$ > 15.0 V).
14. Common mode transient immunity at output low is the maximum tolerable positive dVcm/dt on the leading edge of the common pulse signal, $V_{CM}$, to ensure that the output remains low (i.e., $V_O$ < 1.0 V).

## TYPICAL CHARACTERISTICS

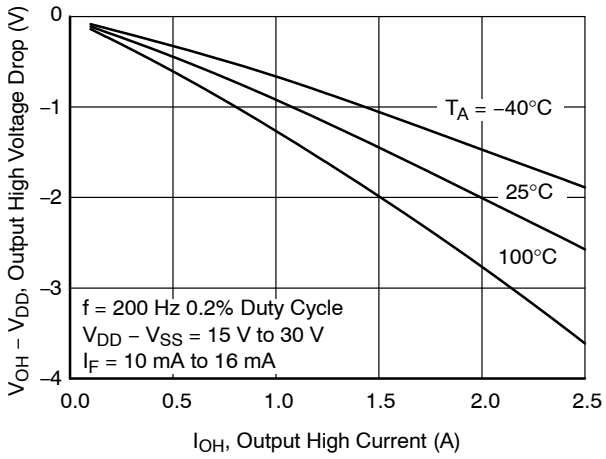



**Figure 2. Output High Voltage Drop vs. Output High Current**

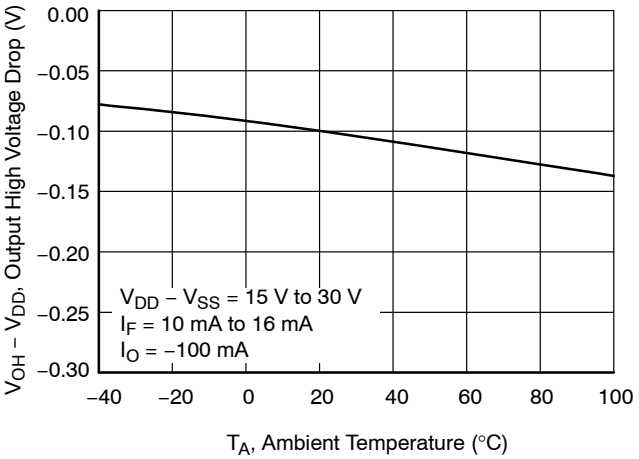



**Figure 3. Output High Voltage Drop vs. Ambient Temperature**

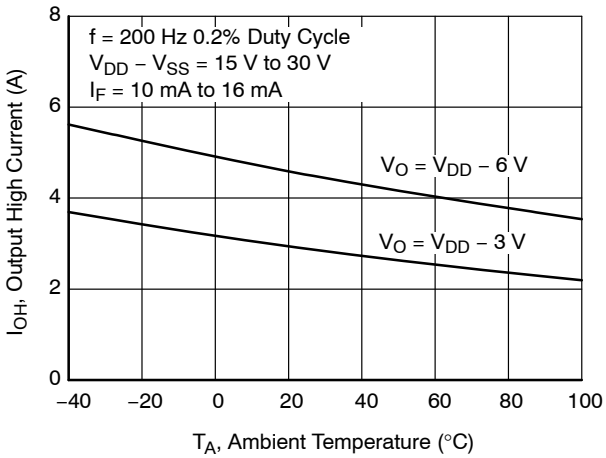



**Figure 4. Output High Current vs. Ambient Temperature**

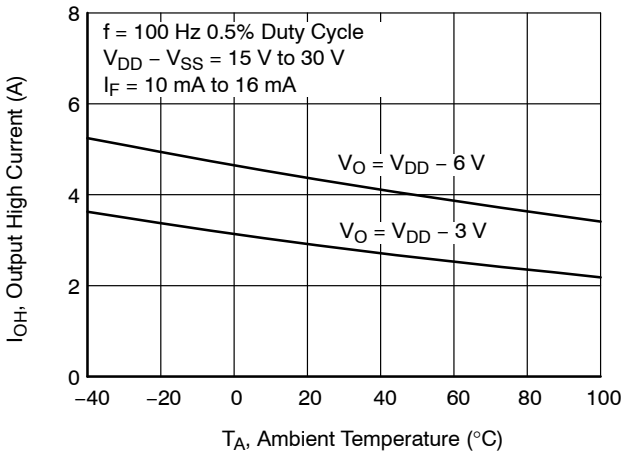



**Figure 5. Output High Current vs. Ambient Temperature**

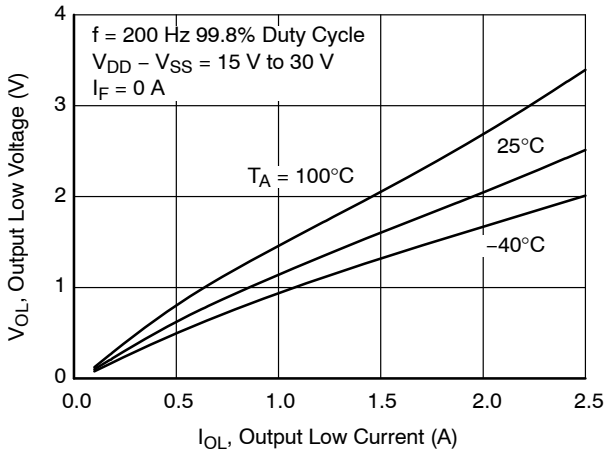



**Figure 6. Output Low Voltage vs. Output Low Current**

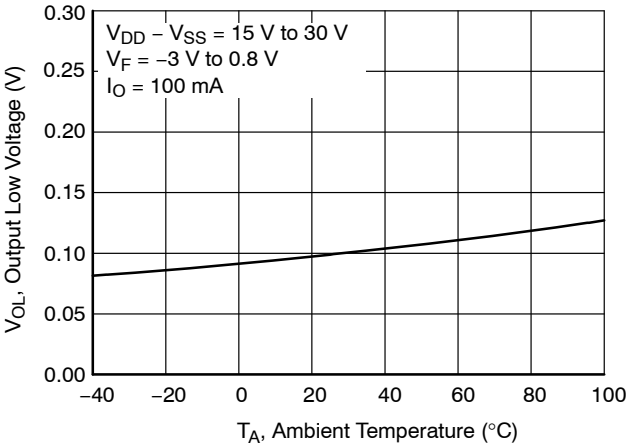



**Figure 7. Output Low Voltage vs. Ambient Temperature**

## TYPICAL CHARACTERISTICS (continued)

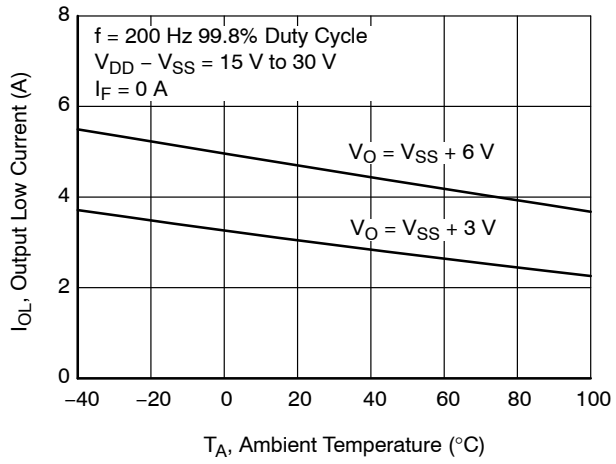



**Figure 8. Output Low Current vs. Ambient Temperature**

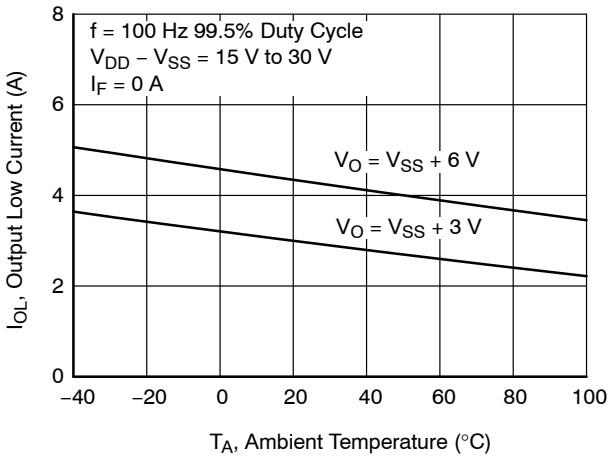



**Figure 9. Output Low Current vs. Ambient Temperature**

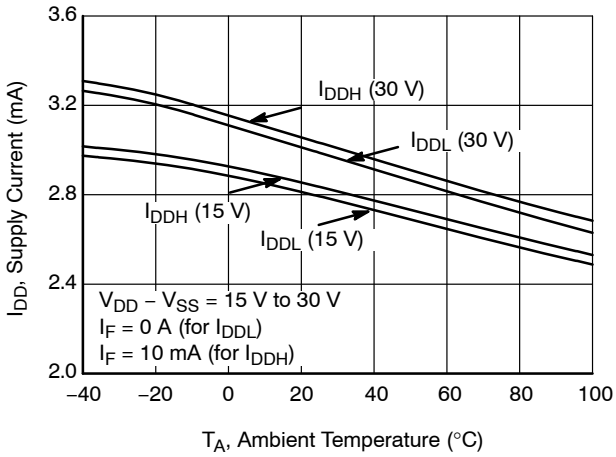



**Figure 10. Supply Current vs. Ambient Temperature**

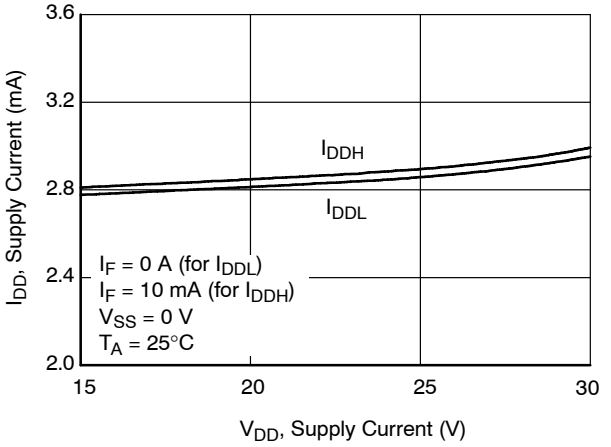



**Figure 11. Supply Current vs. Supply Voltage**

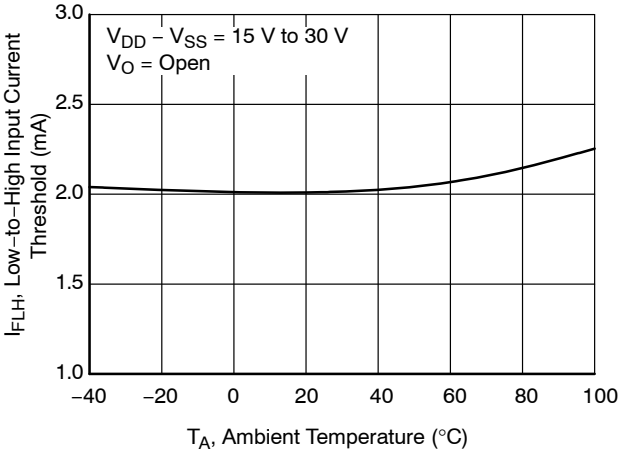



**Figure 12. Low−to−High Input Current Threshold vs. Ambient Temperature**

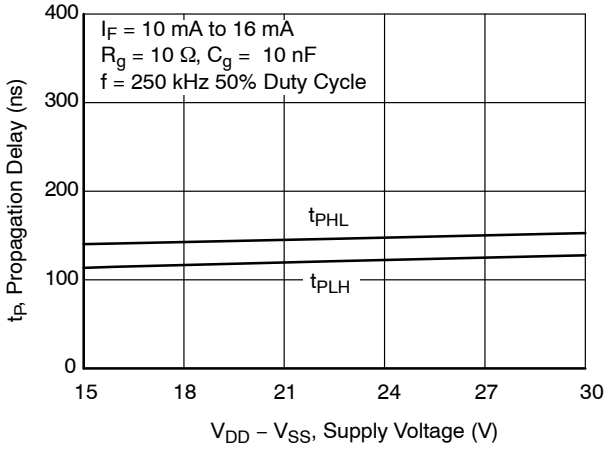



**Figure 13. Propagation Delay vs. Supply Voltage**

## TYPICAL CHARACTERISTICS (continued)

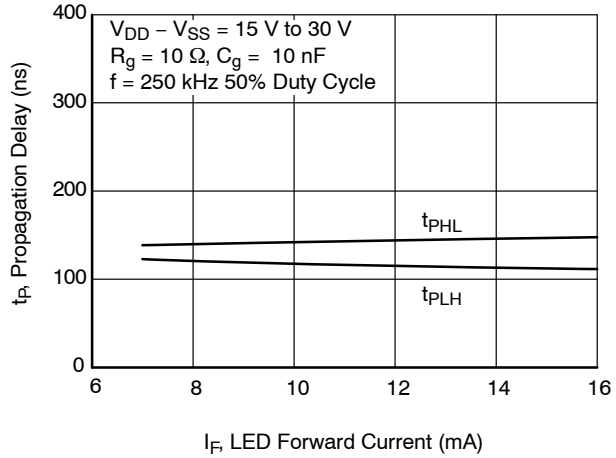



**Figure 14. Propagation Delay vs. LED Forward Current**

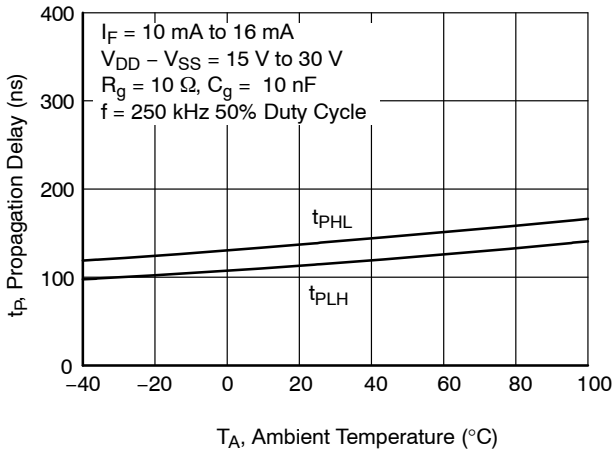



**Figure 15. Propagation Delay vs. Ambient Temperature**

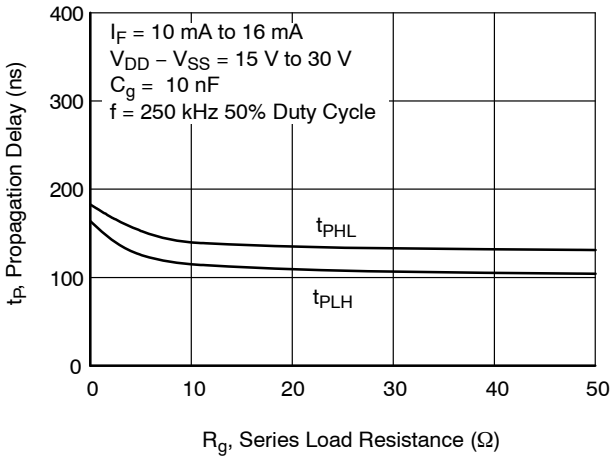



**Figure 16. Propagation Delay vs. Series Load Resistance**

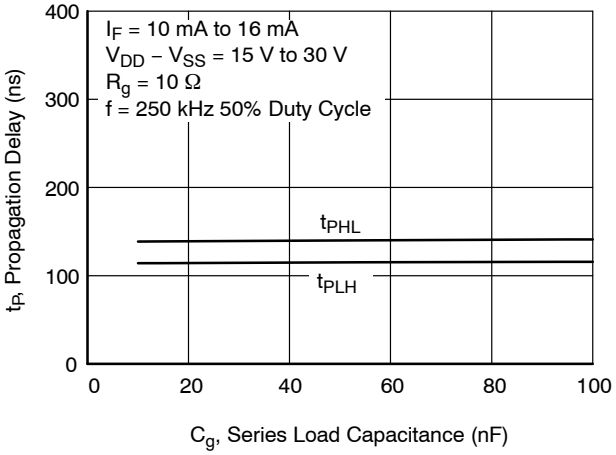



**Figure 17. Propagation Delay vs. Series Load Capacitance**

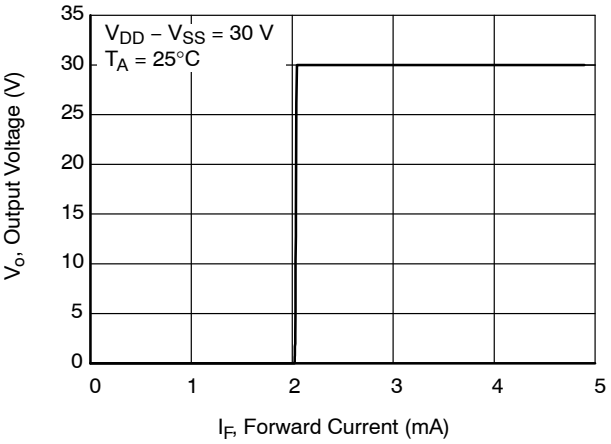



**Figure 18. Transfer Characteristics**

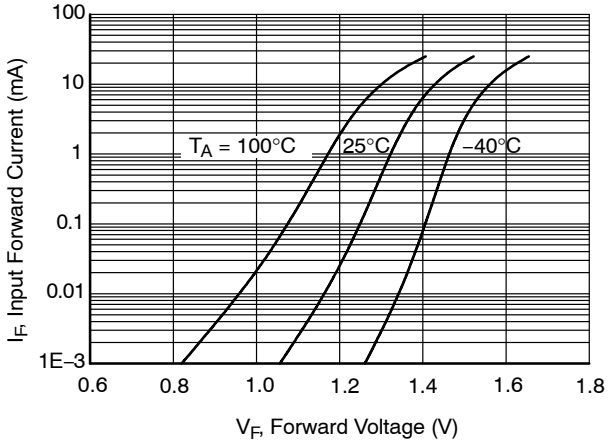



**Figure 19. Input Forward Current vs. Forward Voltage**

## TYPICAL CHARACTERISTICS (continued)

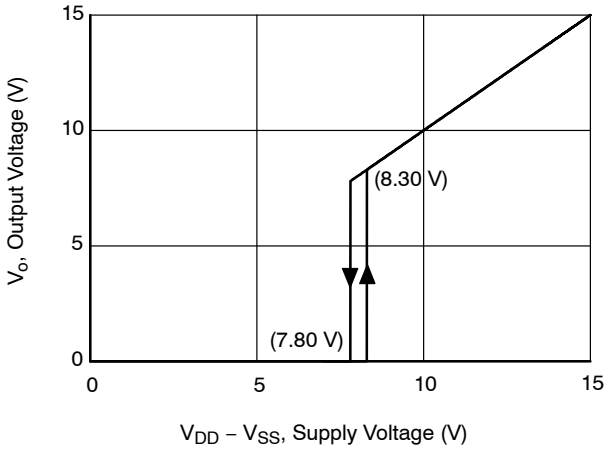



**Figure 20. Under Voltage Lockout**

## TEST CIRCUIT

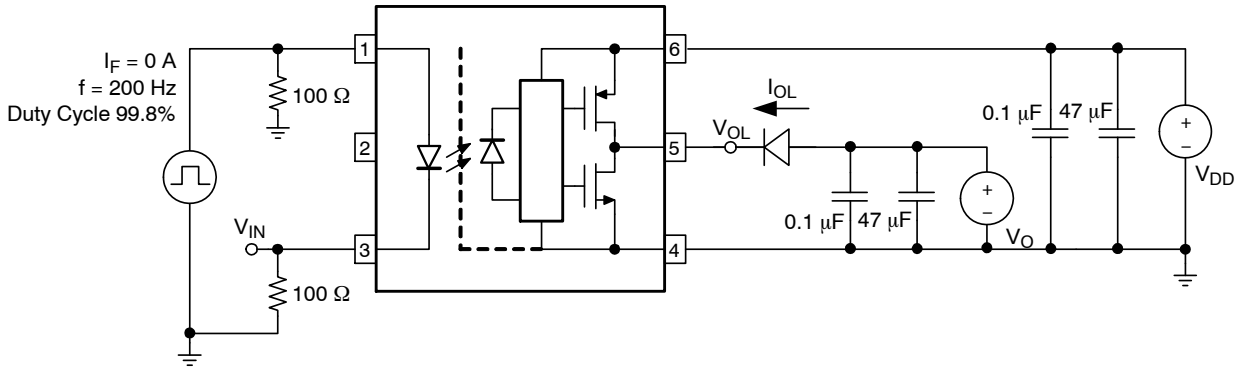



**Figure 21. $I_{OL}$ Test Circuit**

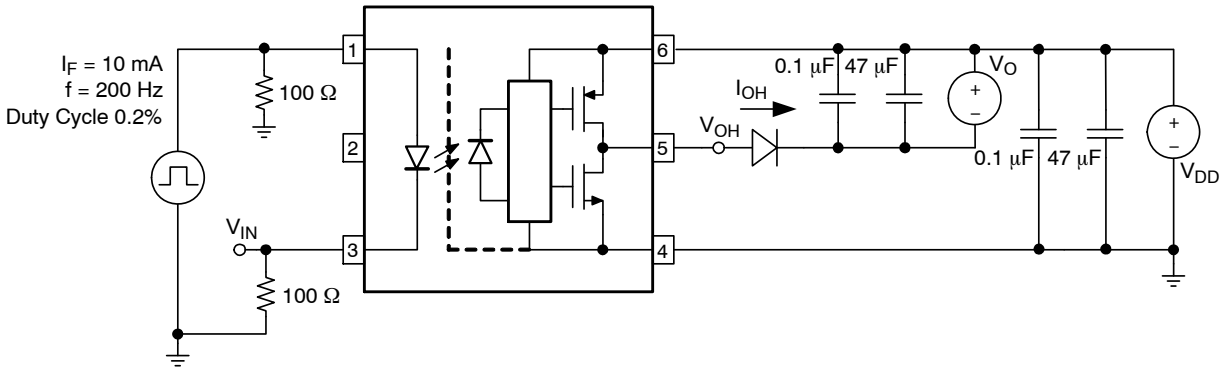



**Figure 22. $I_{OH}$ Test Circuit**

**TEST CIRCUIT** (continued)

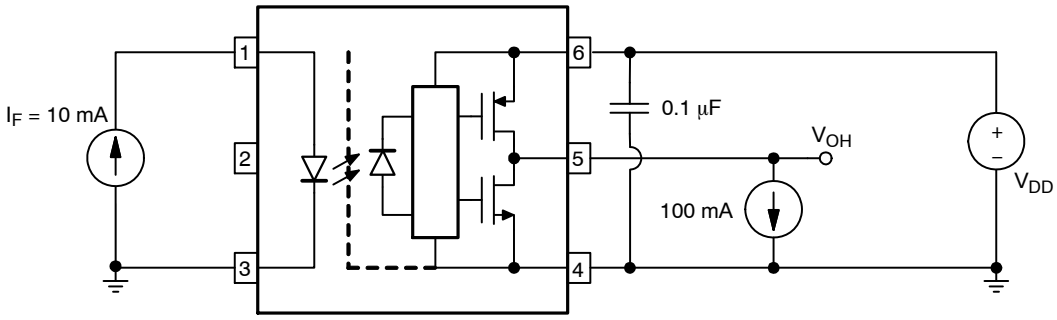



**Figure 23. $V_{OH}$ Test Circuit**

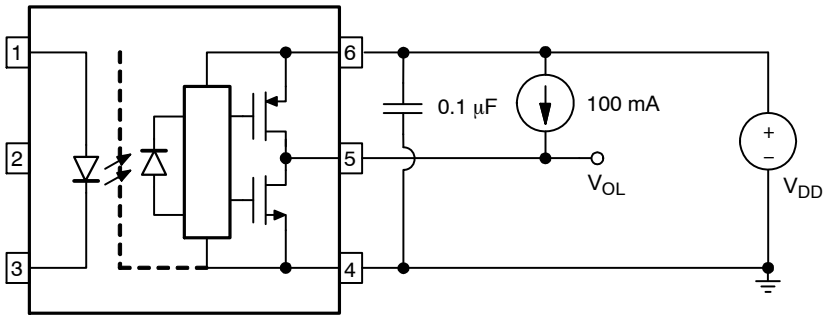



**Figure 24. $V_{OL}$ Test Circuit**

## TEST CIRCUIT (continued)

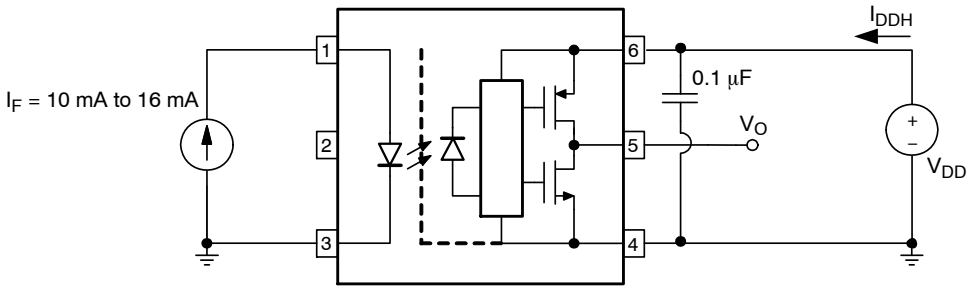



**Figure 25. $I_{DDH}$ Test Circuit**

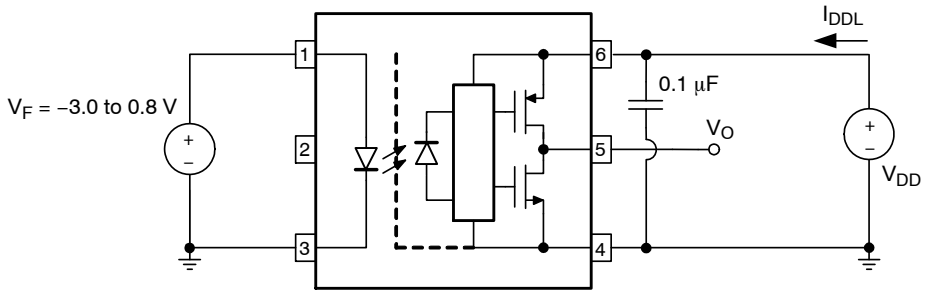



**Figure 26. $I_{DDL}$ Test Circuit**

## TEST CIRCUIT (continued)

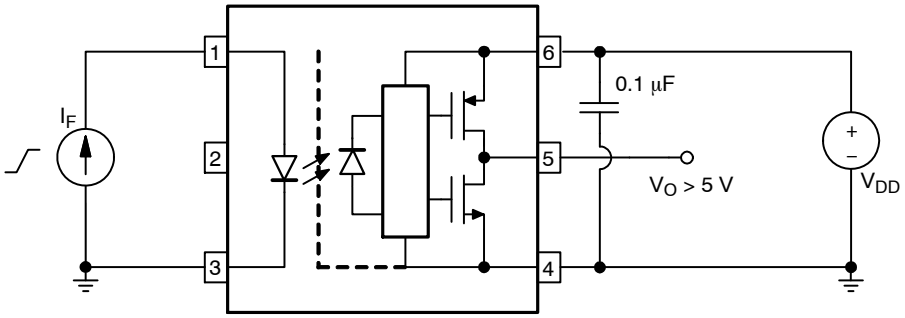



**Figure 27. $I_{FLH}$ Test Circuit**

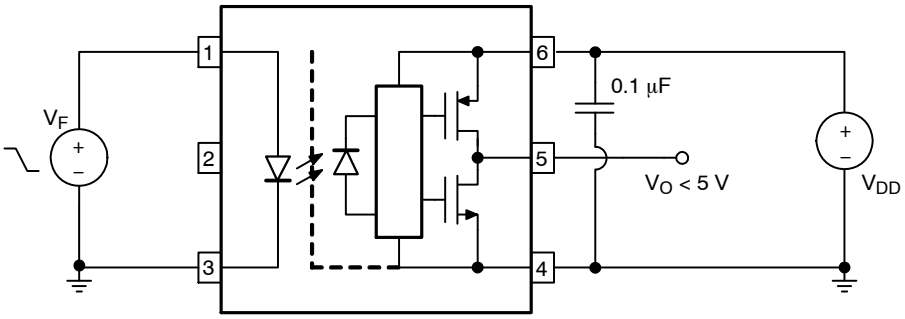



**Figure 28. $V_{FHL}$ Test Circuit**

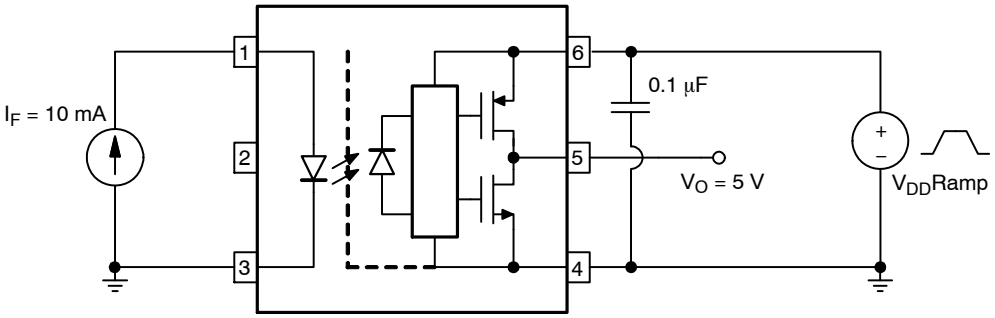



**Figure 29. UVLO Test Circuit**

## TEST CIRCUIT (continued)

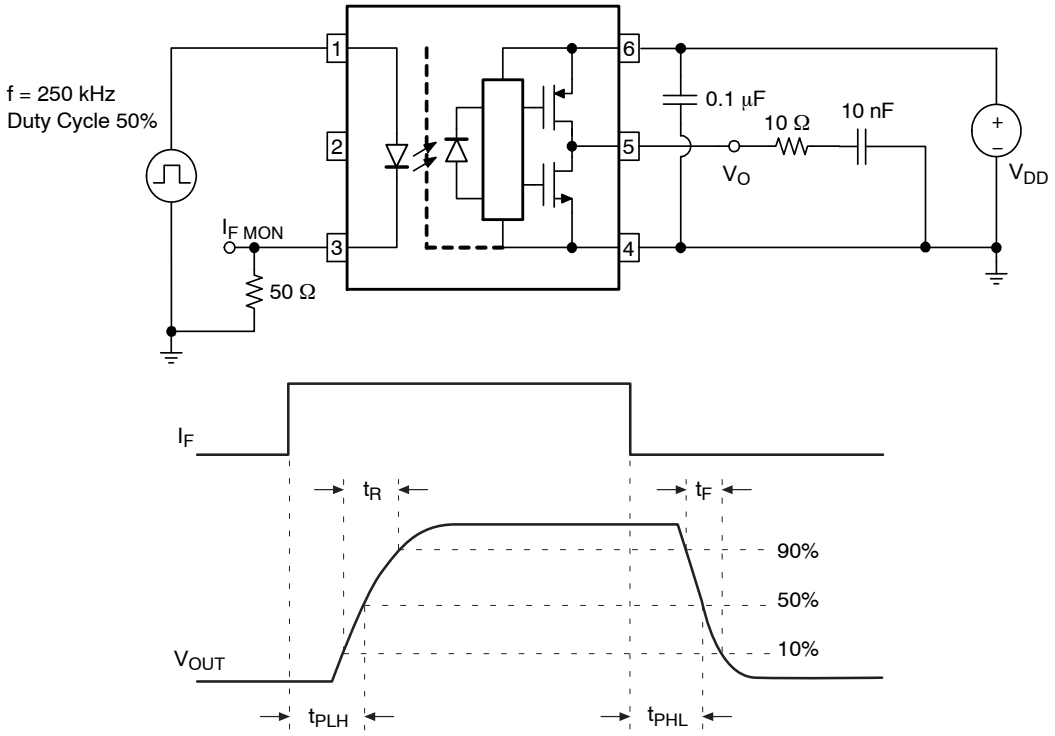
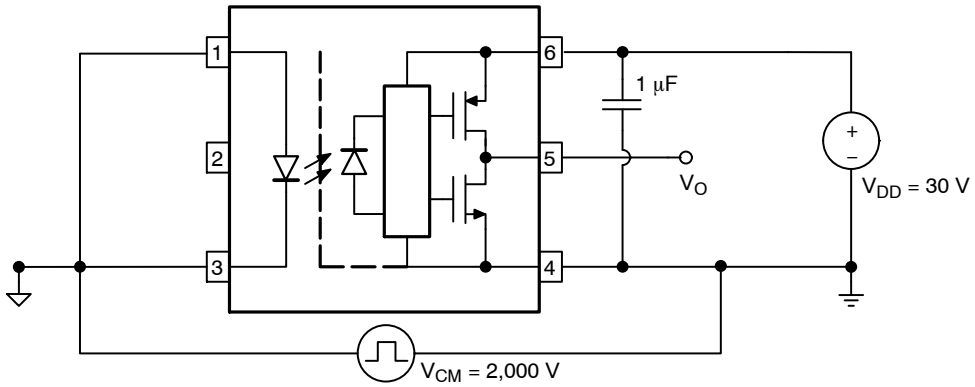
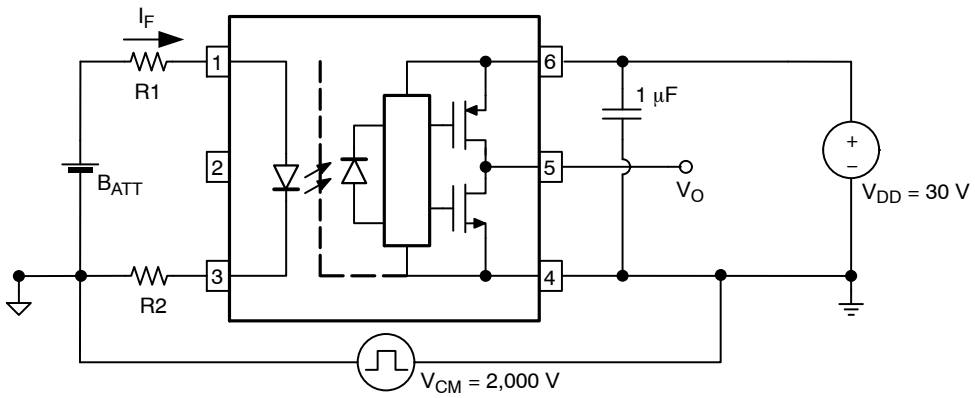



**Figure 30. $t_{PHL}$, $t_{PLH}$, $t_R$ and $t_F$ Test Circuit and Waveforms**

## TEST CIRCUIT (continued)




**Common−Mode Low (CML) Test Circuit**




**Common−Mode High (CMH) Test Circuit**

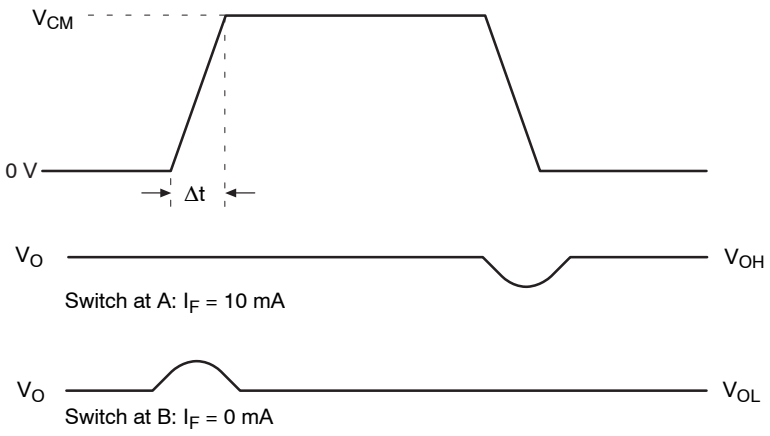
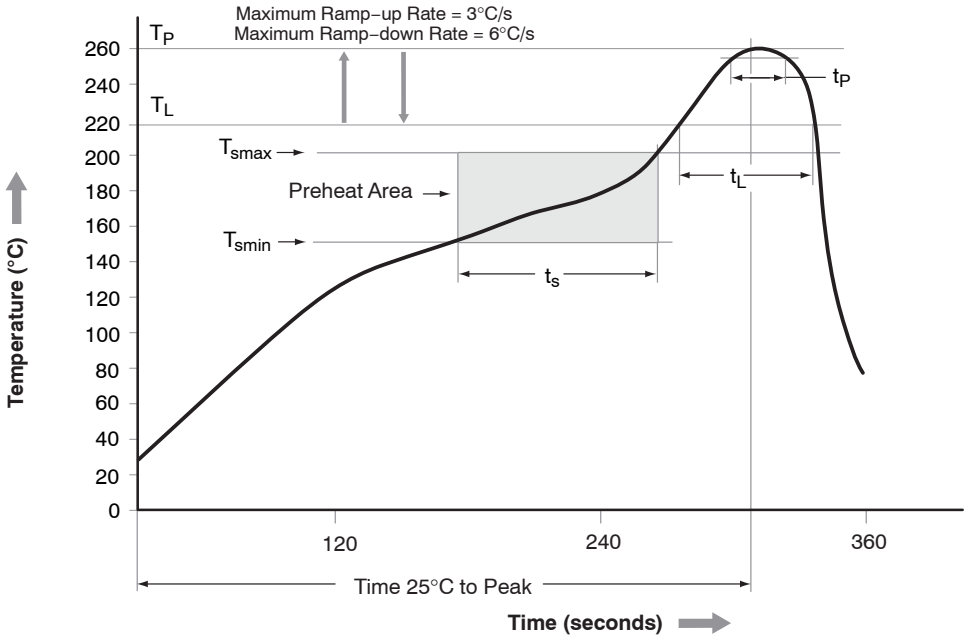



**Figure 31. CMR Test Circuit and Waveforms**

## REFLOW PROFILE




| Profile Freature | Pb−Free Assembly Profile |
|---|---|
| Temperature Minimum ($T_{smin}$) | 150°C |
| Temperature Maximum ($T_{smax}$) | 200°C |
| Time ($t_S$) from ($T_{smin}$ to $T_{smax}$) | 60 s to 120 s |
| Ramp−up Rate ($t_L$ to $t_P$) | 3°C/s maximum |
| Liquidous Temperature ($T_L$) | 217°C |
| Time ($t_L$) Maintained Above ($T_L$) | 60 s to 150 s |
| Peak Body Package Temperature | 260°C +0°C / −5°C |
| Time ($t_P$) within 5°C of 260°C | 30 s |
| Ramp−Down Rate ($T_P$ to $T_L$) | 6°C/s maximum |
| Time 25°C to Peak Temperature | 8 minutes maximum |

**Figure 32. Reflow Profile**

## ORDERING INFORMATION

| Part Number | Package | Packing Method |
|---|---|---|
| FOD8342 | Stretched Body SOP 6−Pin | Tube (100 units per tube) |
| FOD8342R2 | Stretched Body SOP 6−Pin | Tape and Reel (1,000 units per reel) |
| FOD8342V | Stretched Body SOP 6−Pin,<br>DIN EN/IEC60747−5−5 Option | Tube (100 units per tube) |
| FOD8342R2V | Stretched Body SOP 6−Pin,<br>DIN EN/ IEC60747−5−5 Option | Tape and Reel (1,000 units per reel) |
| FOD8342T | Stretched Body SOP 6−Pin, Wide Lead | Tube (100 units per tube) |
| FOD8342TR2 | Stretched Body SOP 6−Pin, Wide Lead | Tape and Reel (1,000 units per reel) |
| FOD8342TV | Stretched Body SOP 6−Pin, Wide Lead,<br>DIN EN/IEC60747−5−5 Option | Tube (100 units per tube) |
| FOD8342TR2V | Stretched Body SOP 6−Pin, Wide Lead,<br>DIN EN/ IEC60747−5−5 Option | Tape and Reel (1,000 units per reel) |

*All packages are lead free per JEDEC: J−STD−020B standard.

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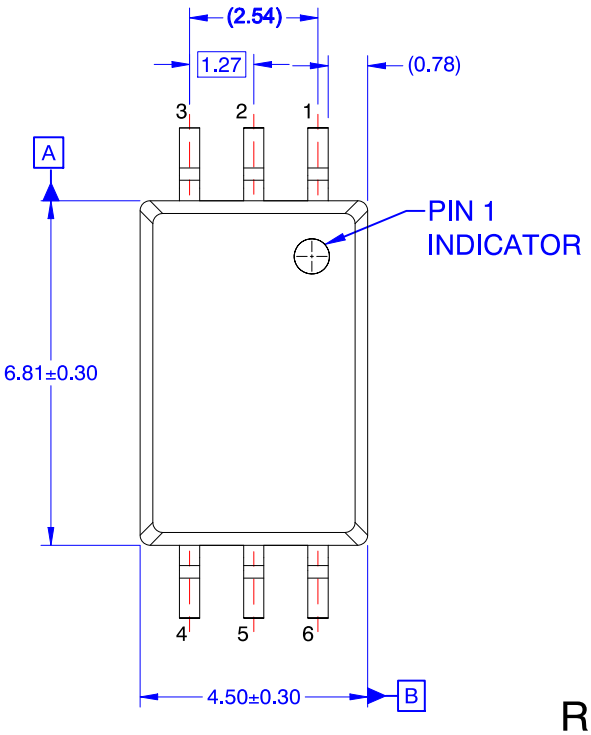
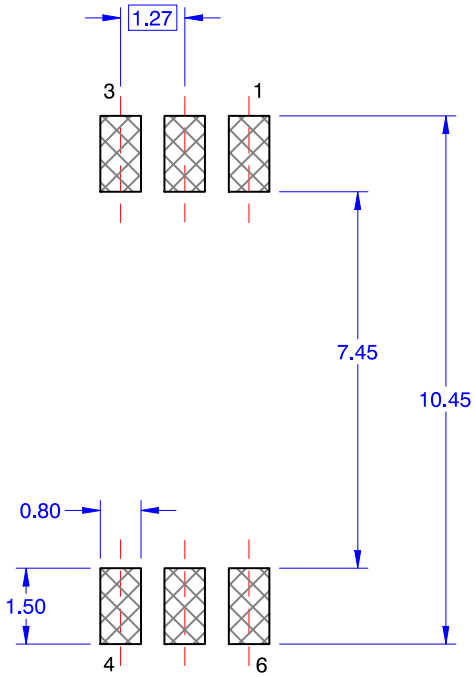
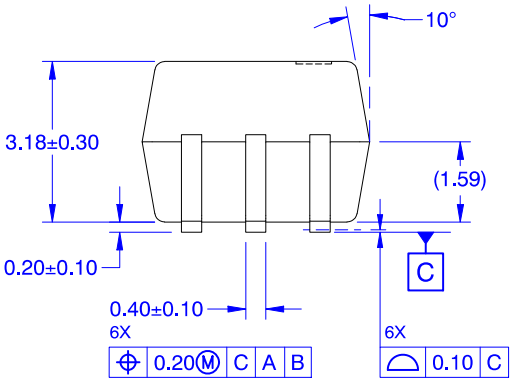
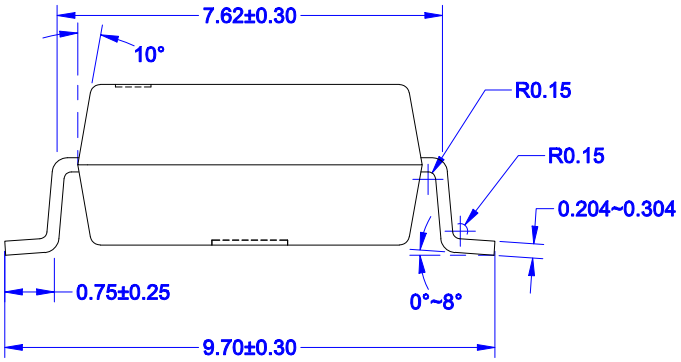



## RECOMMENDED LAND PATTERN

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C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH, AND TIE BAR EXTRUSION.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M–2009.

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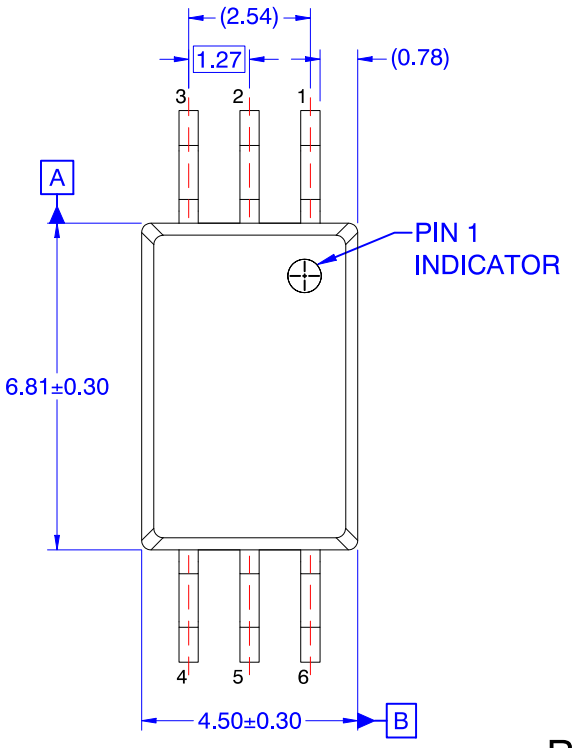


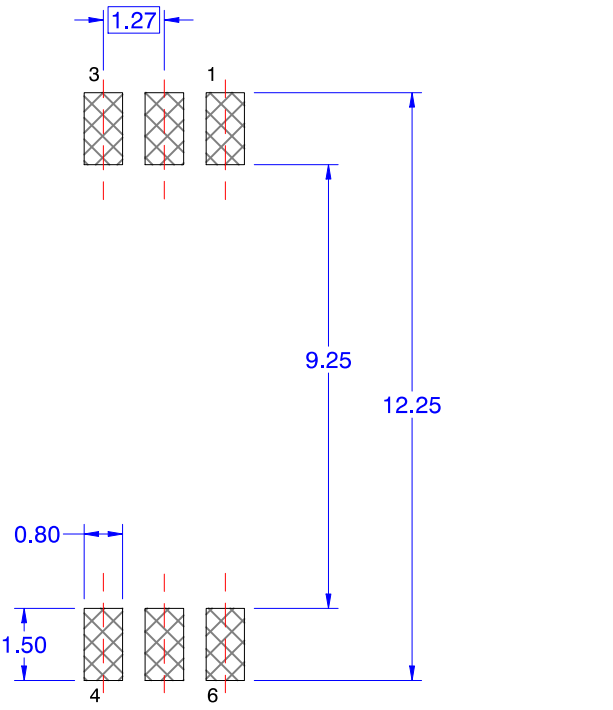


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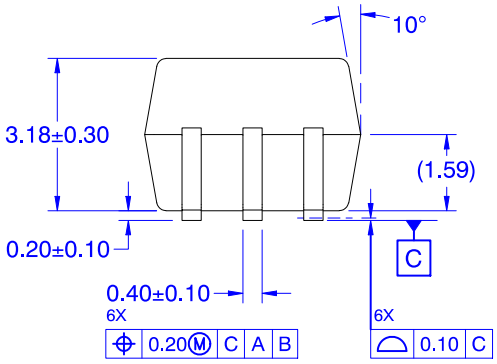


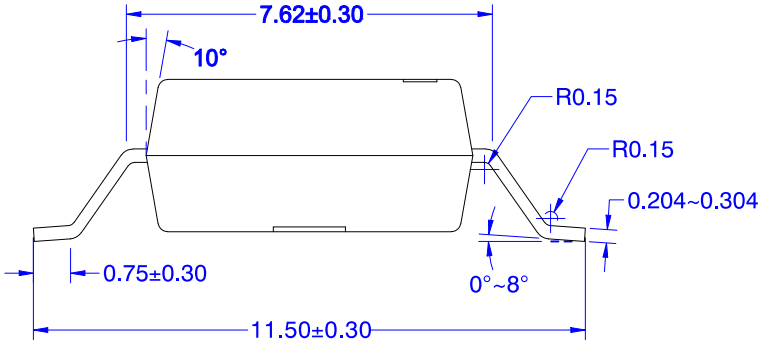


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