UM11637

FRDMGD3160DCMHB evaluation board

Rev. 2 — 3 February 2022 User guide

Document information

Information	Content
Keywords	GD3160, DCM™1000X SiC, high-voltage gate driver, SiC power module
Abstract	This document describes the operation of the FRDMGD3160DCMHB evaluation board, compatible with the DCM™1000X SiC evaluation kit.

Revision history

Rev	Date	Description
2	20220203	release version
Modifications:	• Update with latest board images	
1	20210921	initial version

1 Important notice

IMPORTANT NOTICE

For engineering development or evaluation purposes only

NXP provides the product under the following conditions:

This evaluation kit is for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed-circuit board to make it easier to access inputs, outputs and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by connecting it to the host MCU computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application heavily depends on proper printed-circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The product provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end device incorporating the product. Due to the open construction of the product, it is the responsibility of the user to take all appropriate precautions for electric discharge. In order to minimize risks associated with the customers' applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

2 FRDMGD3160DCMHB

Figure 1. FRDMGD3160DCMHB

3 Getting started

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal, and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost, and improved performance in powering state-of-the-art systems.

The tool summary page for FRDMGD3160DCMHB is at http://www.nxp.com/FRDMGD3160DCMHB. The overview tab provides an overview of the device, product features, a description of the kit contents, a list of (and links to) supported devices, a list of (and links to) any related products, and a **Get Started** section.

The **Get Started** section provides links to everything needed to start using the device and contains the most relevant, current information applicable to the FRDMGD3160DCMHB.

1. Go to http://www.nxp.com/FRDMGD3160DCMHB.
2. On the **Overview** tab, locate the **Jump To** navigation feature on the left side of the window.
3. Select the **Get Started** link, review each entry, and download an entry by clicking the title.
4. After reviewing the **Overview** tab, visit the other product-related tabs for additional information:
   - **Documentation**: download current documentation
   - **Software & Tools**: download current hardware and software tools
   - **Buy/Parametrics**: purchase the product and view the product parametrics

After downloading files, review each file, including the user guide, which includes setup instructions. If applicable, the bill of materials (BOM) and supporting schematics are also available for download in the **Get Started** section of the **Overview** tab.

3.1 Kit contents/packing list

The FRDMGD3160DCMHB kit contents include:

- Assembled and tested FRDMGD3160DCMHB board in an anti-static bag
- 3.3 V to 5.0 V translator board (KITGD316xTREVB) connected to FRDM-KL25Z
- USB cable, type A male/type mini B male, 3 ft
- Quick start guide

3.2 Required equipment

To use this kit, you need:

- 1.27 mm jumpers for configuration (included with kit)
- 30 µH to 50 µH, high current air core inductor for double pulse testing
- HV power supply with protection shield and hearing protection
- 12 V, 1.0 A DC power supply
- 500 MHz 2.5 GS/s 4-channel oscilloscope
- Rogowski coil, PEM Model CWT Mini HF60R, or CTW MiniHF30 (smaller diameter)
- Isolated high-voltage probe (CAL Test Electric CT2593-1, Tektronix THDP0200)
- Digital voltmeter

For half-bridge evaluation, you need:

- DCM™1000X SiC MOSFET module from Danfoss Silicon Power (Danfoss P/N: 135L0655; BR1056 DP660B1200T105606)
- DC link capacitor compatible with the DCM™1000X module (Danfoss P/N: 135B0234)

For three-phase evaluation, you need:

- DCM™1000X SiC evaluation kit from Danfoss Silicon Power (three power modules, DC link, cooler plate, and accessories) (Danfoss P/N: 135F9007)
- Two additional FRDMGD3160DCMHB boards (one for each power module)

3.3 System requirements

The kit requires the following to function properly with the software:

- Windows 7 or higher operating system

4 Getting to know the hardware

4.1 Overview

The FRDMGD3160DCMHB is a half-bridge evaluation kit populated with two GD3160 single channel gate drive devices. The kit includes the Freedom KL25Z microcontroller hardware for interfacing a PC installed with FlexGUI software for communication to the serial peripheral interface (SPI) registers on the GD3160 gate drive devices in either daisy chain or standalone configuration.

The KITGD316xTREVB translator board is used to translate 3.3 V signals to 5.0 V signals between the MCU and GD3160 gate drivers. The evaluation kit can be connected to a compatible SiC module for half-bridge or three-phase evaluations and applications development.

4.2 Board features

- Capability to connect to DCM™1000X module for half-bridge or three-phase evaluations
- Negative VEE gate low drive level (−3.9 V DC)
- VCCREG regulated high gate drive level (+15 V DC)
- Jumper configurable for disabling dead time fault protection when short-circuit testing
- Easy access power, ground, and signal test points, external pulse width modulation (PWM) input
- Easy to install and use FlexGUI for interfacing via SPI through PC; software includes double pulse and short-circuit testing capability
- DC link bus voltage monitor on low-side driver via AMUXIN and AOUT
- Positive temperature coefficient (PTC) connection and configurable for monitoring module temperature

4.3 Device features

Table 1. Device features

Device	Description	Features
GD3160	The GD3160 is an advanced single channel gate driver for insulated gate bipolar transistor (IGBT) and SiC.	• Compatible with current sense and temp sense IGBT/SiC modules • DESAT detection capability for detecting V_{CE} desaturation condition • Fast short-circuit protection for IGBTs with current sense feedback • Compliant with automotive safety integrity level (ASIL) C/D ISO 26262 functional safety requirements • SPI interface for safety monitoring, programmability, and flexibility • Integrated galvanic signal isolation • Integrated gate drive power stage capable of 10 A peak source and sink • Interrupt pin for fast response to faults • Compatible with negative gate supply • Compatible with 200 V to 1700 V IGBTs, power range > 125 kW

4.4 Board description

The FRDMGD3160DCMHB is a half-bridge or three-phase evaluation board populated with two GD3160 single channel IGBT or SiC gate drive devices. The board supports connection to an FRDM-KL25Z microcontroller for SPI communication configuration programming and monitoring. The board includes DESAT circuitry for short-circuit detection and implementation of GD3160 shutdown protection capabilities.

The evaluation board is designed to connect to a single DCM™1000X module (half-bridge configuration) or a full evaluation kit (three-phase configuration, with two additional FRDMGD3160DCMHB boards) for evaluation of the GD3160 performance and capabilities.

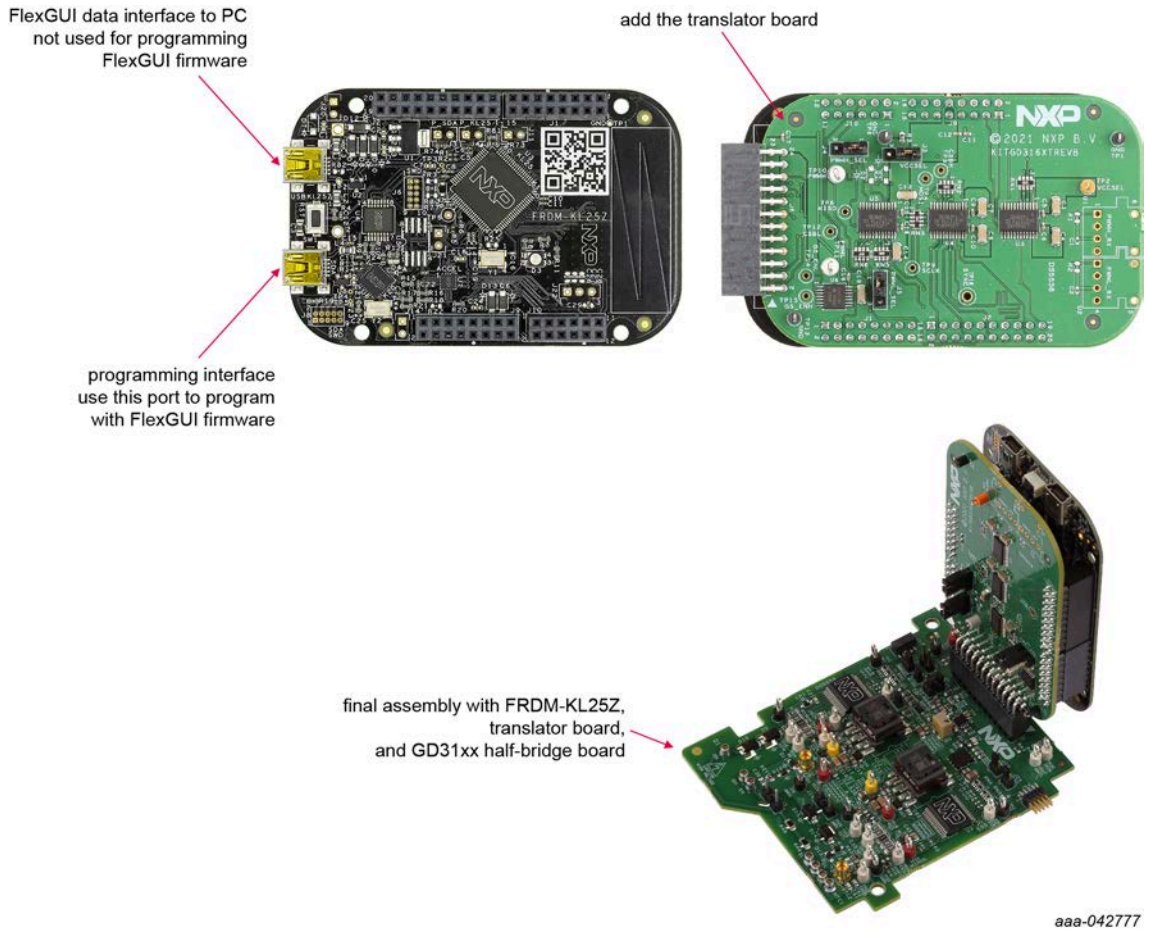

Figure 2. Connecting FRDM-KL25Z, GD31xx half-bridge EVB and translator board

4.4.1 Low-voltage logic and control connector

Low-voltage domain is 12 V VSUP domain that interfaces with the MCU and GD3160 control registers through the 24-pin connector interface.

Low-side driver and high-side driver domains are driver control interfaces to DCM™1000X module single phase connections and test points.

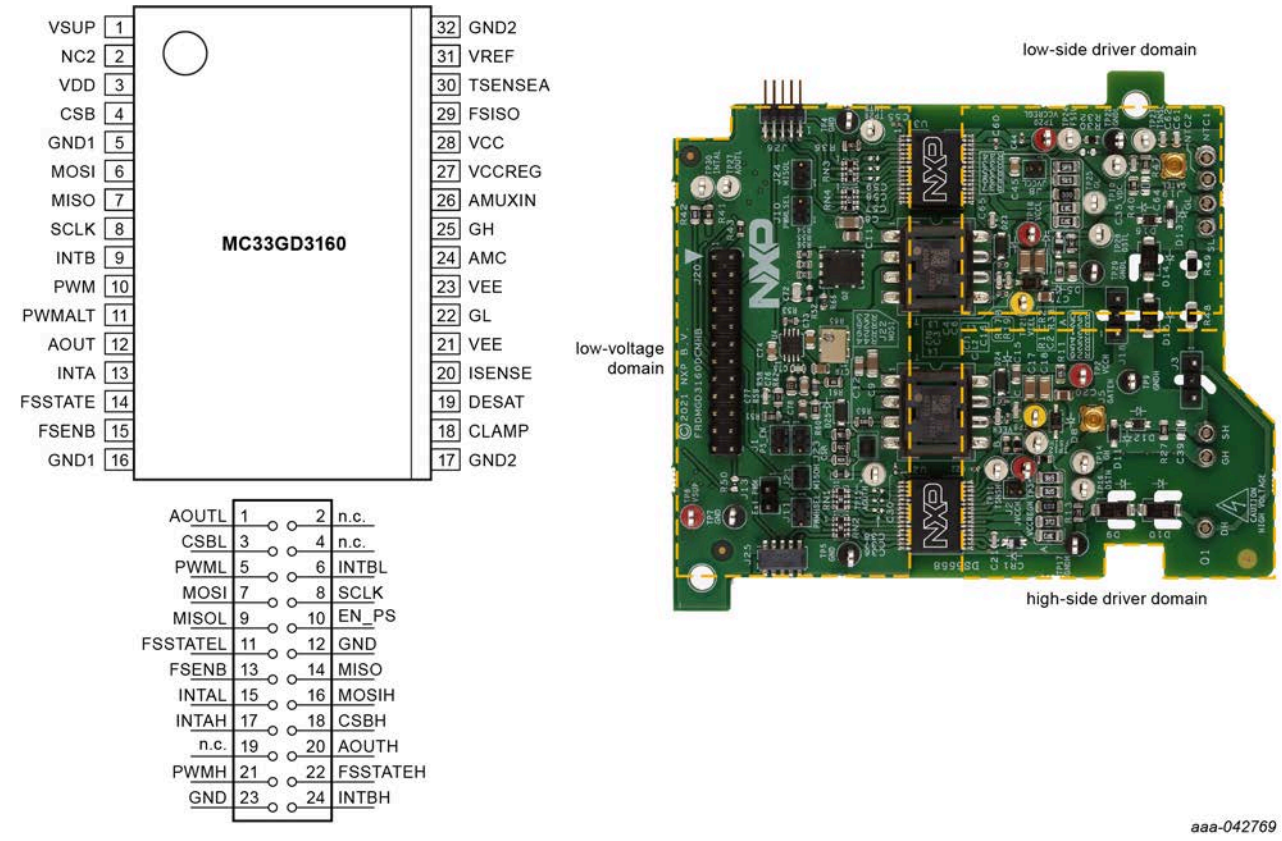

Figure 3. Evaluation board voltage and interface domains

Table 2. Low-voltage domain 24-pin connector definitions

Pin	Name	Function
1	AOUTL	analog output duty cycle encoded signal (low side) for reading temperature via TSENSEA or DC link voltage via AMUXIN
2	n.c.	not connected
3	CSBL	chip select bar (low side)
4	n.c.	not connected
5	PWML	pulse width modulation (PWM) input (low side)
6	INTBL	interrupt bar (low side)
7	MOSI	master out slave in (low side or both sides)
8	SCLK	serial clock input
9	MISOL	master in slave out (low side)
10	EN_PS	MCU control of flyback power supply
11	FSSTATEL	fail-safe state (low side)
12	GND	ground
13	FSENB	fail-safe enable (high side and low side)
14	MISO	master in slave out (high side or both sides)

Table 2. Low-voltage domain 24-pin connector definitions...*continued*

Pin	Name	Function
15	INTAL	fault reporting and real time V_{CE} and VGE monitoring (low side)
16	MOSIH	master out slave in (high side)
17	INTAH	fault reporting and real time V_{CE} and VGE monitoring (high side)
18	CSBH	chip select bar (high side)
19	n.c.	not connected
20	AOUTH	duty cycle encoded signal (high side)
21	PWMH	PWM input (high side)
22	FSSTATEH	fail-safe state (high side)
23	GND	ground
24	INTBH	interrupt bar (high side)

4.4.2 Test point definitions

All test points are clearly marked on the evaluation board. Figure 4 shows the location of various test points.

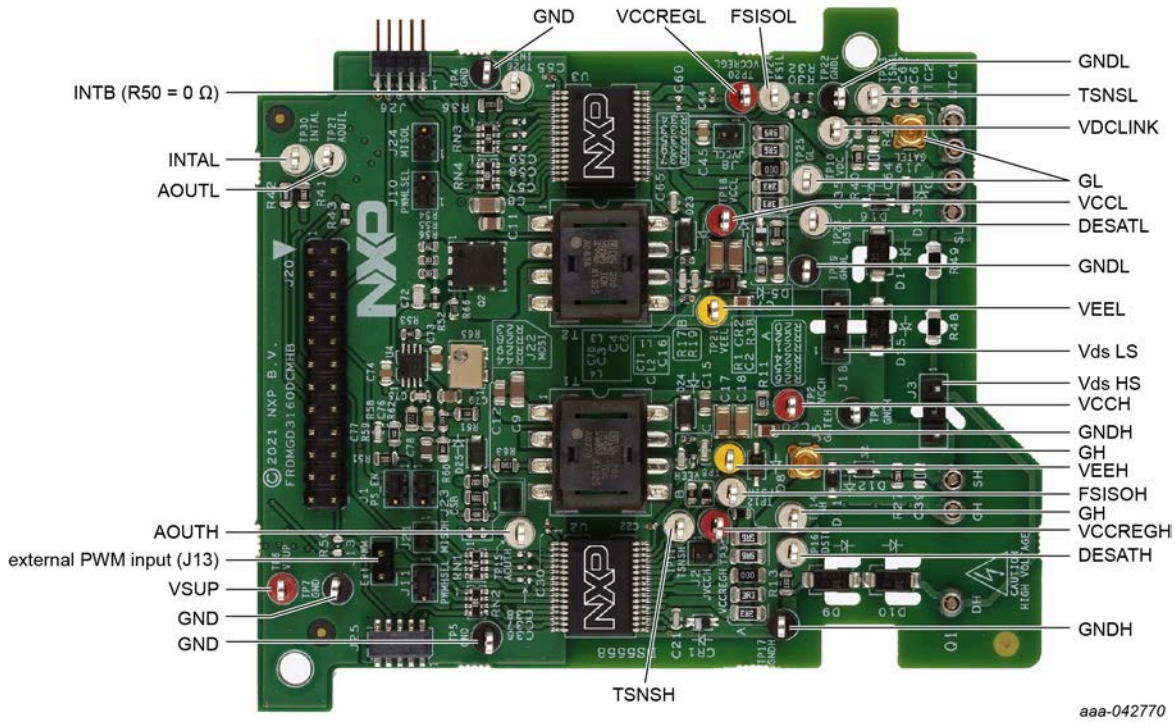

Figure 4. Key test point locations

Table 3. Test point definitions

Test point	Definition
Low-voltage domain	
VSUP	DC voltage source connection point for VSUP power input of GD3160 devices. Supply 12 V DC between this point and GND.
GND	grounding points for low-voltage domain
INTAL	fault monitor and VCE/VGE monitor low-side test point
AOUTH	duty cycle encoded output of isolated analog-to-digital converter (ADC) high-side test point
AOUTL	duty cycle encoded output of isolated ADC low-side test point
INTB	interrupt bar low-side test point if R50 is do not place (default), high-side and low-side test point if R50 is populated
Low-side driver domain	
GNDL	low-side domain ground point
VCCL	positive voltage supply test point for isolated circuitry and low-side driver domain
TSNSL	temperature sense connection low-side test point
GL	MMCX connector and test point on module gate low-side driver domain
FSISOL	high-voltage domain fail-safe low-side test point
DESATL	V_{CE} desaturation test point connected to low-side driver DESAT pin and circuitry
VCCREGL	VCC regulator low-side test point
VEEL	negative voltage supply test point for low-side driver gate
VDCLINK	DC link voltage test point at voltage divider
Vds LS	collector test point/connection terminal on low side
High-side driver domain	
VCCH	positive voltage supply test point for isolated circuitry and high-side driver domain
GNDH	high-side domain ground point
Vds HS	collector test point/connection high side
VCCREGH	VCC regulator high-side test point
FSISOH	high-voltage domain fail-safe high-side test point
GH	MMCX connector and test point on module gate high-side driver domain
DESATH	V_{CE} desaturation test point connected to high-side driver DESAT pin and circuitry
VEEH	negative voltage supply test point for high-side driver gate

4.4.3 Power supply and jumper configuration

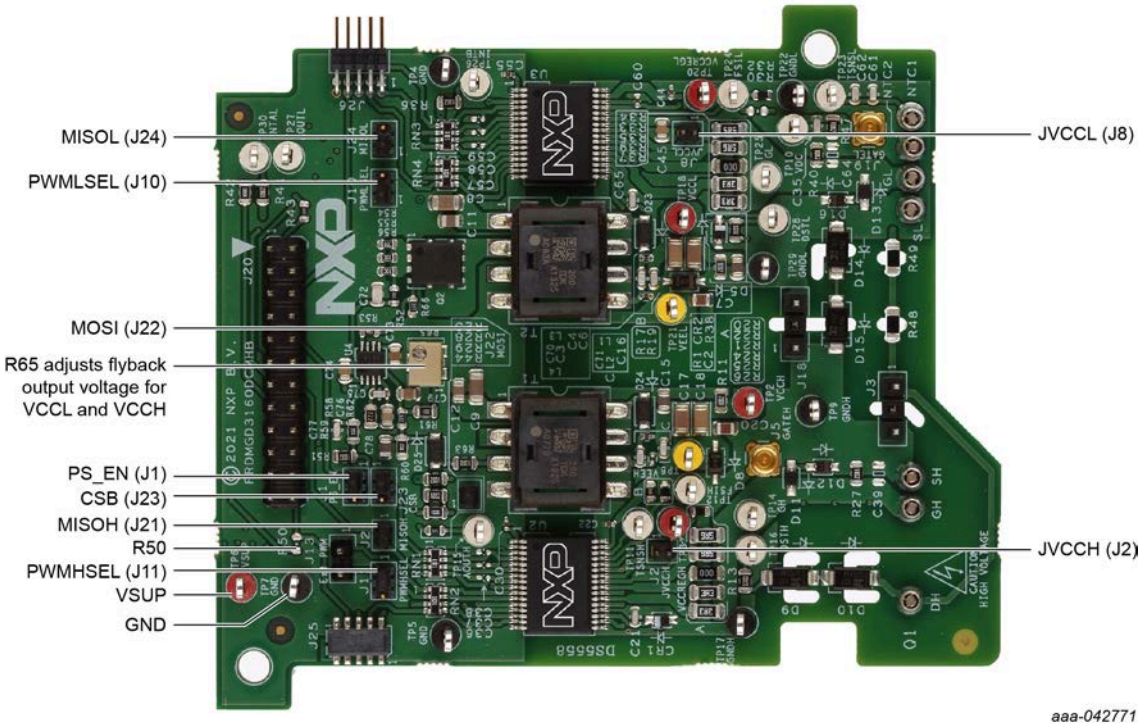

Figure 5. Power supply and jumper configuration

Table 4. Jumper definitions

Jumper	Position	Function
PWMHSEL (J11)	1-2 (default)	dead time fault protection enabled (high side)
	2-3	dead time fault protection disabled (use for short-circuit testing)
PWMLSEL (J10)	1-2 (default)	dead time fault protection enabled (low side)
	2-3	dead time fault protection disabled (use for short-circuit testing)
JVCCH (J2) and JVCCL (J8)	open (default)	VCCREG controls gate voltage
	closed	VCC and VCCREG are tied together
CSB (J23)	1-2 (default)	chip select for normal operation
	2-3	chip select for daisy chain operation
MOSI (J22)	closed (default)	normal operation
	open	daisy chain operation
MISO (J24)	1-2 (default)	normal operation
	2-3	daisy chain operation
MISO (J21)	closed (default)	normal operation
	open	daisy chain operation, except for last board in chain

Table 4. Jumper definitions*...continued*

Jumper	Position	Function
PS_EN (J1)	1-2	MCU control of flyback supply enable
	2-3 (default)	flyback supply enable tied to VSUP

4.4.4 Bottom view

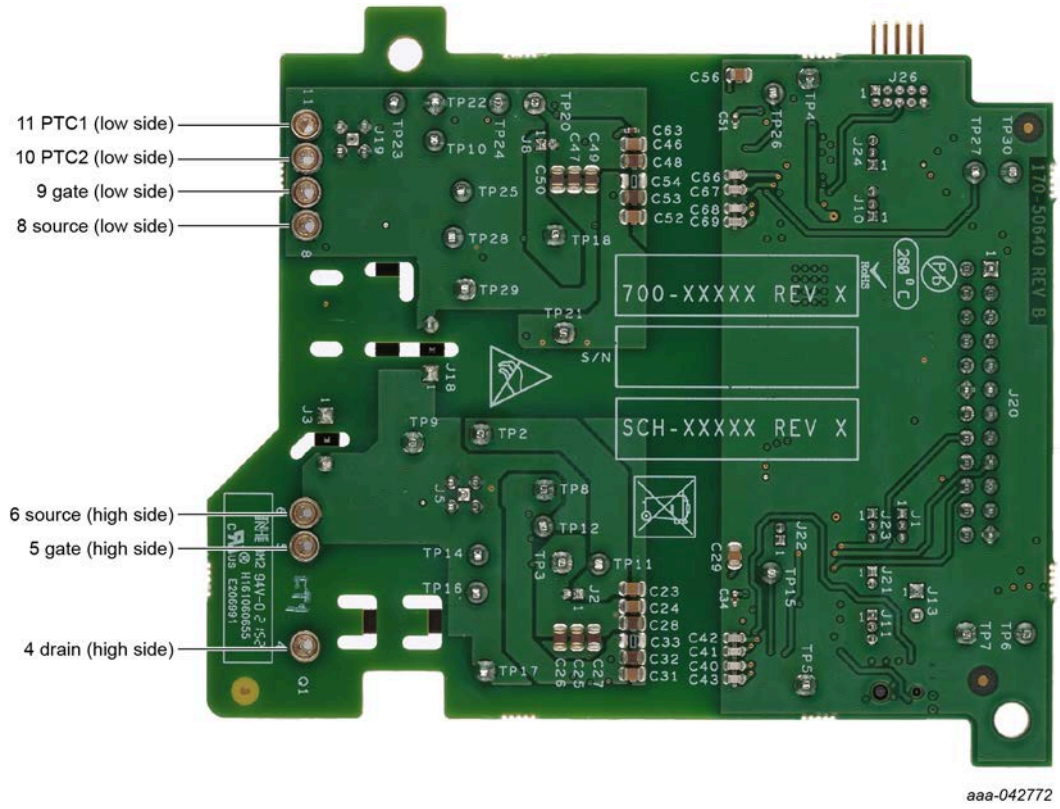

Figure 6. Evaluation board bottom view

4.4.5 Gate drive resistors

- RGH - gate high resistor in series with the GH pin at the output of the GD3160 gate high driver and DCM™1000X module gate that controls the turn-on current for SiC MOSFET gate.
- RGL - gate low resistor in series with the GL pin at the output of the GD3160 gate low driver and DCM™1000X module gate that controls the turn-off current for SiC MOSFET gate.
- RAMC - series resistor between SiC gate and AMC input pin of the GD3160 driver for gate sensing and active Miller clamping.

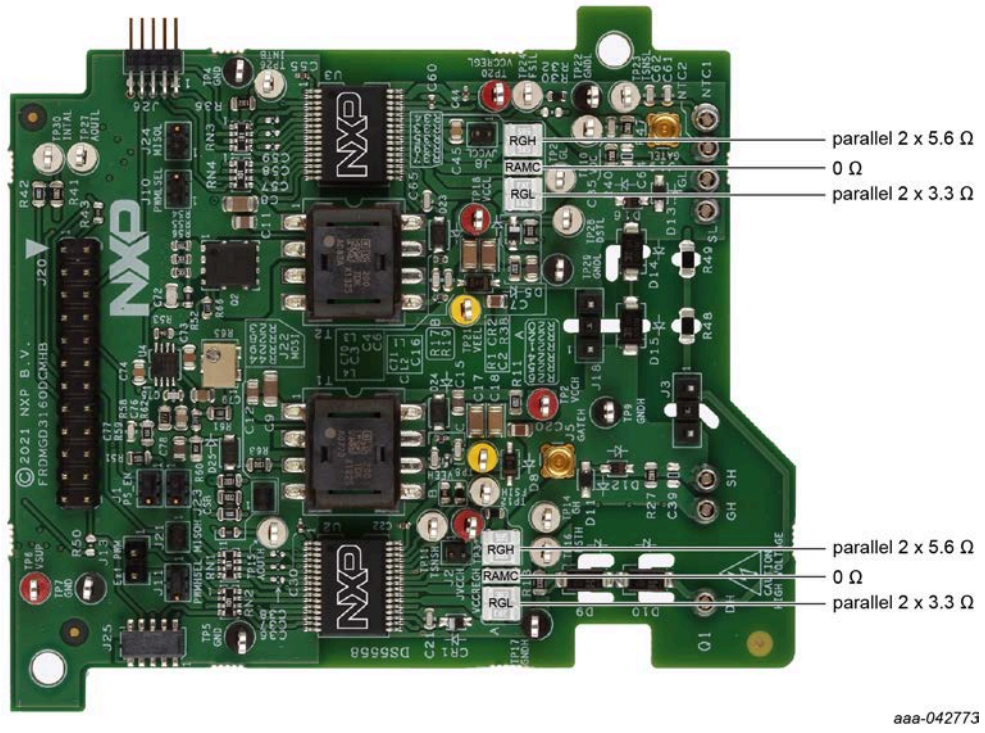

Figure 7. Gate drive resistors

The selected gate resistors are default values compatible with DCM™1000X module. It remains the responsibility of the user always to verify the operation within the safe operating area (SOA) of the power module.

4.5 Kinetis KL25Z Freedom board

The Freedom KL25Z is an ultra low-cost development platform for Kinetis L series MCU built on Arm Cortex-M0+ processor.

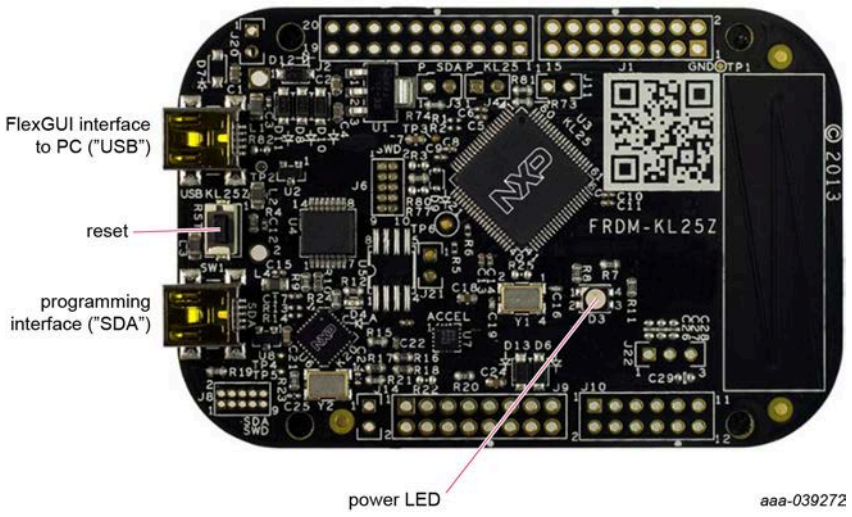

Figure 8. Freedom development platform

4.6 3.3 V to 5.0 V translator board

KITGD316xTREVB translator enables level shifting of signals from MCU 3.3 V to 5.0 V SPI communication.

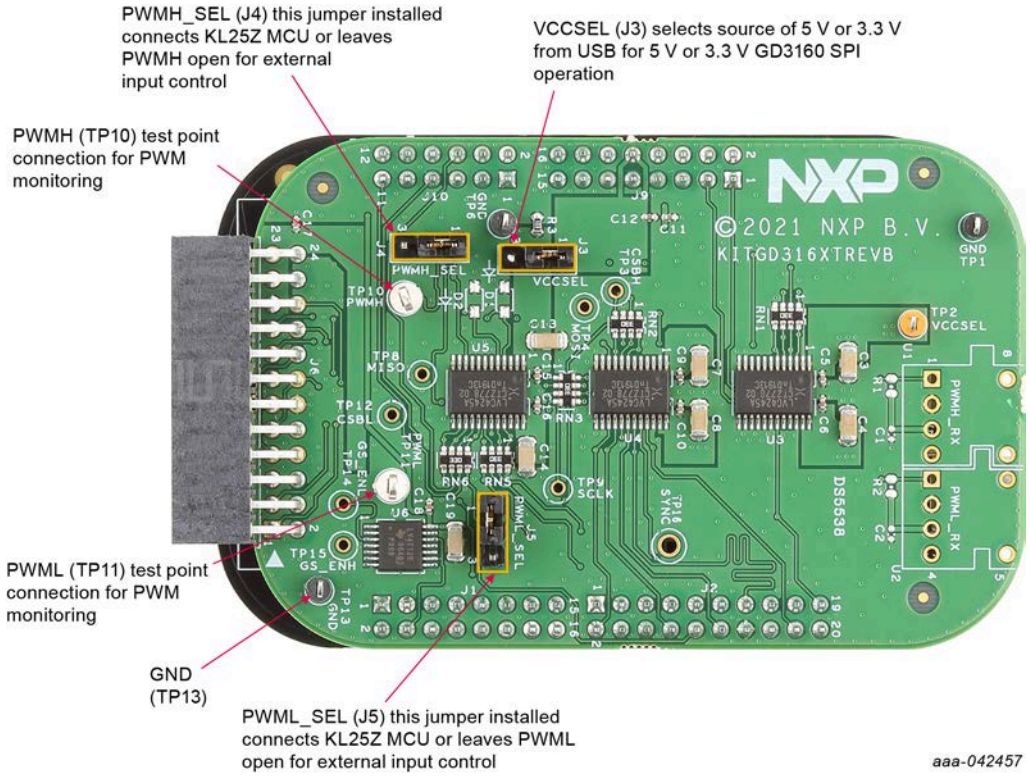

Figure 9. Translator board

Table 5. Translator board jumper definitions

Jumper	Position	Function
VCCSEL (J3)	1-2	selects 5.0 V for 5.0 V compatible gate drive
	2-3	selects 3.3 V for 3.3 V compatible gate drive
PWMH_SEL (J4)	1-2 (default)	selects PWM high-side control from KL25Z MCU
	2-3	leaves PWM high-side open for control from external input (FRDMGD3160DCMHB J13)
PWML_SEL (J5)	1-2 (default)	selects PWM low-side control from KL25Z MCU
	2-3	leaves PWM low-side open for control from external input (FRDMGD3160DCMHB J13)

5 Configuring the hardware

The FRDMGD3160DCMHB board can be used in half-bridge mode to evaluate a single power module by running double pulse and short-circuit tests.

Alternatively, three FRDMGD3160DCMHB boards can be chained together to evaluate a three-phase assembly such as provided with the DCM™1000X SiC evaluation kit. The following sections detail the required configuration for both modes of operation.

5.1 Half-bridge configuration

5.1.1 System setup

FRDMGD3160DCMHB is connected to a compatible DCM™1000X module with a suitable DC link capacitor as shown in Figure 10. Double pulse and short-circuit testing can be conducted utilizing Windows-based PC with FlexGUI software.

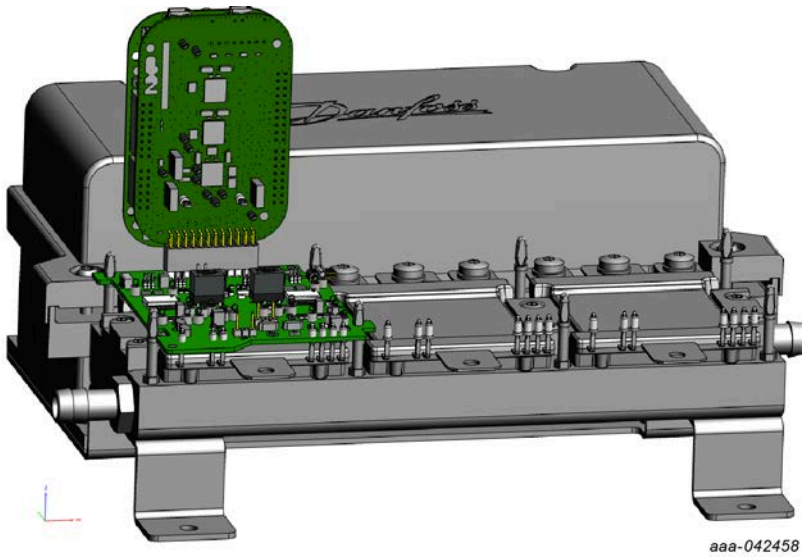

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Figure 10. Half-bridge setup

Suggested equipment needed for test:

- DCM™1000X module and compatible DC link capacitor from Danfoss Silicon Power
- 1 × FRDMGD3160DCMHB, 1 × KITGD316xTREVB and 1 × FRDM-KL25Z
- Rogowski coil high-current probe
- High-voltage differential voltage probe
- High sample rate digital oscilloscope with probes
- Windows-based PC
- High-voltage DC power supply for DC link voltage
- Low-voltage DC power supply for VSUP (12 V)
- Load coil for double pulse and short-circuit testing

5.1.2 Quick start

1. Download and install the latest FlexGUI software (see Installing FlexGUI on your computer)
2. Assemble the FRDMGD3160DCMHB with the translator board and KL25Z on the power module as shown in Figure 10
3. Check jumper configuration on the evaluation board before powering up, and ensure that the configuration meets desired use case. See Section 5.1.3 and Section 5.1.4 for alternate SPI configurations. If R50 is closed, FlexGUI displays the same information for INTBL and INTBH.
4. KL25Z generates the PWM signals for short circuit or double pulse testing. No external input on J13 (Ext PWM) is required. Check that J4 and J5 use PWM from MCU (1-2) on translator board.
5. Launch FlexGUI application software on PC, and select the configuration matching the chosen SPI mode. Connect USB cable from PC to USB KL25Z port on KL25Z microcontroller board. KL25Z microcontroller is shipped with proper firmware already flashed. See Section 6 for additional details.
6. Supply 12 V DC power to the low-voltage domain of the evaluation board by using VSUP TP6 and GND TP7.
7. Start FlexGUI communications and check VCCL, VCCH, VEEL, VEEH voltage levels regarding GNDH and GNDL test points. If VCC voltages are low, adjust R65 potentiometer.
8. PWM, double pulse, and short circuit tests can be generated from the Pulse tab. For short-circuit testing, PWMHSEL (J11) and PWMLSEL (J10) must be configured to bypass dead time control (see Table 4).

5.1.3 Normal mode SPI configuration

To access each GD3160 separately (default configuration), check the position of the following jumpers:

Table 6. Normal mode SPI jumpers configuration

Designator	Signal	Position
J21	MISO	closed
J22	MOSI	closed
J23	CSB	1-2
J24	MISO	1-2

Select the appropriate FlexGUI kit: GD3160 Half Bridge EVBs, and check that the Feature Set under Advanced Settings is set to standard.

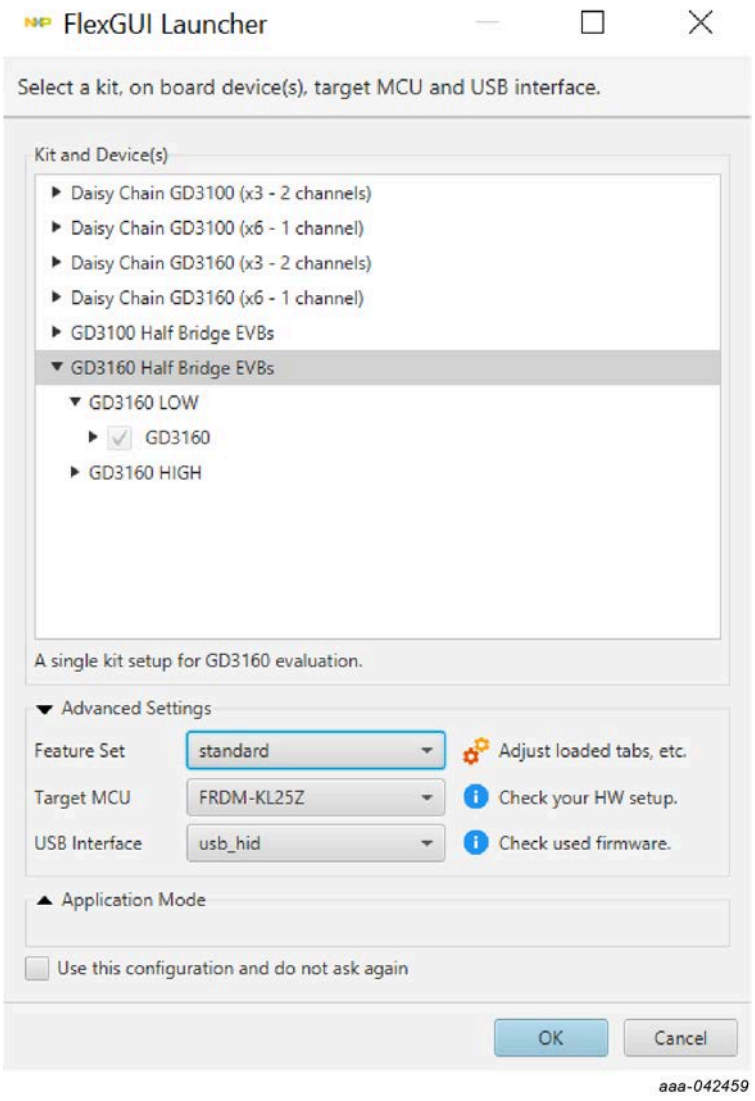

Figure 11. Normal mode SPI for half-bridge configuration

5.1.4 Daisy chain SPI configuration

To access the GD3160 in daisy chain mode, check the position of the following jumpers:

Table 7. Daisy chain SPI jumpers configuration

Designator	Signal	Position
J21	MISO	closed
J22	MOSI	open
J23	CSB	2-3
J24	MISO	2-3

Select the appropriate FlexGUI kit: GD3160 Half Bridge EVBs, and check that the Feature Set under Advanced Settings is set to daisy-chain.

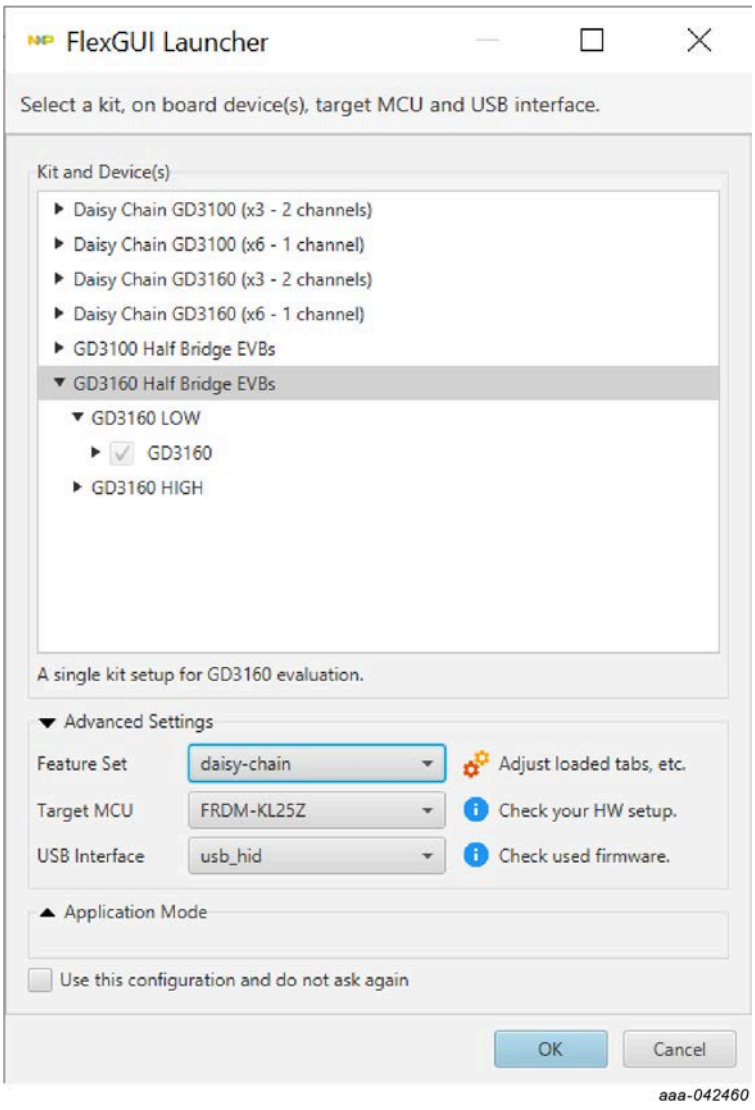

Figure 12. Daisy chain 1 × 2 for half-bridge configuration

5.2 Three-phase configuration

5.2.1 System setup

FRDMGD3160DCMHB is connected to a compatible DCM™1000X SiC three-phase evaluation kit as shown in Figure 13. The full three phases can be run simultaneously via externally provided PWM. A single KL25Z + translator board assembly can configure all six gate drivers and collect faults.

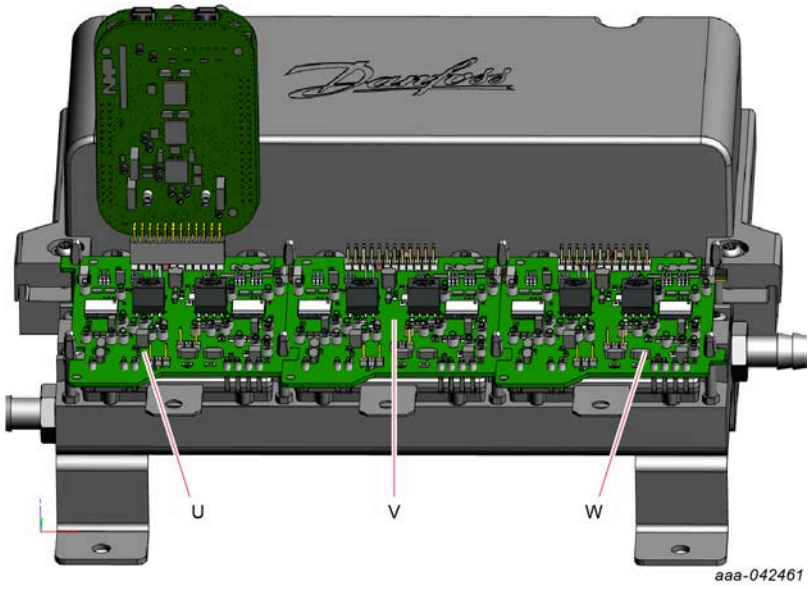

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Figure 13. Three-phase setup

Suggested equipment needed for test:

- DCM™1000X SiC evaluation kit (Danfoss P/N: 135F9007) from Danfoss Silicon Power containing 3 × DCM™1000X SiC power modules, DC link capacitor, cooler plate, and mounting hardware
- 3 × FRDMGD3160DCMHB, 1 × KITGD316xTREVB and 1 × FRDM-KL25Z
- Rogowski coil high-current probe
- High-voltage differential voltage probe
- High sample rate digital oscilloscope with probes
- Windows-based PC
- High-voltage high current DC power supply for DC link voltage
- Low-voltage DC power supply for VSUP (12 V)
- Signal generator to provide three-phase PWM (high side and low side)
- Three-phase load

5.2.2 Quick start

1. Download and install the latest FlexGUI software (see Installing FlexGUI on your computer)
2. Assemble the DCM™1000X SiC kit:
   a. Assemble the three FRDMGD3160DCMHB boards together making sure that the board edge connectors J25 and J26 are correctly plugged into each other. The letters U, V, and W identify the boards according to Figure 13.
   b. Plug the translator board and KL25Z assembly on board U.
   c. Place the assembly on the evaluation kit, taking care to align the pins of the power module to the corresponding sockets. The boards should click the plastic standoffs once fully seated.
3. Check jumper configuration on the evaluation boards before powering up, and ensure that the configuration meets desired use case; see Table 8.
4. PWM signals must be provided on the three J13 (Ext PWM) connectors, referenced to GND. Check the translator board J4 and J5 connectors to ensure that external PWM control is used. PWMHSEL (J11) and PWMLSEL (J10) jumpers can be used on each board to enforce or bypass deadtime control (see Table 4).
5. Launch FlexGUI application software on PC, and select the Daisy chain GD3160 (x6 – 1 channel) kit mode (see Figure 14). Connect USB cable from PC to USB KL25Z port on KL25Z microcontroller board. KL25Z microcontroller is shipped with proper firmware already flashed. See Section 6 for additional details.
6. Supply 12 V DC power (1 A current capability minimum) to the low-voltage domain of FRDMGD3160DCMHB boards. Power one board through VSUP TP6 and GND TP7, the other two boards are supplied by the first one. Check VCCL, VCCH, VEEL, VEEH voltage levels regarding GNDH and GNDL test points on all three boards. If VCC voltages are low, adjust their respective R65 potentiometer.
7. Start FlexGUI communications. All six GD3160 can now be configured, faults, and ADC measurements collected.

Table 8. Mandatory jumper positions for three-phase configuration

Designator	Signal	Position	Definition
Translator board			
J4 J5	PWMH_SEL PWML_SEL	2-3	PWM control from MCU disabled, input from J13 (Ext PWM) on each FRDMGD3160 board
FRDMGD3160DCMHB boards			
J13	Ext PWM	-	input external PWM for each phase on this connector
J1	PS_EN	2-3	flyback power supplies always enabled (9.3 V UVLO)
R50	INTBL INTBH	closed	FlexGUI displays the same information on INTBL and INTBH: LOW if any of the six devices reports a fault
J21	MISO		open for boards U and V, closed for board W
J22	MOSI	open	for all boards
J23	CSB	2-3	for all boards
J24	MISO	2-3	for all boards

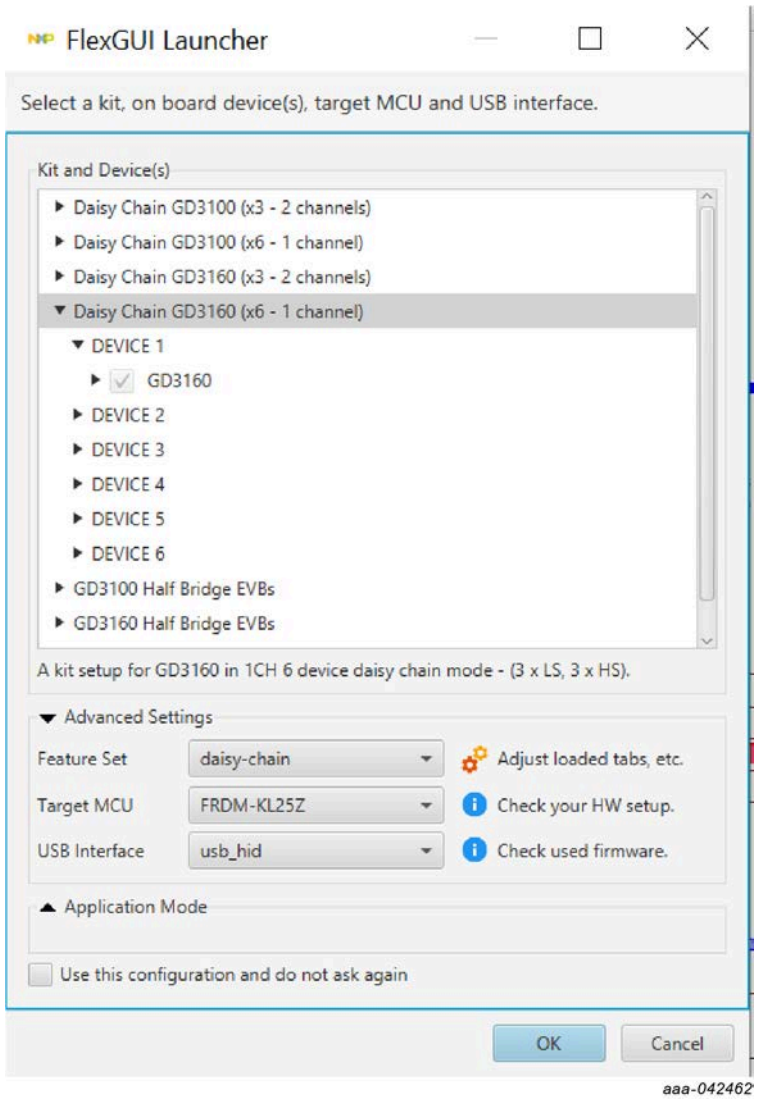

Figure 14. Daisy chain 1 × 6 for three-phase board configuration

6 Installation and use of software tools

Software for FRDMGD3160DCMHB is distributed with the FlexGUI tool (available on NXP.com). Necessary firmware comes pre-installed on the FRDM-KL25Z with the kit.

Even if the user intends to test with other software or PWM, it is recommended to install this software as a backup or to help debugging.

6.1 Installing FlexGUI on your computer

The latest version of FlexGUI supports the GD3100 and GD3160. It is designed to run on any Windows 10 or Windows 8 based operating system. To install the software, do the following:

1. Go to www.nxp.com/FlexGUI and click **Download**.
2. When the FlexGUI software page appears, click **Download** and select the version associated with your PC operating system.
3. FlexGUI wizard creates a shortcut, an NXP FlexGUI icon appears on the desktop. By default, the FlexGUI executable file is installed at **C:\flexgui-app-des-gd31xx.exe**. Installing the device drivers overwrites any previous FlexGUI installation and replaces it with a current version containing the GD31xx drivers. However, configuration files (.spi) from the previous version remain intact.

6.2 Configuring the FRDM-KL25Z microcode

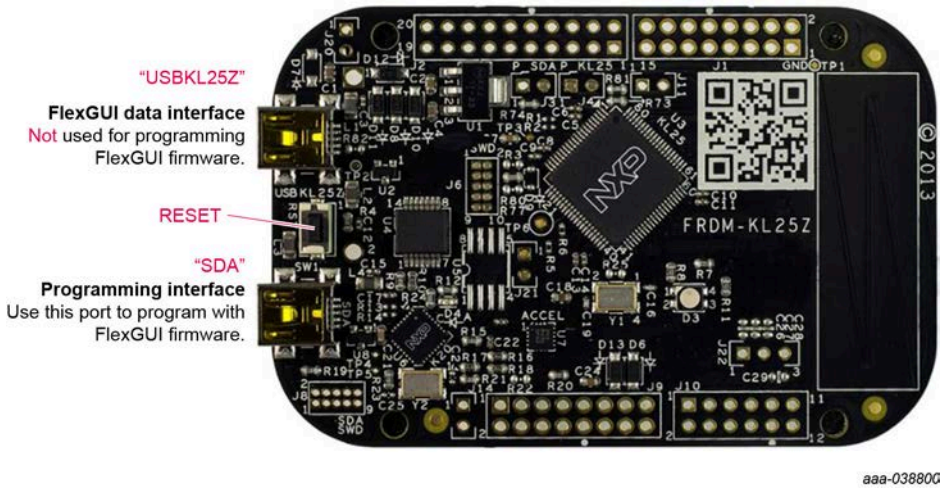

Figure 15. FRDM-KL25Z setup and interface

By default, the FRDM-KL25Z delivered with this kit is preprogrammed with the current and most up-to-date firmware available for the kit.

A way to check quickly that the microcode is programmed and the board is functioning properly, is to plug the KL25Z into the computer, open FlexGUI, and verify that the software version at the bottom is 6.4 or later.

If a loss of functionality following a board reset, reprogramming, or a corrupted data issue, the microcode may be rewritten per the following steps:

1. To clear the memory and place the board in boot loader mode, hold down the reset button while plugging a USB cable into the **OpenSDA** USB port.
2. Verify that the board appears as a BOOTLOADER device and continue with step 3. If the board appears as KL25Z, you may go to step 6.
3. Download the **Firmware Apps** .zip archive from the PEmicro OpenSDA webpage (http://www.pemicro.com/opensda/). Validate your email address to access the files.
4. Find the most recent MDS-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA and copy/drag-and-drop into the **BOOTLOADER** device.
5. Reboot the board by unplugging and replugging the connection to the **OpenSDA** port. Verify now that the device appears as a KL25Z device to continue.
6. Locate the most recent KL25Z firmware; which is distributed as part of the FlexGUI package.
   a. From the FlexGUI install directory, which is located in the **flexgui-app-des-gd31xx\bin** folder and is named in the form “flexgui-fw-KL25Z_usb_hid_gd31xxC_vx.x.x.bin”.
   b. This .bin file is a product/family-specific configuration file for FRDM-KL25Z containing the pin definitions, SPI/PWM generation code, and pin mapping assignments necessary to interface with the translator board as part of FRDMGD3160DCMHB.
7. With the KL25Z still plugged through the **OpenSDA** port, copy/drag-and-drop the .bin file into the KL25Z device memory. Once done, disconnect the USB and plug into the other USB port, labeled **KL25Z**.
   a. The device may not appear as a distinct device to the computer while connected through the KL25Z USB port, this is normal.
8. The FRDM-KL25Z board is now fully set up to work with FRDMGD3160DCMHB and the FlexGUI.
   a. There is no software stored or present on either the driver or translator boards, only on the FRDM-KL25Z MCU board.

All uploaded firmware is stored in non-volatile memory until the reset button is hit on the FRDM-KL25Z. There is no need to repeat this process upon every power up, and there is no loss of data associated with a single unplug event.

6.3 Using the FlexGUI

The FlexGUI is available from http://www.nxp.com/FlexGUI as an evaluation tool demonstrating GD31xx-specific functionality, configuration, and fault reporting. FlexGUI also includes basic capacity for the FRDMGD3160DCMHB to control an IGBT or SiC module, enabling double pulse or short-circuit testing.

SPI messages can be realized graphically or in hexadecimal format. CSB is selectable to address one or both GD31xx on the board via daisy chain. See Figure 26 to Figure 34 for FlexGUI for GD31xx internal register read and write access.

Starting FlexGUI for GD31xx

- FlexGUI install program (flexgui-app-des-gd31xx-0.x.x.exe)
- Download FlexGUI and run the install program on your PC.
- When you start the application, you can select the target application board, feature set (standard or daisy chain), target MCU, and USB interface. Refer to Section 5.1 and Section 5.2 for kit selection.

FlexGUI settings

- Access settings by selecting Settings from the File menu

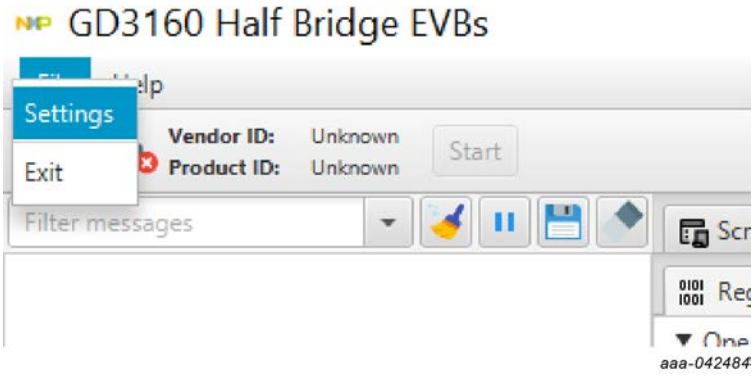

Figure 16. GUI settings menu

- The Loader and Logs settings are shown below:

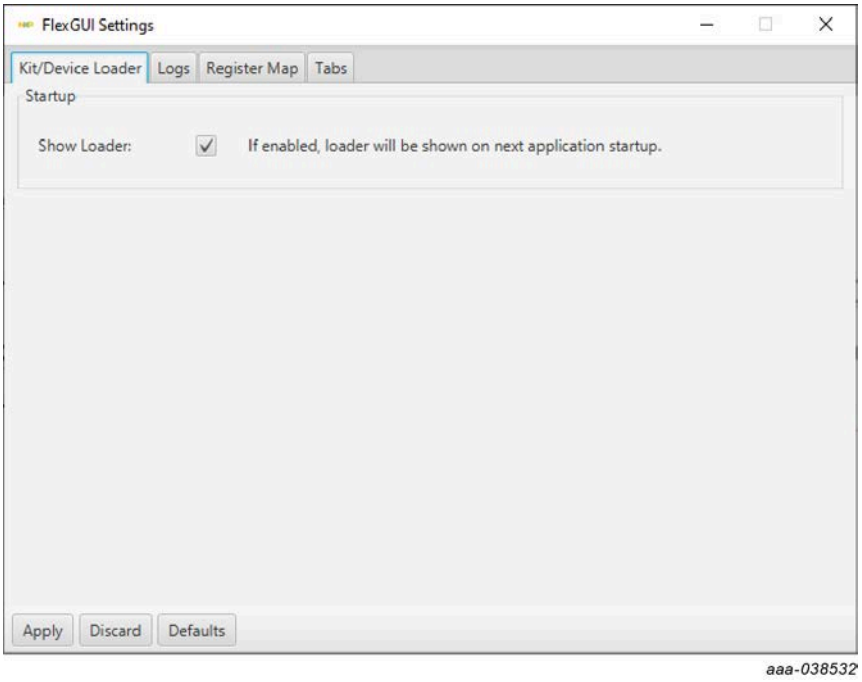

Figure 17. Loader settings

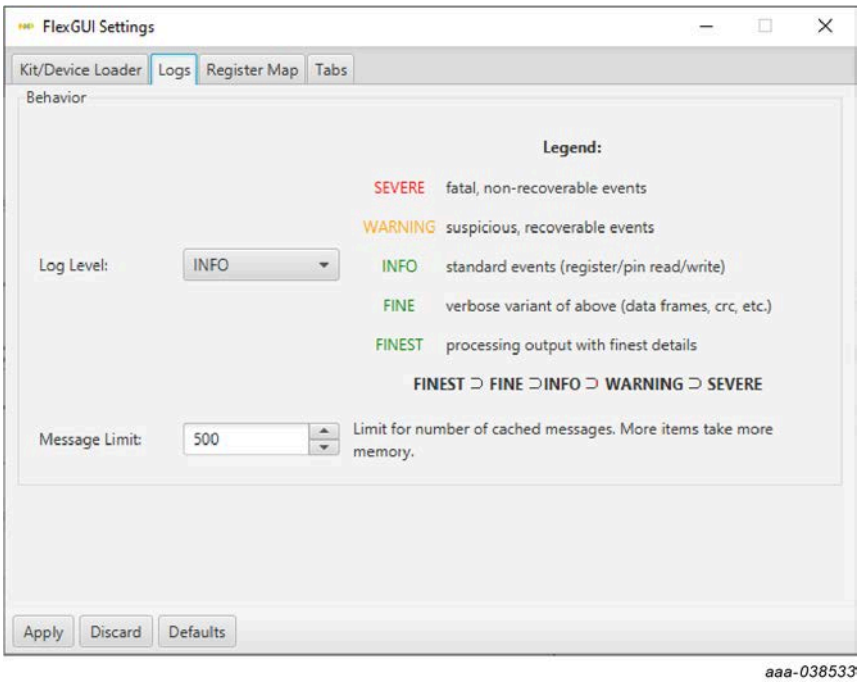

Figure 18. Logs settings

- Access settings by selecting Settings from the File menu.
- The Register Map and Tabs settings are shown below:

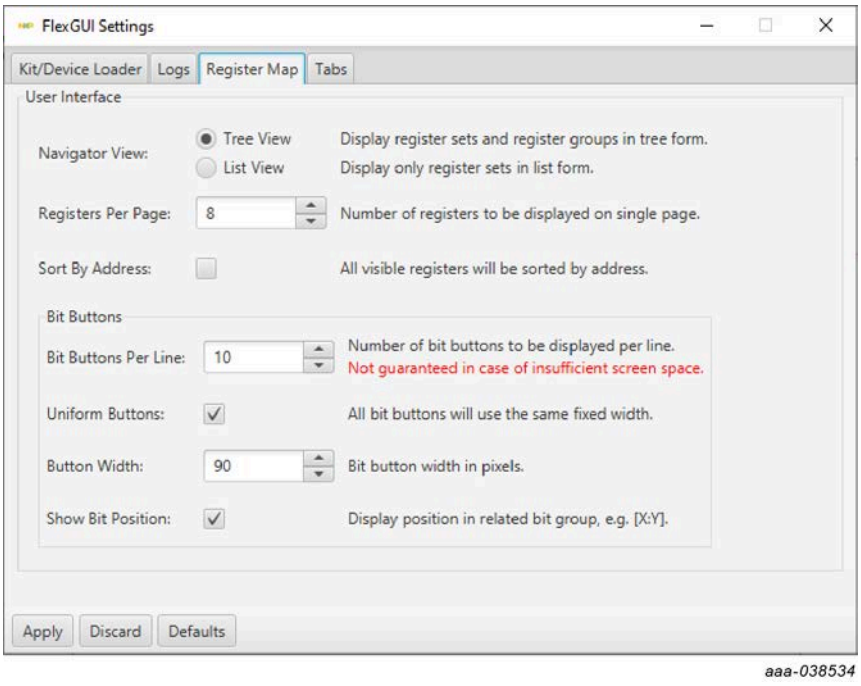

Figure 19. Register map settings

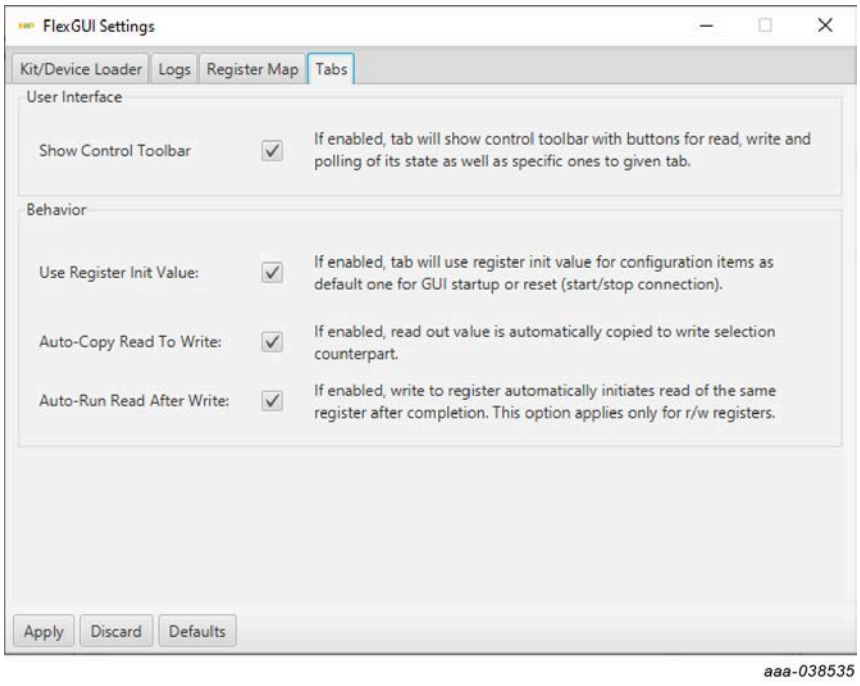

Figure 20. Tabs settings

Command Log window

- The Command Log area informs the user about application events.

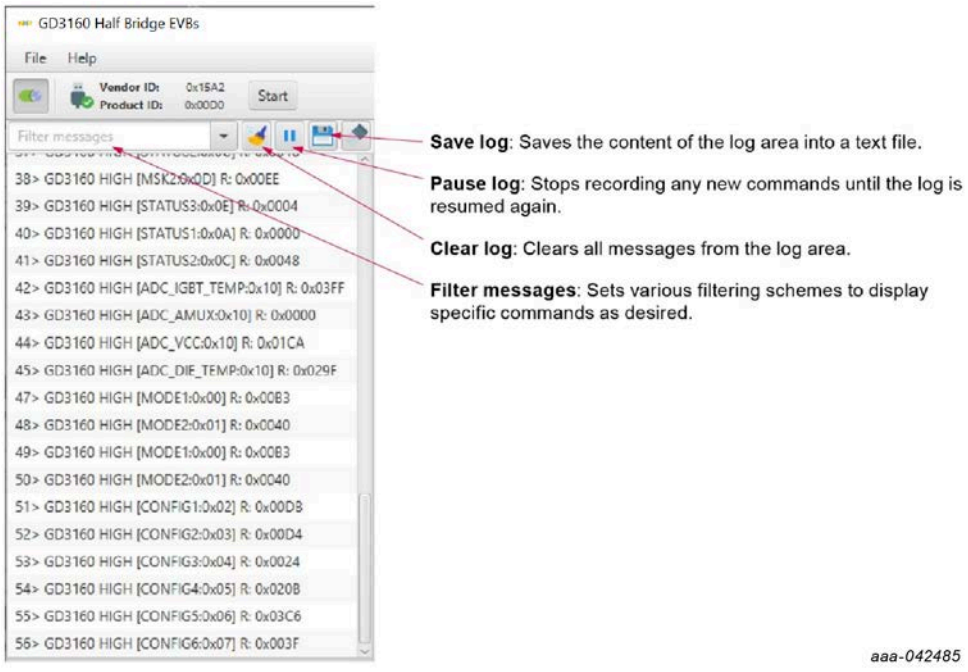

Figure 21. Command Log area

Global workspace controls

- Always visible in the lower left corner of the main application window.
  - GD3160 tab functionality
    - Switch modes between run and configuration mode
    - Set SPI frequency

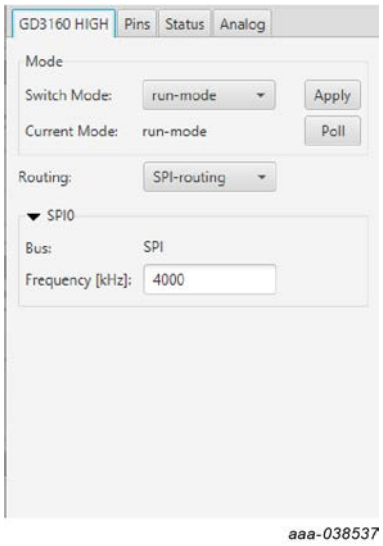

Figure 22. Device pins settings and status menus

- Pins tab functionality
  - Set control levels. Default values are shown.
  - Read and automatically poll INTB pins (INTA pins are added for GD3160).
  - Control pins set values to a default to a functional state.
    - FSENB - enable/disable fail-safe enable
    - EN_PS - enables flyback supply on EVB at 17 V V_{CC} on high side and low side
    - FSSTATEL and FSSTATEH set the fail-safe state when FSENB is enabled
    - PWML and PWMH set the default state PWM inputs for high side and low side

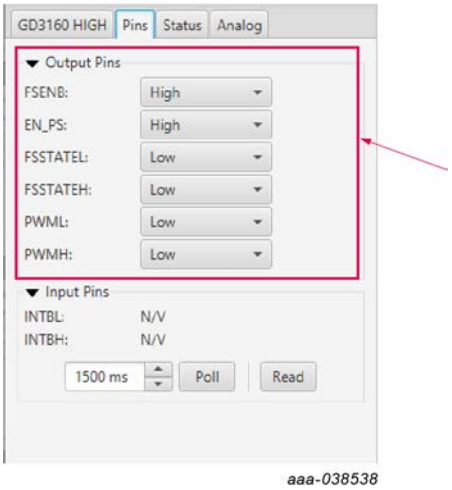

Figure 23. Pins tab functionality

- Status tab functionality
  - Monitors Status 1 and Status 2 fault bits. Bits that are set are shown in red.
  - Ability to clear all faults and automatically poll status registers.

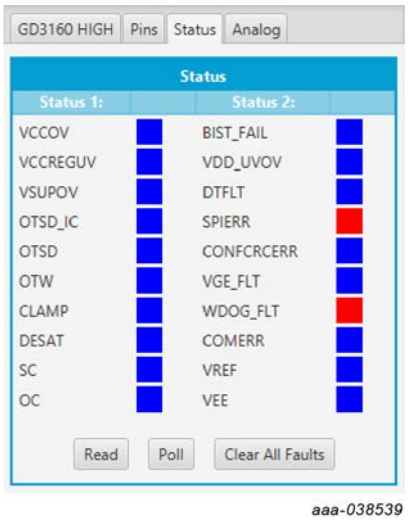

Figure 24. Status tab functionality

- Analog tab functionality
  - Read and poll ADC values from the high-voltage domain
  - Displays raw ADC and converted values

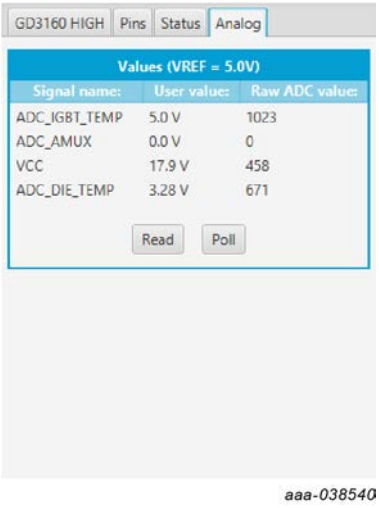

Figure 25. Analog tab functionality

Register map

- Registers are grouped according to function; independent lines to read and write the registers
- Individual registers can be read by clicking the R button and can be written by using the W button.
- Copy button to copy the read values to the write line; can be set to copy automatically
- Reset button to undo the changes on the write line and reset to the previous value
- Global register controls perform the selected command on all registers with the checkbox selected.

Figure 26. Register map

Gate Drive tab

- Allows setting of parameters related to the gate drive; controls are disabled when not in config mode
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

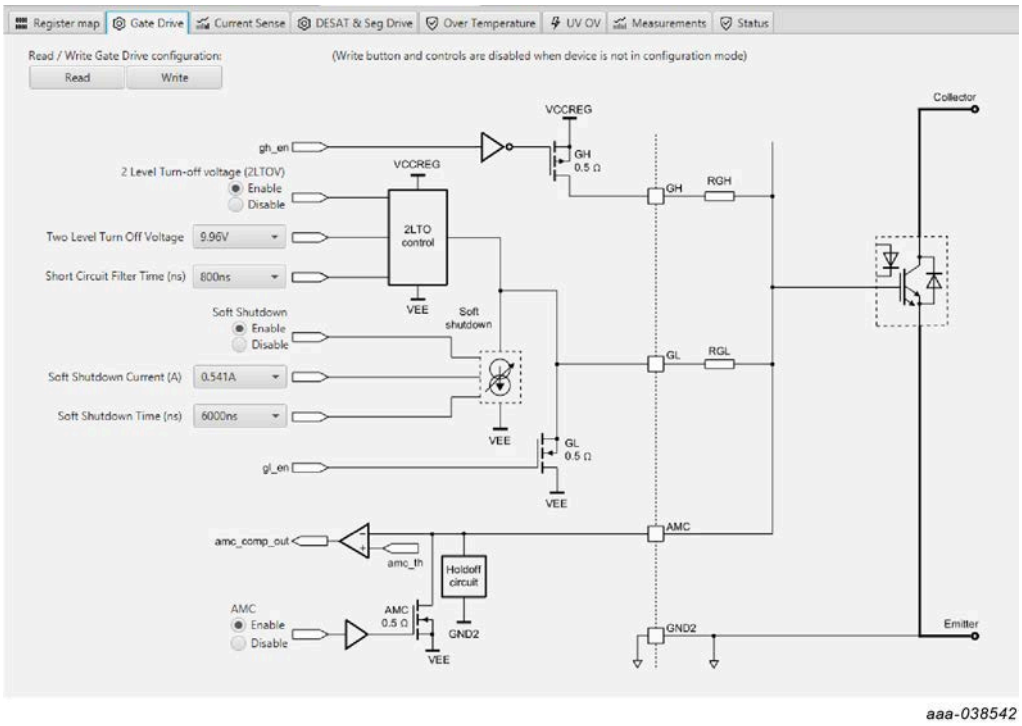

Figure 27. Gate drive tab

Current Sense tab

- Allows setting of parameters related to current sense
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

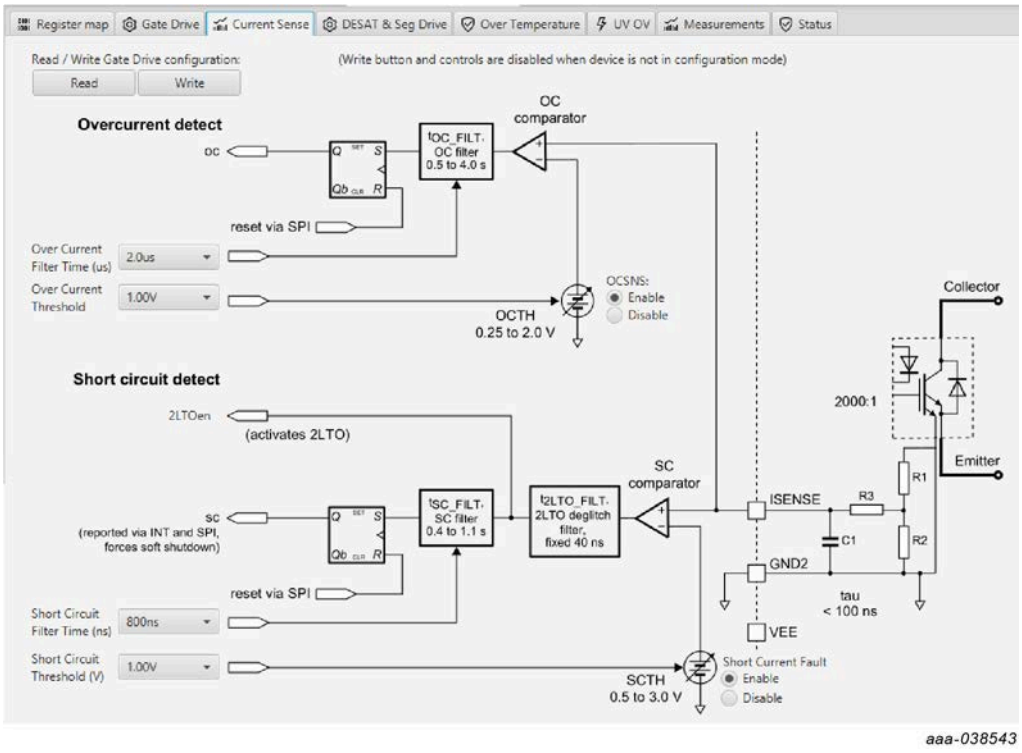

Figure 28. Current sense tab

DESAT & Seg Drive tab

- Allows setting of parameters related to desat and segmented drive
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

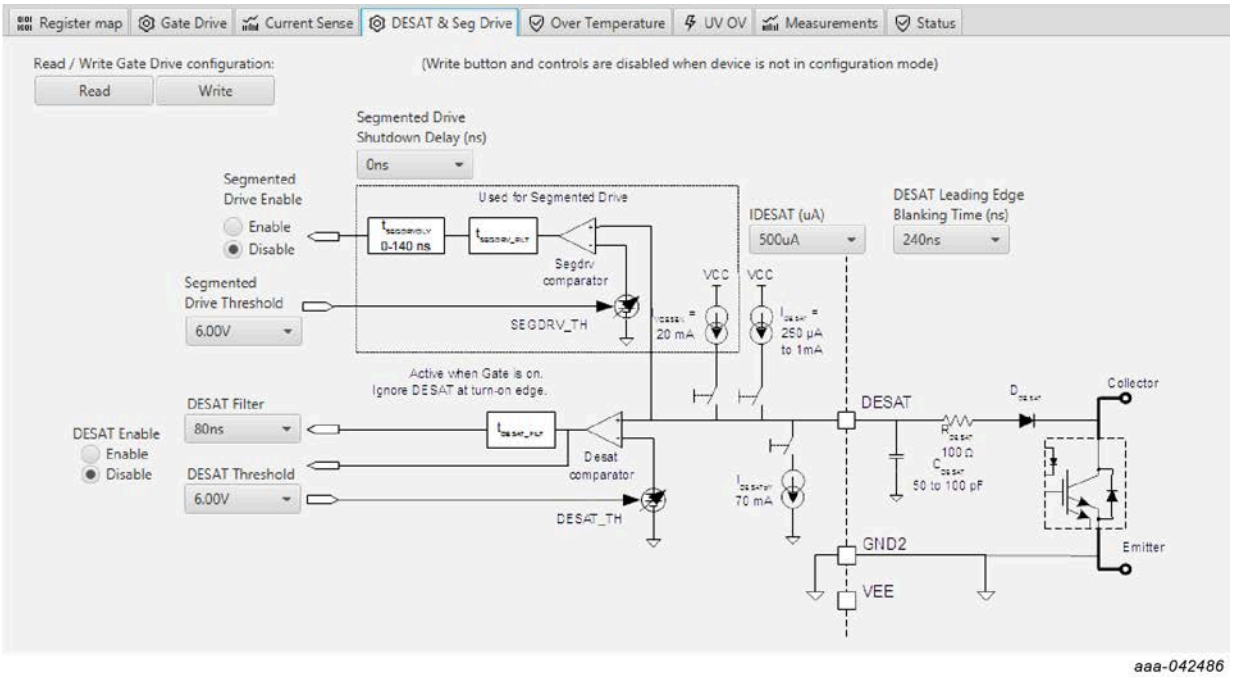

Figure 29. Desat and segmented drive tab

Overtemperature tab

- Allows setting of parameters related to overtemperature and overtemperature warning thresholds
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

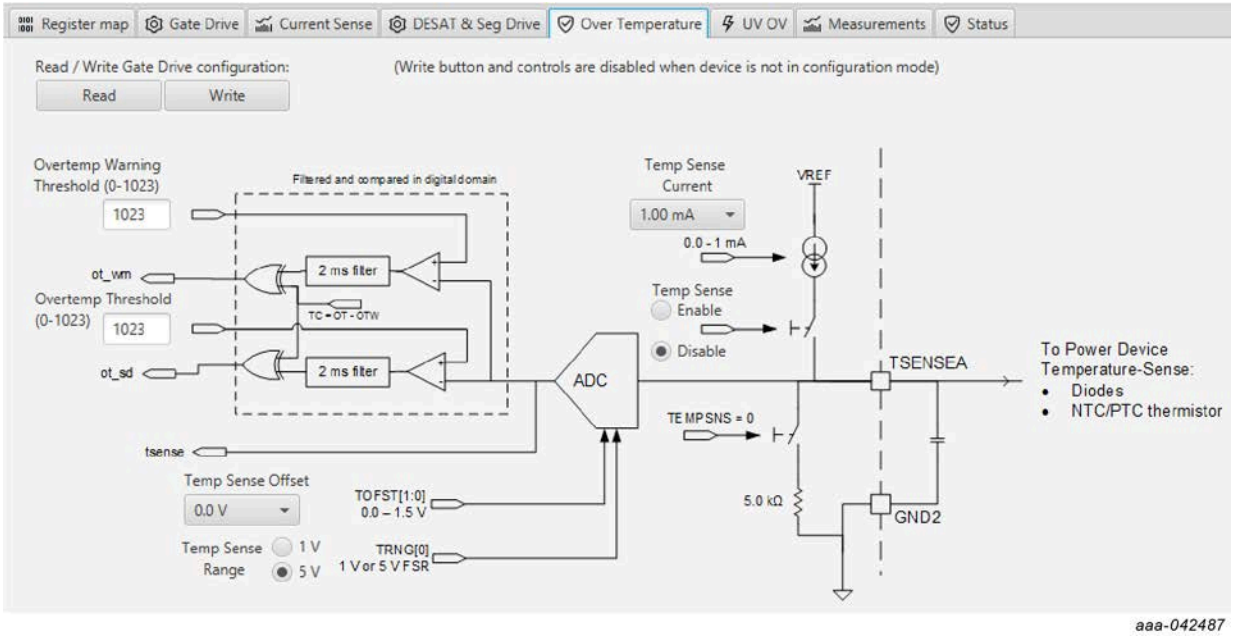

Figure 30. Overtemperature tab

Undervoltage and overvoltage threshold tab

- Allows setting of parameters related to undervoltage and overvoltage threshold
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

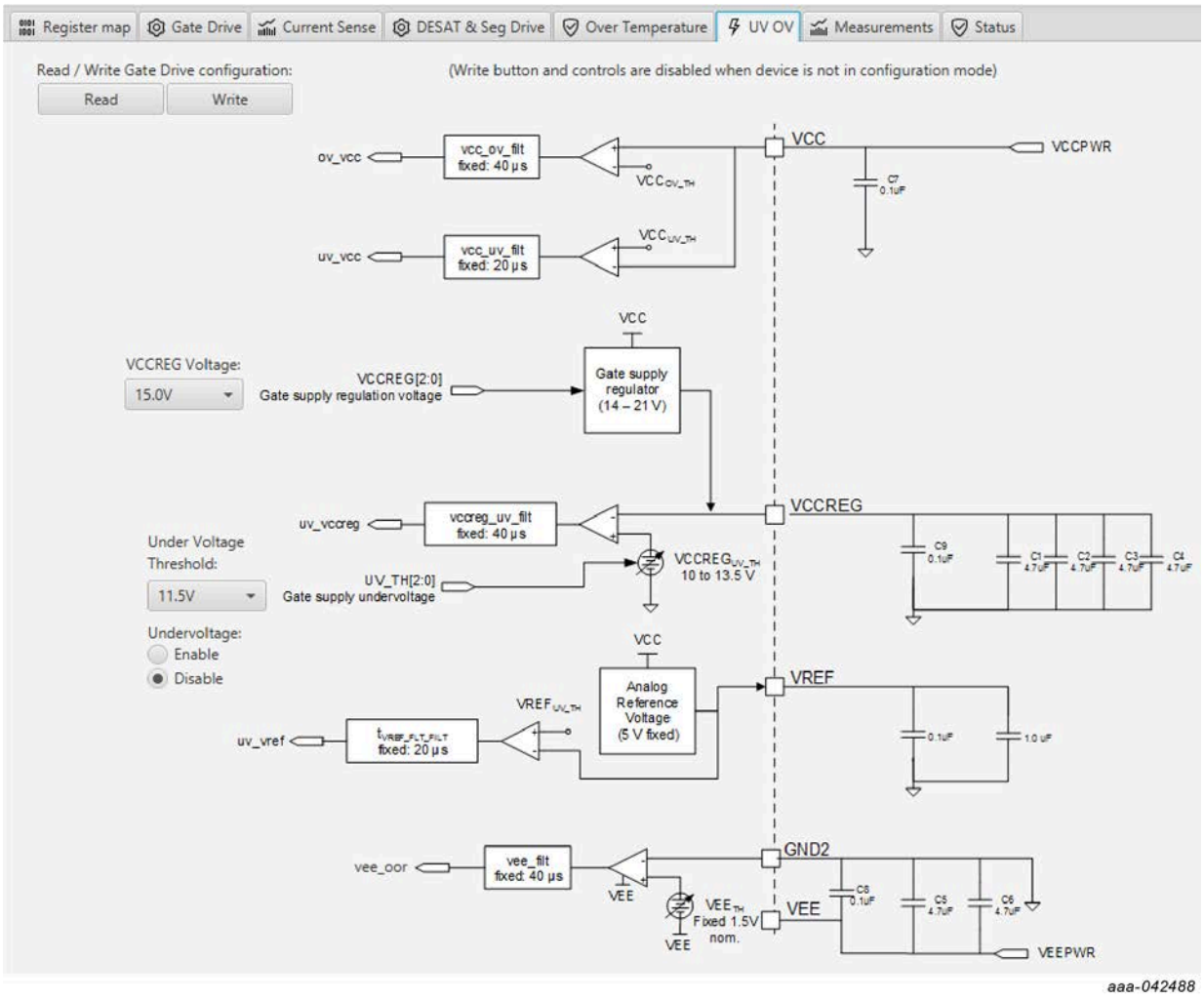

Figure 31. Undervoltage and overvoltage threshold tab

Measurements tab

- Allows monitoring and graphing of ADC and temperature values

Figure 32. Measurements tab

Status tab

- Allows monitoring of Status 1, Status 2, and Status 3 register values
- Status 1 and Status 2 faults can be cleared
- Status mask registers can be modified when in configuration mode

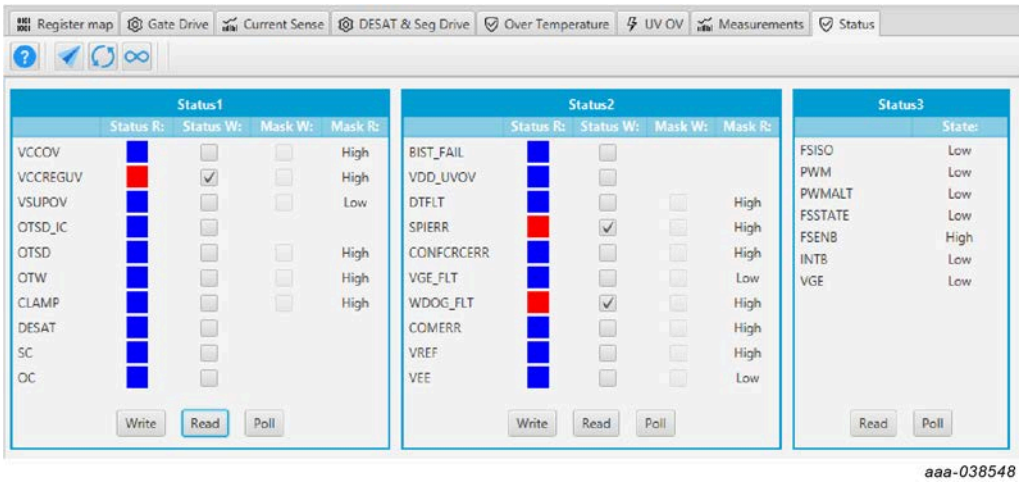

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Figure 33. Status tab

Pulse tab

- Used for double pulse, short circuit, and PWM testing
- Select desired T1, T2, and T3 timings for each test type; select enable then generate pulses

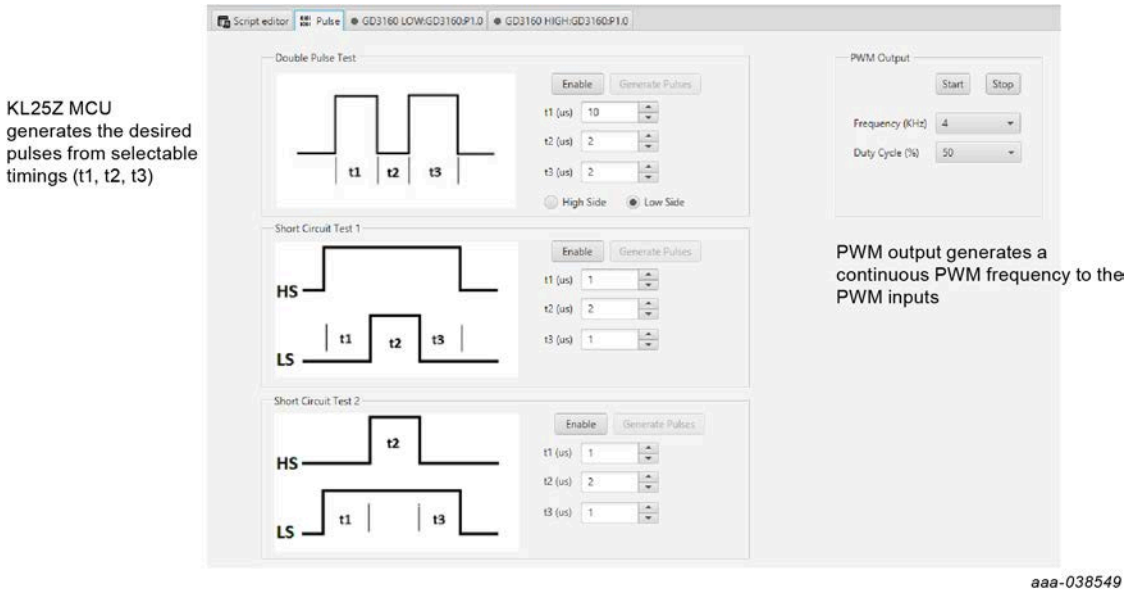

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Figure 34. Pulse tab

6.4 Troubleshooting

Some common issues and troubleshooting procedures are detailed below. This is not an exhaustive list by any means, and additional debug may be needed:

Problem	Evaluation	Explanation	Corrective action(s)
No PWM output (no fault reported)	Check PWM jumper position on translator board	Incorrect PWM jumpers obstruct signal path but not report fault	Set PWMH_SEL (J4) and PWML_SEL (J5) jumpers properly, for desired control method: • 3.3 V to 5.0 V translator board reviewed in Section 4.6
	Check PWM control signal	Ensure that proper PWM signal is reaching GD3160	Monitor EXT_PWML (TP14) and EXT_PWMH (TP15) for commanded PWM state
	Check FSENB status (see GD3160 pin 15, STATUS3)	PWM is disabled when FSENB = LOW	Set pin FSENB = HIGH (pin 15) to continue
	Check CONFIG_EN bit (MODE2)	PWM is disabled when CONFIG_EN is logic 1	Write CONFIG_EN = logic 0 to continue
No PWM output (fault reported)	Check VGE fault (VGE_FLT)	A short on IGBT or SiC module gate, or too low of VGEMON delay setting causes VGE fault, locking out PWM control of the gate.	Clear VGE_FLT bit (STATUS2) to continue. Increase VGEMON delay setting (CONFIG6). If safe operating condition can be guaranteed, set VGE_FLTM (MSK2) bit to logic 0, to mask fault.
	Check for short-circuit fault (SC) in STATUS1 register	SC is a severe fault that disables PWM. SC fault cannot be masked	Clear SC fault to continue. Consider adjusting SC fault settings on GD3160: • Adjust short-circuit threshold setting (CONFIG2) • Adjust short-circuit filter setting (CONFIG2)
PWM output is good, but with persistent fault reported	Check for dead time fault (DTFLT) in STATUS2 register	Dead time is enforced, but fault indicates that PWM controls signals are in violation	Clear DTFLT fault bit (STATUS2). Check PWMHSEL (J11) and PWMLSEL (J10) are configured to bypass dead time faults. Consider adjusting dead time settings on GD3160: • Change mandatory PWM dead time setting (CONFIG5) • Mask dead time fault (MSK2)
	Check for overcurrent (OC) fault in STATUS1 register	OC fault latches, but does not disable PWM. OC fault cannot be masked.	Clear OC fault bit (STATUS1). Adjust OC fault detection settings on GD3160: • Adjust overcurrent threshold setting (CONFIG1) • Adjust overcurrent filter setting (CONFIG1)
PWM or FSSTATE rising edge has longer delay than falling edge	Check translator output voltage versus GD3160 VDD voltage	Low translator output voltage (compared with correct VDD at GD3160) causes the high threshold at the GD3160 pin to be crossed later than commanded	Check translator output voltage selection (J233) is configured to the same level as the GD3160 VDD Check VCCSEL supply or translator outputs on the translator board for excessive loading or supply droop/pulldown
WDOG_FLT reported on startup	Check VSUP and VCC are powered	On initialization, watchdog fault is reported when one die is powered up before the other	Check VSUP and VCC both have power applied. Clear WDOG_FLT bit (STATUS2) to continue.
SPIERR reported on startup	Check KL25Z/translator connection	On initialization, SPIERR can occur when the SPI bus is open, or when GD3160 IC is powered up before the translator (which provides CSB).	Clear SPIERR fault to continue. Reinitialize power to GD3160 after translator is powered (over USB).

Problem	Evaluation	Explanation	Corrective action(s)
SPIERR reported after SPI message	Check bit length of message sent	There is SPIERR if SCLK does not see a n*24 multiple of cycles	Use 24-bit message length for SPI messages
	Check CRC	SPIERR faults if CRC provided in sent message is not good	Use FlexGUI to generate commands with valid CRC. The command can be copied in binary or hexadecimal and sent from another program.
	Check for sufficient dead time between SPI messages	SPIERR fault bit is set when the time between SPI messages (txfer_delay) received is too short. Minimum required delay time is 19 µs.	Check time between CSB rising edge (old message end) and CSB falling edge (new message start) during normal SPI read, and ensure transfer delay dead time check. SPIERR can also be cleared in BIST.
VCCREGUV reported on startup	Check VCCREG potential	Caused by low VCC	Clear VCCREGUV fault bit (STATUS1). Tune VCC-GNDISO potential with power supply potentiometer (R65).
VREFUV reported on startup	Check HV domain is powered correctly	Related to slow rise time of VCC supply on HV domain, or failed VREF regulator	Clear VREFUV bit (STATUS2). Reset HV domain supply if fault bit does not clear.
	Check VCC for undervoltage condition	Low VCC is visible indirectly through other HV domain faults	Tune VCC-GNDISO using R65 potentiometer.
VCCOV fault reported on startup	Check VEE level on suspect domain.	If VEE level is not at desired negative voltage it could cause excessive VCC level.	Check Zener diode in power supply circuit for proper value in setting VEE level. Clear VCCOV bit (STATUS1) to continue.
	Check VCC-GNDISO potential	PWM is disabled during a VCC overvoltage (20 V nom.)	Tune VCC-GNDISO potential to suitable level with power supply set potentiometer (R65). Clear VCCOV bit (STATUS1) to continue.
No PWM during short circuit test	Check PWMxSEL jumpers	Incorrect configuration of PWMALT pins prevent short-circuit test by enforcing dead time	For short-circuit test, set PWMLSEL (J10) and PWMHSEL (J11) to bypass dead time. See Section 4.4.3 for details.
Bad SPI data, appears to repeat previous response	Check VSUP/VDD for undervoltage condition	VDD_UV latches SPI buffer contents, preventing updated fault reporting.	Check voltage provided at VDD pin (pin 3). On each read, compare the address from the sent command and response (a difference indicates that the SPI response is latched due to inactive). Read multiple addresses to ensure a good comparison.
	Check PS_EN is set to HIGH in FlexGUI; see Figure 23	VCC/VEE can be enabled/disabled in software.	Enable VCC/VEE from FlexGUI
	Check VCC for undervoltage	Unpowered VCC prevents HV domain from updating data	Tune VCC-GNDISO using R65 potentiometer

7 Schematics, board layout, and bill of materials

The board schematics, board layout, and bill of materials are available at http://www.nxp.com/FRDMGD3160DCMHB on the Overview tab under Get Started.

8 References

[1] Tool summary page for FRDMGD3160DCMHB http://www.nxp.com/FRDMGD3160DCMHB

[2] Product summary page for GD3160 device http://www.nxp.com/GD3160

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Tables

Figures