UM11729

FRDMGD3162HBIEVM half-bridge evaluation board

Rev. 1 — 21 February 2022 User manual

Document information

Information	Content
Keywords	automotive, half-bridge, GD3162, gate driver
Abstract	This document describes key features and usage requirements for performing evaluation of GD3162 gate driver with FRDMGD3162HBIEVM.

Revision history

Rev	Date	Description
1	20220221	initial version

1 Important notice

IMPORTANT NOTICE

For engineering development or evaluation purposes only

NXP provides the product under the following conditions:

This evaluation kit is for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed-circuit board to make it easier to access inputs, outputs and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by connecting it to the host MCU computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application heavily depends on proper printed-circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

The product provided may not be complete in terms of required design, marketing, and or manufacturing related protective considerations, including product safety measures typically found in the end device incorporating the product. Due to the open construction of the product, it is the responsibility of the user to take all appropriate precautions for electric discharge. In order to minimize risks associated with the customers' applications, adequate design and operating safeguards must be provided by the customer to minimize inherent or procedural hazards. For any safety concerns, contact NXP sales and technical support services.

2 FRDMGD3162HBIEVM

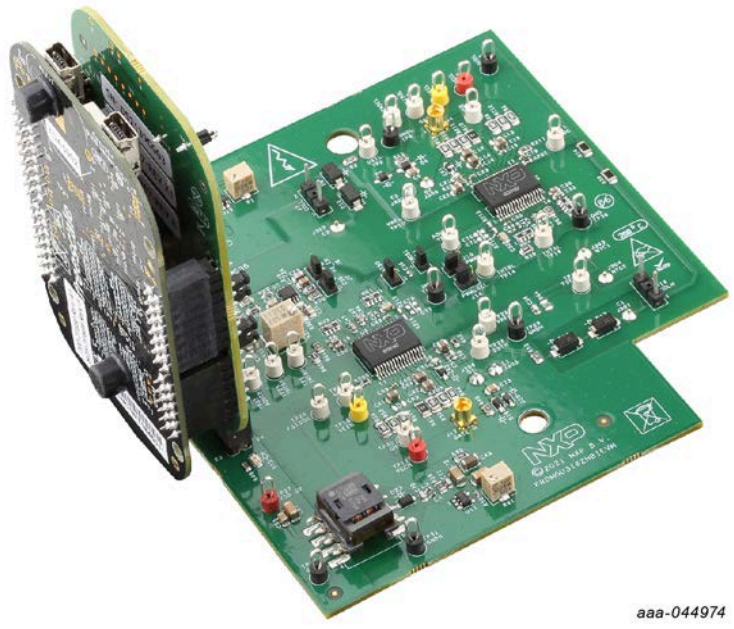


Figure 1. FRDMGD3162HBIEVM

3 Getting started

The NXP analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal, and power solutions. They incorporate monolithic integrated circuits and system-in-package devices that use proven high-volume technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost, and improved performance in powering state-of-the-art systems.

The tool summary page for FRDMGD3162HBIEVM is at http://www.nxp.com/FRDMGD3162HBIEVM. The overview tab provides an overview of the device, product features, a description of the kit contents, a list of (and links to) supported devices, a list of (and links to) any related products, and a **Get Started** section.

The **Get Started** section provides links to everything needed to start using the device and contains the most relevant, current information applicable to the FRDMGD3162HBIEVM.

1. Go to http://www.nxp.com/FRDMGD3162HBIEVM.
2. On the **Overview** tab, locate the **Jump To** navigation feature on the left side of the window.
3. Select the **Get Started** link, review each entry, and download an entry by clicking the title.
4. After reviewing the **Overview** tab, visit the other product-related tabs for additional information:
   - **Documentation**: download current documentation
   - **Software & Tools**: download current hardware and software tools
   - **Buy/Parametrics**: purchase the product and view the product parametrics

After downloading files, review each file, including the user guide, which includes setup instructions. If applicable, the bill of materials (BOM) and supporting schematics are also available for download in the **Get Started** section of the **Overview** tab.

3.1 Kit contents/packing list

The FRDMGD3162HBIEVM kit contents include:

- Assembled and tested FRDMGD3162HBIEVM board in an anti-static bag
- 3.3 V to 5.0 V translator board (KITGD316xTREVB) connected to FRDM-KL25Z
- USB cable, type A male/type mini B male, 3 ft
- Quick start guide

3.2 Required equipment

To use this kit, you need:

- Compatible HybridPACK Drive insulated gate bipolar transistor (IGBT) or SiC metal-oxide-semiconductor field-effect transistor (MOSFET) module
- DC link capacitor compatible with the HybridPACK Drive module
- 1.27 mm jumpers for configuration (included with kit)
- 30 µH to 50 µH, high current air core inductor for double pulse testing
- HV power supply with protection shield and hearing protection
- 20 V, 1.0 A DC power supply
- 500 MHz 2.5 GS/s 4-channel oscilloscope
- Rogowski coil, PEM Model CWT Mini HF60R, or CTW MiniHF30 (smaller diameter)
- Isolated high-voltage probes
- Digital voltmeter

3.3 System requirements

The kit requires the following to function properly with the software:

- Windows 7 or higher operating system

4 Getting to know the hardware

4.1 Overview

The FRDMGD3162HBIEVM is a half-bridge evaluation kit populated with two GD3162 single channel gate drive devices. The kit includes the Freedom KL25Z microcontroller hardware for interfacing a PC installed with FlexGUI software for communication to the serial peripheral interface (SPI) registers on the GD3162 gate drive devices in either daisy chain or standalone configuration.

The KITGD316xTREVB translator board is used to translate 3.3 V signals to 5.0 V signals between the MCU and GD3162 gate drivers. The evaluation kit can be connected to a compatible IGBT or SiC module for half-bridge evaluations and applications development.

4.2 Board features

- Capability to connect to HybridPACK Drive module for half-bridge evaluations
- Adjustable negative VEE gate low drive level (0 V to −10 V DC)
- Adjustable VCC gate high drive level (10 V to 25 V DC)
- Jumper configurable for disabling dead time fault protection when short-circuit testing
- Easy access power, ground, and signal test points
- Easy to install and use FlexGUI for interfacing via SPI through PC; software includes double pulse and short-circuit testing capability
- DC link bus voltage monitor on low-side driver via AMUXIN and AOUT
- Negative or positive temperature coefficient connection and configurable for monitoring module temperature

4.3 Device features

Table 1. Device features

Device	Description	Features
GD3162	The GD3162 is an advanced single channel gate driver for IGBT and SiC with dynamic gate strength adjust.	• Compatible with current sense and temp sense IGBT and SiC MOSFET modules • DESAT detection capability for detecting V_{CE} desaturation condition • Fast short-circuit protection for IGBT and SiC MOSFET with current sense feedback • Compliant with automotive safety integrity level (ASIL) C/D ISO 26262 functional safety requirements • SPI interface for safety monitoring, programmability, and flexibility • Integrated galvanic signal isolation up to 8 kV • Integrated boost capability for increased drive strength • Interrupt pins for fast response to faults and real-time reporting capability • Compatible with negative gate supply • Active bus discharge functionality

4.4 Board description

The FRDMGD3162HBIEVM is a half-bridge evaluation board populated with two GD3162 single channel IGBT or SiC gate drive devices. The board supports connection to an FRDM-KL25Z microcontroller for SPI communication configuration programming and monitoring. The board includes DESAT circuitry for short-circuit detection and implementation of GD3162 shutdown protection capabilities.

The evaluation board is designed to connect to a HybridPACK Drive module for evaluation of the GD3162 performance and capabilities.

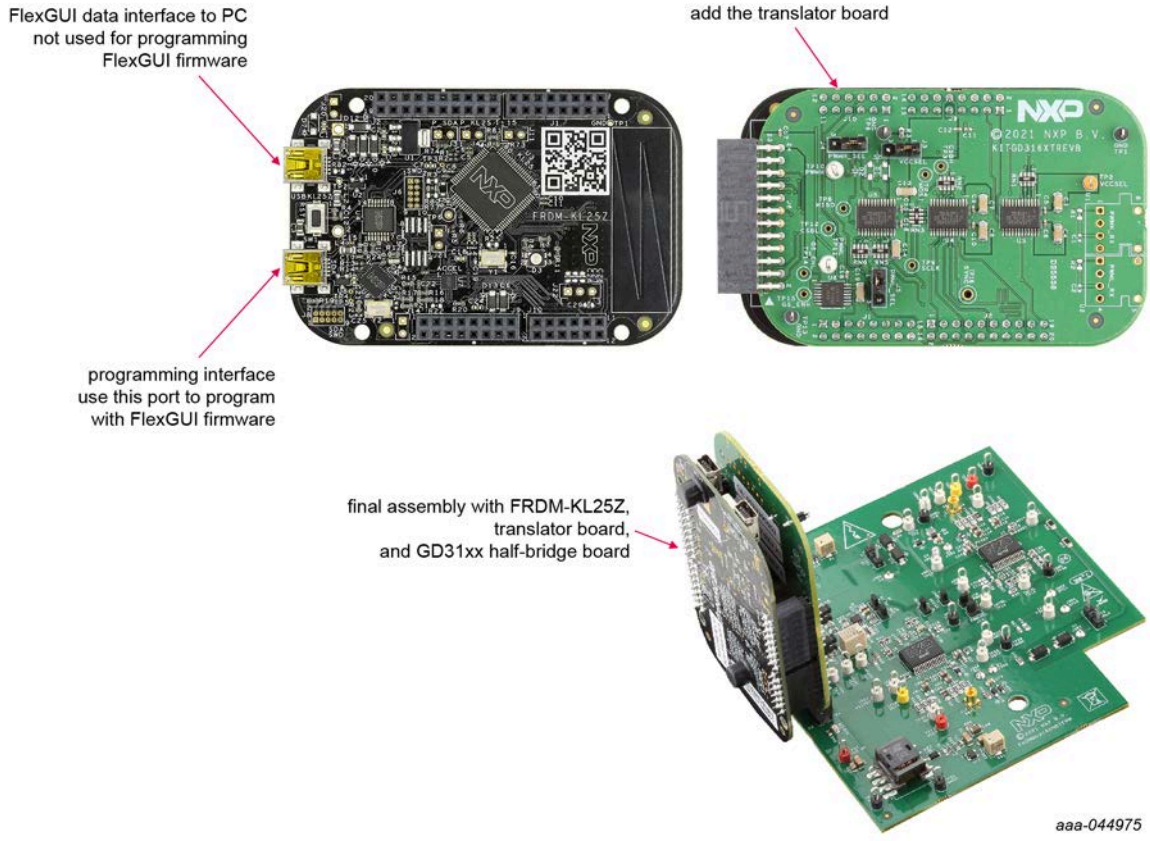


Figure 2. Connecting FRDM-KL25Z, GD31xx half-bridge EVB and translator board

4.4.1 Low-voltage logic and control connector

Low-voltage domain is 5 V VDD domain that interfaces with the MCU and GD3162 control registers through the 24-pin connector interface.

Low-side driver and high-side driver domains are driver control interfaces to HybridPACK Drive module single phase connections and test points.

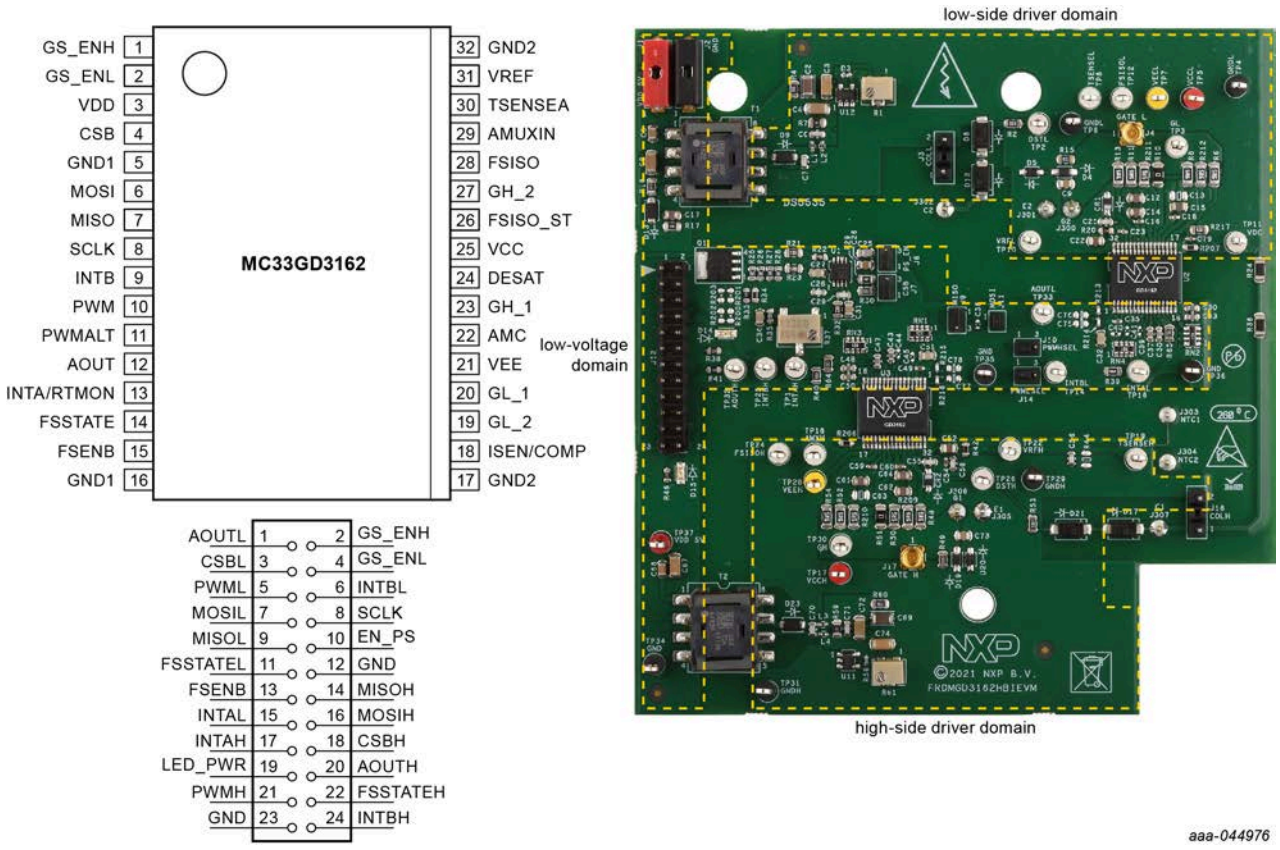


Figure 3. Evaluation board voltage and interface domains

Table 2. Low-voltage domain 24-pin connector definitions

Pin	Name	Function
1	AOUTL	analog output duty cycle encoded signal (low side) for reading temperature via TSENSEA or voltage via AMUXIN
2	GS_ENH	gate strength enable HIGH; gate drive pull-up strength control logic
3	CSBL	chip select bar (low side)
4	GS_ENL	gate strength enable LOW; gate drive pull-down strength control logic
5	PWML	pulse width modulation (PWM) input (low side)
6	INTBL	interrupt bar (low side)
7	MOSIL	master out slave in (low side)
8	SCLK	serial clock input
9	MISOL	master in slave out (low side)
10	EN_PS	MCU control of flyback power supply
11	FSSTATEL	fail-safe state (low side)
12	GND	ground
13	FSENB	fail-safe enable (high side and low side)
14	MISOH	master in slave out (high side)

Table 2. Low-voltage domain 24-pin connector definitions...*continued*

Pin	Name	Function
15	INTAL	fault reporting and real time V_{CE} and VGE monitoring (low side)
16	MOSIH	master out slave in (high side)
17	INTAH	fault reporting and real time V_{CE} and VGE monitoring (high side)
18	CSBH	chip select bar (high side)
19	LED_PWR	USB 3.3 V power for INTB LEDs (high side and low side)
20	AOUTH	duty cycle encoded signal (high side)
21	PWMH	PWM input (high side)
22	FSSTATEH	fail-safe state (high side)
23	GND	ground
24	INTBH	interrupt bar (high side)

4.4.2 Test point definitions

All test points are clearly marked on the evaluation board. Figure 4 shows the location of various test points.

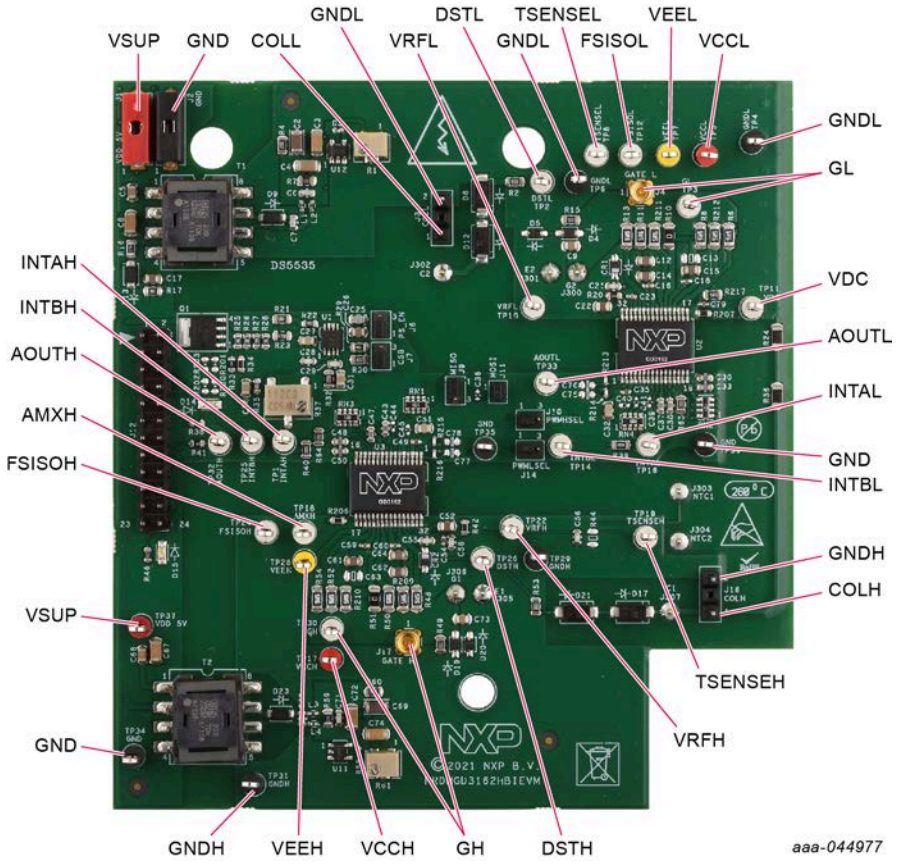


Figure 4. Key test point locations

Table 3. Test point definitions

Test point	Definition
Low-voltage domain	
VSUP	DC voltage source connection point for VSUP power input of GD3162 devices. Externally supplied 12 V DC supply voltage. VSUP supplies 5 V regulator for gate drive VDD.
GND	grounding points for low-voltage domain
INTAH	fault monitor and VCE/VGE real-time report monitor high-side test point
INTBL	interrupt bar low-side test point
INTAL	fault monitor and VCE/VGE real-time report monitor low-side test point
INTBH	interrupt bar high-side test point
Low-side driver domain	
GNDL	low-side domain ground point
VCCL	positive voltage supply test point for isolated circuitry and low-side driver domain
VRFL	5.0 V reference test point for isolated analog circuitry on low-side driver
TSENSEL	temperature sense connection low-side test point
GL	module gate test point on low-side driver domain which is the charging pin of gate; including MMCX probe connection
FSISOL	high-voltage domain fail-safe low-side test point
DSTL	V_{CE} desaturation test point connected to low-side driver DESAT pin and circuitry
VEEL	negative voltage supply test point for low-side driver gate of IGBT or SiC module
VDC	DC link voltage test point at voltage divider
COLL	collector test point/connection terminal on low side
High-side driver domain	
VCCH	positive voltage supply test point for isolated circuitry and high-side driver domain
GNDH	high-side domain ground point
COLH	collector test point/connection high side
TSENSEH	temperature sense connection high-side test point
VRFH	5.0 V reference test point for isolated analog circuitry on high-side driver
FSISOH	high-voltage domain fail-safe high-side test point
GH	module gate test point on high-side driver domain which is the charging pin of gate; including MMCX probe connection
DSTH	V_{CE} desaturation test point connected to high-side driver DESAT pin and circuitry
VEEH	negative voltage supply test point for high-side driver gate of IGBT or SiC module
AMXH	analog MUX input test point for high-side driver

4.4.3 Power supply and jumper configuration

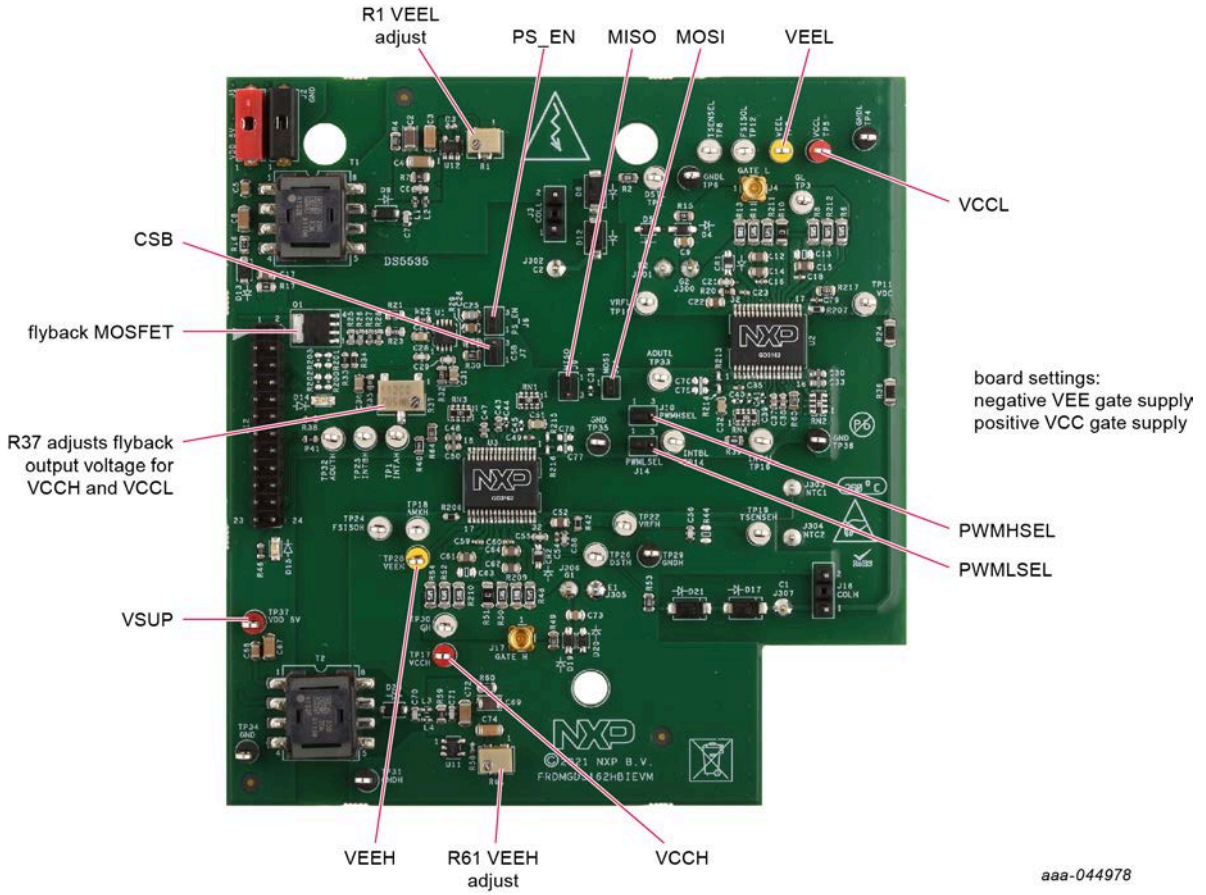


Figure 5. Power supply and jumper configuration

Table 4. Jumper definitions

Jumper	Position	Function
PWMHSEL (J10)	1-2	dead time fault protection enabled (high side)
	2-3	dead time fault protection disabled (use for short-circuit testing)
PWMLSEL (J14)	1-2	dead time fault protection enabled (low side)
	2-3	dead time fault protection disabled (use for short-circuit testing)
VCCH and VCCL	open	VCCREG controls gate voltage
	closed	VCC and VCCREG are tied together
CSB (J7)	1-2	chip select for normal operation
	2-3	chip select for daisy chain operation
MOSI (J11)	closed	normal operation
	open	daisy chain operation
MISO (J9)	1-2	normal operation
	2-3	daisy chain operation

Table 4. Jumper definitions...*continued*

Jumper	Position	Function
PS_EN (J6)	1-2	MCU control of flyback supply enable
	2-3	flyback supply enable tied to VSUP
R37	-	adjusts VCCH and VCCL level
R1	-	adjusts negative VEEL level
R61	-	adjusts negative VEEH level

4.4.4 Bottom view

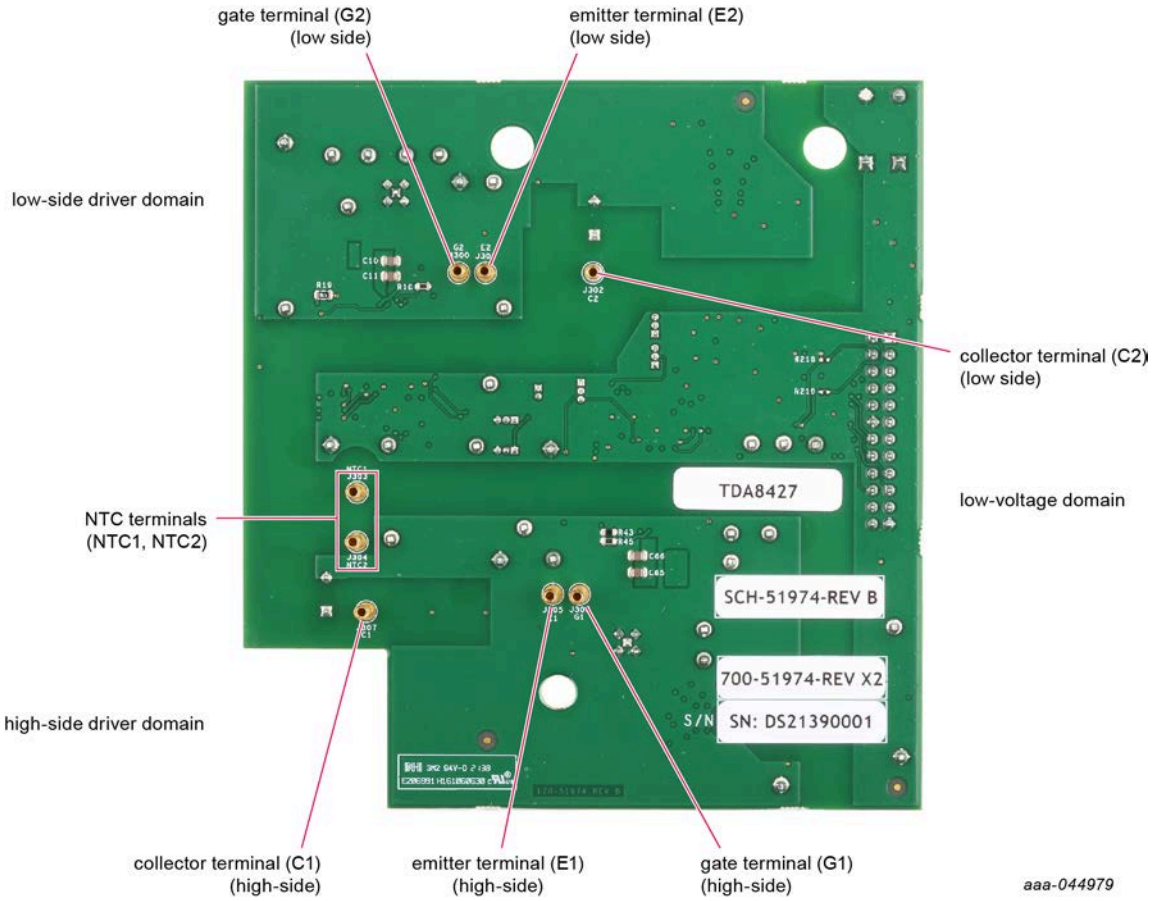


Figure 6. Evaluation board bottom view

4.4.5 Gate drive resistors

- RGH - gate high resistors in series with GH_1 (strong gate charge/turn-on pin) and GH_2 (weak gate charge/turn-on pin) and HybridPACK Drive module gate. These gate drive output pins control the turn on of the SiC MOSFET gate and are enabled when PWM is logic HIGH and setting match GS_ENH.
- RGL - gate low resistors in series with GL_1 (strong gate discharge/turn-off pin) and GL_2 (weak gate discharge/turn-off pin) and HybridPACK Drive module gate. These gate drive output pins control the turn off of the SiC MOSFET gate and are enabled when PWM is logic LOW and setting match GS_ENL.
- RAMC - series resistor between HybridPACK Drive module gate and AMC input pin of the GD3162 driver for gate sensing and active Miller clamping.

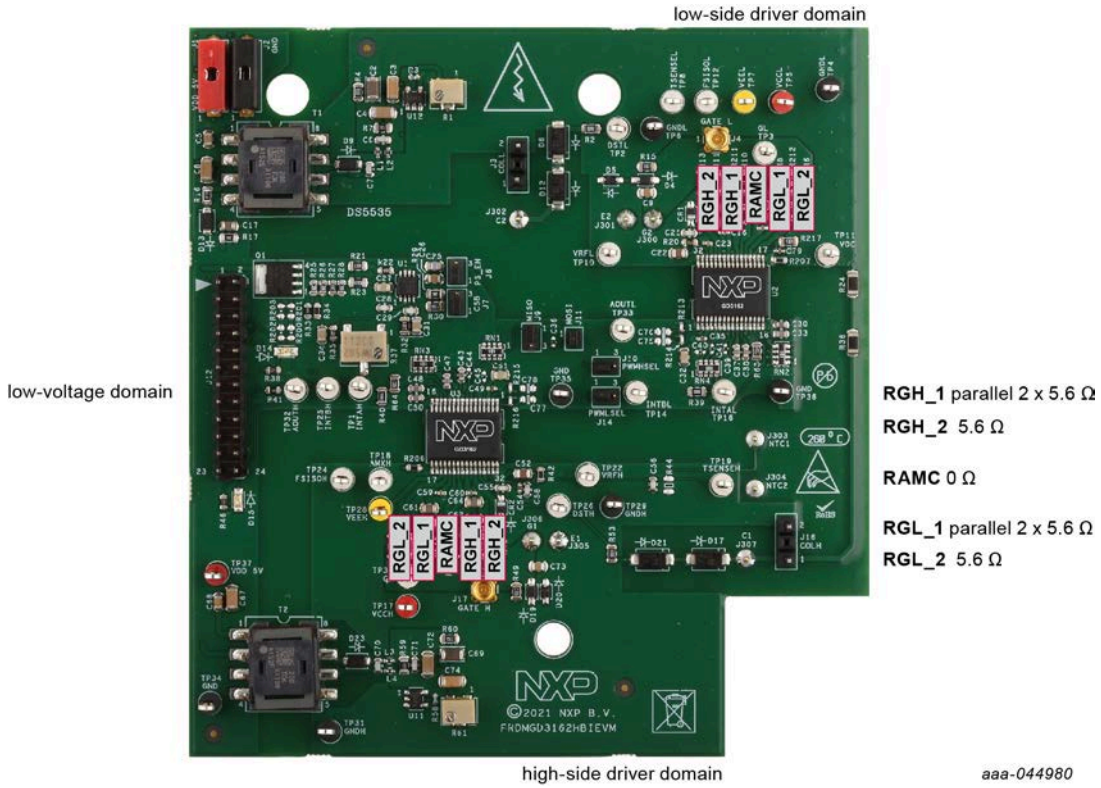


Figure 7. Gate drive resistors

4.4.6 LED interrupt indicators

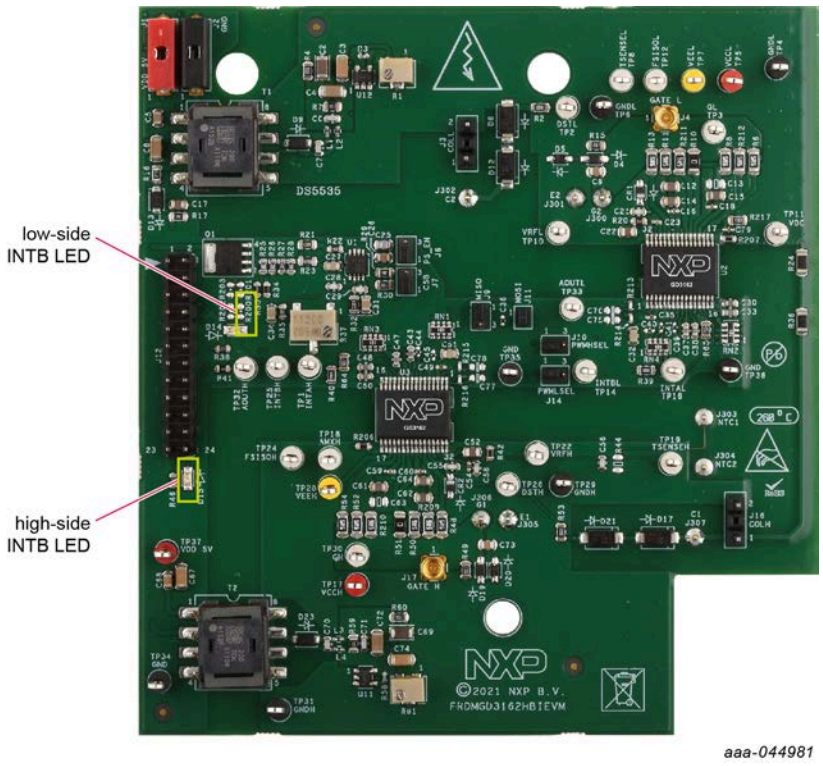


Figure 8. LED interrupt indicators

Table 5. LED interrupt indicators

LED	Description
Low-side INTB	connected to the INTB output pin of low-side driver indicating reported fault status when on (active LOW)
High-side INTB	connected to the INTB interrupt output pin of high-side driver indicating reported fault status when on (active LOW)

4.5 Kinetis KL25Z Freedom board

The Freedom KL25Z is an ultra low-cost development platform for Kinetis L series MCU built on Arm Cortex-M0+ processor.

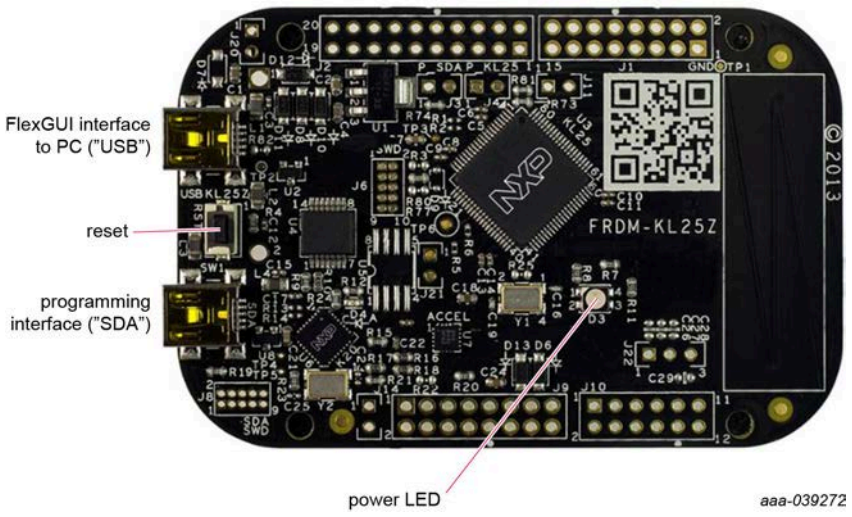


Figure 9. Freedom development platform

4.6 3.3 V to 5.0 V translator board

KITGD316xTREVB translator enables level shifting of signals from MCU 3.3 V to 5.0 V SPI communication.

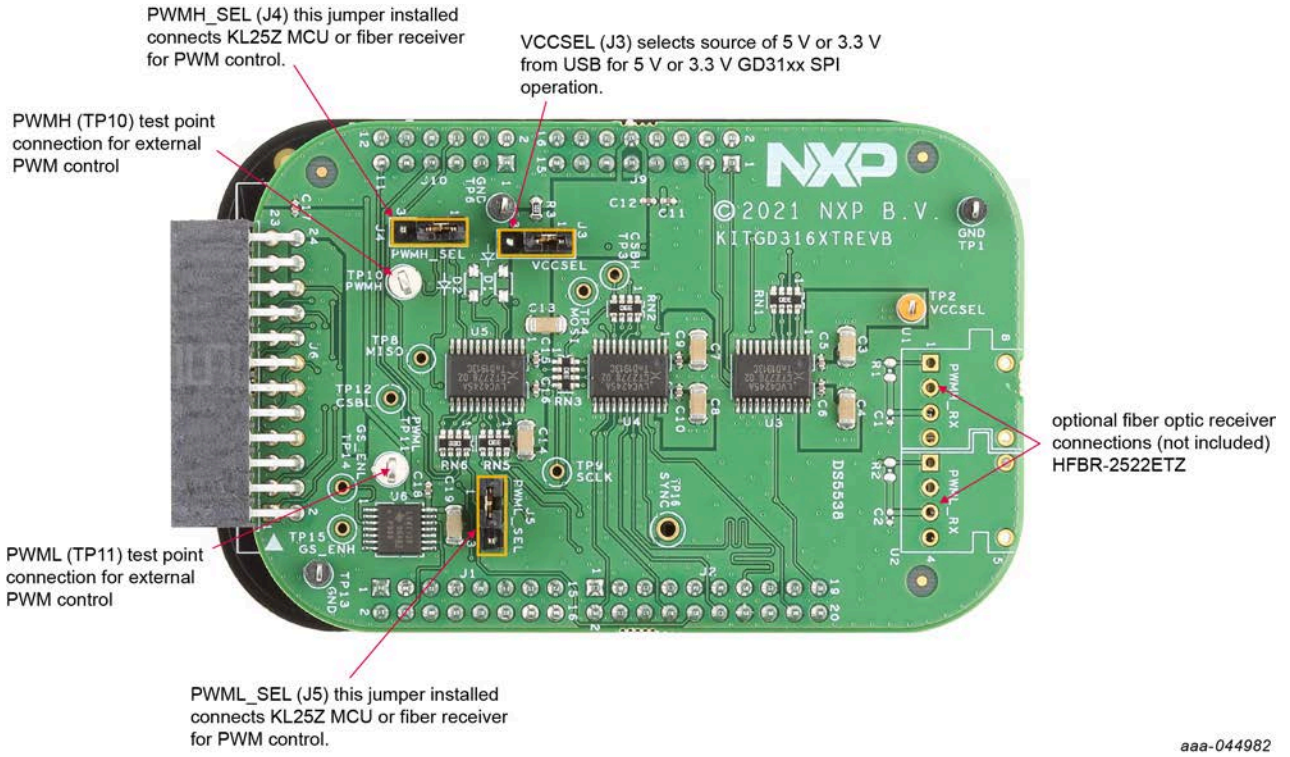


Figure 10. Translator board

Table 6. Translator board jumper definitions

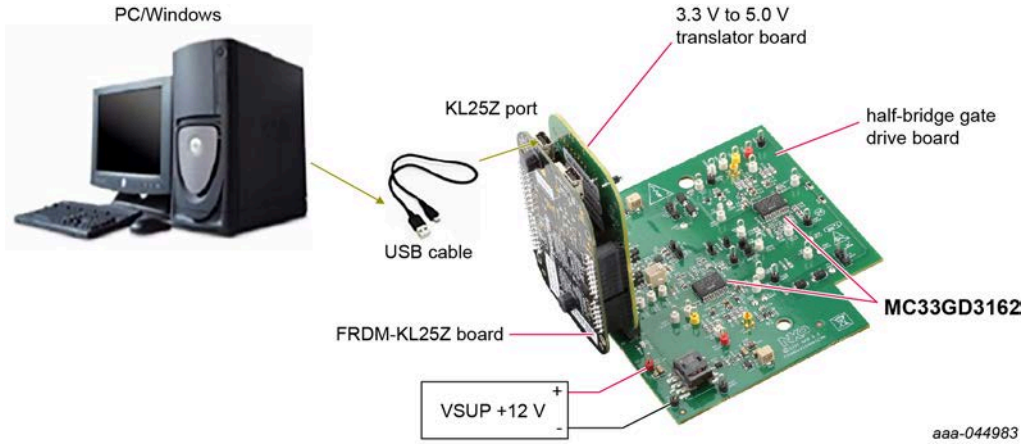
Jumper	Position	Function
VCCSEL (J3)	1-2	selects 5.0 V for 5.0 V compatible gate drive
	2-3	selects 3.3 V for 3.3 V compatible gate drive
PWMH_SEL (J4)	1-2	selects PWM high-side control from KL25Z MCU
	2-3	selects PWM high-side control from fiber optic receiver inputs
PWML_SEL (J5)	1-2	selects PWM low-side control from KL25Z MCU
	2-3	selects PWM low-side control from fiber optic receiver inputs

5 Configuring the hardware

FRDMGD3162HBIEVM is connected to compatible SiC MOSFET HybridPACK Drive module with a DC link capacitor as shown in Figure 11. Double pulse and short-circuit testing can be conducted utilizing Windows based PC with FlexGUI software.

Suggested equipment needed for test:

- Rogowski coil high-current probe
- High-voltage differential voltage probe
- High sample rate digital oscilloscope with probes
- DC link capacitor compatible with HybridPACK Drive module
- IGBT or SiC MOSFET HybridPACK Drive module
- Windows based PC
- High-voltage DC power supply for DC link voltage
- Low-voltage DC power supply for VSUP
  - +12 V DC gate drive board low-voltage domain
- Voltmeter for monitoring high-voltage DC link supply
- Load coil for double pulse testing



DC link capacitor is not shown

Figure 11. Evaluation board and system setup

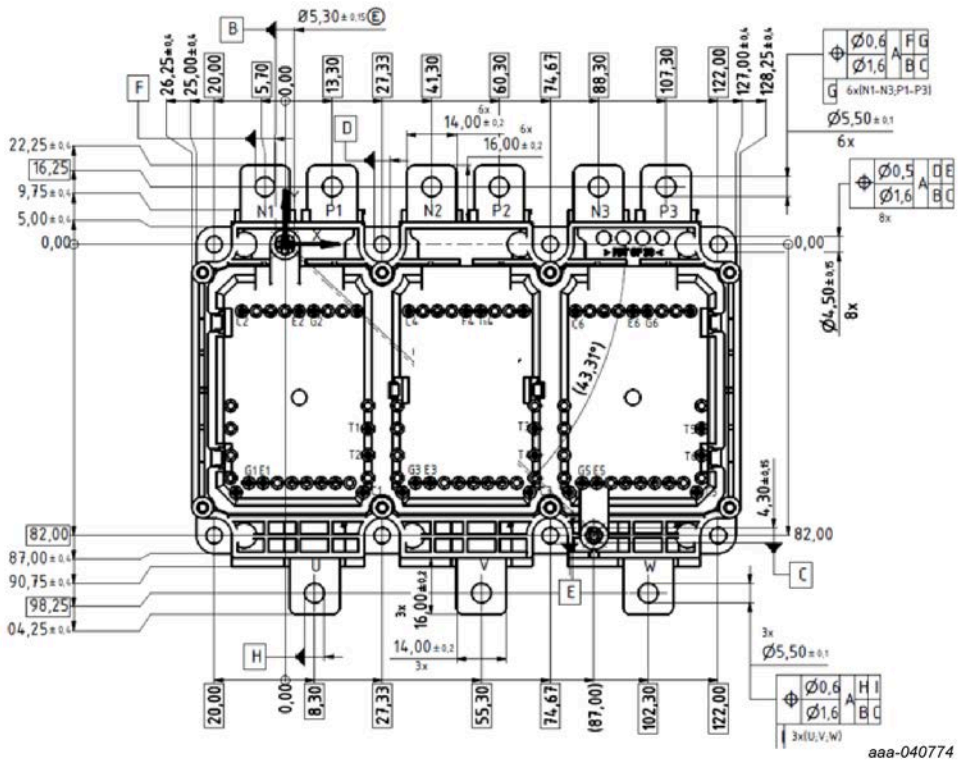


Figure 12. Power module

6 Installation and use of software tools

Software for FRDMGD3162HBIEVM is distributed with the FlexGUI tool (available on NXP.com). Necessary firmware comes pre-installed on the FRDM-KL25Z with the kit.

Even if the user intends to test with other software or PWM, it is recommended to install this software as a backup or to help debugging.

6.1 Installing FlexGUI on your computer

The latest version of FlexGUI supports the GD3100, GD3160, and GD3162. It is designed to run on any Windows 10 or Windows 8 based operating system. To install the software, do the following:

1. Go to www.nxp.com/FlexGUI and click **Download**.
2. When the FlexGUI software page appears, click **Download** and select the version associated with your PC operating system.
3. FlexGUI wizard creates a shortcut, an NXP FlexGUI icon appears on the desktop. By default, the FlexGUI executable file is installed at **C:\NXP_GD31xx_GUI-x.x.x.msi**. Installing the device drivers overwrites any previous FlexGUI installation and replaces it with a current version containing the GD31xx drivers. However, configuration files from the previous version remain intact.

6.2 Configuring the FRDM-KL25Z microcode

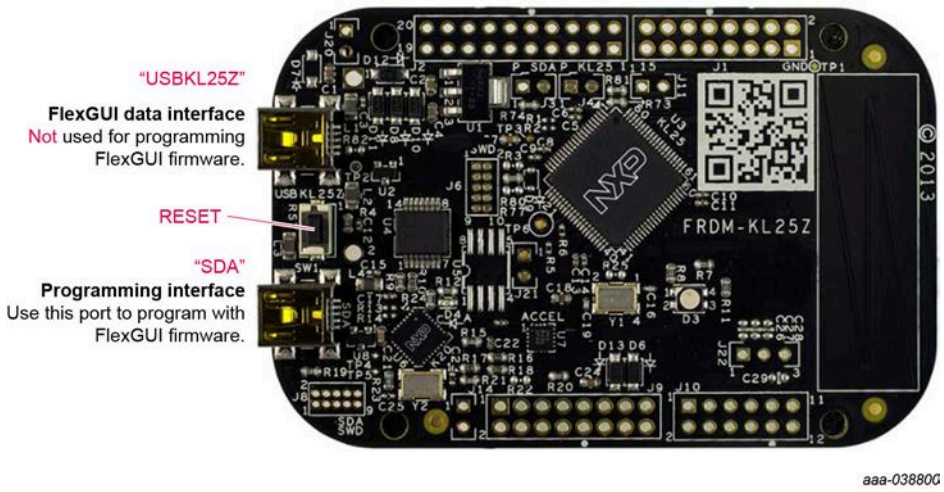


Figure 13. FRDM-KL25Z setup and interface

By default, the FRDM-KL25Z delivered with this kit is preprogrammed with the current and most up-to-date firmware available for the kit.

A way to check quickly that the microcode is programmed and the board is functioning properly, is to plug the KL25Z into the computer, open FlexGUI, and verify that the software version at the bottom is 6.4 or later (see Figure 14).

If a loss of functionality following a board reset, reprogramming, or a corrupted data issue, the microcode may be rewritten per the following steps:

1. To clear the memory and place the board in boot loader mode, hold down the reset button while plugging a USB cable into the **OpenSDA** USB port.
2. Verify that the board appears as a BOOTLOADER device and continue with step 3. If the board appears as KL25Z, you may go to step 6.
3. Download the **Firmware Apps** .zip archive from the PEmicro OpenSDA webpage (http://www.pemicro.com/opensda/). Validate your email address to access the files.
4. Find the most recent MDS-DEBUG-FRDM-KL25Z_Pemicro_v118.SDA and copy/drag-and-drop into the **BOOTLOADER** device.
5. Reboot the board by unplugging and replugging the connection to the **OpenSDA** port. Verify now that the device appears as a KL25Z device to continue.
6. Locate the most recent KL25Z firmware; which is distributed as part of the FlexGUI package.
   a. From the FlexGUI install directory or zip file, downloaded, find the firmware bin file "flexgui-fw-KL25Z_usb_hid_gd31xx-Vx.x.x.bin".
   b. This .bin file is a product/family-specific configuration file for FRDM-KL25Z containing the pin definitions, SPI/PWM generation code, and pin mapping assignments necessary to interface with the translator board as part of FRDMGD3162HBIEVM.

7. With the KL25Z still plugged through the **OpenSDA** port, copy/drag-and-drop the .bin file into the KL25Z device memory. Once done, disconnect the USB for OpenSDA port and plug into the other USB port, labeled **KL25Z**.
   a. The device may not appear as a distinct device to the computer while connected through the KL25Z USB port, this is normal.
8. The FRDM-KL25Z board is now fully set up to work with FRDMGD3162HBIEVM and the FlexGUI.
   a. There is no software stored or present on either the driver or translator boards, only on the FRDM-KL25Z MCU board.

All uploaded firmware is stored in non-volatile memory until the reset button is hit on the FRDM-KL25Z. There is no need to repeat this process upon every power up, and there is no loss of data associated with a single unplug event.

6.3 Using the FlexGUI

The FlexGUI is available from http://www.nxp.com/FlexGUI as an evaluation tool demonstrating GD31xx-specific functionality, configuration, and fault reporting. FlexGUI also includes basic capacity for the FRDMGD3162HBIEVM to control an IGBT or SiC module, enabling double pulse or short-circuit testing.

SPI messages can be realized graphically or in hexadecimal format. CSB is selectable to address one or both GD31xx on the board via daisy chain. See Figure 14 to Figure 34 for FlexGUI for GD31xx internal register read and write access.

Starting FlexGUI for GD31xx

- FlexGUI install program (C:\NXP_GD31xx_GUI-x.x.x.msi)
- Download FlexGUI and run the install program on your PC.
- When you start the application, Figure 14 allows you to select the target application board, feature set (standard or daisy chain), target MCU, and USB interface. Leave all settings as shown.

Figure 14. Kit selection

FlexGUI settings

- Access settings by selecting Settings from the File menu

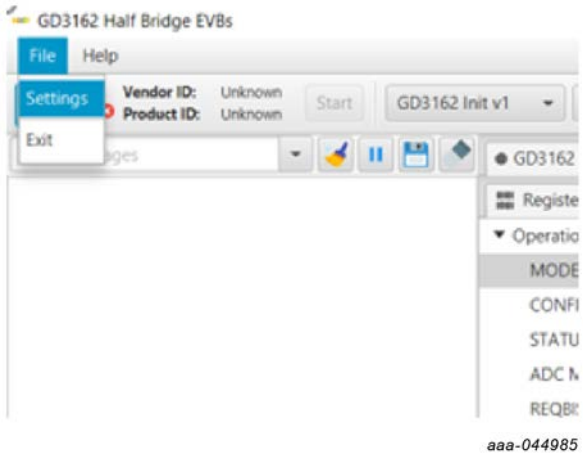


Figure 15. GUI settings menu

- The Loader and Logs settings are shown below:

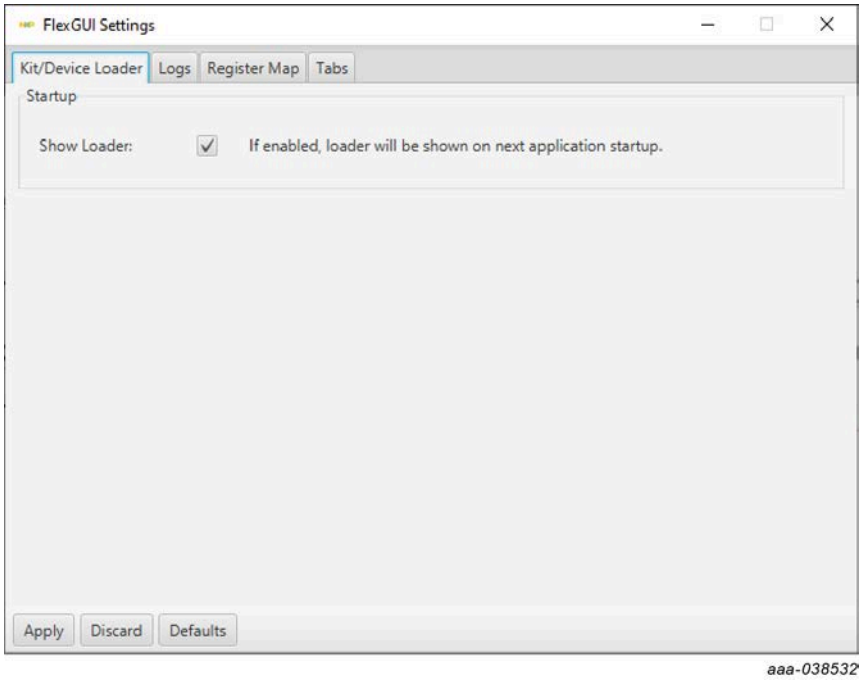


Figure 16. Loader settings

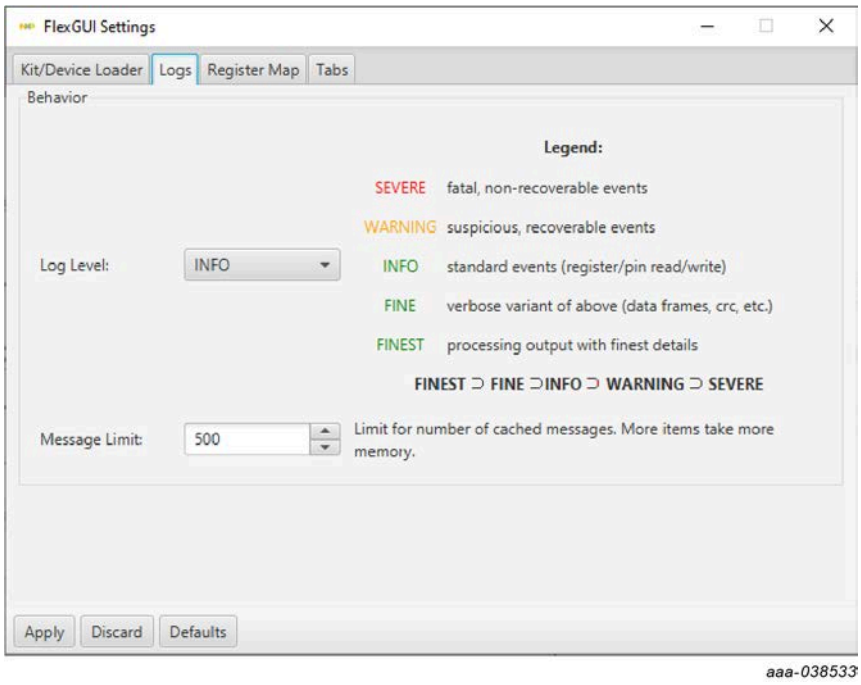


Figure 17. Logs settings

- Access settings by selecting Settings from the File menu.
- The Register Map and Tabs settings are shown below:

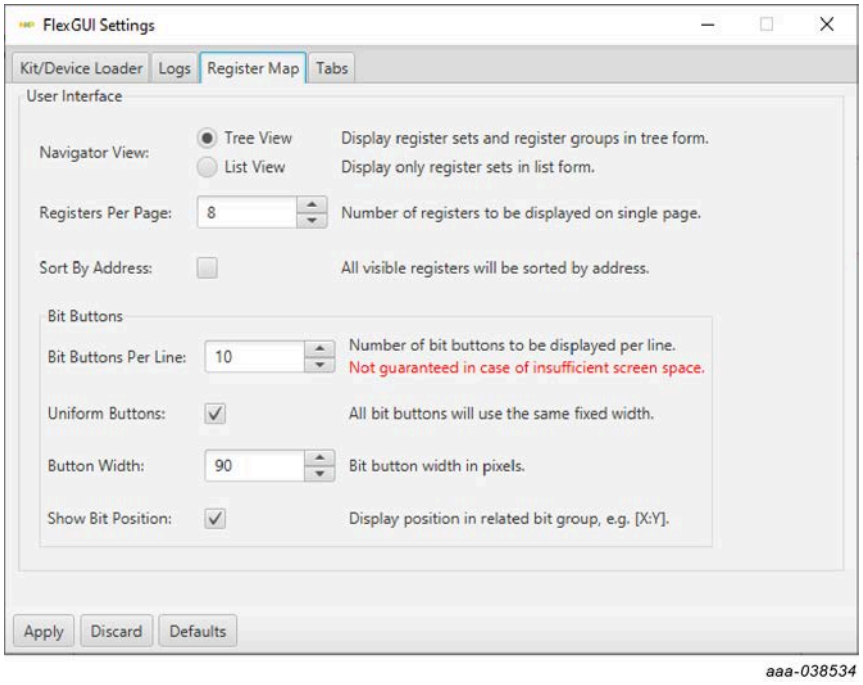


Figure 18. Register map settings

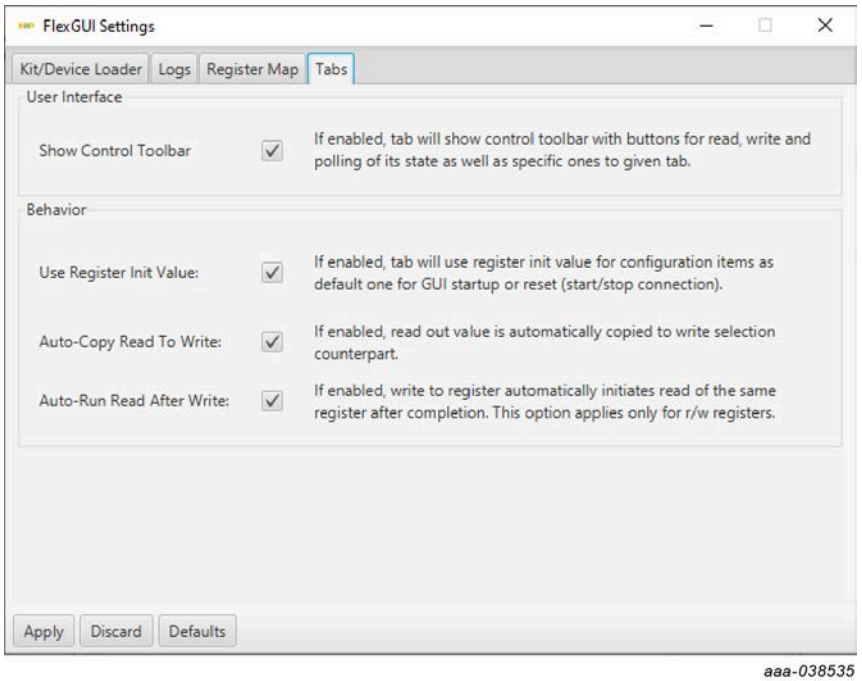


Figure 19. Tabs settings

Command Log window

- The Command Log area informs the user about application events.

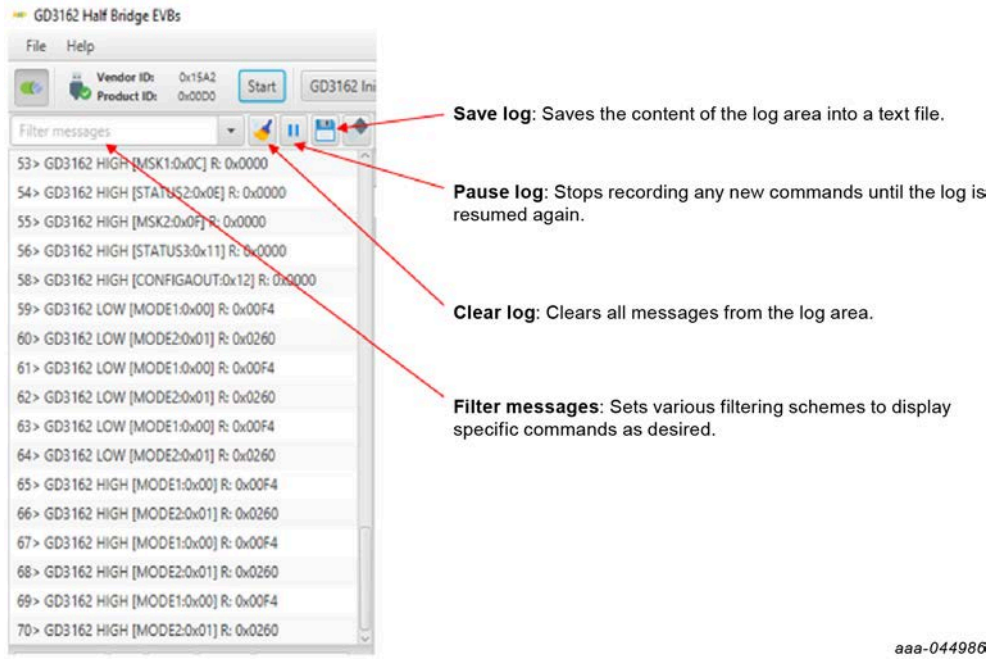


Figure 20. Command Log area

Global workspace controls

- Always visible in the lower left corner of the main application window.
  - GD3162 tab functionality
    - Switch modes between run and configuration mode
    - Set SPI frequency

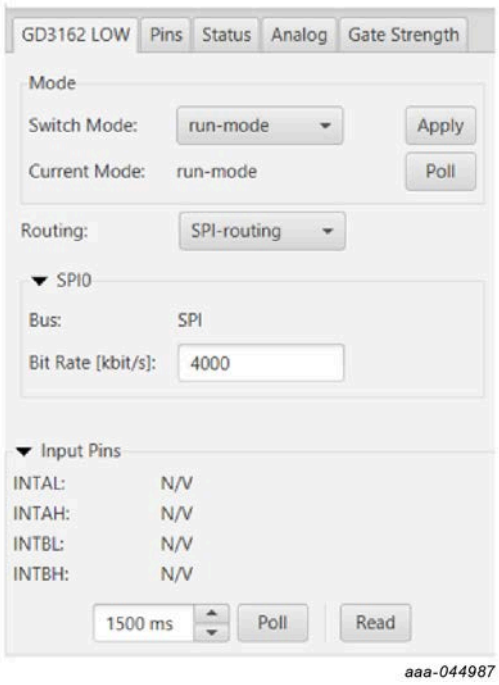


Figure 21. Device pins settings and status menus

- Pins tab functionality
  - Set control levels. Default values are shown.
  - Read and automatically poll INTB pins (INTA pins are added for GD3162).
  - Control pins set values to a default to a functional state.
    - FSENB - enable/disable fail-safe enable
    - EN_PS - enables flyback supply on EVB at 17 V V_{CC} on high side and low side
    - FSSTATEL and FSSTATEH set the fail-safe state when FSENB is enabled
    - PWML and PWMH set the default state PWM inputs for high side and low side

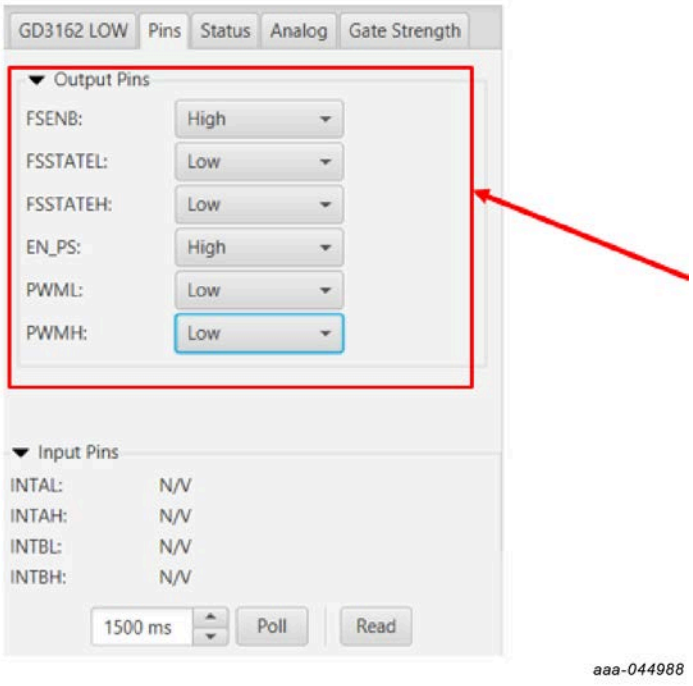


Figure 22. Pins tab functionality

- Status tab functionality
  - Monitors Status 1 and Status 2 fault bits. Bits that are set are shown in red.
  - Ability to clear all faults and automatically poll status registers.

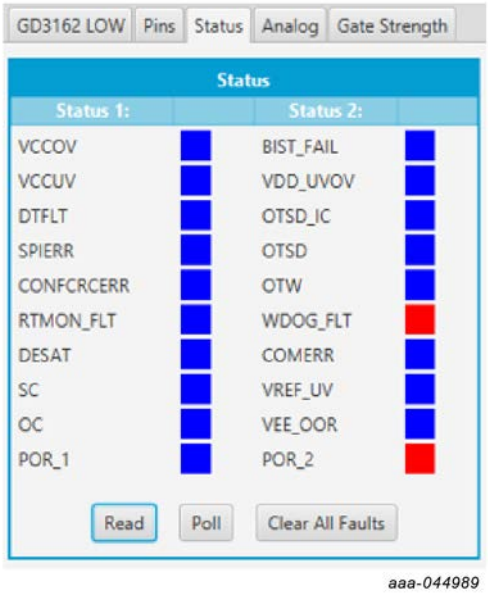


Figure 23. Status tab functionality

- Analog tab functionality
  - Read and poll ADC values from the high-voltage domain
  - Displays raw ADC and converted values

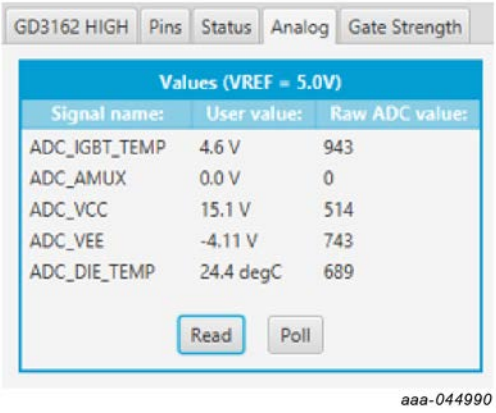


Figure 24. Analog tab functionality

- Gate strength tab functionality
  - Read and poll the pull-up and pull-down gate strength that can either be controlled by GSSPI_EN set to logic 1 in MODE2 register and bit settings in config register STATCON4
  - Gate strength can also be configured providing logic level in drop-down menu on GS_ENH and GS_ENL input pins. GSSPI_EN must be logic 0 (default state)

Figure 25. Gate strength tab functionality

Register map

- Registers are grouped according to function; independent lines to read and write the registers
- Individual registers can be read by clicking the R button and can be written by using the W button.
- Copy button to copy the read values to the write line; can be set to copy automatically
- Reset button to undo the changes on the write line and reset to the previous value
- Global register controls perform the selected command on all registers with the checkbox selected.
- Clear button clears all or selected register values
- Add to Script adds current and selected register values to a script in the script editor window

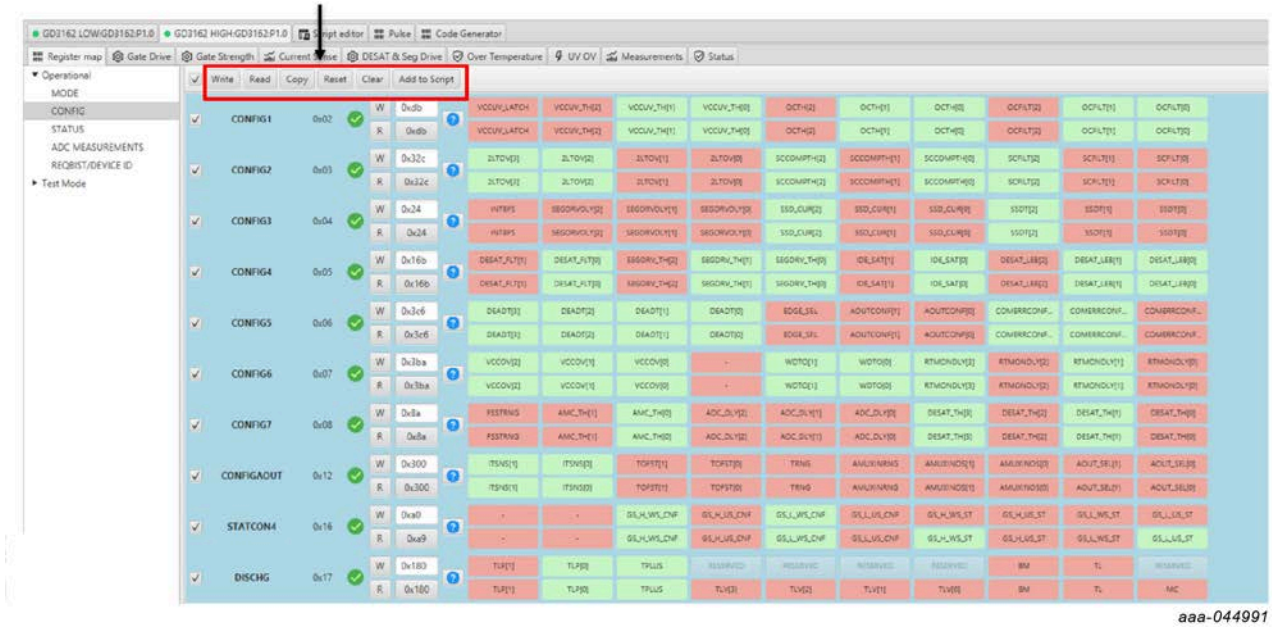


Figure 26. Register map

Gate Drive tab

- Allows setting of parameters related to the gate drive; controls are disabled when not in config mode
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

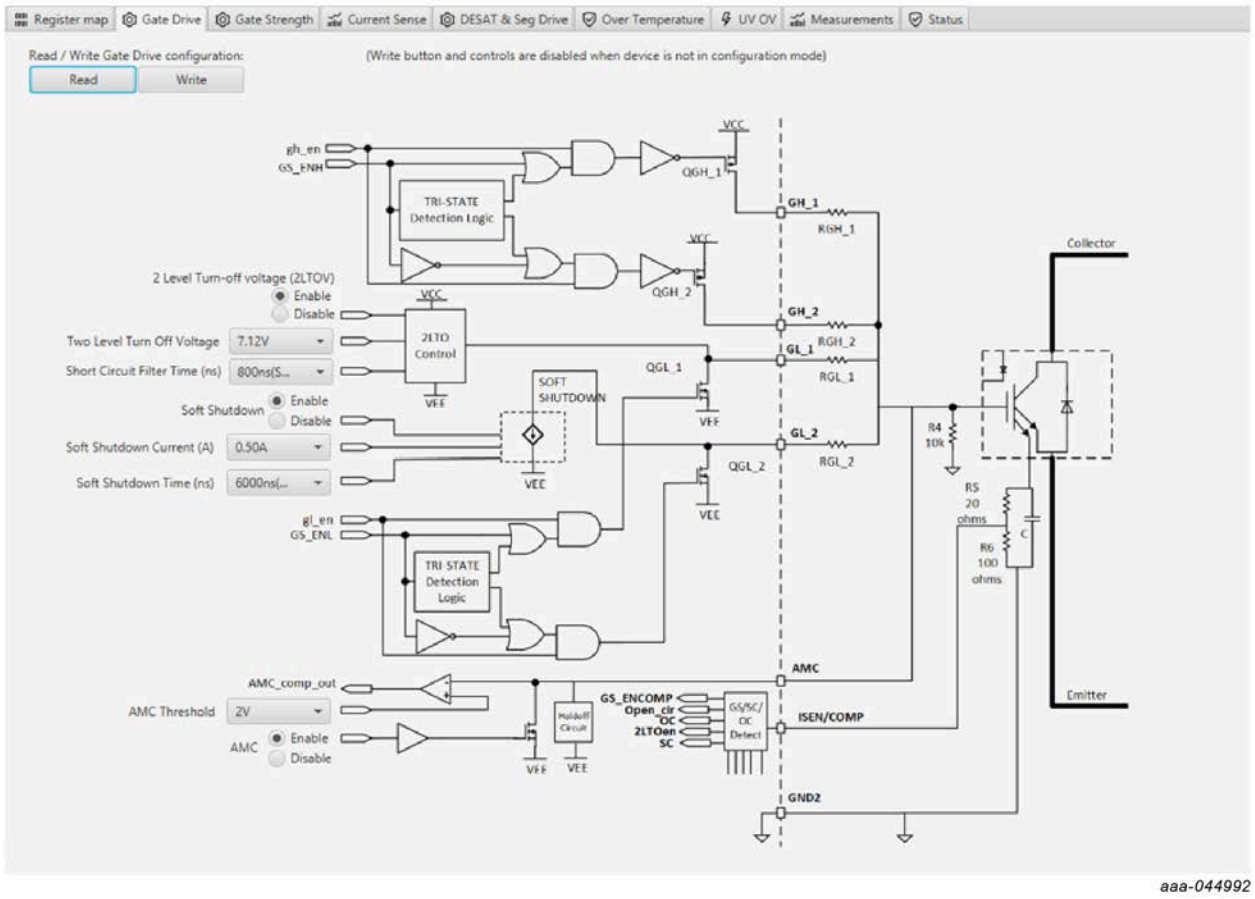


Figure 27. Gate drive tab

Current Sense tab

- Allows setting of parameters related to current sense
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

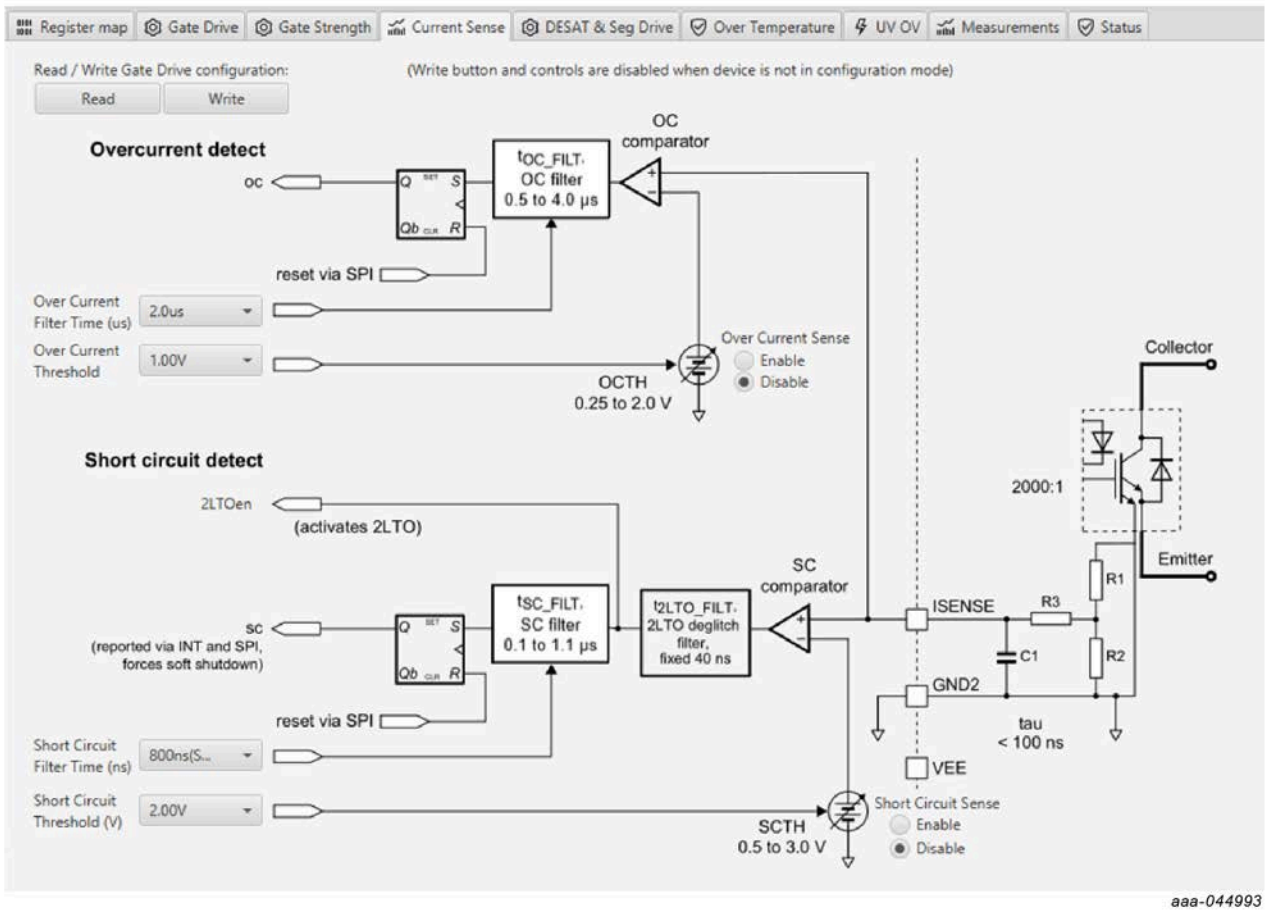


Figure 28. Current sense tab

DESAT & Seg Drive tab

- Allows setting of parameters related to desat and segmented drive
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

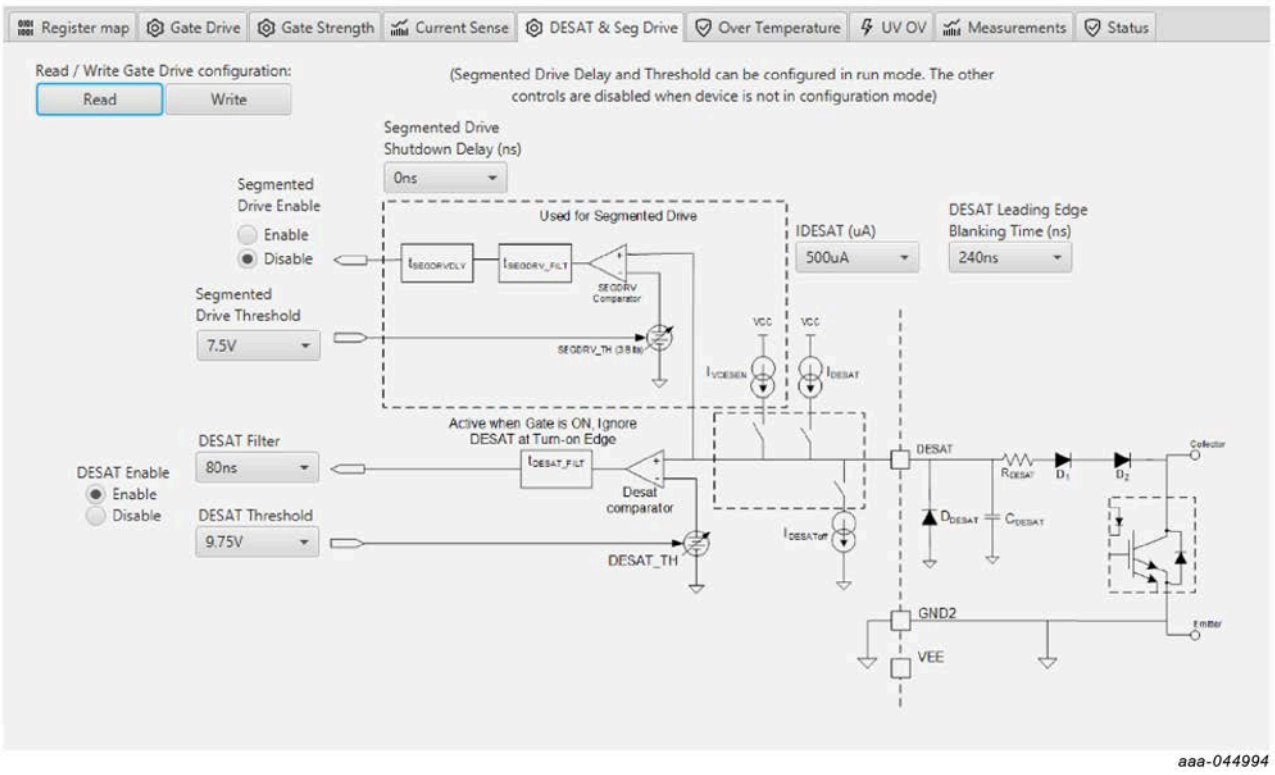


Figure 29. Desat and segmented drive tab

Overtemperature tab

- Allows setting of parameters related to overtemperature and overtemperature warning thresholds
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

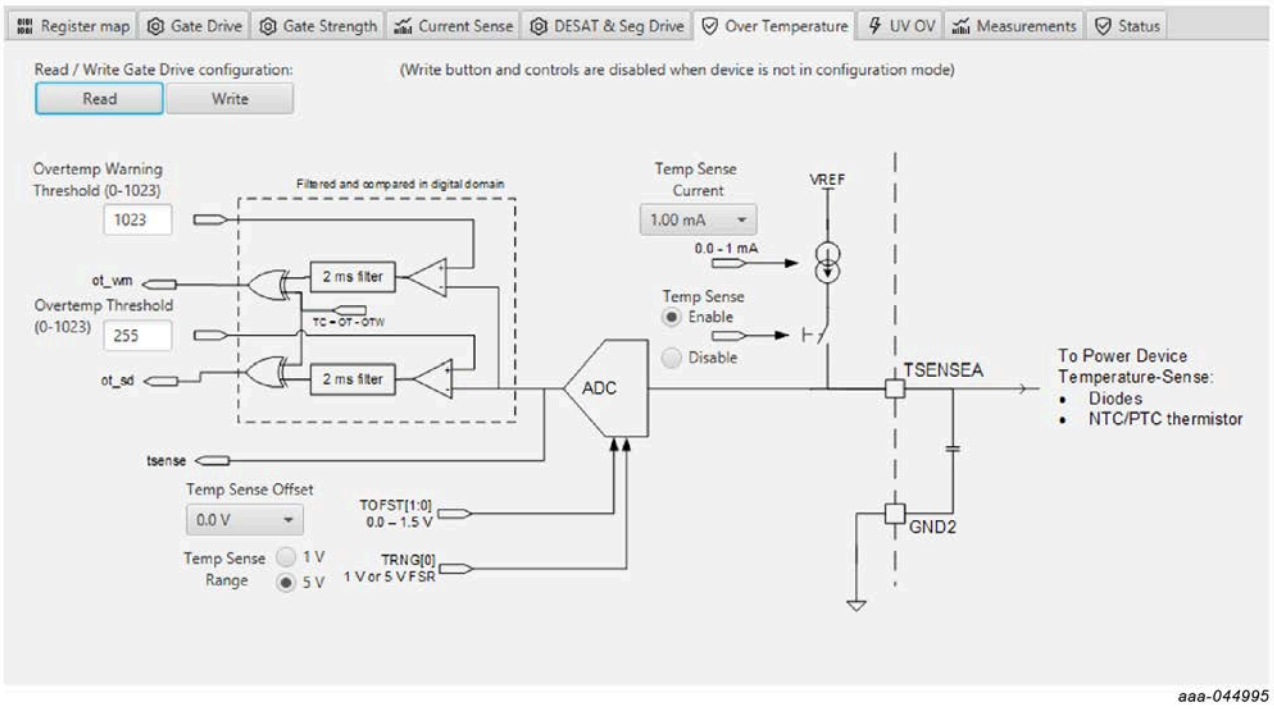


Figure 30. Overtemperature tab

Undervoltage and overvoltage threshold tab

- Allows setting of parameters related to undervoltage and overvoltage threshold
- Provides a more intuitive visual way to set parameters
- All settings are automatically synchronized with the register controls.

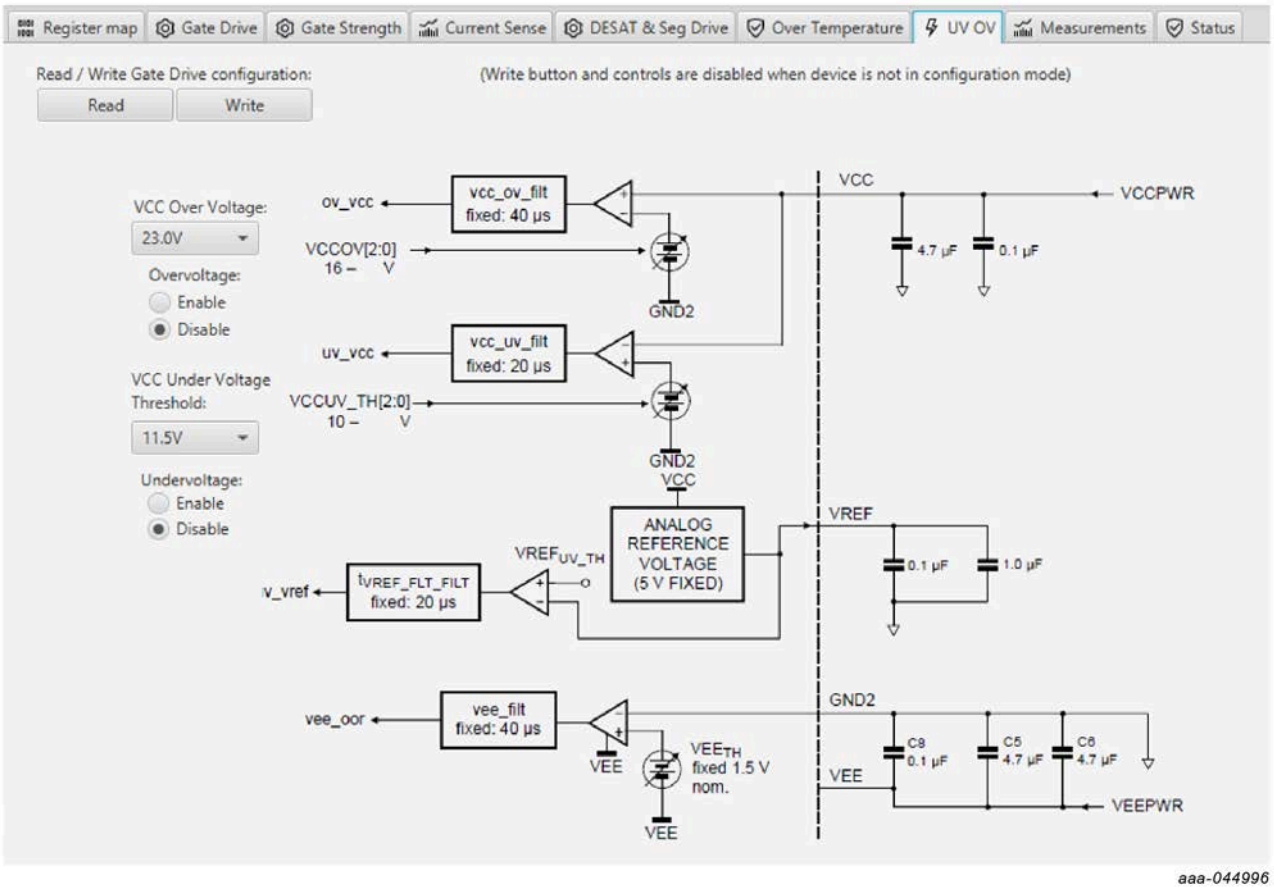


Figure 31. Undervoltage and overvoltage threshold tab

Measurements tab

- Allows monitoring and graphing of ADC and temperature values

Figure 32. Measurements tab

Status tab

- Allows monitoring of Status 1, Status 2, and Status 3 register values
- Status 1 and Status 2 faults can be cleared
- Status mask registers can be modified when in configuration mode
- Red indicates, that a fault has been latched

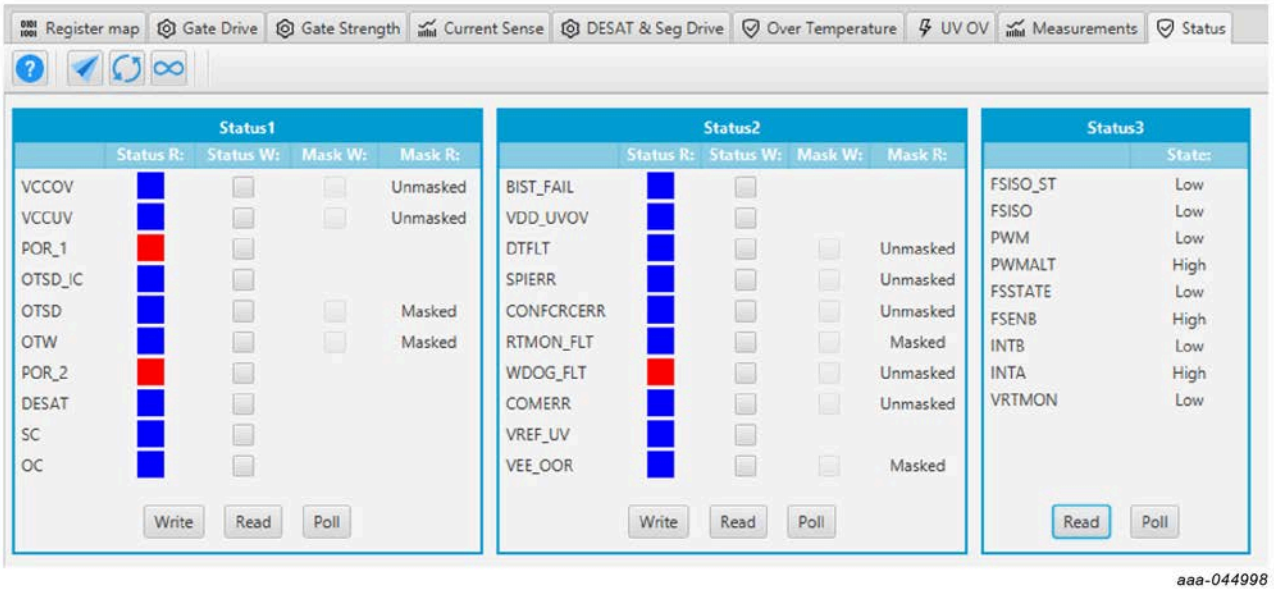


Figure 33. Status tab

Pulse tab

- Used for double pulse, short circuit, and PWM testing
- Select desired T1, T2, and T3 timings for each test type; select enable then generate pulses

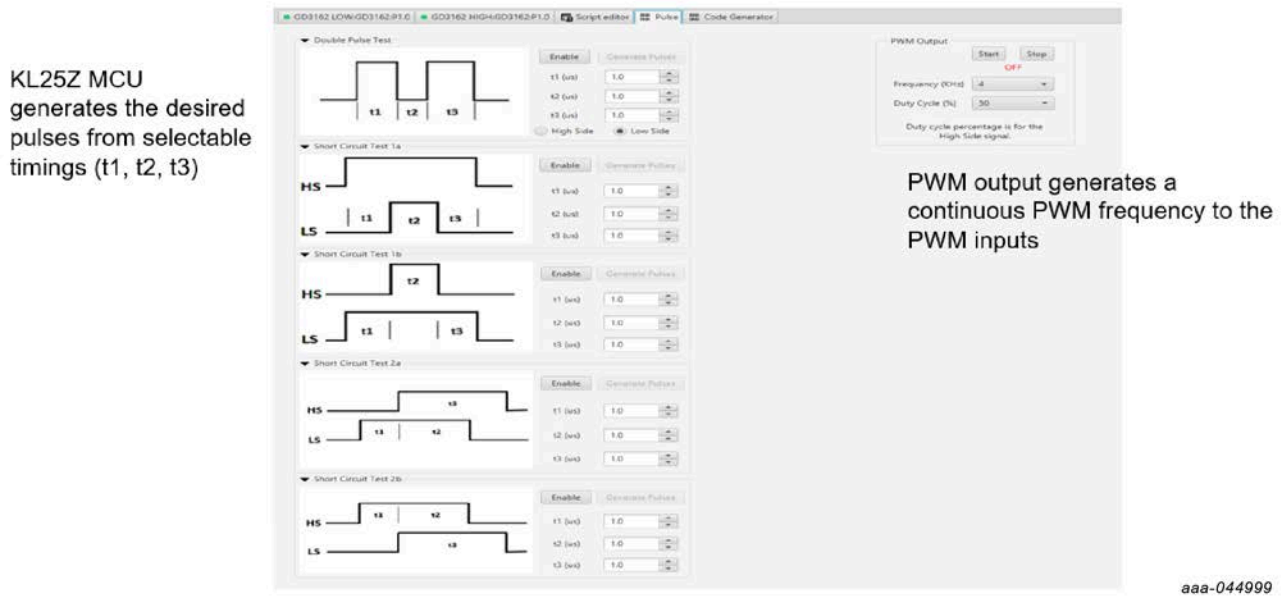


Figure 34. Pulse tab

6.4 Troubleshooting

Some common issues and troubleshooting procedures are detailed below. This is not an exhaustive list by any means, and additional debug may be needed:

Problem	Evaluation	Explanation	Corrective action(s)
No PWM output (no fault reported)	Check PWM jumper position on translator board	Incorrect PWM jumpers obstruct signal path but not report fault	Set PWMH_SEL (J4) and PWML_SEL (J5) jumpers properly, for desired control method: • 3.3 V to 5.0 V translator board reviewed in Section 4.6
	Check PWM control signal	Ensure that proper PWM signal is reaching GD3162	Monitor PWML (TP11) and PWMH (TP10) on translator board for commanded PWM state. Check position of jumpers J4 and J5 on translator board.
	Check FSENB status (see GD3162 pin 15, STATUS3)	PWM is disabled when FSENB = LOW	Set pin FSENB = HIGH (pin 15) to continue
	Check CONFIG_EN bit (MODE2)	PWM is disabled when CONFIG_EN is logic 1	Write CONFIG_EN = logic 0 to continue

Problem	Evaluation	Explanation	Corrective action(s)
No PWM output (fault reported)	Check VGE fault (VGE_FLT)	A short on IGBT or SiC module gate, or too low of VGEMON delay setting causes VGE fault, locking out PWM control of the gate.	Clear VGE_FLT bit (STATUS2) to continue. Increase VGEMON delay setting (CONFIG6). If safe operating condition can be guaranteed, set VGE_FLTM (MSK2) bit to logic 0, to mask fault.
	Check for short-circuit fault (SC) in STATUS1 register	SC is a severe fault that disables PWM. SC fault cannot be masked	Clear SC fault to continue. Consider adjusting SC fault settings on GD3162: • Adjust short-circuit threshold setting (CONFIG2) • Adjust short-circuit filter setting (CONFIG2)
PWM output is good, but with persistent fault reported	Check for dead time fault (DTFLT) in STATUS2 register	Dead time is enforced, but fault indicates that PWM controls signals are in violation	Clear DTFLT fault bit (STATUS2). Check PWMHSEL (J10) and PWMLSEL (J14) are configured to bypass dead time faults. Consider adjusting dead time settings on GD3162: • Change mandatory PWM dead time setting (CONFIG5) • Mask dead time fault (MSK2)
	Check for overcurrent (OC) fault in STATUS1 register	OC fault latches, but does not disable PWM. OC fault cannot be masked.	Clear OC fault bit (STATUS1). Adjust OC fault detection settings on GD3162: • Adjust overcurrent threshold setting (CONFIG1) • Adjust overcurrent filter setting (CONFIG1)
PWM or FSSTATE rising edge has longer delay than falling edge	Check translator output voltage versus GD3162 VDD voltage	Low translator output voltage (compared with correct VDD at GD3162) causes the high threshold at the GD3162 pin to be crossed later than commanded	Check translator output voltage selection (J3) is configured to the same level as the GD3162 VDD Check VCCSEL supply or translator outputs on the translator board for excessive loading or supply droop/pulldown
WDOG_FLT reported on startup	Check VSUP and VCC are powered	On initialization, watchdog fault is reported when one die is powered up before the other	Check VSUP and VCC both have power applied. Clear WDOG_FLT bit (STATUS2) to continue.
SPIERR reported on startup	Check KL25Z/translator connection	On initialization, SPIERR can occur when the SPI bus is open, or when GD3162 IC is powered up before the translator (which provides CSB).	Clear SPIERR fault to continue. Reinitialize power to GD3162 after translator is powered (over USB).
SPIERR reported after SPI message	Check bit length of message sent	There is SPIERR if SCLK does not see a n*24 multiple of cycles	Use 24-bit message length for SPI messages
	Check CRC	SPIERR faults if CRC provided in sent message is not good	Use FlexGUI to generate commands with valid CRC. The command can be copied in binary or hexadecimal and sent from another program.
	Check for sufficient dead time between SPI messages	SPIERR fault bit is set when the time between SPI messages (txfer_delay) received is too short. Minimum required delay time is 19 µs.	Check time between CSB rising edge (old message end) and CSB falling edge (new message start) during normal SPI read, and ensure transfer delay dead time check. SPIERR can also be cleared in BIST.
VCCREGUV reported on startup	Check VCCREG potential	Caused by low VCC	Clear VCCREGUV fault bit (STATUS1). Tune VCC-GNDISO potential with power supply set resistor (R37).

Problem	Evaluation	Explanation	Corrective action(s)
VREFUV reported on startup	Check HV domain is powered correctly	Related to slow rise time of VCC supply on HV domain, or failed VREF regulator	Clear VREFUV bit (STATUS2). Reset HV domain supply if fault bit does not clear.
	Check VCC for undervoltage condition	Low VCC is visible indirectly through other HV domain faults	Tune VCC-GNDISO using R37 feedback
VCCOV fault reported on startup	Check VEE level on suspect domain.	If VEE level is not at desired negative voltage it could cause excessive VCC level.	Check Zener diode in power supply circuit for proper value in setting VEE level. Clear VCCOV bit (STATUS1) to continue.
	Check VCC-GNDISO potential	PWM is disabled during a VCC overvoltage (20 V nom.)	Tune VCC-GNDISO potential to suitable level with power supply set resistor (R37). Clear VCCOV bit (STATUS1) to continue.
No PWM during short circuit test	Check PWMxSEL jumpers	Incorrect configuration of PWMALT pins prevent short-circuit test by enforcing dead time	For short-circuit test, set PWMLSEL (J14) and PWMHSEL (J10) to bypass dead time. See Section 4.4.3 for details.
Bad SPI data, appears to repeat previous response	Check VSUP/VDD for undervoltage condition	VDD_UV latches SPI buffer contents, preventing updated fault reporting.	Check voltage provided at VDD pin (pin 3). On each read, compare the address from the sent command and response (a difference indicates that the SPI response is latched due to inactive). Read multiple addresses to ensure a good comparison.
	Check PS_EN is set to HIGH in FlexGUI; see Figure 22	VCC/VEE can be enabled/disabled in software.	Enable VCC/VEE from FlexGUI. See Section 4.4.3 for details.
	Check VCC for undervoltage	Unpowered VCC prevents HV domain from updating data	Tune VCC-GNDISO using R37 feedback

7 Schematics, board layout, and bill of materials

The board schematics, board layout, and bill of materials are available at http://www.nxp.com/FRDMGD3162HBIEVM on the Overview tab under Get Started.

8 References

[1] Tool summary page for FRDMGD3162HBIEVM http://www.nxp.com/FRDMGD3162HBIEVM

[2] Product summary page for GD3162 device http://www.nxp.com/GD3162

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Tables

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