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Ultra Small, Low Power, 4 Data Lane, 2:1 Switch for MIPI, SuperSpeed USB, PCIe and DisplayPort

Product Preview

FSA636

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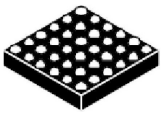


WLCSP36 2.06x2.06x0.432
CASE 567XU

Description

The FSA636 may be configured as a four data lane MIPI D−PHY, V2.1 switch or a three data lane MIPI C−PHY, V1.2 switch. This single pole, double throw (SPDT) switch is optimized for switching between both high speed and low power MIPI sources. The FSA636 is designed for the MIPI specification and allows connection to a CSI or DSI module. It may also be used for any high speed switching application with amplitudes of 2 V or less and is capable of a total data throughput of up to 23.9 Gbps.

Features

- Switch Type: SPDT (10x)
- Signal Type:
  - MIPI D−PHY V2.1
  - MIPI C−PHY V1.2
  - SuperSpeed USB
  - PCIe 2.0
  - DisplayPort HBR
- Input Signal: 0 V to 2 V
- V_{CC}: 1.5 to 5.0 V
- R_{ON}: 6 Ω Typical HS/LP MIPI
- ΔR_{ON}: 0.1 Ω Typical
- R_{ON_FLAT}: 0.9 Ω Typical
- I_{CCZ}: 1.0 μA Maximum
- I_{CC}: 30 μA Maximum
- O_{IRR}: −24 dB Typical
- Bandwidth: 4 GHz Typical
- Xtalk: −30 dB Typical
- C_{ON}: 1.5 pF Typical
- Skew: 6 ps Typical

Applications

- Cellular Phones, Smart Phones
- Cameras
- Tablets
- Laptops
- Displays

This document contains information on a product under development. ON Semiconductor reserves the right to change or discontinue this product without notice.

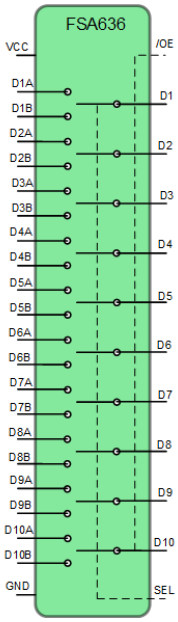
MARKING DIAGRAMS

VR	= Specific Device Code
KK	= Assembly Lot
X	= Year
Y	= Work Week
Z	= Assembly Location

ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

PIN DESCRIPTIONS



PIN NAME	DESCRIPTION		
Dn	Common Data Path		
DnA	Data Path A		
DnB	Data Path B		
/OE	Output Enable		
SEL	Control Pin	SEL=0	Dn = DnA
		SEL=1	Dn = DnB
VCC	Power		
GND	Ground		

Figure 1. Analog Symbol

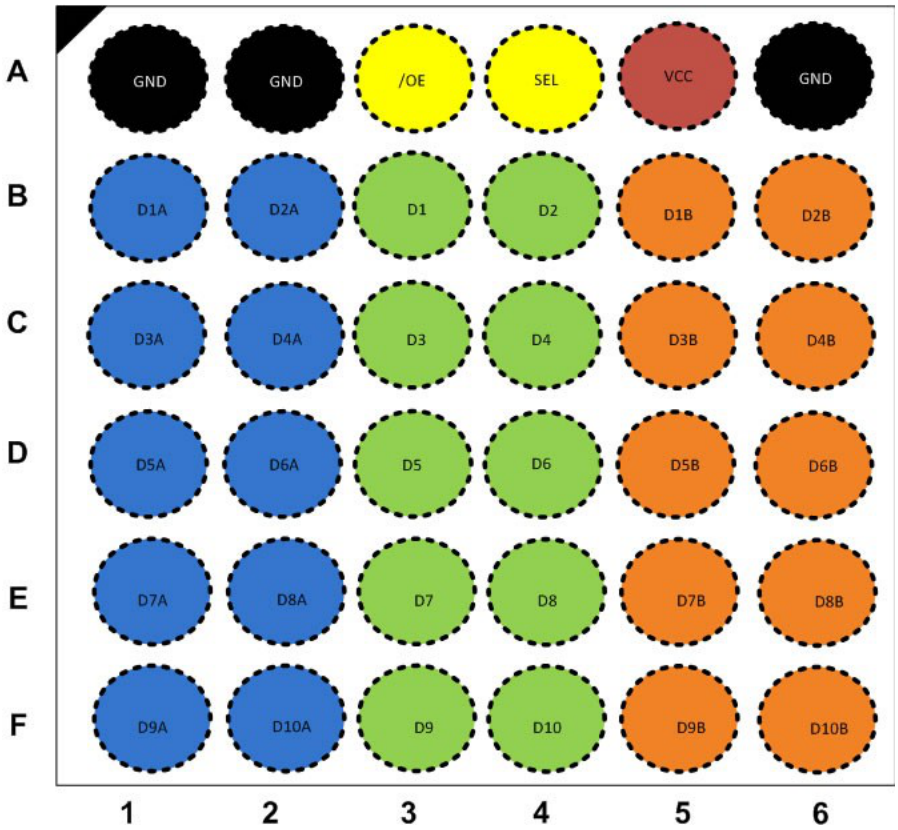


Figure 2. Top Through View

BALL−TO−PIN MAPPINGS

Ball	Pin Name	Ball	Pin Name	Ball	Pin Name
A1	GND	C1	D3A	E1	D7A
A2	GND	C2	D4A	E2	D8A
A3	/OE	C3	D3	E3	D7
A4	SEL	C4	D4	E4	D8
A5	VCC	C5	D3B	E5	D7B
A6	GND	C6	D4B	E6	D8B
B1	D1A	D1	D5A	F1	D9A
B2	D2A	D2	D6A	F2	D10A
B3	D1	D3	D5	F3	D9
B4	D2	D4	D6	F4	D10
B5	D1B	D5	D5B	F5	D9B
B6	D2B	D6	D6B	F6	D10B

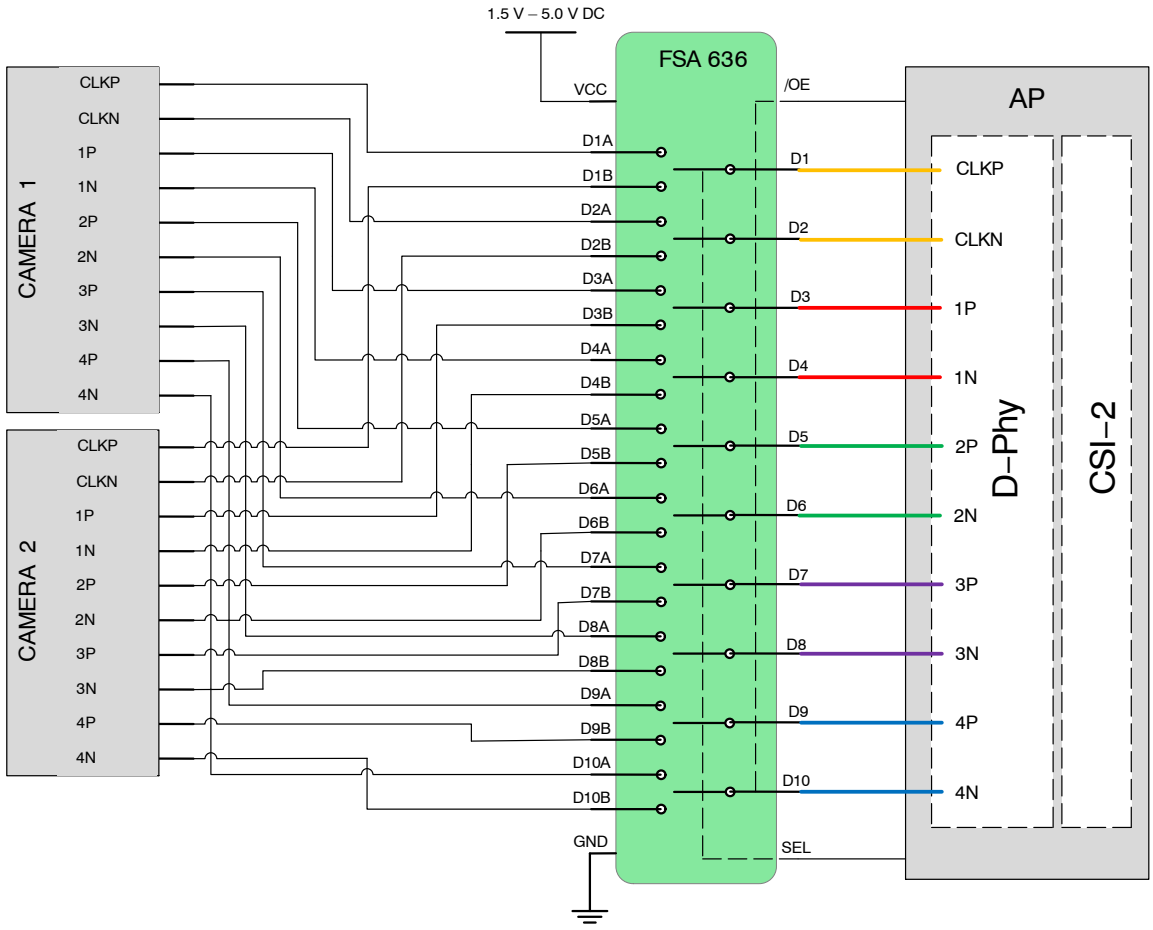


Figure 3. Suggested Configuration for 4 Lane D−PHY

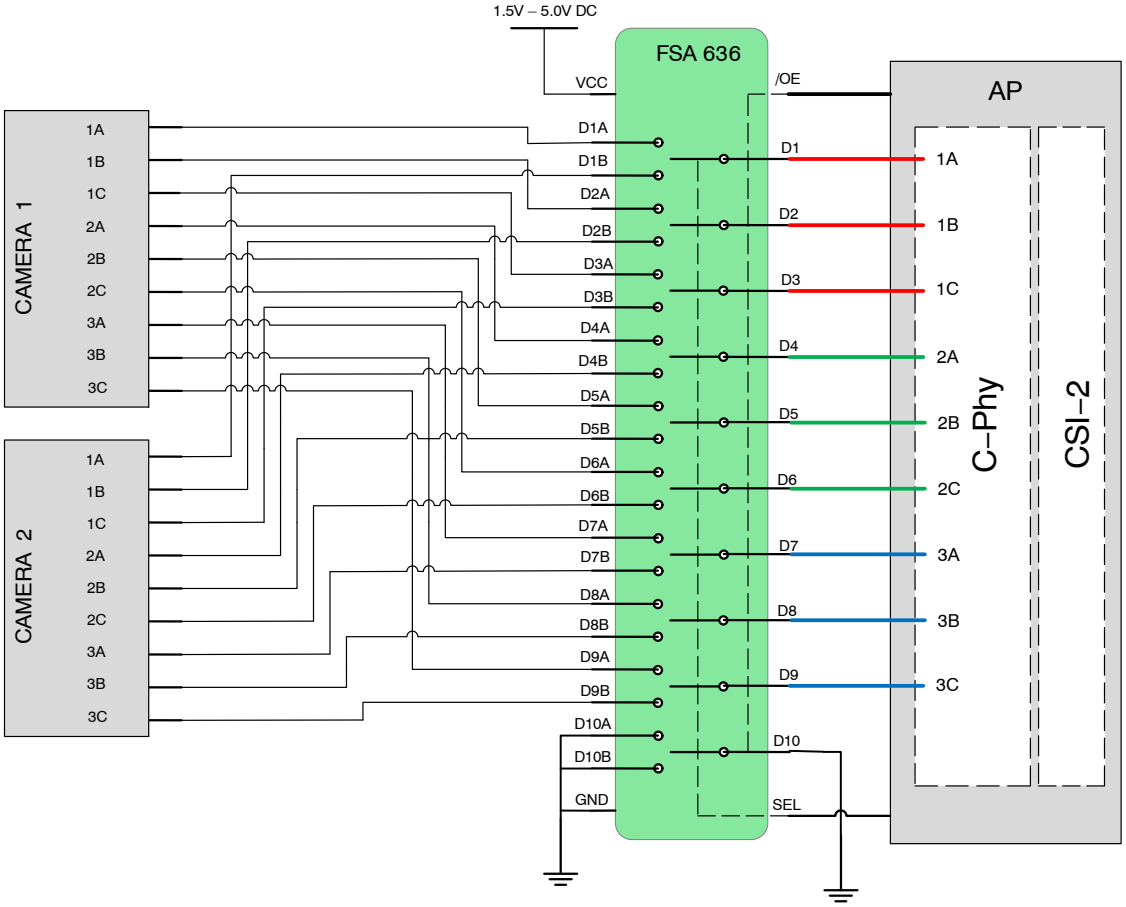


Figure 4. Suggested Configuration for 3 Lane C−PHY

TRUTH TABLE

SEL	/OE	Function
LOW	LOW	Dn = DnA
HIGH	LOW	Dn = DnB
X	HIGH	All Ports High Impedance

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		−0.5	6.0	V
V_{CNTRL}	DC Input Voltage (/OE, SEL) (Note 1)		−0.5	V_{CC}	V
V_{SW}	DC Switch I/O Voltage (Note 1, 2)		−0.3	2.1	V
I_{IK}	DC Input Diode Current		−50		mA
I_{OUT}	DC Output Current			25	mA
T_{STG}	Storage Temperature		−65	+150	°C
ESD	Human Body Model, JEDEC: JESD22−A114	All Pins	2.0		kV
	Charged Device Model, JEDEC: JESD22−C101		0.5		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. The input and output negative ratings may be exceeded if the input and output diode current ratings are observed.
2. V_{SW} refers to analog data switch paths.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	Supply Voltage		1.5	5.0	V
V_{CNTRL}	Control Input Voltage (SEL, /OE) (Note 3)		0	V_{CC}	V
V_{SW}	Switch I/O Voltage (Dn, DAn, DBn)	HS Mode	0	0.425	V
		LP Mode	−0.05	2.0	V
T_A	Operating Temperature		−40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. The control inputs must be held HIGH or LOW; they must not float.

ELECTRICAL SPECIFICATION TABLE Typical values are at T_A = 25°C, V_{CC} = 3.3 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
DC ELECTRICAL PARAMETERS						
VIK	Clamp Diode Voltage (/OE, SEL)	IIN = −18 mA, VCC = 1.5 V	−1.2		−0.6	V
VIH	Input Voltage High (/OE, SEL)	VCC = 1.5 V to 5.0 V	1.3			V
VIL	Input Voltage Low (/OE, SEL)	VCC = 1.5 V to 5.0 V			0.5	V
IIN	Control Input Leakage (SEL, /OE)	VCNTRL = 0 to VCC	−0.5		0.5	μA
INO(OFF), INC(OFF)	Off Leakage Current of Port Dn, DnA, DnB	VSW = 0.0 ⇐ DATA ⇐ 2.0 V, VCC = 5 V	−0.5		0.5	μA
IA(ON)	On Leakage Current of Common Ports (Dn)	VSW = 0.0 ⇐ DATA ⇐ 2.0 V, VCC = 5 V	−0.5		0.5	μA
IOFF	Power−Off Leakage Current	VSW = 0 V or 2.0 V; VCC = 0 V	−0.5		0.5	μA
IOZ	Off−State Leakage	VSW = 0.0 ⇐ DATA ⇐ 2.0 V, /OE = High, VCC = 5 V	−0.5		0.5	μA
RON_MIPI_HS	Switch On Resistance for HS MIPI Applications	ION = −8 mA, /OE = 0 V, SEL = VCC or 0 V, DnA or DnB = 0.2 V, VCC = 1.5 V to 5.0 V		6	9	Ω
RON_MIPI_LP	Switch On Resistance for LP MIPI Applications	ION = −8 mA, /OE = 0 V, SEL = VCC or 0 V, DnA or DnB = 1.2 V, VCC = 1.5 V to 5.0 V		6	9	Ω
ΔRON_MIPI_HS	On Resistance Matching Between HS MIPI Channels (Note 4)	ION = −8 mA, /OE = 0 V, SEL = VCC or 0 V, DnA or DnB = 0.2 V, VCC = 1.5 V to 5.0 V		0.1	0.25	Ω
ΔRON_MIPI_LP	On Resistance Matching Between LP MIPI Channels (Note 4)	ION = −8 mA, /OE = 0 V, SEL = VCC or 0 V, DnA or DnB = 1.2 V, VCC = 1.5 V to 5.0 V		0.1	0.25	Ω
RON_FLAT_MIPI_HS	On Resistance Flatness for HS MIPI Signals (Note 4)	ION = −8 mA, /OE = 0 V, SEL = VCC or 0 V, DnA or DnB = 0 V to 0.3 V, VCC = 1.5 V to 5.0 V		0.9		Ω
RON_FLAT_MIPI_LP	On Resistance Flatness for LP MIPI Signals (Note 4)	ION = −8 mA, /OE = 0 V, SEL = VCC or 0 V, DnA or DnB = 0V to 1.2 V, VCC = 1.5 V to 5.0 V		0.9		Ω
ICCZ	Quiescent Hi−Z Supply Current	VIN = 0 V or VCC, VSEL = 0 V or VCC, IOUT = 0 A, VCC = 5.0 V, /OE = 5.0 V			1	μA
ICC	Quiescent Supply Current	VIN = 0 or VCC, IOUT= 0 A, VCC = 5.0 V, /OE = 0 V			30	μA
ICCT	Increase in ICC Current Per Control Voltage and VCC	VSEL = 1.5 V, /OE = 5.0 V, VCC = 5.0 V		1	4	μA

ELECTRICAL SPECIFICATION TABLE Typical values are at T_A = 25°C, V_{CC} = 3.3 V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
AC ELECTRICAL PARAMETERS						
tINIT	Initialization Time VCC to Output (Note 4)	RL = 50 Ω, CL = 0 pF, VSW = 0.6 V		60	150	μs
tEN	Enable Turn−On Time, /OE to Output	RL = 50 Ω, CL = 0 pF, VSW = 0.6 V		60	150	μs
tDIS	Disable Turn−Off Time, /OE to Output	RL = 50 Ω, CL =0 pF, VSW = 0.6 V		25	250	ns
tON	Turn−On Time, SEL to Output	RL = 50 Ω, CL = 0 pF, VSW = 0.6 V, SEL H to L, SEL L to H		350	1100	ns
tOFF	Turn−Off Time SEL to Output	RL = 50 Ω, CL = 0 pF, VSW = 0.6 V, SEL H to L, SEL L to H		125	1100	ns
tBBM	Break−Before−Make Time (Note 4)	RL = 50 Ω, CL = 0 pF, VSW = 0.6 V, 50%DnA/B to 50%DnB/A		150		ns
tPD	Propagation Delay (Note 4)	RL = 50 Ω, CL = 0 pF		TBD		ps
OIRR	Off Isolation for MIPI (Note 4)	RL = 50 Ω, f = 2250 MHz, /OE = VCC, VSW = 200 mVpp		−24		dB
XTALK	Crosstalk for MIPI (Note 4)	RL = 50 Ω, f = 2250 MHz, VSW = 200 mVpp, SEL = H & L		−30		dB
BW	Bandwidth at −3dB (Note 4)	RL = 50 Ω, CL = 0 pF, VSW = 200 mVpp		4.0		GHz
IL	Insertion Loss at 750 MHz (Note 4)	RL = 50 Ω, CL = 0 pF, VSW = 200 mVpp		−0.7		dB
tSK(O)	Channel−to−Channel Single−Ended Skew (Note 4)	RL = 50 Ω, CL = 0 pF, VSW = 0.3 V		6		ps
tSK(P)	Skew of Opposite Transitions of the Same Output (Note 4)	RL = 50 Ω, CL = 0 pF, VSW = 0.3 V		6		ps
CAPACITANCE						
CIN	Control Pin Input Capacitance (Note 5)	VCC = 0 V, f = 1 MHz		2.1		pF
CON	On Capacitance (Note 5)	VCC = 3.3 V, /OE = 0 V, f = 2250 MHz		1.5		pF
COFF	Off Capacitance (Note 5)	VCC and /OE = 3.3 V, f = 2250 MHz		0.9		pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES: Guarantee Levels:

4. Guaranteed by Design. Characterized on the ATE or Bench.
5. Guaranteed by Design and Characterization, not Production Tested

The table below pertains to the Packaging information on the following page

ORDERING INFORMATION

Part Number	Operating Temperature Range	Package	Top Mark
FSA636UCX	−40 to +85°C	36−Ball WLCSP, Non−JEDEC 2.06 x 2.06 mm, 0.35 mm Pitch	VR