Green Mode Power Switch for Valley Switching Converter - Low EMI and High Efficiency

FSQ0365, FSQ0265, FSQ0165, FSQ321

Description

A Valley Switching Converter generally shows lower EMI and higher power conversion efficiency than a conventional hard−switched converter with a fixed switching frequency. The FSQ−series is an integrated Pulse−Width Modulation (PWM) controller and SENSEFET® specifically designed for valley switching operation with minimal external components. The PWM controller includes an integrated fixed−frequency oscillator, under−voltage lockout, Leading−Edge Blanking (LEB), optimized gate driver, internal soft−start, temperature−compensated precise current sources for loop compensation, and self−protection circuitry.

Compared with discrete MOSFET and PWM controller solutions, the FSQ−series reduces total cost, component count, size and weight; while simultaneously increasing efficiency, productivity, and system reliability. This device provides a basic platform for cost−effective designs of valley switching fly−back converters.

Features

- Optimized for Valley Switching Converter (VSC)
- Low EMI through Variable Frequency Control and Inherent Frequency Modulation
- High Efficiency through Minimum Voltage Switching
- Narrow Frequency Variation Range Over Wide Load and Input Voltage Variation
- Advanced Burst−Mode Operation for Low Standby Power Consumption
- Pulse−by−Pulse Current Limit
- Protection Functions: Overload Protection (OLP), Over−Voltage Protection (OVP), Abnormal Over−Current Protection (AOCP), Internal Thermal Shutdown (TSD)
- Under−Voltage Lockout (UVLO) with Hysteresis
- Internal Startup Circuit
- Internal High−Voltage SENSEFET: 650 V
- Built−in Soft−Start: 15 ms

Related Application Notes

- http://www.onsemi.com/pub/Collateral/AN−4137.pdf.pdf
- http://www.onsemi.com/pub/Collateral/AN−4141.pdf.pdf
- http://www.onsemi.com/pub/Collateral/AN−4150.pdf.pdf
- https://www.onsemi.com/pub/Collateral/AN−4134.PDF

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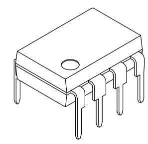
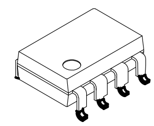
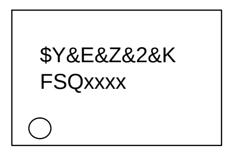


PDIP−8
CASE 626−05



PDIP8 GW
CASE 709AJ

MARKING DIAGRAM



$Y	= ON Semiconductor Logo
&E	= Designated Space
&Z	= Assembly Plant Code
&2	= 2−Digit Date code format
&K	= 2−Digits Lot Run Traceability Code
FSQxxxx	= Specific Device Code Data

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Applications

- Power Supplies for DVD Player, DVD Recorder, Set−Top Box
- Adapter
- Auxiliary Power Supply for PC, LCD TV, and PDP TV

December, 2020 − Rev. 3
Publication Order Number:
FSQ0365/D

Table 1. ORDERING INFORMATION

Part Number	Package	Shipping†	Operating Temperature	Current Limit	$R_{DS(ON)}$ (Max.)	Maximum Output Table[1]			
						230 V_{AC} ±15%[2]		85 − 265 V_{AC}	
						Adapter[3]	Open Frame[4]	Adapter[3]	Open Frame[4]
FSQ321	PDIP−8	3000 / Tube	−40 to +85°C	0.6 A	19 Ω	8W	12W	7W	10W
FSQ321LX	PDIP8 GW	1000 / Tape & Reel							
FSQ0165RN	PDIP−8	3000 / Tube	−40 to +85°C	0.9 A	10 Ω	10W	15W	9W	13W
FSQ0165RLX	PDIP8 GW	1000 / Tape & Reel							
FSQ0265RN	PDIP−8	3000 / Tube	−40 to +85°C	1.2 A	6 Ω	14W	20W	11W	16W
FSQ0265RLX	PDIP8 GW	1000 / Tape & Reel							
FSQ0365RN	PDIP−8	3000 / Tube	−40 to +85°C	1.5 A	4.5 Ω	17.5W	25W	13W	19W
FSQ0365RLX	PDIP8 GW	1000 / Tape & Reel							

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
1. The junction temperature can limit the maximum output power.
2. 230 V_{AC} or 100/115 V_{AC} with voltage doubler. The maximum power with CCM operation.
3. Typical continuous power in a non−ventilated, enclosed adapter measured at 50°C ambient temperature.
4. Maximum practical continuous power in an open−frame design at 50°C ambient temperature.

Application Circuit

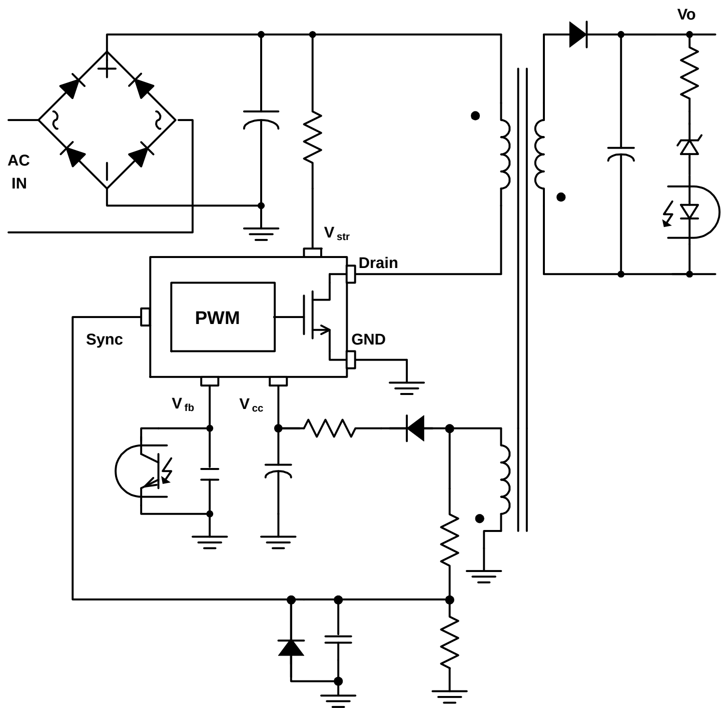


Figure 1. Typical Flyback Application

Internal Block Diagram

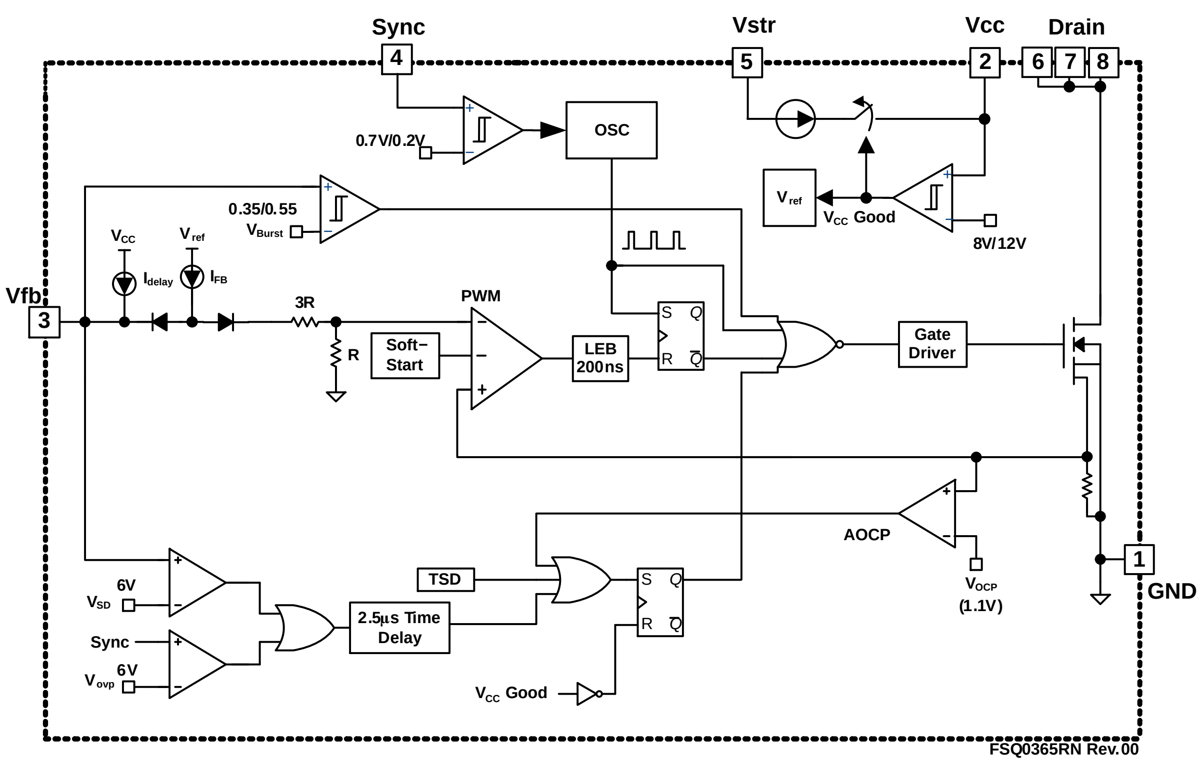


Figure 2. Internal Block Diagram

Pin Assignments

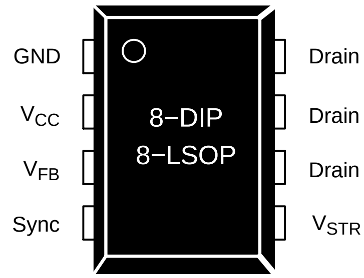


Figure 3. Pin Configuration (Top View)

Table 2. PIN DEFINITIONS

Pin#	Name	Description
1	GND	SENSEFET source terminal on primary side and internal control ground.
2	V_{CC}	Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during startup (see Figure 2). It is not until V_{CC} reaches the UVLO upper threshold (12 V) that the internal startup switch opens and device power is supplied via the auxiliary transformer winding.
3	Vfb	The feedback voltage pin is the non−inverting input to the PWM comparator. It has a 0.9 mA current source connected internally while a capacitor and opto-coupler are typically connected externally. There is a time delay while charging external capacitor C_{fb} from 3 V to 6 V using an internal 5 μA current source. This delay prevents false triggering under transient conditions, but still allows the protection mechanism to operate under true overload conditions.
4	Sync	This pin is internally connected to the sync−detect comparator for valley switching. Typically the voltage of the auxiliary winding is used as Sync input voltage and external resistors and capacitor are needed to make delay to match valley point. The threshold of the internal sync comparator is 0.7 V / 0.2 V.
5	Vstr	This pin is connected to the rectified AC line voltage source. At startup, the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the V_{CC} reaches 12 V, the internal switch is opened.
6, 7, 8	Drain	The drain pins are designed to connect directly to the primary lead of the transformer and are capable of switching a maximum of 650 V. Minimizing the length of the trace connecting these pins to the transformer decreases leakage inductance.

Table 3. ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise specified)

Symbol	Parameter		Min.	Max.	Unit
V_{STR}	Vstr Pin Voltage		500		V
V_{DS}	Drain Pin Voltage		650		V
V_{CC}	Supply Voltage			20	V
V_{FB}	Feedback Voltage Range		−0.3	9.0	V
V_{Sync}	Sync Pin Voltage		−0.3	9.0	V
I_{DM}	Drain Current Pulsed (Note 5)	FSQ0365		12.0	A
		FSQ0265		8.0	
		FSQ0165		4.0	
		FSQ321		1.5	
E_{AS}	Single Pulsed Avalanche Energy (Note 6)	FSQ0365		230	mJ
		FSQ0265		140	
		FSQ0165		50	
		FSQ321		10	
P_D	Total Power Dissipation			1.5	W
T_J	Recommended Operating Junction Temperature		−40	Internally Limited	°C
T_A	Operating Ambient Temperature		−40	+85	°C
T_{STG}	Storage Temperature		−55	+150	°C
ESD	Human Body Model; JESD22−A114		CLASS 1C		
	Machine Model; JESD22−A115		CLASS B		

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

5. Repetitive rating: pulse width limited by maximum junction temperature.
6. L = 51 mH, starting T_J = 25°C.

Table 4. THERMAL IMPEDANCE

Symbol	Parameter	Value	Unit
8−DIP (Note 7)			
θ_{JA}	Junction−to−Ambient Thermal Resistance (Note 8)	80	°C/W
θ_{JC}	Junction−to−Case Thermal Resistance (Note 9)	20	
θ_{JT}	Junction−to−Top Thermal Resistance (Note 10)	35	

7. All items are tested with the standards JESD 51−2 and 51−10 (DIP)
8. Free−standing with no heat−sink, under natural convection
9. Infinite cooling condition − refer to the SEMI G30−88
10. Measured on the package top surface.

Table 5. ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Symbol	Parameter		Condition	Min.	Typ.	Max.	Unit
SENSEFET Section							
BV_{DSS}	Drain−Source Breakdown Voltage		V_{CC} = 0 V, I_D = 100 μA	650			V
I_{DSS}	Zero−Gate−Voltage Drain Current		V_{DS} = 650 V			100	A
$R_{DS(ON)}$	Drain−Source On−State Resistance (Note 11)	FSQ0365	T_J = 25°C, I_D = 0.5 A		3.5	4.5	Ω
		FSQ0265			5.0	6.0	
		FSQ0165			8.0	10.0	
		FSQ321			14.0	19.0	
C_{ISS}	Input Capacitance	FSQ0365	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		315		pF
		FSQ0265			550		
		FSQ0165			250		
		FSQ321			162		
C_{OSS}	Output Capacitance	FSQ0365	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		47		pF
		FSQ0265			38		
		FSQ0165			25		
		FSQ321			18		
C_{RSS}	Reverse Transfer Capacitance	FSQ0365	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		9.0		pF
		FSQ0265			17.0		
		FSQ0165			10.0		
		FSQ321			3.8		
$t_{d(on)}$	Turn−On Delay	FSQ0365	V_{DD} = 350 V, I_D = 25 mA		11.2		ns
		FSQ0265			20.0		
		FSQ0165			12.0		
		FSQ321			9.5		
t_r	Rise Time	FSQ0365	V_{DD} = 350 V, I_D = 25 mA		34		ns
		FSQ0265			15		
		FSQ0165			4		
		FSQ321			19		
$t_{d(off)}$	Turn−Off Delay	FSQ0365	V_{DD} = 350 V, I_D = 25 mA		28.2		ns
		FSQ0265			55.0		
		FSQ0165			30.0		
		FSQ321			33.0		
t_f	Fall Time	FSQ0365	V_{DD} = 350 V, I_D = 25 mA		32		ns
		FSQ0265			25		
		FSQ0165			10		
		FSQ321			42		
Burst−Mode Section							
V_{BURH}	Burst−Mode Voltage		T_J = 25°C, t_{PD} = 200 ns (Note 12)	0.45	0.55	0.65	V
V_{BURL}				0.25	0.35	0.45	V
$V_{BUR(HYS)}$					200		mV

Table 5. ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (continued)

Symbol	Parameter		Conditions	Min.	Typ.	Max.	Unit
Control Section							
$t_{ON.MAX1}$	Maximum On Time1	All but FSQ321	T_J = 25°C	10.5	12.0	13.5	μs
$t_{ON.MAX2}$	Maximum On Time2	FSQ321	T_J = 25°C	6.35	7.06	7.77	μs
t_{B1}	Blanking Time1	All but FSQ321		13.2	15.0	16.8	μs
t_{B2}	Blanking Time2	FSQ321		7.5	8.2		μs
t_W	Detection Time Window		T_J = 25°C, V_{sync} = 0 V		3.0		μs
Δf_S	Switching Frequency Variation (Note 14)		−25°C < T_J < 85°C		±5	±10	%
I_{FB}	Feedback Source Current		V_{FB} = 0 V	700	900	1100	μA
D_{MIN}	Minimum Duty Cycle		V_{FB} = 0 V			0	%
V_{START}	UVLO Threshold Voltage		After Turn−on	11	12	13	V
V_{STOP}				7	8	9	V
$t_{S/S1}$	Internal Soft−Start Time 1	All but FSQ321	With Free−Running Frequency		15		ms
$t_{S/S2}$	Internal Soft−Start Time 2	FSQ321	With Free−Running Frequency		10		ms
Protection Section							
I_{LIM}	Peak Current Limit	FSQ0365	T_J = 25°C, di/dt = 240 mA/μs	1.32	1.50	1.68	A
		FSQ0265	T_J = 25°C, di/dt = 200 mA/μs	1.06	1.20	1.34	
		FSQ0165	T_J = 25°C, di/dt = 175 mA/μs	0.8	0.9	1.0	
		FSQ321	T_J = 25°C, di/dt = 125 mA/μs	0.53	0.60	0.67	
V_{SD}	Shutdown Feedback Voltage		V_{CC} = 15 V	5.5	6.0	6.5	V
I_{DELAY}	Shutdown Delay Current		V_{FB} = 5 V	4.0	5.0	6.0	μA
t_{LEB}	Leading−Edge Blanking Time(13)				200		ns
V_{OVP}	Over−Voltage Protection		V_{CC} = 15 V, V_{FB} = 2 V	5.5	6.0	6.5	V
t_{OVP}	Over−Voltage Protection Blanking Time			2	3	4	μs
T_{SD}	Thermal Shutdown Temperature (Note 13)			125	140	155	°C
Sync Section							
V_{SH}	Sync Threshold Voltage			0.55	0.70	0.85	V
V_{SL}				0.14	0.20	0.26	V
t_{Sync}	Sync Delay Time (Notes 13, 14)				300		ns
Total Device Section							
I_{OP}	Operating Supply Current (Control Part Only)		V_{CC} = 15 V	1	3	5	mA
I_{START}	Start Current		V_{CC} = V_{START} − 0.1 V (Before V_{CC} Reaches V_{START})	270	360	450	μA
I_{CH}	Startup Charging Current		V_{CC} = 0 V, V_{STR} = Minimum 40 V	0.65	0.85	1.00	mA
V_{STR}	Minimum V_{STR} Supply Voltage				26		V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

11. Pulse test: Pulse−Width = 300 μs, duty = 2%
12. Propagation delay in the control IC.
13. Though guaranteed, it is not 100% tested in production.
14. Includes gate turn−on time.

TYPICAL PERFORMANCE CHARACTERISTICS

(Characteristics graphs are normalized at T_A = 25°C)

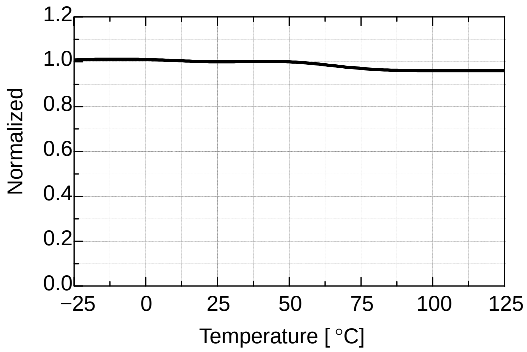


Figure 4. Operating Supply Current (I_{OP}) vs. T_A

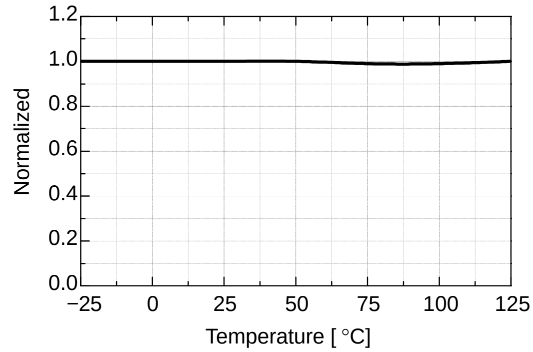


Figure 5. UVLO Start Threshold Voltage (V_{START}) vs. T_A

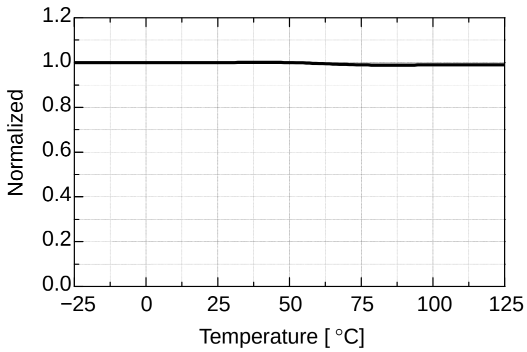


Figure 6. UVLO Stop Threshold Voltage (V_{STOP}) vs. T_A

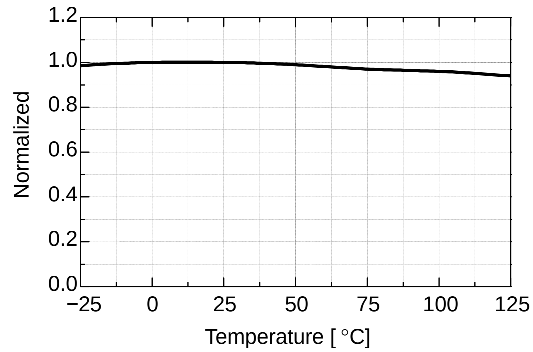


Figure 7. Startup Charging Current (I_{CH}) vs. T_A

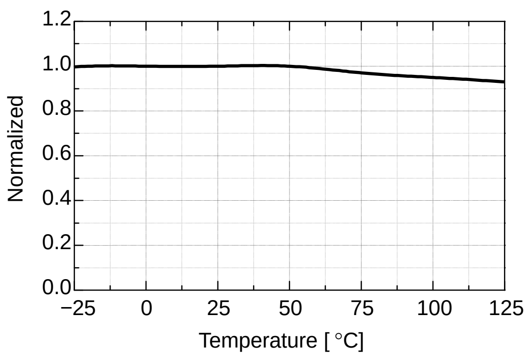


Figure 8. Initial Switching Frequency (f_S) vs. T_A

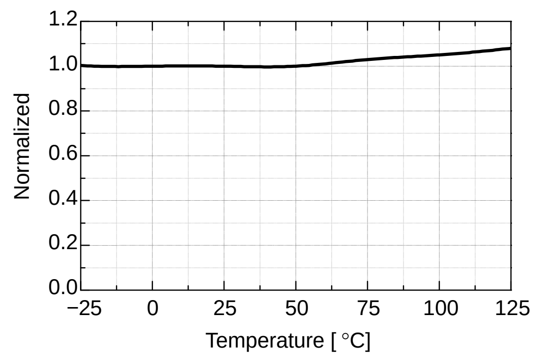


Figure 9. Maximum On Time ($t_{ON.MAX}$) vs. T_A

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Characteristics graphs are normalized at T_A = 25°C)

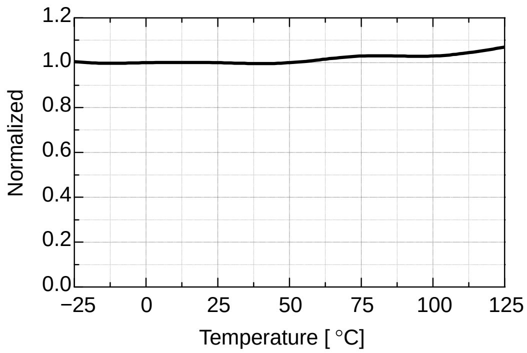


Figure 10. Blanking Time (t_B) vs. T_A

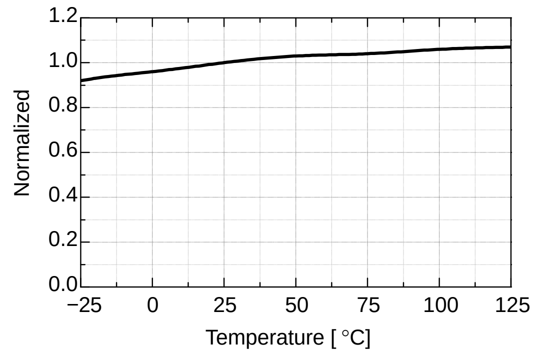


Figure 11. Feedback Source Current (I_{FB}) vs. T_A

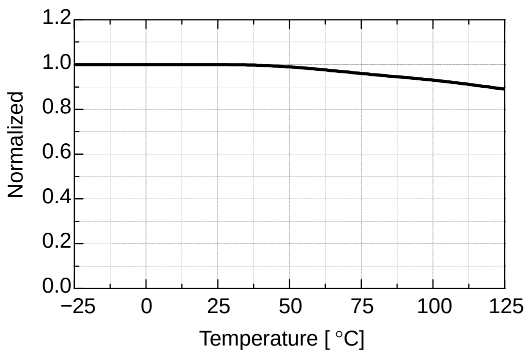


Figure 12. Shutdown Delay Current (I_{DELAY}) vs. T_A

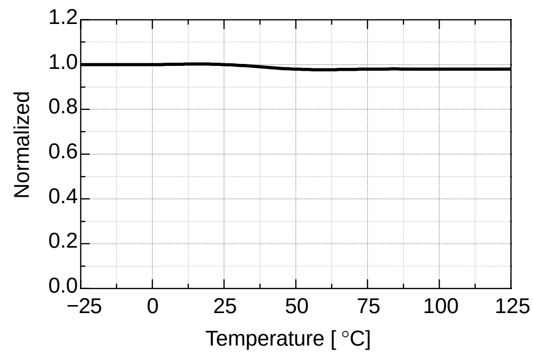


Figure 13. Burst Mode High Threshold Voltage (V_{burh}) vs. T_A

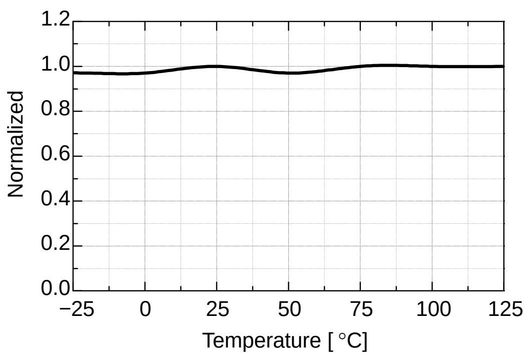


Figure 14. Burst Mode Low Threshold Voltage (V_{burl}) vs. T_A

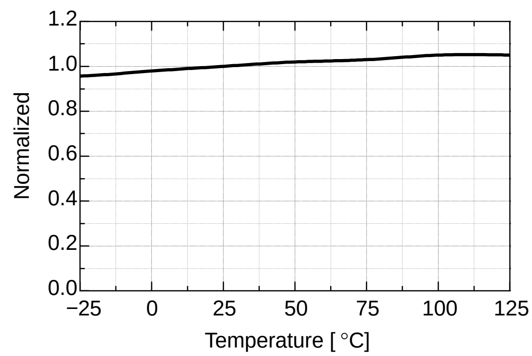


Figure 15. Peak Current Limit (I_{LIM}) vs. T_A

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(Characteristics graphs are normalized at T_A = 25°C)

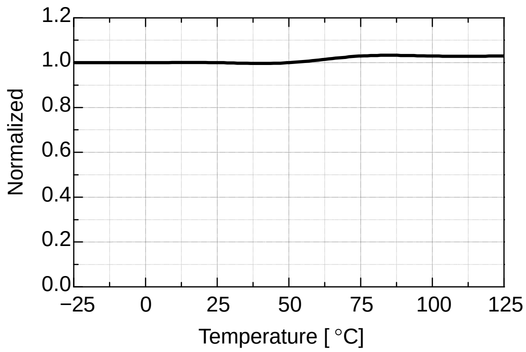


Figure 16. Sync High Threshold (V_{SH}) vs. T_A

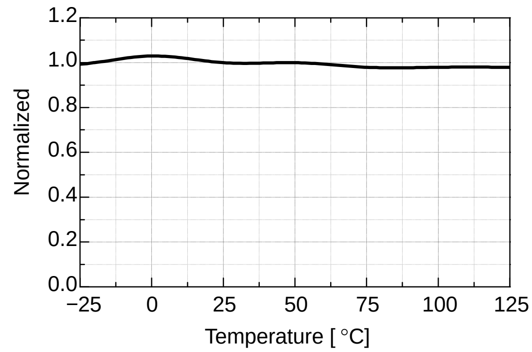


Figure 17. Sync Low Threshold (V_{SL}) vs. T_A

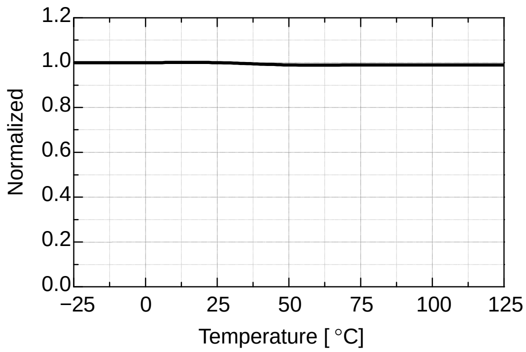


Figure 18. Shutdown Feedback Voltage (V_{SD}) vs. T_A

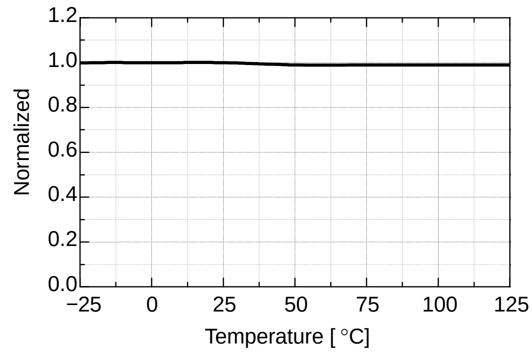


Figure 19. Over−Voltage Protection (V_{OP}) vs. T_A

FUNCTIONAL DESCRIPTION

Startup

At startup, an internal high−voltage current source supplies the internal bias and charges the external capacitor (C_a) connected to the V_{CC} pin, as illustrated in Figure 20. When V_{CC} reaches 12 V, the power switch begins switching and the internal high−voltage current source is disabled. The power switch continues its normal switching operation and the power is supplied from the auxiliary transformer winding unless V_{CC} goes below the stop voltage of 8 V.

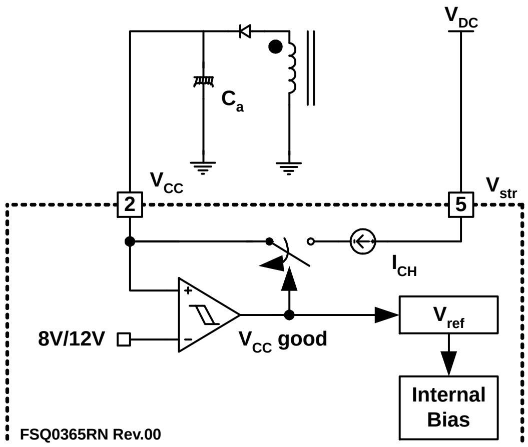


Figure 20. Startup Circuit

Feedback Control

Power Switch employs Current Mode control, as shown in Figure 21. An opto−coupler (such as FOD817A) and shunt regulator (such as KA431) are often used to implement the feedback network. Comparing the feedback voltage with the voltage across the R_{SENSE} resistor makes it possible to control the switching duty cycle. When the reference pin voltage of the shunt regulator exceeds the internal reference voltage of 2.5 V, the opto−coupler LED current increases, pulling down the feedback voltage and reducing the duty cycle. This event typically occurs when input voltage is increased or output load is decreased.

Pulse−by−Pulse Current Limit

Because Current Mode control is employed, the peak current through the SENSEFET is limited by the inverting input of PWM comparator (V_{FB}*), as shown in Figure 21. Assuming that the 0.9mA current source flows only through the internal resistor (3R + R = 2.8 kΩ), the cathode voltage of diode D2 is about 2.5 V. Since D1 is blocked when the feedback voltage (V_{FB}) exceeds 2.5V, the maximum voltage of the cathode of D2 is clamped at this voltage, clamping V_{FB}*. Therefore, the peak value of the current through the SENSEFET is limited.

Leading−Edge Blanking (LEB)

At the instant the internal SENSEFET is turned on, a high−current spike usually occurs through the SENSEFET, caused by primary−side capacitance and secondary−side rectifier reverse recovery. Excessive voltage across the R_{sense} resistor would lead to incorrect feedback operation in the Current Mode PWM control. To counter this effect, the power switch employs a leading−edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (t_{LEB}) after the SENSEFET is turned on.

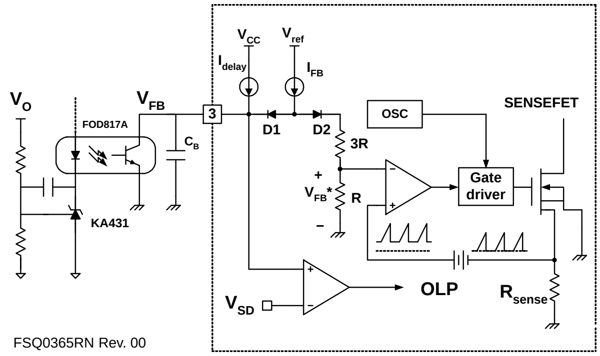


Figure 21. Pulse−Width−Modulation Circuit

Synchronization

The FSQ−series employs a valley switching technique to minimize the switching noise and loss. The basic waveforms of the valley switching converter are shown in Figure 22. To minimize the MOSFET's switching loss, the MOSFET should be turned on when the drain voltage reaches its minimum value, as shown in Figure 22. The minimum drain voltage is indirectly detected by monitoring the V_{CC} winding voltage, as shown in Figure 22.

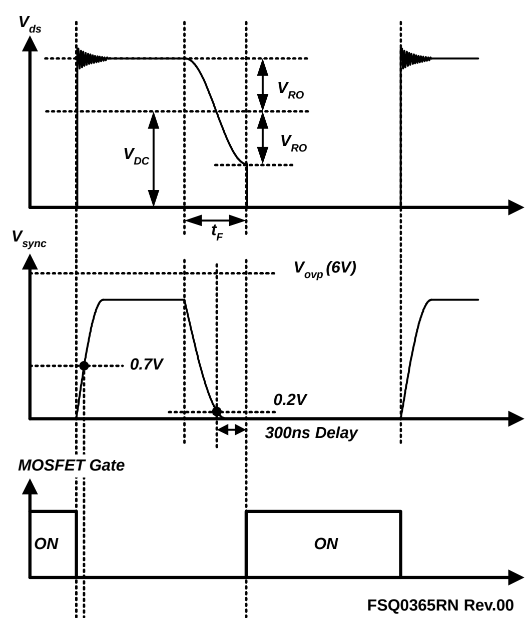


Figure 22. Valley Resonant Switching Waveforms

Protection Circuits

The FSQ−series has several self−protective functions, such as Overload Protection (OLP), Abnormal Over−Current protection (AOCP), Over−Voltage Protection (OVP), and Thermal Shutdown (TSD). All the protections are implemented as Auto−Restart Mode. Once the fault condition is detected, switching is terminated and the SENSEFET remains off. This causes V_{CC} to fall. When V_{CC} falls down to the Under−Voltage Lockout (UVLO) stop voltage of 8 V, the protection is reset and the startup circuit charges the V_{CC} capacitor. When the V_{CC} reaches the start voltage of 12 V, the FSQ−series resumes normal operation. If the fault condition is not removed, the SENSEFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto−restart can alternately enable and disable the switching of the power SENSEFET until the fault condition is eliminated. Because these protection circuits are fully integrated into the IC without external components, the reliability is improved without increasing cost.

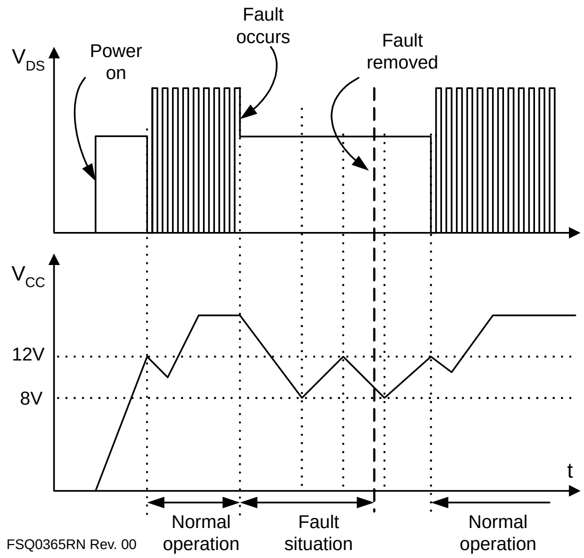


Figure 23. Auto−Restart Protection Waveforms

Overload Protection (OLP)

Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in the normal operation, the overload protection circuit can be triggered during load transition. To avoid this undesired operation, the overload protection circuit is designed to trigger only after a specified time to determine whether it is a transient situation or a true overload situation. Because of the pulse−by−pulse current limit capability, the maximum peak current through the SENSEFET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (V_O) decreases below the set voltage. This reduces the current through the opto−coupler LED, which also reduces the opto−coupler transistor current, thus increasing the feedback voltage (V_{FB}). If V_{FB} exceeds 2.8 V, D1 is blocked and the 5 μA current source starts to charge CB slowly up to V_{CC}. In this condition, V_{FB} continues increasing until it reaches 6 V, when the switching operation is terminated, as shown in Figure 24. The delay for shutdown is the time required to charge CB from 2.8 V to 6 V with 5 μA. A 20 ~ 50 ms delay is typical for most applications.

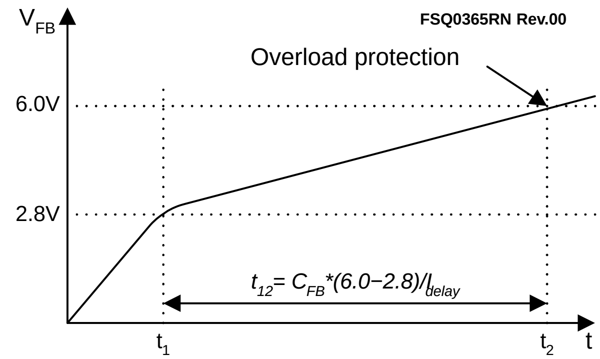


Figure 24. Overload Protection

Abnormal Over−Current Protection (AOCP)

When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high−di/dt can flow through the SENSEFET during the LEB time. Even though the FSQ−series has Overload Protection (OLP), it is not enough to protect the FSQ−series in that abnormal case, since severe current stress is imposed on the SENSEFET until OLP triggers. The FSQ−series has an internal Abnormal Over−Current Protection (AOCP) circuit as shown in Figure 25. When the gate turn−on signal is applied to the power SENSEFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the latch, resulting in the shutdown of the SMPS.

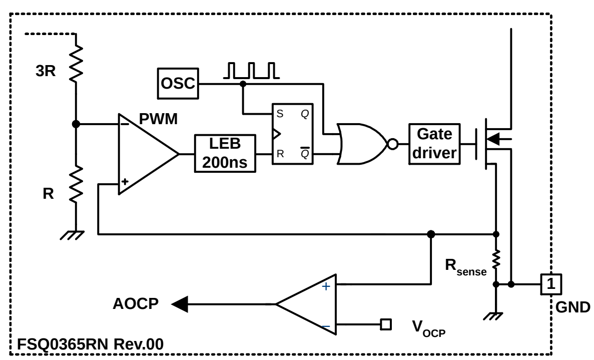


Figure 25. Abnormal Over−Current Protection

Over−Voltage Protection (OVP)

If the secondary−side feedback circuit malfunctions or a solder defect causes an opening in the feedback path, the current through the opto−coupler transistor becomes almost zero. Then V_{FB} climbs up in a similar manner to the overload situation, forcing the preset maximum current to be supplied to the SMPS until the overload protection triggers. Because more energy than required is provided to the output, the output voltage may exceed the rated voltage before the overload protection triggers, resulting in the breakdown of the devices in the secondary side. To prevent this situation, an OVP circuit is employed. In general, the peak voltage of the sync signal is proportional to the output voltage and the FSQ−series uses a sync signal instead of directly monitoring the output voltage. If the sync signal exceeds 6 V, an OVP is triggered, shutting down the SMPS. To avoid undesired triggering of OVP during normal operation, the peak voltage of the sync signal should be designed below 6 V.

Thermal Shutdown (TSD)

The SENSEFET and the control IC are built in one package. This makes it easy for the control IC to detect the abnormal over temperature of the SENSEFET. If the temperature exceeds ~150°C, the thermal shutdown triggers.

Soft−Start

An internal soft−start circuit increases PWM comparator inverting input voltage with the SENSEFET current slowly after it starts up. The typical soft−start time is 15 ms. The pulsewidth to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. This helps prevent transformer saturation and reduces stress on the secondary diode during startup.

Burst Operation

To minimize power dissipation in Standby Mode, the power switch enters Burst−Mode operation. As the load decreases, the feedback voltage decreases. As shown in Figure 26, the device automatically enters Burst Mode when the feedback voltage drops below V_{BURL} (350 mV). At this point, switching stops and the output voltages start to drop at a rate dependent on standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (550 mV), switching resumes. The feedback voltage then falls and the process repeats. Burst Mode alternately enables and disables switching of the power SENSEFET, reducing switching loss in Standby Mode.

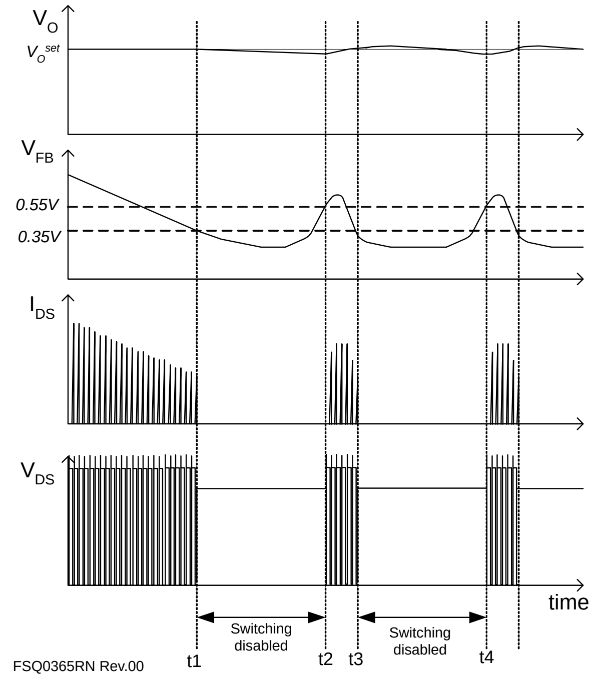


Figure 26. Waveforms of Burst Operation

Switching Frequency Limit

To minimize switching loss and Electromagnetic Interference (EMI), the MOSFET turns on when the drain voltage reaches its minimum value in valley switching operation. However, this causes switching frequency to increases at light load conditions. As the load decreases, the peak drain current diminishes and the switching frequency increases. This results in severe switching losses at light−load condition, as well as intermittent switching and audible noise. Because of these problems, the valley switching converter topology has limitations in a wide range of applications.

To overcome this problem, FSQ−series employs a frequency−limit function, as shown in Figure 27 and Figure 28. Once the SENSEFET is turned on, the next turn−on is prohibited during the blanking time (t_B). After the blanking time, the controller finds the valley within the detection time window (t_W) and turns on the MOSFET, as shown in Figure 27 and Figure 28 (cases A, B, and C). If no valley is found during t_W, the internal SENSEFET is forced to turn on at the end of t_W (case D). Therefore, FSQ devices have a minimum switching frequency of 55kHz and a maximum switching frequency of 67kHz, as shown in Figure 28.

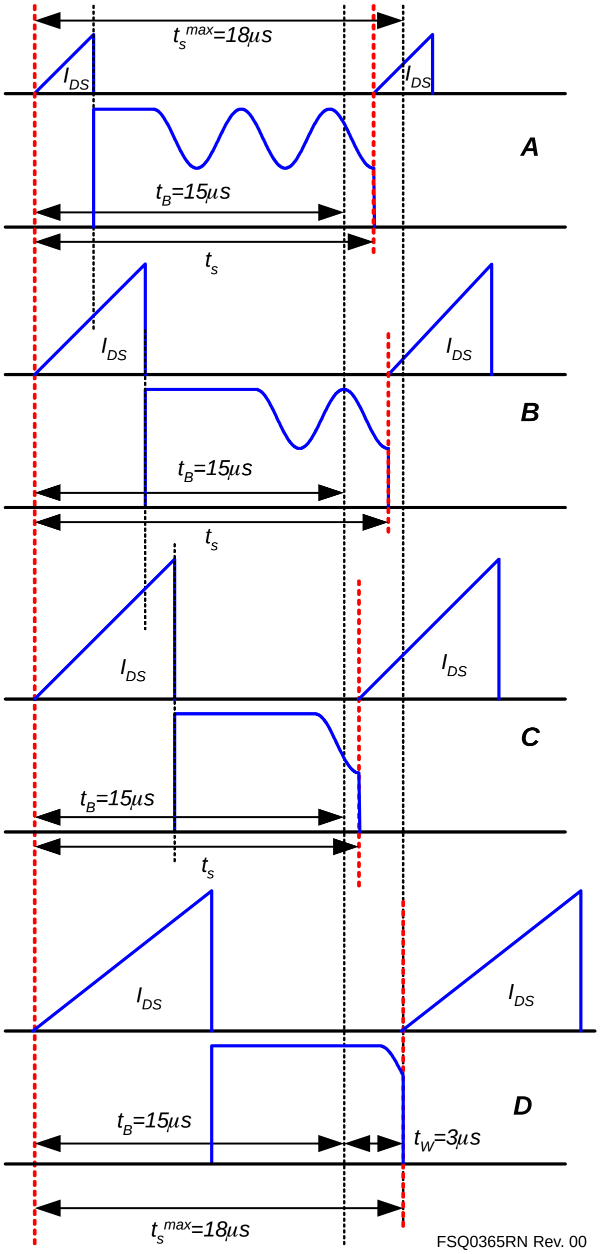


Figure 27. Valley Switching with Limited Frequency

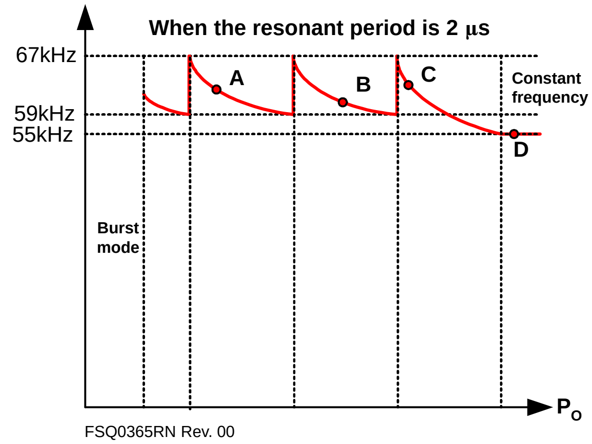


Figure 28. Switching Frequency Range

Typical Application Circuit of FSQ0365RN

Application	Power Switch Device	Input Voltage Range	Rated Output Power	Output Voltage (Maximum Current)
DVD Player Power Supply	FSQ0365RN	85−265 V_{AC}	19 W	5.1 V (1.0 A) 3.4 V (1.0 A) 12 V (0.4 A) 16 V (0.3 A)

Features

- High efficiency (> 77% at universal input)
- Low standby mode power consumption (< 1 W at 230 V_{AC} input and 0.5 W load)
- Reduce EMI noise through Valley Switching operation
- Enhanced system reliability through various protection functions
- Internal soft−start: 15 ms

Key Design Notes

- The delay time for overload protection is designed to be about 30 ms with C107 of 47nF. If faster/slower triggering of OLP is required, C107 can be changed to a smaller/larger value (eg. 100 nF for 60 ms).
- The input voltage of V_{sync} must be higher than −0.3 V. By proper voltage sharing by R106 & R107 resistors, the input voltage can be adjusted.
- The SMD−type 100 nF capacitor must be placed as close as possible to V_{CC} pin to avoid malfunction by abrupt pulsating noises and to improved surge immunity.

Schematic

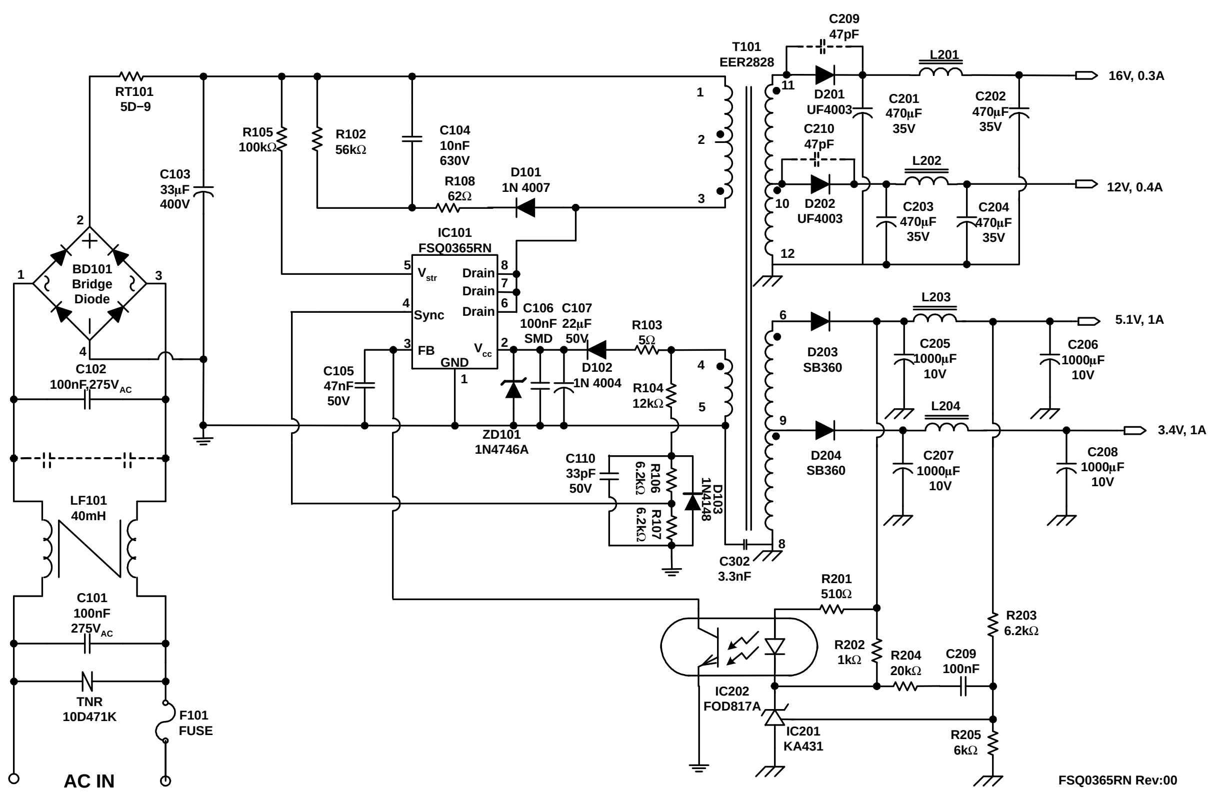


Figure 29. Demo Circuit of FSQ0365RN

Transformer

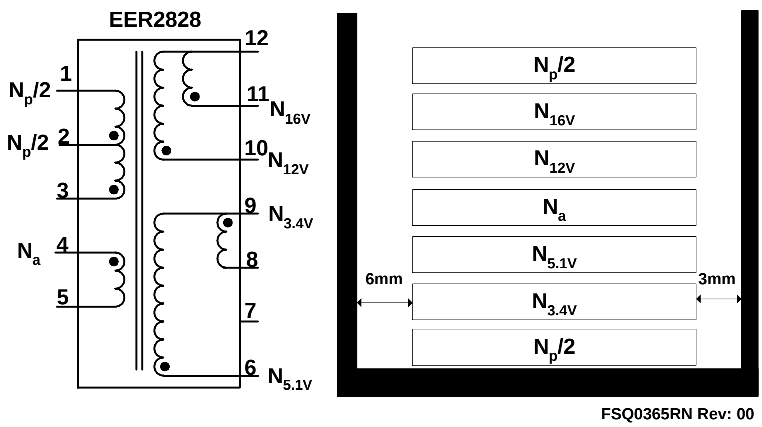


Figure 30. Transformer Schematic Diagram of FSQ0365RN

Table 6. WINDING SPECIFICATION

No.	Pin (s → f)	Wire	Turns	Winding Method
$N_p/2$	3 → 2	0.25$^{\phi}$ x 1	50	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050 mm, 2−Layer				
$N_{3.4V}$	9 → 8	0.33$^{\phi}$ x 2	4	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050 mm, 2−Layer				
N_{5V}	6 → 9	0.33$^{\phi}$ x 1	2	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050 mm, 2−Layer				
N_a	4 → 5	0.25$^{\phi}$ x 1	16	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050 mm, 2−Layer				
N_{12V}	10 → 12	0.33$^{\phi}$ x 3	14	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050 mm, 3−Layer				
N_{16V}	11 → 12	0.33$^{\phi}$ x 3	18	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050 mm, 2−Layer				
$N_p/2$	2 → 1	0.25$^{\phi}$ x 1	50	Center Solenoid Winding
Insulation: Polyester Tape t = 0.050 mm, 2−Layer				

Table 7. TRANSFORMER ELECTRICAL CHARACTERISTICS

	Pin	Specification	Remarks
Inductance	1 − 3	1.4 mH ± 10%	100 kHz, 1 V
Leakage	1 − 3	25 μH Maximum	Short All Other Pins

Core & Bobbin

Core: EER2828 (Ae = 86.66 mm^2)
Bobbin: EER2828

Table 8. EVALUATION BOARD PART LIST

Part	Value	Note	Part	Value	Note
Resistor			**Inductor**		
R102	56 kΩ	1 W	L201	10 μH	
R103	5 Ω	1/2 W	L202	10 μH	
R104	12 kΩ	1/4 W	L203	4.9 μH	
R105	100 kΩ	1/4 W	L204	4.9 μH	
R106	6.2 kΩ	1/4 W	**Diode**		
R107	6.2 kΩ	1/4 W	D101	IN4007	
R108	62 Ω	1 W	D102	IN4004	
R201	510 Ω	1/4 W	ZD101	1N4746A	
R202	1 kΩ	1/4 W	D103	1N4148	
R203	6.2 kΩ	1/4 W	D201	UF4003	
R204	20 kΩ	1/4 W	D202	UF4003	
R205	6 kΩ	1/4 W	D203	SB360	
Capacitor			D204	SB360	
C101	100 nF / 275 V_{AC}	Box Capacitor			
C102	100 nF / 275 V_{AC}	Box Capacitor	**IC**		
C103	33 μF / 400 V	Electrolytic Capacitor	IC101	FSQ0365RN	Power Switch
C104	10 nF / 630 V	Film Capacitor	IC201	KA431 (TL431)	Voltage reference
C105	47 nF / 50 V	Mono Capacitor	IC202	FOD817A	Opto−coupler
C106	100 nF / 50 V	SMD (1206)	**Fuse**		
C107	22 μF / 50 V	Electrolytic Capacitor	Fuse	2A/250V	
C110	33 pF / 50 V	Ceramic Capacitor	**NTC**		
C201	470 μF / 35 V	Electrolytic Capacitor	RT101	5D−9	
C202	470 μF / 35 V	Electrolytic Capacitor	**Bridge Diode**		
C203	470 μF / 35 V	Electrolytic Capacitor	BD101	2KBP06M2N257	Bridge Diode
C204	470 μF / 35 V	Electrolytic Capacitor	**Line Filter**		
C205	1000 μF / 10 V	Electrolytic Capacitor	LF101	40 mH	
C206	1000 μF / 10 V	Electrolytic Capacitor	**Transformer**		
C207	1000 μF / 10 V	Electrolytic Capacitor	T101		
C208	1000 μF / 10 V	Electrolytic Capacitor	**Varistor**		
C209	100 nF / 50 V	Ceramic Capacitor	TNR	10D471K	

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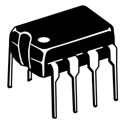

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PDIP−8
CASE 626−05
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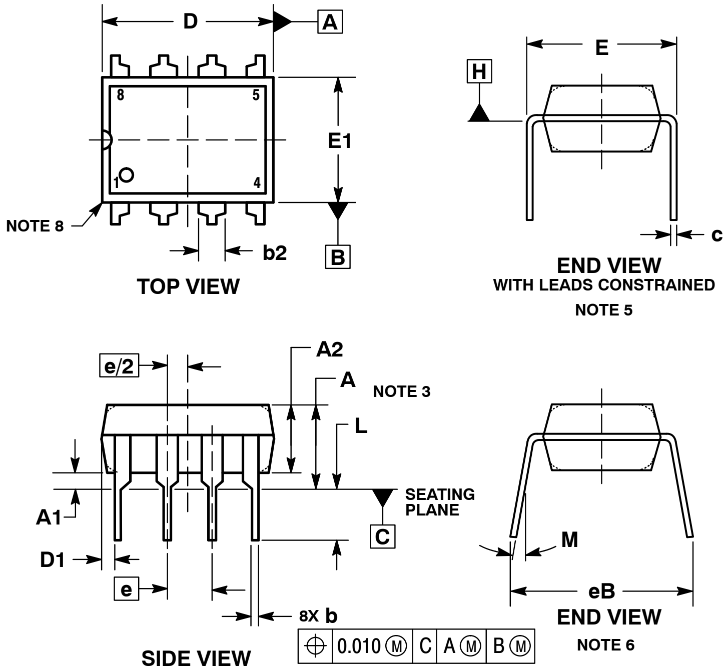
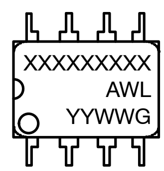


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. DIMENSIONS A, A1 AND L ARE MEASURED WITH THE PACKAGE SEATED IN JEDEC SEATING PLANE GAUGE GS−3.
4. DIMENSIONS D, D1 AND E1 DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS. MOLD FLASH OR PROTRUSIONS ARE NOT TO EXCEED 0.10 INCH.
5. DIMENSION E IS MEASURED AT A POINT 0.015 BELOW DATUM PLANE H WITH THE LEADS CONSTRAINED PERPENDICULAR TO DATUM C.
6. DIMENSION eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
7. DATUM PLANE H IS COINCIDENT WITH THE BOTTOM OF THE LEADS, WHERE THE LEADS EXIT THE BODY.
8. PACKAGE CONTOUR IS OPTIONAL (ROUNDED OR SQUARE CORNERS).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	----	0.210	---	5.33
A1	0.015	----	0.38	---
A2	0.115	0.195	2.92	4.95
b	0.014	0.022	0.35	0.56
b2	0.060 TYP		1.52 TYP	
C	0.008	0.014	0.20	0.36
D	0.355	0.400	9.02	10.16
D1	0.005	----	0.13	---
E	0.300	0.325	7.62	8.26
E1	0.240	0.280	6.10	7.11
e	0.100 BSC		2.54 BSC	
eB	----	0.430	---	10.92
L	0.115	0.150	2.92	3.81
M	----	10°	---	10°

STYLE 1:
PIN 1. AC IN
2. DC + IN
3. DC − IN
4. AC IN
5. GROUND
6. OUTPUT
7. AUXILIARY
8. V_{CC}

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present.

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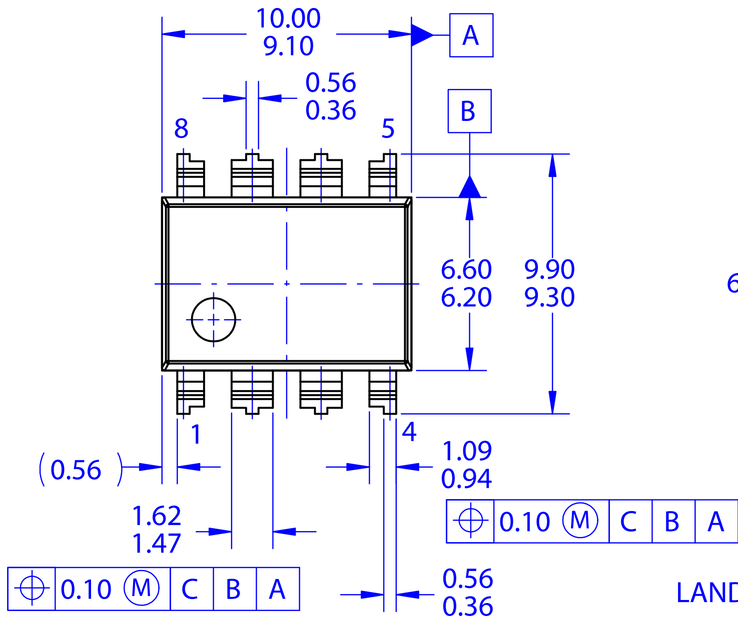
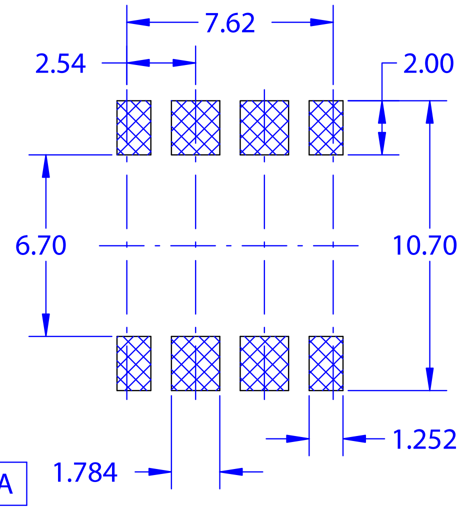


TOP VIEW



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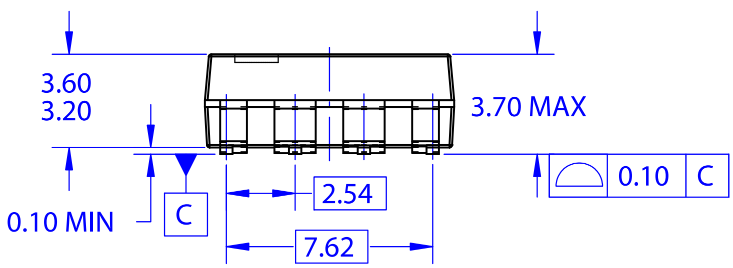

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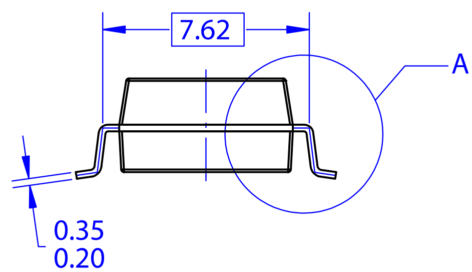
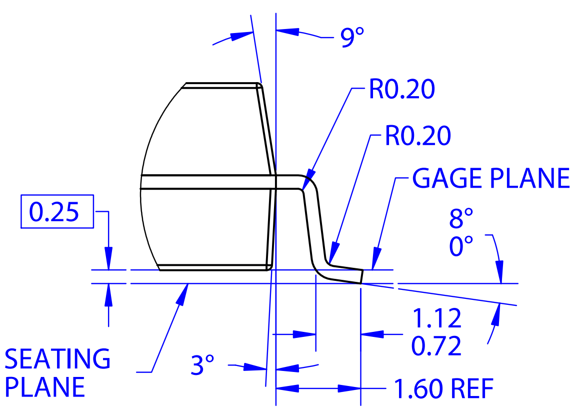


SIDE VIEW



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B. ALL DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
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