Future Technology Devices International Ltd

FT233HP/FT232HP

(High Speed USB Bridge with Type-C/PD3.0 Controller)

The FT233HP/FT232HP is a Hi-Speed USB device with Type-C/PD 3.0 controller IC that fully supports the latest USB Type-C and Power Delivery (PD) standards enabling support for power negotiation with the ability to sink or source current to a USB host device. The USB bridge function delivers 1 independent channel compatible with the existing FT232H – Single Hi-speed USB to multipurpose UART/FIFO solution. The FT233HP/FT232HP has the following advanced features:

- Supports the USB-PD Specification Rev 3.0.
- 2 USB PD 3.0 Ports Support. Port 1 supports Dual Role Swap Function while Port 2 supports sink mode with charging function through to Port 1 (FT233HPQ and FT233HPL only).
- Supports 5V3A, 9V3A, 12V3A, 15V3A, 20V3A PDOs as sink or source.
- Type-C/PD Physical Layer Protocol.
- PD policy engine using 32-bit RISC controller with 8kB data RAM and 48kB code ROM.
- PD mode configuration through external EEPROM.
- Options to use external MCU controlling PD policy through I2C interface.
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- Single channel USB to serial / parallel ports with a variety of configurations.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- USB 2.0 Hi-Speed (480Mbits/Second) and Full Speed (12Mbits/Second) compatible.
- Multi-Protocol Synchronous Serial Engine (MPSSE) to simplify synchronous serial protocol (USB to JTAG, I^2C (MASTER), SPI (MASTER) or bit-bang) design.
- RS232/RS422/RS485 UART transfer data rate up to 12Mbaud. (RS232 Data Rate limited by external level shifter).
- USB to asynchronous 245 FIFO mode for transfer data rate up to 8 Mbyte/Sec.
- USB to synchronous 245 parallel FIFO mode for transfers up to 40 Mbytes/Sec
- Supports a proprietary half duplex FT1248 interface with a configurable width, bi-directional data bus (1, 2, 4 or 8 bits wide).
- CPU-style FIFO interface mode simplifies CPU interface design.
- Fast serial interface option.
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Adjustable receive buffer timeout.
- Option for transmit and receive LED drive signals.
- Bit-bang Mode interface option with RD# and WR# strobes
- Highly integrated design includes +1.2V LDO regulator for VCORE, integrated POR function
- Asynchronous serial UART interface option with full hardware handshaking and modem interface signals.
- Fully assisted hardware or X-On / X-Off software handshaking.
- UART Interface supports 7/8-bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity.
- Auto-transmit enable control for RS485 serial applications using the TXDEN pin.
- Operational mode configuration and USB Description strings configurable in external EEPROM over the USB interface.
- Configurable I/O drives strength (4, 8, 12 or 16mA) and slew rate.
- Low operating and USB suspend current.
- UHCI/OHCI/EHCI host controller compatible.
- USB Bulk data transfer mode (512-byte packets in Hi-Speed mode).
- +1.2V (chip core) and +3.3V I/O interfacing (+5V Tolerant).
- Extended -40°C to 85°C industrial operating temperature range.
- 3 IC Package with RoHS compliant support:
  - FT233HPQ: Compact 64-pin Pb Free QFN package supports 2 PD 3.0 Ports
  - FT233HPL: Compact 64-pin Pb Free LQFP package supports 2 PD 3.0 Ports
  - FT232HPQ: Compact 56-pin Pb Free QFN package supports 1 PD 3.0 Port
- Configurable ACBUS I/O pins.

1 Typical Applications

- USB Bridge with Type-C/PD3.0 (chargers and devices).
- Up to 60W power delivery via USB PD and/or Type-C port
- Get power from USB device functions, e.g., portable USB host needs charging when USB is connected.
- Single chip USB to UART (RS232, RS422 or RS485)
- USB to FIFO
- USB to FT1248
- USB to JTAG
- USB to SPI
- USB to I^2C
- USB to Bit-Bang
- USB to Fast Serial Interface
- USB to CPU target interface (as memory)
- USB Instrumentation
- USB Industrial Control
- USB EPOS Control
- USB MP3 Player Interface
- USB FLASH Card Reader / Writers
- Set Top Box - USB interface
- USB Digital Camera Interface
- USB Bar Code Readers

1.1 Driver Support

The FT233HP/FT232HP requires USB device drivers (listed below), available free from https://ftdichip.com/, to operate. The VCP version of the driver creates a Virtual COM Port allowing legacy serial port applications to operate over USB e.g., serial emulator application TTY. Another FTDI USB driver, the D2XX driver, can also be used with application software to directly access the FT233HP/FT232HP through a DLL.

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 10 32,64-bit
- Windows 8/8.1 32,64-bit
- Windows 7 32,64-bit
- Windows Server 2008 and server 2012 R2
- Mac OS-X
- Linux 2.4 and greater

Royalty free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 10 32,64-bit
- Windows 8/8.1 32,64-bit
- Windows 7 32,64-bit
- Windows Server 2008 and server 2012 R2
- Mac OS-X
- Linux 2.4 and greater
- Android(J2xx)

For driver installation, please refer to the installation guides on our website:
https://ftdichip.com/document/installation-guides/

The following additional installation guides application notes and technical notes are also available:

- AN_117 - User Guide For libMPSSE – I2C
- AN_110 - Programmers Guide for High Speed FTCJTAG DLL
- AN_178 - User Guide For libMPSSE - SPI
- AN_113 - Interfacing FT2232H Hi-Speed Devices To I2C Bus
- AN_114 - Interfacing FT2232H Hi-Speed Devices To SPI Bus
- AN_135 - MPSSE Basics
- AN_108 - Command Processor For MPSSE and MCU Host Bus Emulation Modes
- AN_411 - FTx232H MPSSE I2C Master Example in C#
- TN_104 - Guide to Debugging Customers Failed Driver Installation
- AN_448 - FT4233HP_FT2233HP_FT233HP_Configuration_Guide
- AN_449 - FT4233HP_FT2233HP_FT4232HP_FT2232HP DCDC_Power Delivery
- AN_551 -FT4232HP_FT2232HP_FT232HP_Configuration_Guide

1.2 Part Numbers

Part Number	Package	Packing
FT232HPQ-TRAY	QFN 56	260 pieces per tray
FT232HPQ-REEL	QFN 56	3,000 pieces per reel
FT233HPQ-TRAY	QFN 64	260 pieces per tray
FT233HPQ-REEL	QFN 64	3,000 pieces per reel
FT233HPL-TRAY	LQFP 64	Not yet available
FT233HPL-REEL	LQFP 64	Not yet available

Please refer to Section 6 for all package mechanical parameters.

1.3 USB Compliant

The FT233HP/FT232HP is fully compliant with the USB 2.0 specification and the USB Type-C & PD 3.0 specification.
It has been given the USB-IF Test-ID (TID) 3425* for FT233HP/5485 for FT232HP.

* for PD port1

The timing of the rise/fall time of the USB signals is not only dependant on the USB signal drivers, but also system and is affected by factors such as PCB layout, external components, and any transient protection present on the USB signals. For USB compliance these may require a slight adjustment. Timing can also be changed by adding appropriate passive components to the USB signals.

2 FT233HP/FT232HP Block Diagram

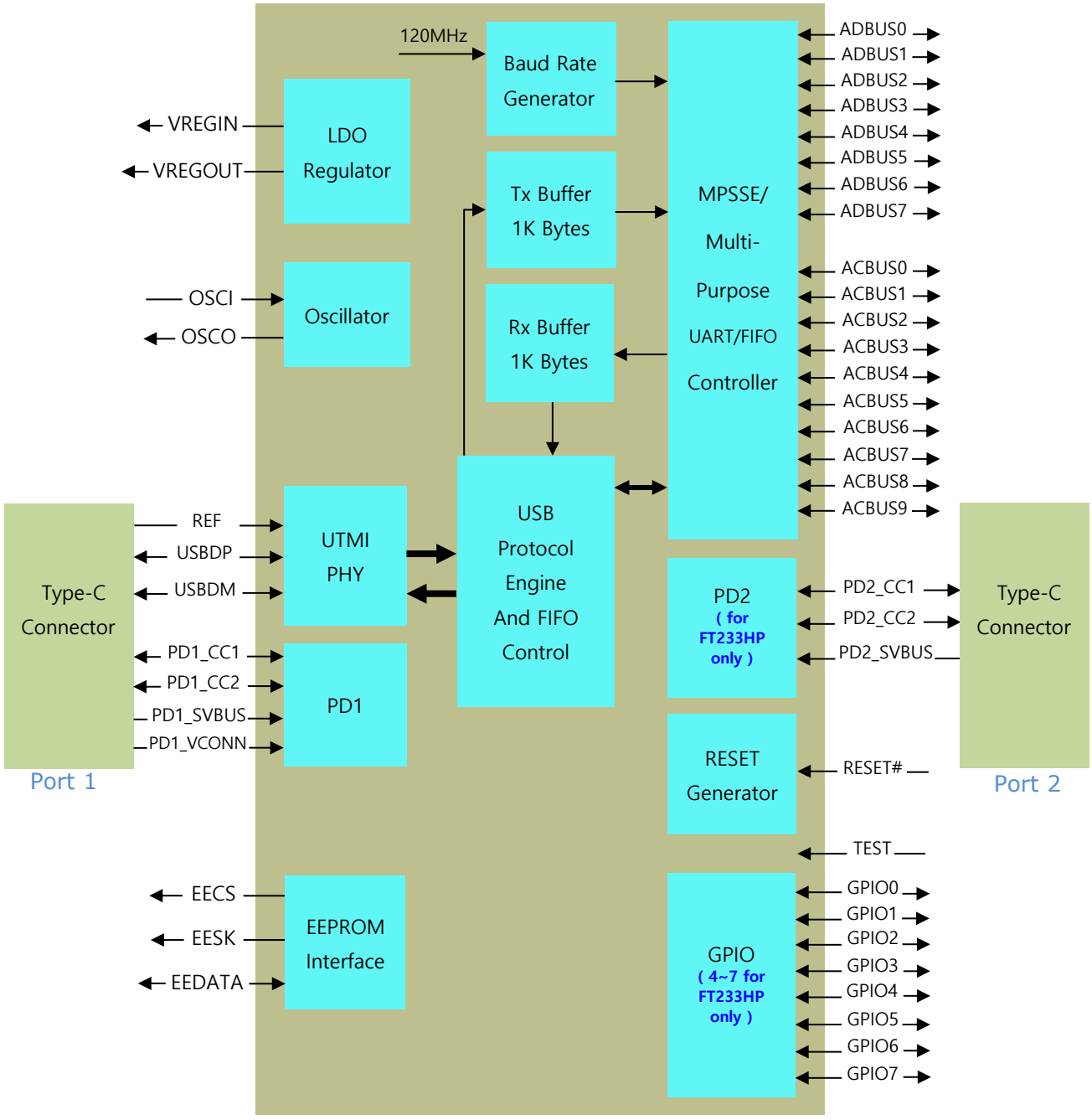

Figure 1 - FT233HP/FT232HP Block Diagram

*A full description of each function is available in Section 4.

Note: FT232HP does not include Port 2.

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3 Device Pin Out and Signal Descriptions

There are three types of IC package for FT233HP IC: 64 pin QFN FT233HPQ, 64 pin LQFP FT233HPL and 56 pin QFN FT232HPQ. There pin numbering is illustrated in the schematic symbol shown in Figure 2, Figure 3 and Figure 4.

3.1 FT233HPQ 64 Pin QFN Package Diagram

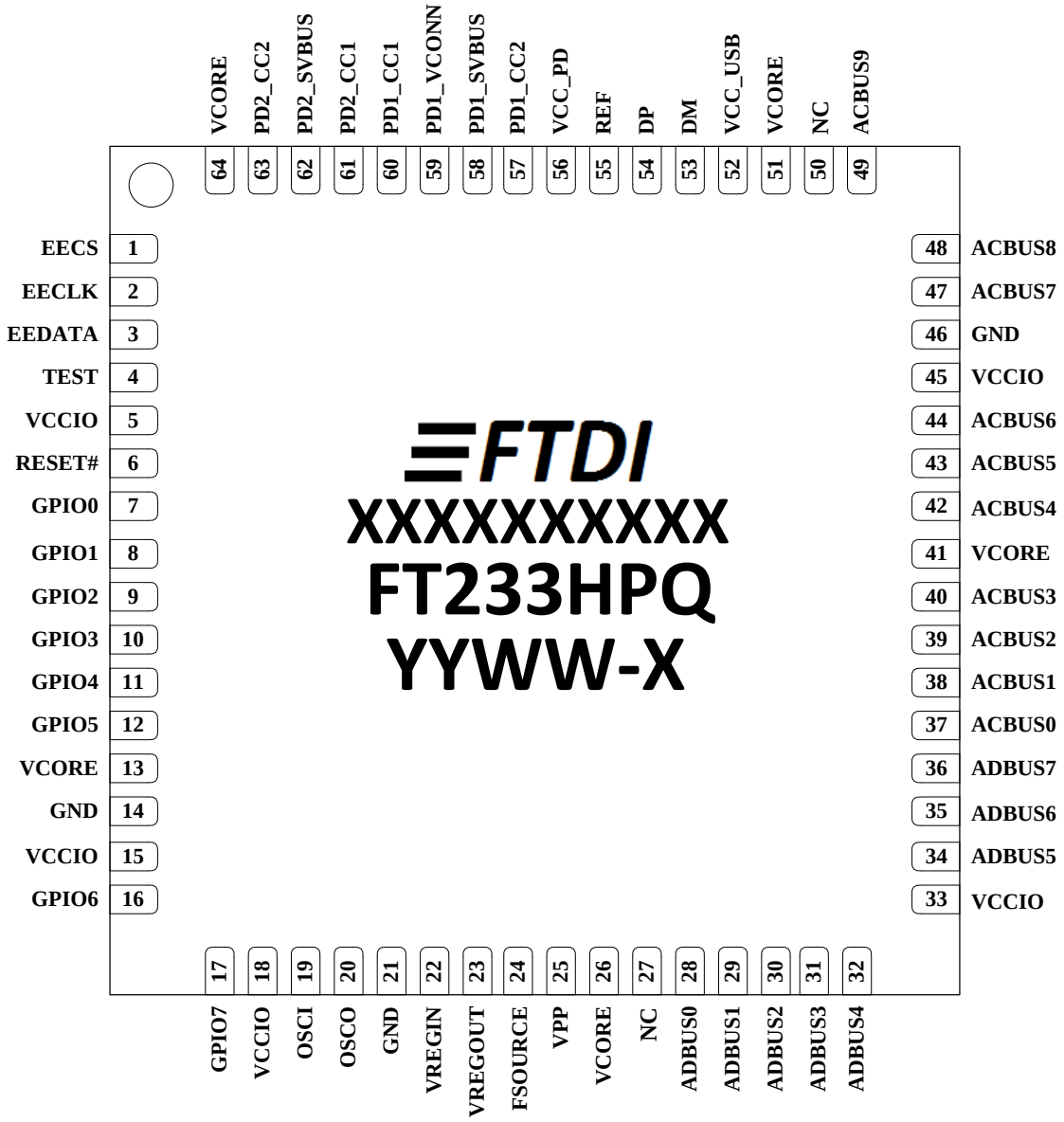


Figure 2 - FT233HPQ-64 Pin Schematic Symbol

3.2 FT233HPL 64 Pin LQFP Package Diagram

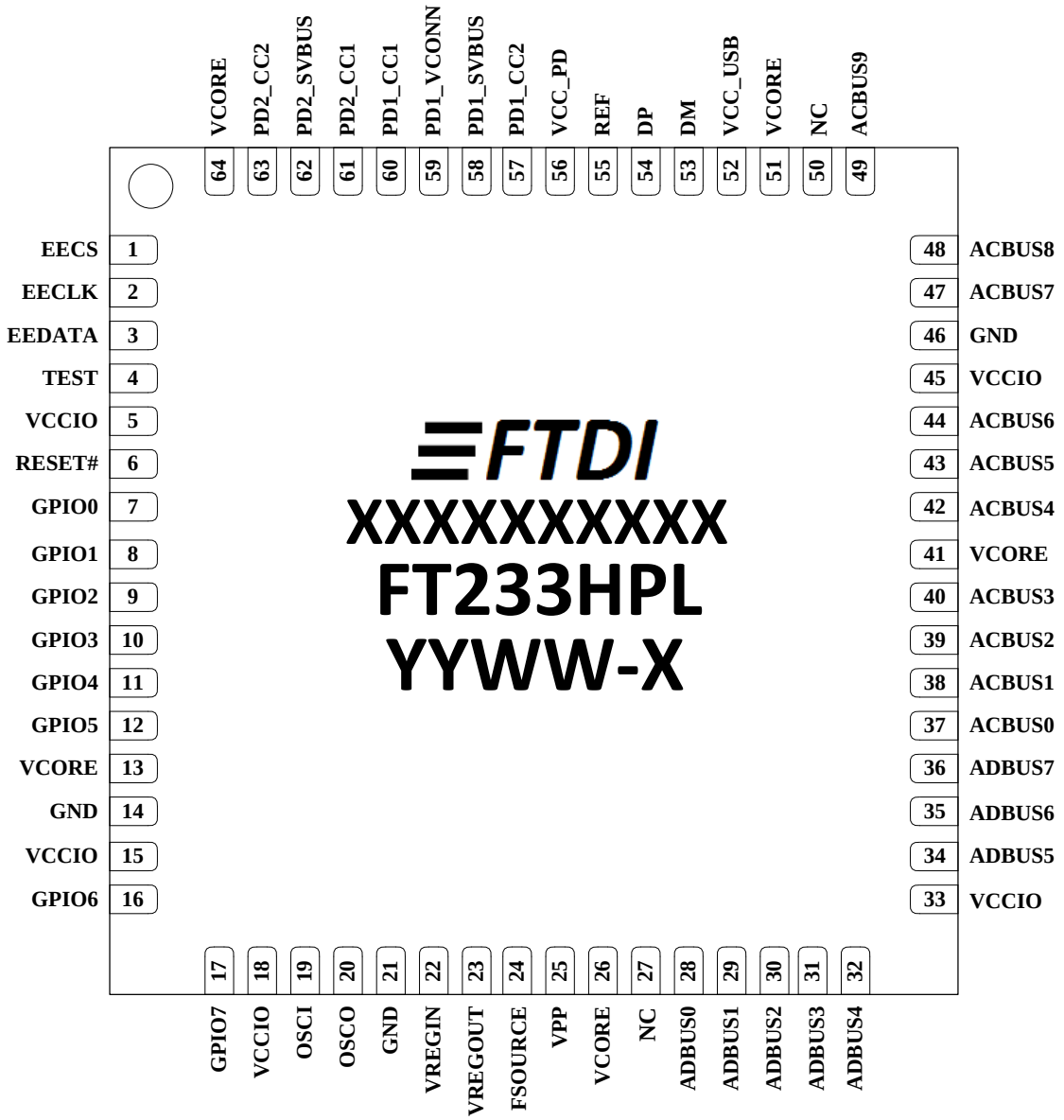


Figure 3 - FT233HPL- 64 Pin Schematic Symbol

3.3 FT232HPQ 56 Pin QFN Package Diagram

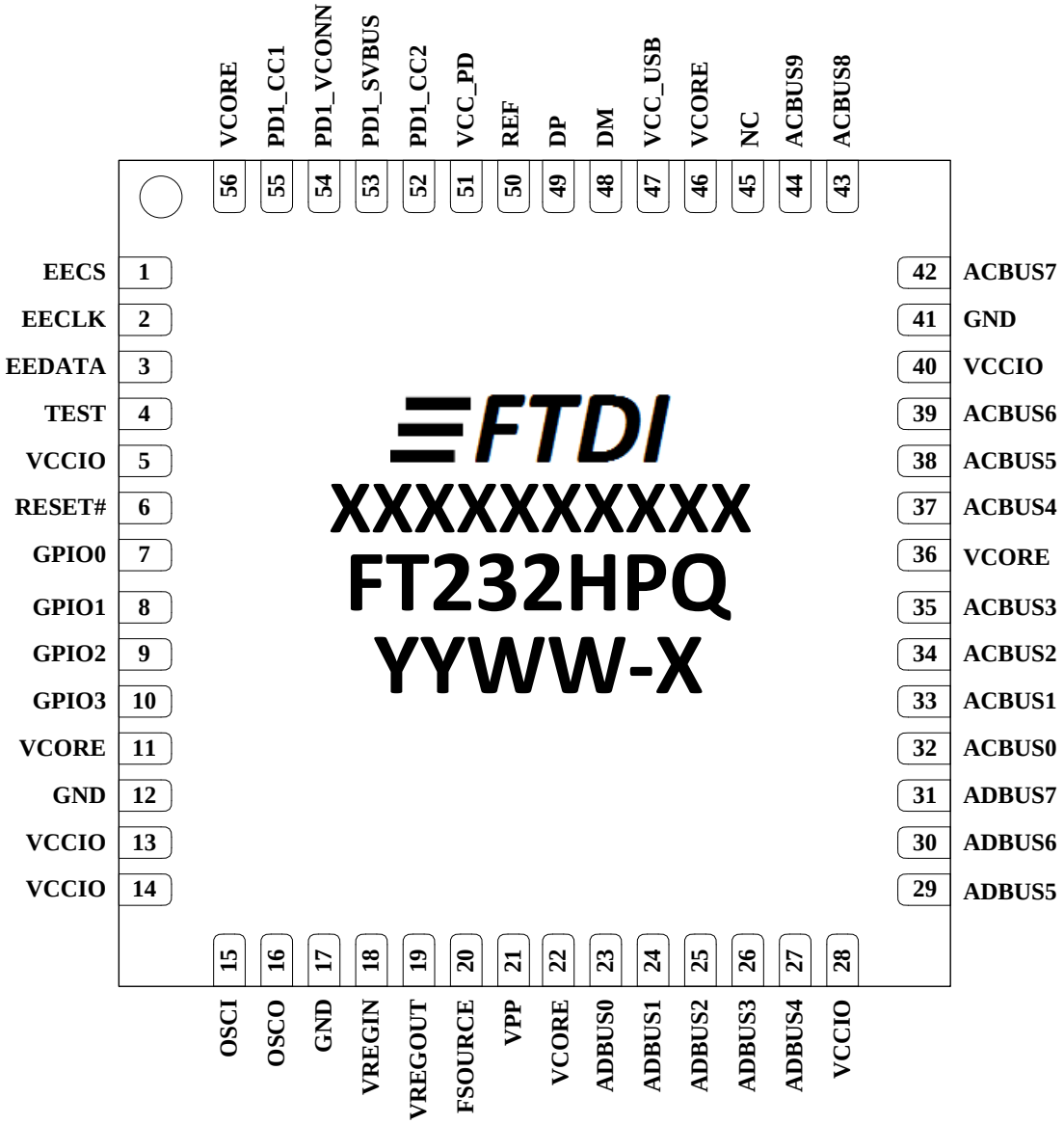


Figure 4 - FT232HPQ-56 Pin Schematic Symbol

3.4 FT233HP/FT232HP Pin Descriptions

This section describes the operation of the FT233HP/FT232HP pins. Both the LQFP and the QFN packages have the same function on each pin. The function of many pins is determined by the configuration of the FT233HP/FT232HP. Table 1 provides details about the function of each pin dependent on the configuration of the interface. Each of the functions are described in the following table (**Note:** The convention used throughout this document for active low signals is the signal name followed by #).

FT233HP / FT232HP											
Pin			Pin functions (depends on configuration)								
64 Pin #	56 Pin #	Pin Name	ASYNC Serial UART (RS232/422 /485)	SYNC 245 FIFO	STYLE ASYNC 245 FIFO	ASYNC Bit-bang	SYNC Bit-bang	MPSSE	Fast Serial interface	CPU Style FIFO	FT1248
28	23	ADBUS0	TXD	D0	D0	D0	D0	TCK/SK	FSDI	D0	MIOSI0
29	24	ADBUS1	RXD	D1	D1	D1	D1	TDI/DO	FSCLK	D1	MIOSI1
30	25	ADBUS2	RTS#	D2	D2	D2	D2	TDO/DI	FSDO	D2	MIOSI2
31	26	ADBUS3	CTS#	D3	D3	D3	D3	TMS/CS	FSCTS	D3	MIOSI3
32	27	ADBUS4	DTR#	D4	D4	D4	D4	GPIOL0	** TriSt-UP	D4	MIOSI4
34	29	ADBUS5	DSR#	D5	D5	D5	D5	GPIOL1	** TriSt-UP	D5	MIOSI5
35	30	ADBUS6	DCD#	D6	D6	D6	D6	GPIOL2	** TriSt-UP	D6	MIOSI6
36	31	ADBUS7	RI#	D7	D7	D7	D7	GPIOL3	** TriSt-UP	D7	MIOSI7
37	32	ACBUS0	* TXDEN	RXF#	RXF#	ACBUS0	ACBUS0	GPIOH0	** ACBUS0	CS#	SCLK
38	33	ACBUS1	** ACBUS1	TXE#	TXE#	WRSTB#	WRSTB#	GPIOH1	** ACBUS1	A0	SS_n
39	34	ACBUS2	** ACBUS2	RD#	RD#	RDSTB#	RDSTB#	GPIOH2	** ACBUS2	RD#	MISO
40	35	ACBUS3	* RXLED#	WR#	WR#	ACBUS3	ACBUS3	GPIOH3	** ACBUS3	WR#	ACBUS3
42	37	ACBUS4	* TXLED#	SIWU#	SIWU#	SIWU#	SIWU#	GPIOH4	SIWU#	Note1	ACBUS4
43	38	ACBUS5	** ACBUS5	CLKOUT	ACBUS5	** ACBUS5	** ACBUS5	GPIOH5	** ACBUS5	** ACBUS5	ACBUS5
44	39	ACBUS6	** ACBUS6	OE#	ACBUS6	ACBUS6	ACBUS6	GPIOH6	** ACBUS6	** ACBUS6	ACBUS6
47	42	ACBUS7	WRSAV#	PWRSAV#	PWRSAV#	PWRSAV#	PWRSAV#	*** GPIOH7	PWRSAV#	PWRSAV#	PWRSAV#
48	43	ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	ACBUS8
49	44	ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	ACBUS9

Table 1 - FT233HP/FT232HP Pin Descriptions

Pins marked * require an EEPROM for assignment to these functions. Default is Tristate, Pull-Up

Pins marked ** default to tri-stated inputs with an internal 75KΩ (approx.) pull up resistor to VCCIO.

Pin marked *** default to GPIO line with an internal 75KΩ pull down resistor to GND. Using the EEPROM this pin can be PWRSAV#(need to pull to VCC_USB) instead of GPIO mode.

Note 1: Initial Pin States - The device will start up as a UART port if no EEPROM is fitted. This also applies if an EEPROM is fitted until the EEPROM is read by the device. Therefore, pins which are output in UART mode will be driving out at start-up. If an application uses a mode other than UART, ensure that any external signals do not cause contention during this time.

Note 2: To wake up the USB device in this mode, put ACBUS0 from "High" to "LOW", set ACBUS1 "High", and put ACBUS3 from "High" to "LOW".

3.5 Signal Description

The operation of the following FT233HP/FT232HP pins are the same regardless of the configured mode:-

64 Pin No.	56 Pin No.	Name	Type	Description
13,26,41, 51, 64	11,22,36,46, 56	VCORE	POWER Input	+1.2V input. Core supply voltage input. Connect to VREGOUT when using internal regulator.
5,15,18, 33,45	5,13,14, 28,40	VCCIO	POWER Input	+3.3V input. I/O interface power supply input. Failure to connect all VCCIO pins will result in failure of the device.
52	47	VCC_USB	POWER Input	+3.3V Input. Internal USB PHY power supply input. Note that this cannot be connected directly to the USB supply. A +3.3V regulator must be used. It is recommended that this supply is filtered using an LC filter. **Note: When migrating designs from the FT232H – note that due to the Power Delivery capabilities of the FT233H, the application may negotiate the VCC_USB voltage to be significantly greater than 5V. The designer must ensure that any signals derived from circuits powered by VCC_USB which are applied to the FT233H pins do not exceed the maximum input voltage for the pins at any time.*
56	51	VCC_PD	POWER Input	+3.3V Input. Internal PD PHY power supply input.
22	18	VREGIN	POWER Input	+3.3V Input. Integrated 1.2V voltage regulator input.
23	19	VREGOUT	POWER Output	+1.2V Output. Integrated voltage regulator output. Connect to VCORE with 3.3uF filter capacitor. This output should not be used to power other circuits apart from VCORE.
24	20	FSOURCE	POWER Input	FSOURCE input pin for EFUSE. Leave float for normal operation
25	21	VPP	POWER Input	VPP input pin for EFUSE. Leave float for normal operation
14,21,46	12,17,41	GND	POWER Input	Ground.

Table 2 - Power and Ground

64 Pin No.	56 Pin No.	Name	Type	Description
19	15	OSCI	INPUT	Oscillator input.
20	16	OSCO	OUTPUT	Oscillator output.
55	50	REF	INPUT	Current reference – connect via a 12KΩ resistor @ 1% to GND.
53	48	DM	I/O	USB Data Signal Minus.
54	49	DP	I/O	USB Data Signal Plus.
4	4	TEST	INPUT	IC test pin – for normal operation must be connected to GND.
6	6	RESET#	INPUT	Reset input (active low).
47	42	PWRSAV#	INPUT	USB Power Save input. This is an EEPROM configurable option which is set using a 'Suspend on ACBUS7 Low' bit in FT_PROG. This option is available when the FT233HP/FT232HP is on a self-powered mode and is used to prevent forcing current down the USB lines when the host or hub is powered off. PWRSAV# = 1 : Normal Operation

				PWRSAV# = 0 : FT233HP/FT232HP forced into SUSPEND mode. PWRSAV# can be connected to VCC_USB (*please see the note for VCC_USB usage in Table2*) of the USB connector (via a 39KΩ resistor). When this input goes high, then it indicates to the FT233HP/FT232HP that it is connected to a host PC. When the host or hub is powered down then the FT233HP/FT232HP is held in SUSPEND mode.

Table 3 – Common Function Pins

64 Pin No.	56 Pin No	Name	Type	Description
1	1	EECS*	I/O	EEPROM – Chip Select. Tri-State during device reset.
2	2	EECLK*	OUTPUT	Clock signal to EEPROM. Tri-State during device reset. When not in reset, this outputs the EEPROM clock.
3	3	EEDATA*	I/O	EEPROM – Data I/O. Connect directly to Data-in of the EEPROM and to Data-out of the EEPROM via a 2.2K resistor. Also, pull Data-Out of the EEPROM to VCC via a 10K resistor for correct operation. Tri-State during device reset.

Table 4 – EEPROM Interface Group

*** Note:** Pull each of these pins via separate 10K resistor to VCCIO if no EEPROM uses.

64 Pin No.	56 Pin No	Name	Type	Description
58	53	PD1_SVBUS	AI	Analog input. Scaled down VBUS sensing input for PD1. VBUS is required to be scaled down between 7.5 and 7.7 before input to this pin.
59	54	PD1_VCONN	Power Input	Power input for PD1 VCONN power source. Connect to 3.3V.
60	55	PD1_CC1	AI/O	Analog IO pin. PD1 CC1 pin
57	52	PD1_CC2	AI/O	Analog IO pin. PD1 CC2 pin
62	N/A	PD2_SVBUS	AI	Analog input. Scaled down VBUS sensing input for PD2. VBUS is required to be scaled down between 7.5 and 7.7 before input to this pin.
61	N/A	PD2_CC1	AI/O	Analog IO pin. PD2 CC1 pin
63	N/A	PD2_CC2	AI/O	Analog IO pin. PD2 CC2 pin

Table 5 – Type-C/PD Port Pins

64 Pin No.	56 Pin No	Name	Type	Description
7	7	GPIO0	I/O	GPIO0 or I2C_SDA pin. Default function is GPIO0 input with weak pull-down.
8	8	GPIO1	I/O	GPIO1 or I2C_SCL pin. Default function is GPIO1 input with weak pull-down.
9	9	GPIO2	I/O	GPIO2 or I2C_INT# pin. Default function is GPIO2 input with weak pull-down.
10	10	GPIO3	I/O	GPIO3 pin. Default function is GPIO3 input with weak pull-down.
11	N/A	GPIO4	I/O	GPIO4 pin. Default function is GPIO4 input with weak pull-down.
12	N/A	GPIO5	I/O	GPIO5 pin. Default function is GPIO5 input with weak pull-down.
16	N/A	GPIO6	I/O	GPIO6 pin. Default function is GPIO6 input with weak pull-down.
17	N/A	GPIO7	I/O	GPIO7 pin. Default function is GPIO7 input with weak pull-down.

Table 6 – GPIO Pins

64 Pin No.	56 Pin No	Name	Type	Description
28	23	ADBUS0	Output	Configurable Output Pin, the default configuration is Transmit Asynchronous Data Output.
29	24	ADBUS1	Input	Configurable Input Pin, the default configuration is Receiving Asynchronous Data Input.
30	25	ADBUS2	Output	Configurable Output Pin, the default configuration is Request to Send Control Output / Handshake Signal.
31	26	ADBUS3	Input	Configurable Input Pin, the default configuration is Clear To Send Control Input / Handshake Signal.
32	27	ADBUS4	Output	Configurable Output Pin, the default configuration is Data Terminal Ready Control Output / Handshake Signal.
34	29	ADBUS5	Input	Configurable Input Pin, the default configuration is Data Set Ready Control Input / Handshake Signal.
35	30	ADBUS6	Input	Configurable Input Pin, the default configuration is Data Carrier Detect Control Input.
36	31	ADBUS7	Input	Configurable Input Pin, the default configuration is Ring Indicator Control Input. When remote wake up is enabled in the EEPROM taking RI# low can be used to resume the PC USB host controller from suspend. (Also see note 1, 2, 3 in Section 4.12)
37	32	ACBUS0	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 8 – ACBUS Configuration Control
38	33	ACBUS1	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 8 – ACBUS Configuration Control
39	34	ACBUS2	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 8 – ACBUS Configuration Control
40	35	ACBUS3	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 8 – ACBUS Configuration Control
42	37	ACBUS4	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 8 – ACBUS Configuration Control
43	38	ACBUS5	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 8 – ACBUS Configuration Control
44	39	ACBUS6	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 8 – ACBUS Configuration Control

47	42	ACBUS7	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PD. See ACBUS Signal Options, Table 8 – ACBUS Configuration Control
48	43	ACBUS8	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 8 – ACBUS Configuration Control
49	44	ACBUS9	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 8 – ACBUS Configuration Control

Table 7 – UART Interface and ACBUS Group

Note:

When used in Input Mode, the input pins are pulled to VCCIO via internal 75kΩ (approx.) resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the EEPROM.

3.6 ACBUS Signal Option

If the external EEPROM is fitted, the following options can be configured on the ACBUS I/O pins using the software utility FT_PROG which can be downloaded from the FTDI utilities page. ACBUS signal options are common to both package versions of the FT233HP/FT232HP.

ACBUS Signal Option	Available On ACBUS Pin	Description
TXDEN	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	TXDEN = (TTL level). Used with RS485 level converters to enable the line driver during data transmit. TXDEN is active from one bit time before the start bit is transmitted on TXD until the end of the stop bit.
*PWREN#	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	Output is low after the device has been configured by USB, then high during USB suspend mode. This output can be used to control power to external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# in this way.*
TXLED#	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	TXLED = Transmit signalling output. Pulses low when transmitting data (TXD) to the external device. This can be connected to an LED.
RXLED#	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	RXLED = Receive signalling output. Pulses low when receiving data (RXD) from the external device. This can be connected to an LED.
TX&RXLED#	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	LED drive – pulses low when transmitting or receiving data from or to the external device.
SLEEP#	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	Goes low during USB suspend mode. Typically used to power down an external TTL to RS232 level converter IC in USB to RS232 converter designs.
**CLK30	ACBUS0, ACBUS5, ACBUS6,ACBUS8, ACBUS9	30MHz Clock output.

ACBUS Signal Option	Available On ACBUS Pin	Description
**CLK15	ACBUS0, ACBUS5, ACBUS6,ACBUS8, ACBUS9	15MHz Clock output.
**CLK7.5	ACBUS0, ACBUS5, ACBUS6,ACBUS8, ACBUS9	7.5MHz Clock output.
TriSt-PU	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	Input Pull Up
DRIVE 1	ACBUS0, ACBUS5, ACBUS6,ACBUS8, ACBUS9	Output High
DRIVE 0	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	Output Low
I/O mode	ACBUS5, ACBUS6,ACBUS8,ACBUS9	ACBUS Bit Bang

Table 8 – ACBUS Configuration Control

* Must be used with a 10kΩ resistor pull up.
**When in USB suspend mode the outputs clocks are also suspended.

3.7 Pin Configurations

The following section describes the function of the pins when the device is configured in different modes of operation.

3.7.1 FT233HP/232HP pins used in an UART interface

The FT233HP/FT232HP can be configured as a UART interface. When configured in this mode, the pins used, and the descriptions of the signals are shown in Table 9.

64 Pin No.	56 pin No	Name	Type	UART Configuration Description
28	23	TXD	OUTPUT	TXD = transmitter output
29	24	RXD	INPUT	RXD = receiver input
30	25	RTS#	OUTPUT	RTS# = Ready To send handshake output
31	26	CTS#	INPUT	CTS# = Clear To Send handshake input
32	27	DTR#	OUTPUT	DTR# = Data Transmit Ready modem signalling line
34	29	DSR#	INPUT	DSR# = Data Set Ready modem signalling line
35	30	DCD#	INPUT	DCD# = Data Carrier Detect modem signalling line
36	31	RI#	INPUT	RI# = Ring Indicator Control Input. When the Remote Wake up option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend. (see note 1,2,3 and 4)
37	32	** TXDEN	OUTPUT	TXDEN = (TTL level). Use to enable RS485 level converter
40	35	** RXLED	OUTPUT	RXLED = Receive signalling output. Pulses low when receiving data (RXD) from the external device (UART Interface). This should be connected to an LED.
42	37	** TXLED	OUTPUT	TXLED = Transmit signalling output. Pulses low when transmitting data (TXD) to the external device (UART Interface). This should be connected to an LED.

Table 9 – UART Configured Pin Descriptions

** ACBUS I/O pins

For a functional description of this mode, please refer to Section 4.3.

Note 1: UART is the device default mode.

Note 2:

1. When using remote wake-up, ensure the resistors are pulled-up in suspend. Also ensure peripheral designs do not allow any current sink paths that may partially power the peripheral.
2. A peripheral is allowed to draw up to 2.5mA in suspend.
3. If a Pull-down is enabled, the FT233HP/FT232HP will not wake up from suspend when using SIWU#
4. In UART mode the RI# pin acts as the wake-up pin.

3.7.2 FT233HP/FT232HP Pins used in an FT245 Synchronous FIFO Interface

The FT233HP/FT232HP can be configured as a FT245 synchronous FIFO interface. When configured in this mode, the pins used, and the descriptions of the signals are shown in Table 10. To set this mode the external EEPROM must be set to 245 modes. A software command (FT_SetBitMode) is then sent by the application to the FTDI D2XX driver to tell the chip to enter 245 synchronous FIFO mode. In this mode, data is written or read on the rising edge of the CLKOUT.

64 Pin No.	56 Pin No	Name	Type	FT245 Configuration Description
28,29,30, 31,32,34, 35,36	23,24,25, 26,27,29, 30,31	ADBUS[7:0]	I/O	D7 to D0 bidirectional FIFO data. This bus is normally input unless OE# is low.
37	32	RXF#	OUTPUT	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by driving RD# low. When in synchronous mode, data is transferred on every clock that RXF# and RD# are both low. Note that the OE# pin must be driven low at least 1 clock period before asserting RD# low.
38	33	TXE#	OUTPUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by driving WR# low. When in synchronous mode, data is transferred on every clock that TXE# and WR# are both low.
39	34	RD#	INPUT	Enables the current FIFO data byte to be driven onto D0...D7 when RD# goes low. The next FIFO data byte (if available) is fetched from the receive FIFO buffer each CLKOUT cycle until RD# goes high.
40	35	WR#	INPUT	Enables the data byte on the D0...D7 pins to be written into the transmit FIFO buffer when WR# is low. The next FIFO data byte is written to the transmit FIFO buffer each CLKOUT cycle until WR# goes high.
42	37	SIWU#	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM, strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device RX buffer will be sent out over USB on the next Bulk-IN request

				from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used.
43	38	CLKOUT	OUTPUT	60 MHz Clock driven from the chip. All signals should be synchronized to this clock.
44	39	OE#	INPUT	Output enable when low to drive data onto D0-7. This should be driven low at least 1 clock period before driving RD# low to allow for data buffer turn-around.

Table 10 – FT245 Synchronous FIFO Configured Pin Descriptions

For functional description of this mode, please refer to Section 4.5. Also refer to TN_167 FTDI FIFO Basics.

3.7.3 FT233HP/FT232HP Pins used in an FT245 Style asynchronous FIFO Interface

The FT233HP/FT232HP can be configured as a FT245 style asynchronous FIFO interface. When configured in this mode, the pins used, and the descriptions of the signals are shown in Table 11. To enter this mode the external EEPROM must be set to 245 asynchronous FIFO mode. In this mode, data is written or read on the falling edge of the RD# or WR# signals.

64 Pin No.	56 pin No	Name	Type	FT245 Configuration Description
28,29,30, 31,32,34, 35,36	23,24,25, 26,27,29, 30,31	ADBUS[7:0]	I/O	D7 to D0 bidirectional FIFO data. This bus is normally input unless RD# is low.
37	32	RXF#	OUTPUT	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by driving RD# low. When RD# goes high again RXF# will always go high and only become low again if there is another byte to read. During reset this signal pin is tristate but pulled up to VCCIO via an internal 200kΩ resistor.
38	33	TXE#	OUTPUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR# high, then low. During reset this signal pin is tristate but pulled up to VCCIO via an internal 200kΩ resistor.
39	34	RD#	INPUT	Enables the current FIFO data byte to be driven onto D0...D7 when RD# goes low. Fetches the next FIFO data byte (if available) from the receive FIFO buffer when RD# goes high.
40	35	WR#	INPUT	Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when WR# goes from high to low.
42	37	SIWU#	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM, strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device RX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used.

Table 11 - FT245 Style Asynchronous FIFO Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.6. Also refer to TN_167 FTDI FIFO Basics.

3.7.4 FT233HP/232HP Configured as Synchronous/ Asynchronous Bit-Bang Interface

Bit-bang mode is an FTDI FT233HP/FT232HP device mode that changes the 8 IO lines into an 8-bit bi-directional data bus. This mode is enabled by sending a software command (FT_SetBitMode) to the FTDI driver. When configured in any bit-bang mode, the pins used, and the descriptions of the signals are shown in Table 12.

64 Pin No.	56 Pin No	Name	Type	Bit-Bang Interface Configuration Description
28,29,30, 31,32,34, 35,36	23,24,25, 26,27,29, 30,31	ADBUS[7:0]	I/O	D7 to D0 bidirectional Bit-Bang parallel I/O data pins
38	33	WRSTB#	OUTPUT	Write strobe, active low output indicates when new data has been written to the I/O pins from the Host PC (via the USB interface).
39	34	RDSTB#	OUTPUT	Read strobe, this output rising edge indicates when data has been read from the parallel I/O pins and sent to the Host PC (via the USB interface).
42	37	SIWU#	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM, strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device RX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used.

Table 12 - Synchronous or Asynchronous Bit-Bang Configured Pin Descriptions

For functional description of this mode, please refer to Section 4.7.

3.7.5 FT233HP/FT232HP Pins used in an MPSSE

The FT233HP/FT232HP has a Multi-Protocol Synchronous Serial Engine (MPSSE). This mode is enabled by sending a software command (FT_SetBitMode) to the FTDI D2xx driver. The MPSSE can be configured to a number of industry standard serial interface protocols such as JTAG, I^2C (MASTER) or SPI (MASTER), or it can be used to implement a proprietary bus protocol. For example, it is possible to connect FT233HP/FT232HP's to an SRAM configurable FPGA such as supplied by Altera or Xilinx. The FPGA device would normally not be configured (i.e., have no defined function) at power-up. Application software on the PC could use the MPSSE (and D2XX driver) to download configuration data to the FPGA over USB. This data would define the hardware function on power up. The MPSSE can be used to control a number of GPIO pins. When configured in this mode, the pins used, and the descriptions of the signals are shown in Table 13.

64 Pin No.	56 Pin No	Name	Type	MPSSE Configuration Description
28	23	TCK/SK	OUTPUT	Clock Signal Output. For example: JTAG – TCK, Test interface clock SPI (MASTER) – SK, Serial Clock I^2C – SCK, Serial Clock Line

29	24	TDI/DO	OUTPUT	Serial Data Output. For example: JTAG – TDI, Test Data Input SPI (MASTER) – DO I²C – SDA, Serial Data Line*
30	25	TDO/DI	INPUT	Serial Data Input. For example: JTAG – TDO, Test Data output SPI (MASTER) – DI, Serial Data Input I²C – SDA, Serial Data Line*
31	26	TMS/CS	OUTPUT	Output Signal Select. For example: JTAG – TMS, Test Mode Select SPI (MASTER) – CS, Serial Chip Select
32	27	GPIOL0	I/O	General Purpose input/output
34	29	GPIOL1	I/O	General Purpose input/output
35	30	GPIOL2	I/O	General Purpose input/output
36	31	GPIOL3	I/O	General Purpose input/output
37	32	GPIOH0	I/O	General Purpose input/output
38	33	GPIOH1	I/O	General Purpose input/output
39	34	GPIOH2	I/O	General Purpose input/output
40	35	GPIOH3	I/O	General Purpose input/output
42	37	GPIOH4	I/O	General Purpose input/output
43	38	GPIOH5	I/O	General Purpose input/output
44	39	GPIOH6	I/O	General Purpose input/output
47	42	GPIOH7	I/O	General Purpose input/output

Table 13 - MPSSE Configured Pin Descriptions

*: The DI and DO pins need connected to create the full SDA signal for I²C. The DO pin requires configuration as an input except when transmitting to avoid driver contention during a slave transmission. For functional description of this mode, please refer to Section 4.8.

3.7.6 FT233HP/FT232HP Pins used as a Fast Serial Interface

The FT233HP/FT232HP can be configured for use with high-speed bi-directional isolated serial data. A proprietary FTDI protocol designed to allow galvanic isolated devices to communicate synchronously with the FT233HP/FT232HP using just 4 signal wires (over two dual opto-isolators), and two power lines. The peripheral circuitry controls the data transfer rate in both directions, whilst maintaining full data integrity. 12 Mbps (USB full speed) data rates can be achieved when using the proper high speed opto-isolators (see App Note AN-131). When configured in this mode, the pins used, and the descriptions of the signals are shown in Table 14.

Table 14 - Fast Serial Interface Configured Pin Descriptions

64 Pin No.	56 Pin No	Name	Type	Fast Serial Interface Configuration Description
28	23	FSDI	INPUT	Fast serial data input.
29	24	FSCLK	INPUT	Fast serial clock input. Clock input to FT233HP/FT232HP chip to clock data in or out.
30	25	FSDO	OUTPUT	Fast serial data output.
31	26	FSCTS	OUTPUT	Fast serial Clear To Send signal output. Driven low to indicate that the chip is ready to send data
42	37	SIWU#	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM, strobing this pin low will cause the device to request a resume on the USB

				Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device RX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used.

Table 14 - Fast Serial Interface Configured Pin Descriptions

For a functional description of this mode, please refer to Section 4.

3.7.7 FT233HP/FT232HP Pins Configured as a CPU-style FIFO Interface

The FT233HP/FT232HP can be configured in a CPU-style FIFO interface mode which allows a CPU to interface to USB via the FT233HP/FT232HP. This mode is enabled in the external EEPROM. When configured in this mode, the pins used, and the descriptions of the signals are shown in Table 15.

Table 15 - CPU-Style FIFO Interface Configured Pin Descriptions

64 Pin No.	56 Pin No	Name	Type	CPU-style FIFO Interface Configuration Description
28,29,30, 31,32,34, 35,36	23,24,25, 26,27,29, 30,31	ADBUS[7:0]	I/O	D7 to D0 bidirectional data bus
37	32	CS#	INPUT	Active low chip select input
38	33	A0	INPUT	Address bit A0
39	34	RD#	INPUT	Active Low FIFO Read input
40	35	WR#	INPUT	Active Low FIFO Write input

Table 15 - CPU-Style FIFO Interface Configured Pin Descriptions

For a functional description of this mode, please refer to Section 4.10.

3.7.8 FT233HP/FT232HP Pins Configured as a FT1248 Interface

The FT233HP/FT232HP can be configured as a proprietary FT1248 interface. This mode is enabled in the external EEPROM. When configured in this mode, the pins used, and the descriptions of the signals are shown in Table 16.

64 Pin No.	56 Pin No	Name	Type	FT1248 Interface Configuration Description
28	23	MIOSIO0	INPUT /OUTPUT	Bi-directional synchronous command and data bus, bit 0 used to transmit and receive data from/to the master
29	24	MIOSIO1	INPUT /OUTPUT	Bi-directional synchronous command and data bus, bit 1 used to transmit and receive data from/to the master
30	25	MIOSIO2	INPUT /OUTPUT	Bi-directional synchronous command and data bus, bit 2 used to transmit and receive data from/to the master
31	26	MIOSIO3	INPUT /OUTPUT	Bi-directional synchronous command and data bus, bit 3 used to transmit and receive data from/to the master
32	27	MIOSIO4	INPUT /OUTPUT	Bi-directional synchronous command and data bus, bit 4 used to transmit and receive data from/to the master
34	29	MIOSIO5	INPUT /OUTPUT	Bi-directional synchronous command and data bus, bit 5 used to transmit and receive data from/to the master

35	30	MIOSIO6	INPUT /OUTPUT	Bi-directional synchronous command and data bus, bit 6 used to transmit and receive data from/to the master
36	31	MIOSIO7	INPUT /OUTPUT	Bi-directional synchronous command and data bus, bit 7 used to transmit and receive data from/to the master
37	32	SCLK	INPUT	Serial clock used to drive the slave device data
38	33	SS_n	INPUT	Active low slave select 0 from master to slave
39	34	MISO	OUTPUT	Slave output used to transmit the status of the transmit and receive buffers are empty and full respectively

Table 16 - FT1248 Configured Pin Descriptions

For functional description of this mode, please refer to Section 4.6.

4 Function Description

The FT233HP/FT232HP is a USB 2.0 Hi-Speed (480Mb/s) to UART/FIFO IC with USB Type-C/PD ports. It can be configured in a variety of industry standard serial or parallel interfaces, such as UART, FIFO, JTAG, SPI (MASTER) or I^2C (MASTER) modes. In addition to these, the FT233HP/FT232HP introduces the FT1248 interface and supports a CPU-Style FIFO mode, bit-bang, and a fast serial interface mode.

The FT233HP has two Type-C/PD ports, with PD1 port supporting both power sink and source roles, and PD2 port (FT233HPQ and FT233HPL only) working as a power sink port. Both PD ports support 5V3A, 9V3A, 12V3A, 15V3A and 20V3A PDO profiles, and these profiles are configurable through the external EEPROM at power-up or reset. PD1 port shares the same Type-C connector with USB data, and the PD2 port is a power port only without USB data.

4.1 Key Features

USB Type-C/PD Controller. The FT233HP/FT232HP supports USB Type-C specification version 1.3. The FT233HP/FT232HP integrates a USB PD 3.0 controller. USB PD port 1 is USB PD3.0 with the USB 2.0 function. The first USB PD power is initial power sink when local power source is presented, it can become power source via PD negotiation. The FT233HP has a second USB PD sink only port to connect to a PD power source. The FT233HP/FT232HP USB PD 3.0 function is backward compatible to the USB PD 2.0 standard.

USB Hi-Speed to UART/FIFO Interface. The FT233HP/FT232HP provides USB 2.0 Hi-Speed (480Mbits/s) to flexible and configurable UART/FIFO Interfaces.

Functional Integration. The FT233HP/FT232HP integrates a USB protocol engine which controls the physical Universal Transceiver Macrocell Interface (UTMI) and handles all aspects of the USB 2.0 Hi-Speed interface. The FT233HP/FT232HP includes an integrated +1.2V Low Drop-Out (LDO) regulator. It also includes 1Kbytes Tx and Rx data buffers. The FT233HP/FT232HP integrates the entire USB protocol on chip with no firmware required.

MPSSE. Multi- Protocol Synchronous Serial Engines (MPSSE), capable of speeds up to 30 Mbits/s, provides flexible synchronous interface configurations.

FT1248 interface. The FT233HP/FT232HP supports a new proprietary half-duplex FT1248 interface with a variable bi-directional data bus interface that can be configured as 1, 2, 4, or 8-bits wide and this enables the flexibility to expand the size of the data bus to 8 pins. For details regarding 2-bit, 4-bit and 8-bit modes, please refer to application note AN_167 FT1248 Serial Parallel Interface Basics.

Data Transfer rate. The FT233HP/FT232HP supports a data transfer rate up to 12 Mbaud when configured as an UART RS232/RS422/RS485 interface up to 40 Mbytes/second over a synchronous 245 parallel FIFO interface or up to 8 Mbyte/Sec over an asynchronous 245 FIFO interface. Please note the FT233HP/FT232HP does not support the baud rates of 7 Mbaud 9 Mbaud, 10 Mbaud and 11 Mbaud. Only limited high speed baud rates are possible down to 6Mbaud, below this rate the divider and sub-integer dividers start to have effect offering a wider range of baud rates.

Latency Timer. A feature of the driver used as a timeout to transmit short packets of data back to the PC. The default is 16ms, but it can be altered between 2ms and 255ms. Lower values may reduce latency but may also increase USB bandwidth usage and reduce efficiency.

Bus (ACBUS) functionality, signal inversion and drive strength selection. There are 11 configurable ACBUS I/O pins. These configurable options are:

1. **TXDEN** – transmit enable for RS485 designs.
2. **PWREN#** - Power control for high power, bus powered designs.
3. **TXLED#** - for pulsing an LED upon transmission of data.
4. **RXLED#** - for pulsing an LED upon receiving data.
5. **TX&RXLED#** - which will pulse an LED upon transmission OR reception of data**.**
6. **SLEEP#** - indicates that the device going into USB suspend mode.
7. **CLK30 / CLK15 / CLK7.5 –** 30MHz, 15MHz and 7.5MHz clock output signal options.
8. **TriSt-PU** – Input pulled up, not used
9. **DRIVE 1** – Output driving high

10. **DRIVE 0** – Output driving low
11. **I/O mode** – ACBUS Bit Bang

The ACBUS pins can also be individually configured as GPIO pins, similar to asynchronous bit bang mode. It is possible to use this mode while the UART interface is being used, thus providing up to 4 general purpose I/O pins (ACBUS 5, 6, 8 and 9) which are available during normal operation. The ACBUS lines can be configured with any one of these input/output options by setting bits in the external EEPROM.

4.2 Functional Block Descriptions

Type-C/PD PHY and Controller. The FT233HP (FT233HPQ and FT233HPL only) has two Type-C/PD ports. Each port has Type-C/PD required Physical Layer (PHY) and controllers. PD1 port has built-in VCONN switches supporting up to 660mW VCONN power.

PD Policy Engine. The PD policy engine is a 32bit RISC processor with 8kB data RAM and 48kB ROM. It manages both PD port 1 and port 2. Default PD configurations are stored in the ROM code. PD1 port can act as power sink or source role, supporting both normal power role swap. PD2 port (FT233HPQ and FT233HPL only) acts as power sink, which can be connected to a PD charger. By using an external EEPROM, it is possible to change the PD configuration based for specific use cases, such as port 1 sink, port 1 sink/source or PD charge through from port 2 to port 1. PDO voltage/current profiles can also be customised using EEPROM.

I2C Slave Interface. The application can also choose to control the PD policy by external MCU through I2C interface. In this case the built-in PD policy engine is halted. The external MCU has full control to the two PD controller registers (FT233HPQ and FT233HPL only) through I2C access. An interrupt signal is also provided, so that an interrupt to an external MCU could be asserted when a PD event occurs.

GPIO block. The GPIO block provides up to 8 GPIO pins which can be used as power switch controls based on the PD policy and profiles.

Multi-Purpose UART/FIFO Controllers. The FT233HP/FT232HP has one independent UART/FIFO Controller. This controls the UART data, 245 FIFO data, Fast Serial (opto isolation) or Bit-Bang mode which can be selected by SETUP (FT_SetBitMode) command. Each Multi-Purpose UART/FIFO Controller also contains an MPSSE (Multi-Protocol Synchronous Serial Engine). Using this MPSSE, the Multi-Purpose UART/FIFO Controller can be configured under software command, to have one of the MPSSE (SPI (MASTER), I^2C, and JTAG).

USB Protocol Engine and FIFO control. The USB Protocol Engine controls and manages the interface between the UTMI PHY and the FIFOs of the chip. It also handles power management and the USB protocol specification.

Port FIFO TX Buffer (1Kbytes). Data from the Host PC is stored in these buffers to be used by the Multi-purpose UART/FIFO controllers. This is controlled by the USB Protocol Engine and FIFO control block.

Port FIFO RX Buffer (1Kbytes). Data from the Multi-purpose UART/FIFO controllers is stored in these blocks to be sent back to the Host PC when requested. This is controlled by the USB Protocol Engine and FIFO control block.

RESET Generator – The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input (with min pulse width 1.5 ms) pin allows an external device to reset the FT233HP/FT232HP. RESET# should be tied to VCCIO (+3.3V) if not being used.

Baud Rate Generators – The Baud Rate Generators provides an x16 or an x10 clock input to the UART's from a 120MHz reference clock and consists of a 14-bit pre-scaler and 4 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction). This determines the Baud Rate of the UART which is programmable from 183 baud to 12 Mbaud. See FTDI application note AN_120 Aliasing VCP Baud Rates for more details.

EEPROM Interface. EEPROM is mandatory for configuration of PD Port and the power profiles. Adding an external EEPROM allows customization of USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT233HP/FT232HP for OEM applications, as well as PD port configurations and power profiles. Other parameters controlled by the EEPROM include Remote Wake Up, Soft Pull Down on Power-Off and I/O pin drive strength.

The EEPROM must have a 16-bit wide configuration such as a Microchip 93LC66B or equivalent capable of

a 1Mbit/s clock rate at VCC = 3.0V to 3.6V. The EEPROM is programmable in-circuit over USB using a utility program called FT_PROG available from FTDI's web site – https://ftdichip.com/. This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process.

If no EEPROM is connected (or the EEPROM is blank), the FT233HP/FT232HP will default to serial ports. The device uses its built-in default VID (0403), PID (6044/6045), Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor. As for the power delivery configuration, please refer to AN_448 for FT233HP and AN_551 for FT232HP.

LDO Regulator. The +1.2V LDO regulator generates the +1.2 volts for the core and the USB transceiver cell. Its input (VREGIN) must be connected to a +3.3V external power source. It is also recommended to add an external filtering capacitor to the VREGIN. There is no direct connection from the +1.2V output (VREGOUT) and the internal functions of the FT233HP/FT232HP. The PCB must be routed to connect VREGOUT to the pins that require the +1.2V including VREGIN.

UTMI PHY. The Universal Transceiver Macrocell Interface (UTMI) physical interface cell. This block handles the Full speed / Hi-Speed SERDES (serialise – de-serialise) function for the USB TX/RX data. It also provides the clocks for the rest of the chip. A 12 MHz crystal with ±30ppm must be connected to the OSCI and OSCO pins or 12 MHz Oscillator must be connected to the OSCI, and the OSCO is left unconnected. A 12K Ohm resistor should be connected between REF and GND on the PCB.

The UTMI PHY functions include:

- Supports 480 Mbit/s "Hi-Speed" (HS)/ 12 Mbit/s "Full Speed" (FS).
- SYNC/EOP generation and checking
- Data and clock recovery from serial stream on the USB.
- Bit-stuffing/un-stuffing; bit stuff error detection.
- Manages USB Resume, Wake Up and Suspend functions.
- Single parallel data clock output with on-chip PLL to generate higher speed serial data clocks.

4.3 FT233HP/FT232HP UART Interface Mode Description

The FT233HP/FT232HP can be configured as a UART with external line drivers, similar to operation with the FTDI FT232R devices. The following examples illustrate how to configure the FT233HP/FT232HP with an RS232, RS422 or RS485 interface.

4.3.1 RS232 Configuration

Figure 5 illustrates how the FT233HP/FT232HP can be configured with an RS232 interface.

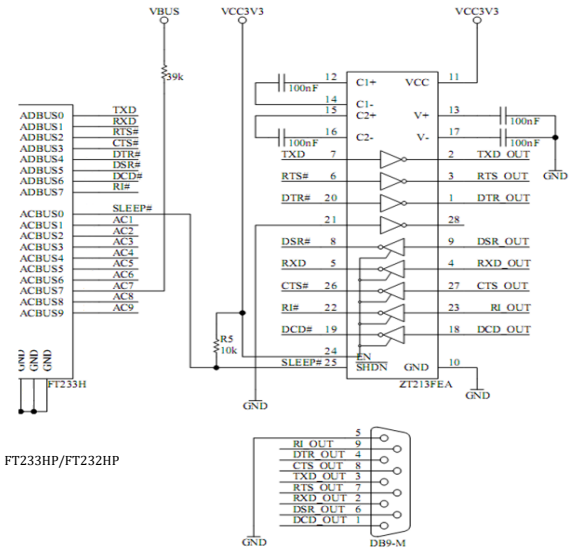


Figure 5 - RS232 Configuration

4.3.2 RS422 Configuration

Figure 6 illustrates how the FT233HP/FT232HP can be configured as a RS422 interface.

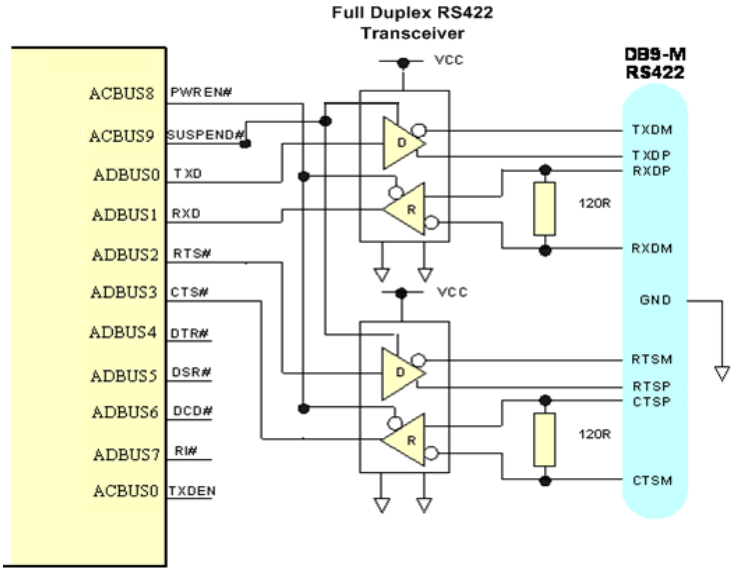


Figure 6 - RS422 Configuration

In this case the FT233HP/FT232HP is configured as UART operating at TTL levels and a level converter device (full duplex RS485 transceiver) is used to convert the TTL level signals from the FT233HP/FT232HP to RS422 levels. The PWREN# signal is used to power down the level shifters such that they operate in a low quiescent current when the USB interface is in suspend mode.

4.3.3 RS485 Configuration

Figure 7 illustrates how the FT233HP/FT232HP can be configured as a RS485 interface.

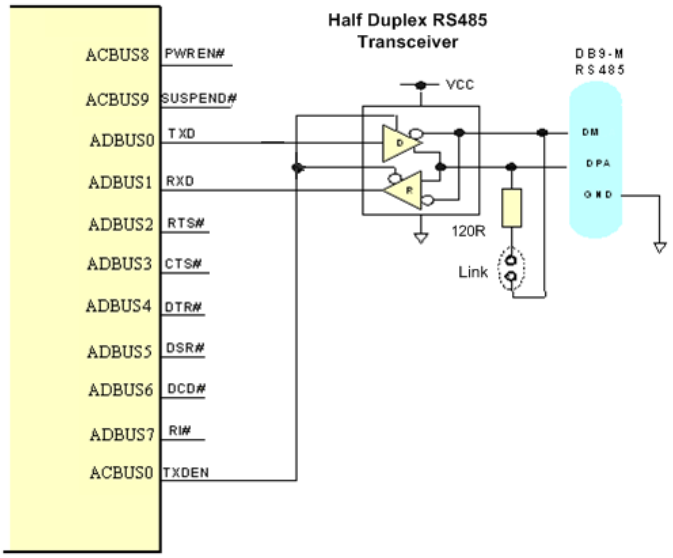


Figure 7 - RS485 Configuration

In this case the FT233HP/FT232HP is configured as a UART operating at TTL levels and a level converter device (half duplex RS485 transceiver) is used to convert the TTL level signals from the FT233HP/FT232HP to RS485 levels. With RS485, the transmitter is only enabled when a character is being transmitted from the UART. The TXDEN pin on the FT233HP/FT232HP is provided for exactly that purpose, and so the transmitter enables are wired to the TXDEN. RS485 is a multi-drop network – i.e., many devices can communicate with each other over a single two wire cable connection. The RS485 cable requires to be

terminated at each end of the cable. Links are provided to allow the cable to be terminated if the device is physically positioned at either end of the cable.

4.4 FT245 Synchronous FIFO Interface Mode Description

When FT233HP/FT232HP is configured in an FT245 Synchronous FIFO interface mode the IO timing of the signals used are shown in Figure 8 which shows details for read and write accesses. The timings are shown in Table 17. Note that only a read or a write cycle can be performed at any one time. Data is read or written on the rising edge of the CLKOUT clock.

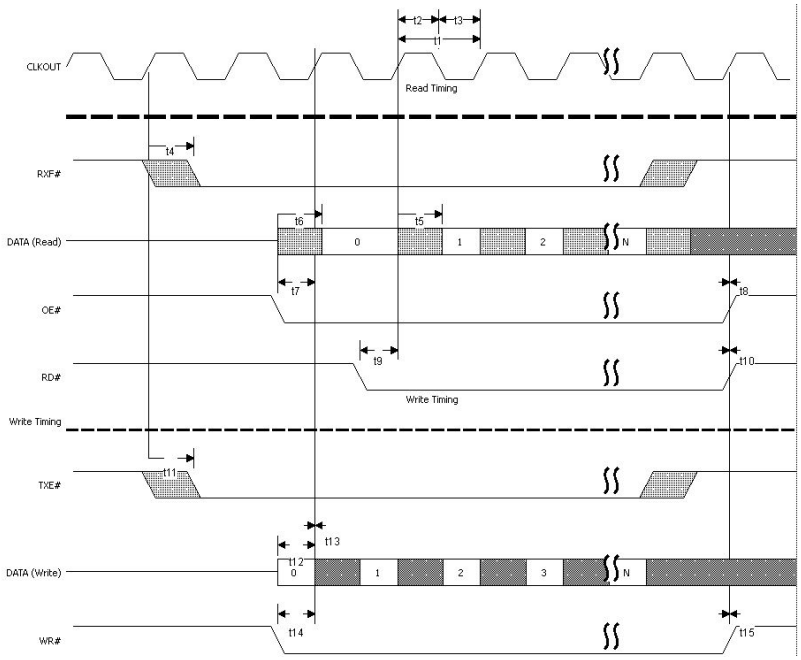


Figure 8 - FT245 Synchronous FIFO Interface Signal Waveforms

Name	Min	Nom	Max	Units	Comments
t1		16.67		ns	CLKOUT period
t2		8.33		ns	CLKOUT high period
t3		8.33		ns	CLKOUT low period
t4	1.4		9	ns	CLKOUT to RXF#
t5	2.4		9	ns	CLKOUT to read DATA valid
t6	2.4		9	ns	OE# to read DATA valid
t7	8		16.67	ns	OE# setup time
t8	0			ns	OE# hold time
t9	7.5		16.67	ns	RD# setup time to CLKOUT (RD# low after OE# low)
t10	0			ns	RD# hold time
t11	1		9	ns	CLKOUT TO TXE#
t12	8		16.67	ns	Write DATA setup time
t13	0			ns	Write DATA hold time
t14	8		16.67	ns	WR# setup time to CLKOUT (WR# low after TXE# low)
t15	0				WR# hold time

Table 17 - FT245 Synchronous FIFO Interface Signal Timings

This mode uses a synchronous interface to get high data transfer speeds. The chip drives a 60 MHz CLKOUT clock for the external system to use.

Note that Asynchronous FIFO mode must be selected in the EEPROM before selecting the Synchronous FIFO mode in software.

4.4.1 FT245 Synchronous FIFO Read Operation

A read operation is started when the chip drives RXF# low. The external system can then drive OE# low to turn the data bus drivers around before acknowledging the data with the RD# signal going low. The first data byte is on the bus after OE# is low. The external system can burst the data out of the chip by keeping RD# low or it can insert wait states in the RD# signal. If there is more data to be read it will change on the clock following RD# sampled low. Once all the data has been consumed, the chip will drive RXF# high. Any data that appears on the data bus, after RXF# is high, is invalid and should be ignored.

4.4.2 FT245 Synchronous FIFO Write Operation

A write operation can be started when TXE# is low. WR# is brought low when the data is valid. A burst operation can be done on every clock providing TXE# is still low. The external system must monitor TXE# and its own WR# to check that data has been accepted. Both TXE# and WR# must be low for each byte of data to be accepted.

4.5 FT245 Style Asynchronous FIFO Interface Mode Description

The FT233HP/FT232HP can be configured as an asynchronous FIFO interface. This mode is similar to the synchronous FIFO interface with the exception that the data is written to or read from the FIFO on the falling edge of the WR# or RD# signals.

This mode does not provide a CLKOUT signal, and it does not expect an OE# input signal. Figure 9 and Figure 10 illustrates the asynchronous FIFO mode timing.

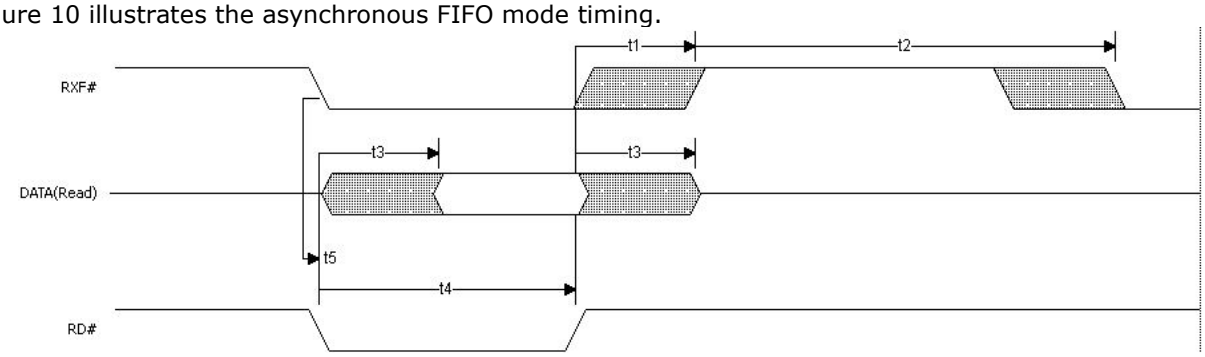


Figure 9 - FT245 Asynchronous FIFO Interface READ Signal Waveforms

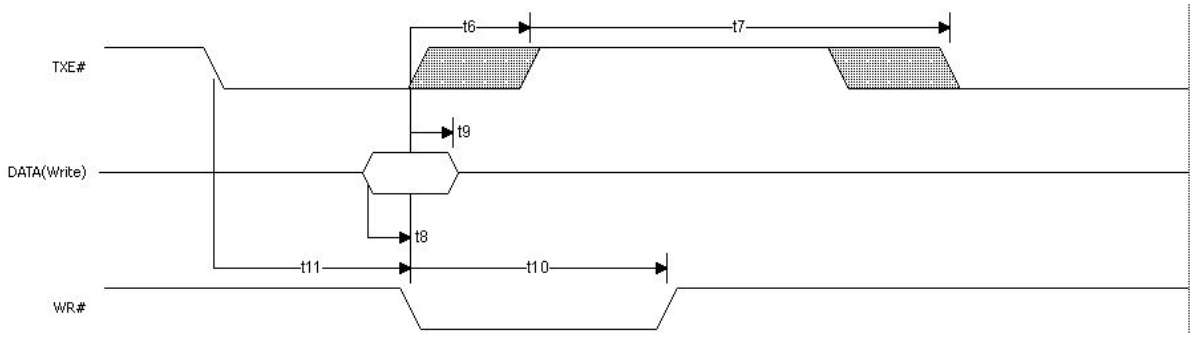


Figure 10 - FT245 Asynchronous FIFO Interface WRITE Signal Waveforms

Time	Description	Min	Max	Units
T1	RD# inactive to RXF#	1	14	Ns
T2	RXF# inactive after RD# cycle	49		Ns
T3	RD# to DATA	1	14	Ns
T4	RD# active pulse width	30		Ns

T5	RD# active after RXF#	0		Ns
T6	WR# active to TXE# inactive	1	14	Ns
T7	TXE# active to TXE# after WR# cycle	49		Ns
T8	DATA to WR# active setup time	5		Ns
T9	DATA hold time after WR# inactive	5		Ns
T10	WR# active pulse width	30		Ns
T11	WR# active after TXE#	0		Ns

Table 18 - Asynchronous FIFO Timings (based on standard drive level outputs)

4.6 FT1248 Interface Mode Description

The FT233HP/FT232HP supports a half-duplex FT1248 Interface that provides a flexible data communication and high-performance interface between the FT233HP/FT232HP as a FT1248 slave and an external FT1248 master. The FT1248 protocol is a dynamic bi-directional data bus interface that can be configured as 1, 2, 4, or 8-bits wide.

Figure 11 - FT1248 Bus with Single Master and Slave

In the FT1248 there are 3 distinct phases:

While SS_n is inactive, the FT1248 reflects the status of the write buffer and read buffers on the MIOSIO[0] and MISO wires respectively. Additionally, the FT1248 slave block supports multiple slave devices where a master can communicate with multiple FT1248 slave devices. When the slave is sharing buses with other FT1248 slave devices, the write and read buffer status cannot be reflected on the MIOSIO[0] and MISO wires during SS_n inactivity as this would cause bus contention. Therefore, it is possible for the user to select whether they wish to have the buffer status switched on or off during inactivity. When SS_n is active a command/bus size phase occurs first. Following the command phase is the data phase, for each data byte transferred the FT1248 slave drives an ACK/NAK status onto the MISO wire. The master can send multiple data bytes so long as SS_n is active, if an unsuccessful data transfer occurs, i.e., a NAK happens on the MISO wire then the master should immediately abort the transfer by de-asserting SS_n.

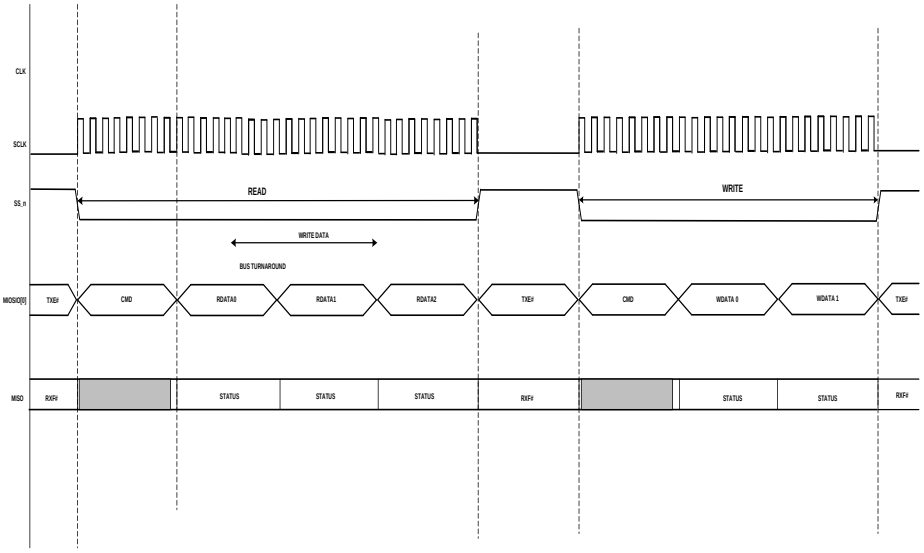


Figure 12 - FT1248 Basic Waveform Protocol

Section 4.6.2 illustrates the FT1248 write and read protocol operating in 1-bit mode. For details regarding 2-bit, 4-bit and 8-bit modes, please refer to application note AN_167 FT1248 Parallel Serial Interface Basics.

4.6.1 Bus Width Protocol Decode

In order for the FT1248 master to determine the bus width within the command phase the bus width is encoded along with the actual commands on the first active clock edge when SS_n is active and has a data width of 8-bits.

If any of the MIOSIO [7:4] signals are low then the data transfer width equals 8-bits.

If any of the MIOSIO [3:2] signals are low then the data transfer width equals 4-bits.

If MIOSIO [1] signal is low then the data transfer width equals 2-bits.

Else the bus width is defaulted to 1-bit.

Please note that if both of the MIOSIO bit signals are low then the data transfer width is equal to the width of high priority MIOSIO bit signal. For example, if both of the MIOSIO [7:3] signals are low then the data transfer width equals 8-bits or if both of the MIOSIO [3:1] signals are low then the data transfer width equals 4-bits.

In order to successfully decode the bus width, all MIOSIO signals must have pull up resistors. By default, all MIOSIO signals shall be seen by the FT233HP/FT232HP in FT1248 mode as logic '1'. This means that when a FT1248 master does not wish to use certain MIOSIO signals the slave (FT233HP/FT232HP) is still capable of determining the requested bus width since any unused MIOSIO signals shall be pull up in the slave.

The remaining bits used during the command phase are used to contain the command itself which means that it is possible to define up to 16 unique commands.

	LSB							MSB
	CMD[3]	BWID 2-bit	BWID 4-bit	CMD[2]	BWID 8-bit	CMD[1]	CMD[0]	X
	0	1	2	3	4	5	6	7
1-bit Bus Width	CMD[3]	X	X	CMD[2]	X	CMD[1]	CMD[0]	X
	0	1	2	3	4	5	6	7
2-bit Bus Width	CMD[3]	0	X	CMD[2]	X	CMD[1]	CMD[0]	X
	0	1	2	3	4	5	6	7
4-bit Bus Width	CMD[3]	X	0	CMD[2]	X	CMD[1]	CMD[0]	X
	0	1	2	3	4	5	6	7
8-bit Bus Width	CMD[3]	X	X	CMD[2]	0	CMD[1]	CMD[0]	X
	0	1	2	3	4	5	6	7

Figure 13 - FT1248 Command Structure

For more details about FT1248 Interface, please refer to application note AN_167 FT1248 Parallel Serial Interface Basics.

4.6.2 FT1248: 1-bit interface

The FT1248 Interface transfers data over different bus widths (1-bit, 2-bit, 4-bit, and 8-bit). Figure 14 and Figure 15 illustrates the waveform detailing the FT1248 write and read protocol operating in 1-bit mode with flow control. Please refer to the application notes AN_167 FT1248 Parallel Serial Interface Basics for more details regarding 1-bit without flow control, 2-bit, 4-bit and 8-bit modes.

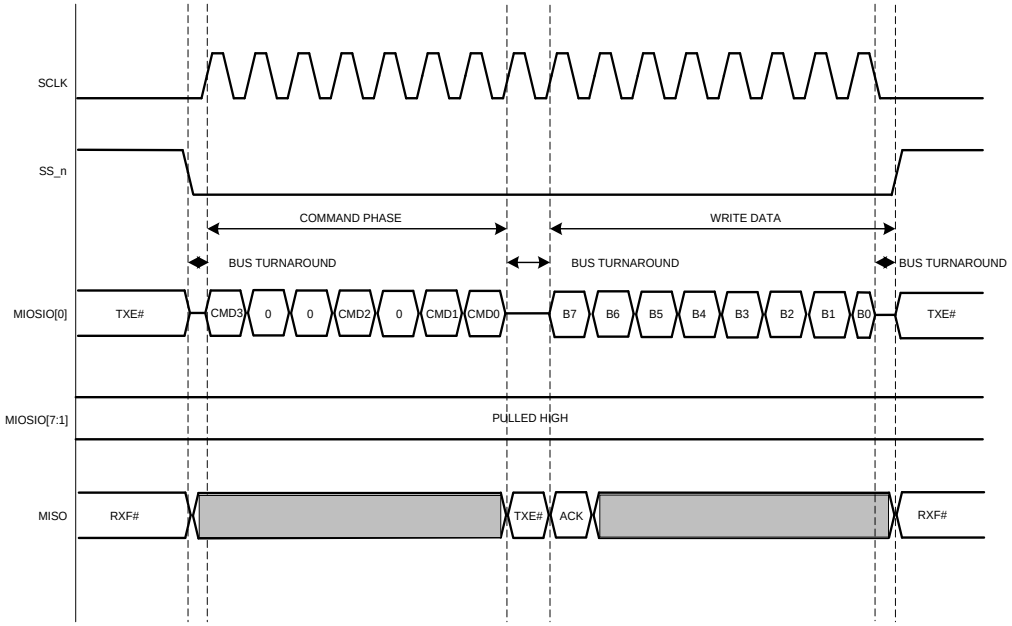


Figure 14 - FT1248 1-bit Mode Protocol (WRITE)

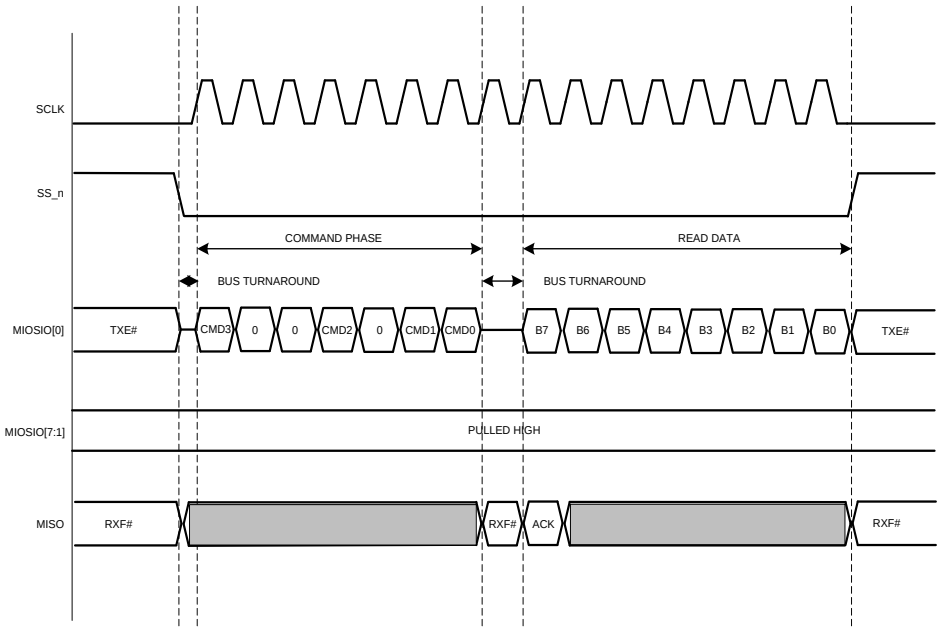


Figure 15 - FT1248 1-bit Mode Protocol (READ)

When SS_n is inactive the write buffer and read buffer status is reflected on the MIOSIO[0] and MISO signals respectively. When the master wishes to initiate a data transfer, SS_n becomes active. As soon as SS_n becomes active the SPI slave immediately stops driving the MIOSIO[0] signal and SPI master is not allowed to begin driving the MIOSIO[0] signal until the first clock edge, this ensures that bus contention is avoided.

On the first clock edge the command is shifted out for 7 clocks, on the 8th clock cycle a bus turnaround is required. The bus turnaround is required as the slave may be required to drive the MIOSIO[0] bus with read data. The data phase occurs in response to the command and so long as SS_n remains active. The data phase in 1-bit mode requires 8 clock cycles where the MIOSIO[0] signal transfers the requested write or read data. The MISO signal indicates to the master the success of the transfer with an ACK or NAK.

The status is reflected through the whole of the data phase and is valid from the first clock edge. If the master is writing data to the slave, then on the last clock edge before it de-asserts SS_n must tristate the MIOSIO[0] signal to enable the bus to be "turned" around as when SS_n becomes inactive the FT1248 slave shall begin to drive the write buffer status onto the MIOSIO[0] signal. When the SPI slave is driving the MIOSIO[0] (the master is reading data) no bus turnaround is required as when SS_n becomes inactive it is required to drive the write buffer status to the FT1248 master.

4.7 Synchronous and Asynchronous Bit-Bang Interface Mode

The FT233HP/FT232HP can be configured as a bit-bang interface. There are two types of bit-bang modes: synchronous and asynchronous. See application note AN2232-02 Bit Mode Functions for the FT232 for more details and examples of using both Synchronous and Asynchronous bit-bang modes.

4.7.1 Asynchronous Bit-Bang Mode

Asynchronous Bit-Bang mode is the same as BM-style Bit-Bang mode, except that the internal RD# and WR# strobes (RDSTB# and WRSTB#) are now brought out of the device to allow external logic to be clocked by accesses to the bit-bang IO bus.

Any data written to the device in the normal manner will be self-clocked onto the data pins (those which have been configured as outputs). Each pin can be independently set as an input or an output. The rate that the data is clocked out at is controlled by the baud rate generator.

New data must be written, and the baud rate clock should tick to change the data. If no new data is written to the chip, the pins configured for output will hold the last value written. Asynchronous Bit-Bang mode is enabled using the FT_SetBitMode D2xx driver command with a hex value of 0x01.

4.7.2 Synchronous Bit-Bang Mode

The synchronous Bit-Bang mode will only update the output parallel port pins whenever data is sent from the USB interface to the parallel interface. When this is done, the WRSTB# will activate to indicate that the data has been read from the USB Rx FIFO buffer and written out on the pins. Data can only be received from the parallel pins (to the USB Tx FIFO interface) after the parallel interface has been written to.

With Synchronous Bit-Bang mode data will only be sent out by the FT233HP/FT232HP if there is space in the FT233HP/FT232HP USB TXFIFO for data to be read from the parallel interface pins. This Synchronous Bit-Bang mode will read the data bus parallel I/O pins first before it transmits data from the USB RxFIFO. It is therefore 1 byte behind the output, and so to read the inputs for the byte that you have just sent, another byte must be sent.

For example:
(1)Pins start at 0xFF
Send 0x55, 0xAA
Pins go to 0x55 and then to 0xAA
Data read = 0xFF,0x55
(2) Pins start at 0xFF
Send 0x55, 0xAA, 0xAA
(repeat the last byte sent)
Pins go to 0x55 and then to 0xAA
Data read = 0xFF, 0x55, 0xAA

Synchronous Bit-Bang Mode differs from Asynchronous Bit-Bang mode in that the device parallel output is only read when the parallel output is written to by the USB interface. This makes it easier for the controlling program to measure the response to a USB output stimulus as the data returned to the USB interface is synchronous to the output data.

Synchronous Bit-Bang mode is enabled using Set Bit Bang Mode driver command with a hex value of 0x04. An example of the synchronous bit-bang mode timing is shown in Figure 16.

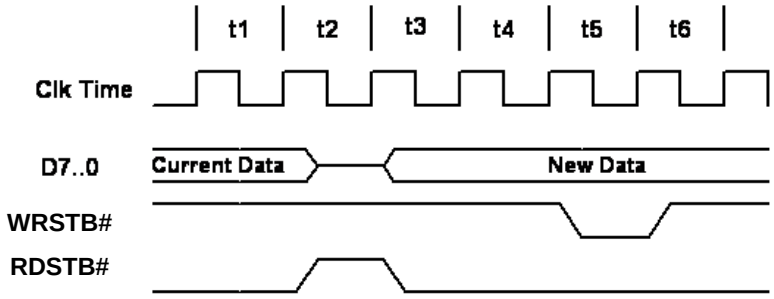


Figure 16 - Synchronous Bit-Bang Mode Timing Interface Example

Name	Description
t1	Current pin state is read
t2	RDSTB# is set inactive and data on the parallel I/O pins is read and sent to the USB host.
T3	RDSTB# is set active again, and any pins that are output will change to their new data
t4	1 clock cycle to allow for data setup
t5	WRSTB# goes active. This indicates that the host PC has written new data to the I/O parallel data pins
t6	WRSTB# goes inactive

Table 19 - Synchronous Bit-Bang Mode Timing Interface Example Timings

WRSTB# = this output indicates when new data has been written to the I/O pins from the Host PC (via the USB interface).

RDSTB# = this output rising edge indicates when data has been read from the I/O pins and sent to the Host PC (via the USB interface).

The WRSTB# goes active in t5. The WRSTB# goes active when data is read from the USB RXFIFO (i.e., sent from the PC). The RDSTB# goes inactive when data is sampled from the pins and written to the USB TXFIFO (i.e., sent to the PC). The SETUP command to the FT233HP/FT232HP is used to setup the bit-mode. This command also contains a byte wide data mask to set the direction of each bit. The direction on each pin doesn't change unless a new SETUP command is used to modify the direction.

The WRSTB# and RDSTB# strobes are only a guide to what may be happening depending on the direction of the bus. For example, if all pins are configured as inputs, it is still necessary to write to these pins in order to get the FT233HP/FT232HP to read those pins even though the data written will never appear on the pins.

Signals and data-flow are illustrated in Figure 17.

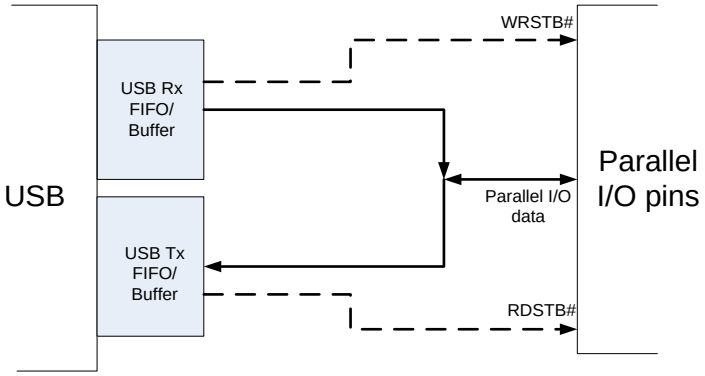


Figure 17 - Bit-Bang Mode Dataflow Illustration Diagram

4.8 MPSSE Interface Mode Description

MPSSE Mode is designed to allow the FT233HP/FT232HP to interface efficiently with synchronous serial protocols such as JTAG, I^2C (MASTER) and SPI (MASTER) Bus. It can also be used to program SRAM based FPGAs over USB. The MPSSE interface is designed to be flexible so that it can be configured to allow any synchronous serial protocol (industry standard or proprietary) to be implemented using the FT233HP/FT232HP.

MPSSE is fully configurable and is programmed by sending commands down the data stream. These can be sent individually or more efficiently in packets. MPSSE is capable of a maximum sustained data rate of 30 Mbits/s.

When the FT233HP/FT232HP is configured in MPSSE mode, the IO timing and signals used are shown in Figure 18 and Table 20. These show timings for CLKOUT=30MHz. CLKOUT can be divided internally to be provide a slower clock.

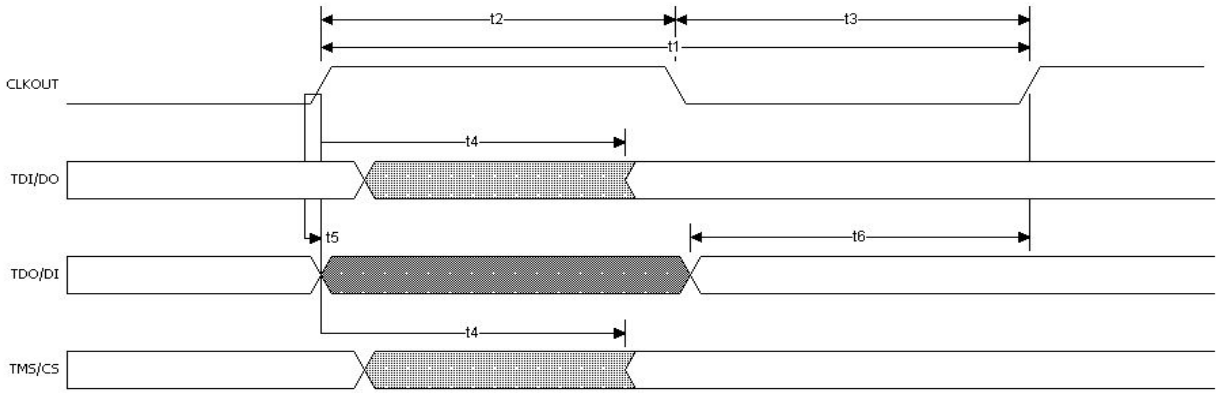


Figure 18 - MPSSE Signal Waveforms

Name	Min	Typ	Max	Units	Comments
t1	32.66	33.33	33.99	Ns	CLKOUT period
t2	15	16.67	18.33	Ns	CLKOUT high period
t3	15	16.67	18.33	Ns	CLKOUT low period
t4	0		7.50	Ns	CLKOUT to TDI/DO delay
t5	0			Ns	TDI/DO hold time
t6	11			Ns	TDI/DO setup time

Table 20 - MPSSE Signal Timings

MPSSE mode is enabled using the FT_SetBitMode D2XX driver command with a hex value of 0x02. A hex value of 0x00 will reset the device. See application note AN135 – MPSSE Basics for more details and examples.

The MPSSE command set is fully described in application note AN108 – Command Processor For MPSSE and MCU Host Bus Emulation Modes.

The following additional libraries and application notes are available for configuring the MPSSE for SPI Master, I2C Master and JTAG at the following link:

https://ftdichip.com/software-examples/mpsse-projects/

4.8.1 MPSSE Adaptive Clocking

The Adaptive Clock mode correlates the CLK signal with a return clock RTCK. This is a technique used by ARM® processors.

The FT233HP/FT232HP will assert the TCK line and wait for the RTCK to be returned from the target device to GPIOL3 line before changing the TDO (data out line).

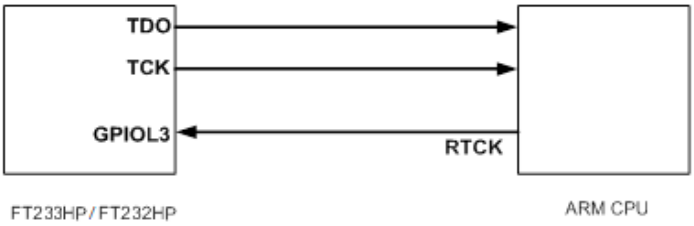


Figure 19 - Adaptive Clocking Interconnect

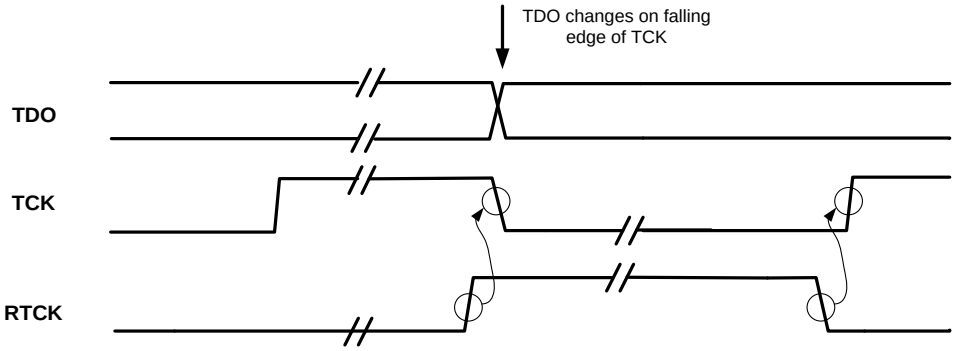


Figure 20 - Adaptive Clocking Waveform

Adaptive clocking is not enabled by default.

For further details on MPSSE adaptive clocking please refer to AN_108 Command Processor For MPSSE and MCU Host Bus Emulation Modes.

4.9 Fast Serial Interface Mode Description

Fast Serial Interface Mode provides a method of communicating with an external device over USB using 4 wires that can have opto-isolators in their path, thus providing galvanic isolation between systems. Fast serial mode is enabled by setting the appropriate bits in the external EEPROM. The fast serial mode can be held in reset by setting a bit value of 0x10 using the FT_SetBitMode D2XX driver command. While this bit is set the device is held reset – data can be sent to the device, but it will not be sent out by the device until the device is enabled again. This is done by sending a bit value of 0x00 using the Set Bit Mode command. When the FT233HP/FT232HP is configured in Fast Serial Interface mode the IO timing of the signals used are shown in Figure 21 and the timings are shown in Table 21.

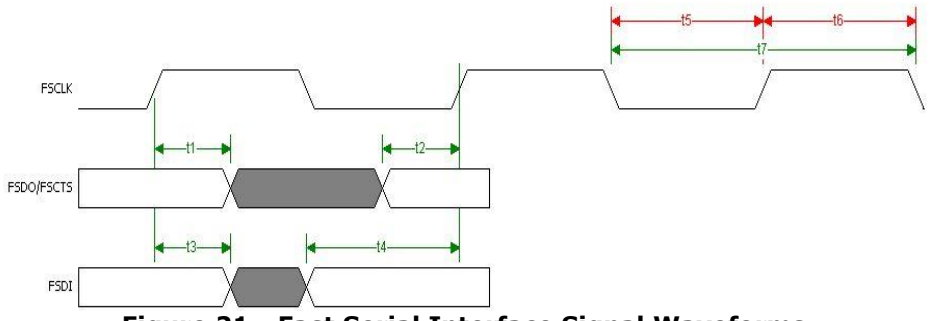


Figure 21 - Fast Serial Interface Signal Waveforms

Name	Minimum	Typical	Maximu	Units	Description
t1	1			ns	FSDO/FSCTS hold time
t2	5			ns	FSDO/FSCTS setup time
t3	5			ns	FSDI hold time
t4	10			ns	FSDI Setup Time
t5	10			ns	FSCLK low
t6	10			ns	FSCLK high
t7	20			ns	FSCLK Period

Table 21 - Fast Serial Interface Signal Timings

4.9.1 Outgoing Fast Serial Data

To send fast serial data out of the FT233HP/FT232HP, the external device must drive the FSCLK clock. If the FT233HP/FT232HP has data ready to send, it will drive FSDO output low to indicate the start bit. It will not do this if it is currently receiving data from the external device. This is illustrated in Figure 22.

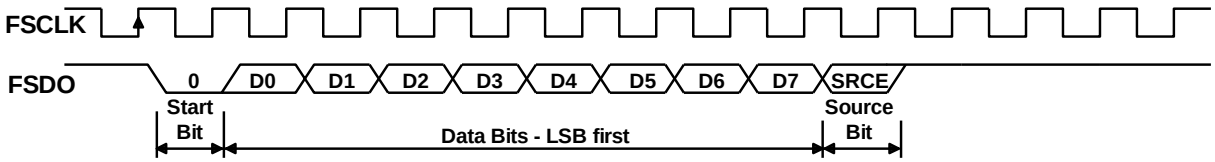


Figure 22 - Fast Serial Interface Output Data

Notes:

1. The first bit output (Start bit) is always 0.
2. FSDO is always sent LSB first.
3. The last serial bit output is the source bit (SRCE) is always 0.
4. If the target device is unable to accept the data when it detects the START bit, it should stop the FSCLK until it can accept the data.

4.9.2 Incoming Fast Serial Data

An external device is allowed to send data into the FT233HP/FT232HP if FSCTS is high. On receipt of a zero START bit on FSDI, the FT233HP/FT232HP will drop FSCTS on the next positive clock edge. The data from bits 0 to 7 are then clocked in (LSB first). The last bit (DEST) determines where the data will be written to. This bit is always 0 with the FT233HP/FT232HP. This is illustrated in Figure 23.

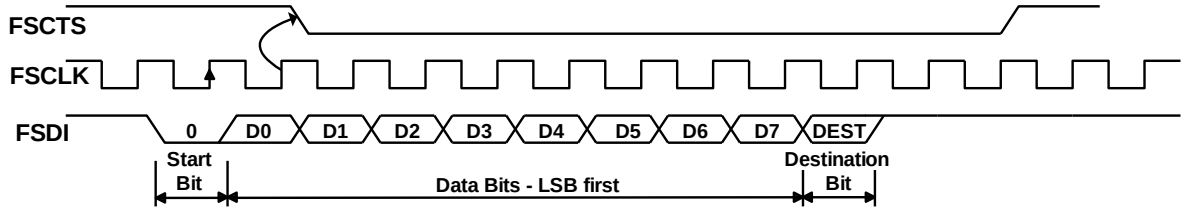


Figure 23 - Fast Serial Interface Input Data

Notes:

1. The first bit input (Start bit) is always 0.
2. FSDI is always received LSB first.
3. The last received serial bit is the destination bit (DEST) is always 0.
4. The target device should ensure that FSCTS is high before it sends data. FSCTS goes low after data bit 0 (D0) and stays low until the chip can accept more data.

4.9.3 Fast Serial Data Interface Example

Figure 24 shows example of two Agilent HCPL-2430 (see the semiconductor section at https://www.broadcom.com/ Hi-Speed opto-couplers used to optically isolate an external device which interfaced to USB using the FT233HP/FT232HP. In this example VCC5V is the USB VBUS supply and VCCE is the supply to the external device.

Care must be taken with the voltage used to power the photo-LED. It must be the same voltage as that which the FT233HP/FT232HP I/Os are driving to, or the LED's may be permanently on. Limiting resistors should be fitted in the lines that drive the diodes. The outputs of the opto-couplers are open-collector and require a pull-up resistor.

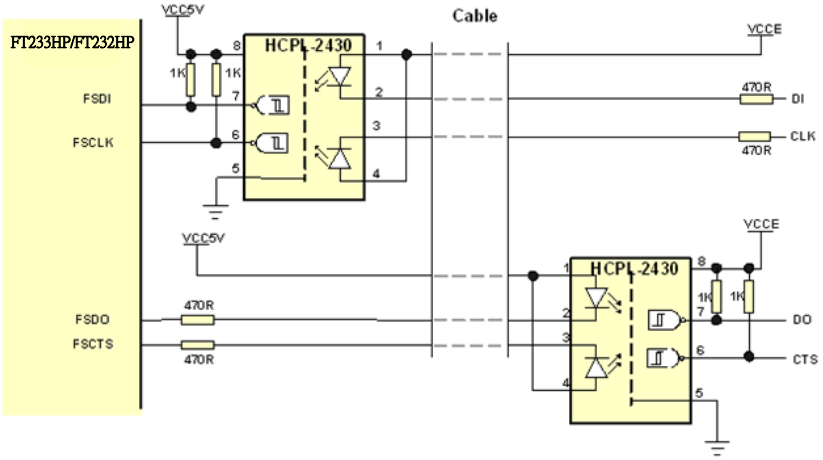


Figure 24 - Fast Serial Interface Example

4.10 CPU-style FIFO Interface Mode Description

CPU-style FIFO interface mode is designed to allow a CPU to interface to USB via the FT233HP/FT232HP. This mode is enabled in the external EEPROM. The interface is achieved using a chip select bit (CS#) and address bit (A0). When the FT233HP/FT232HP is in CPU-style Interface mode, the IO signal lines are configured as given in Table 22. This mode uses a combination of CS# and A0 to determine the operation to be carried out. Table 23 gives the decode values for particular operations.

CS#	A0	RD#	WR#
1	X	X	X
0	0	Read Data Pipe	Write Data Pipe
0	1	Read Status	Send Immediate

Table 22 - CPU-Style FIFO Interface Operation Select

The Status read is shown in Table 23 –

Data Bit	Data	Status
bit 0	1	Data available (=RXF)
bit 1	1	Space available (=TXE)
bit 2	1	Suspend
bit 3	1	Configured
bit 4	X	X
bit 5	X	X
bit 6	X	X
bit 7	X	X

Table 23 - CPU-Style FIFO Interface Operation Read Status Description

Note that bits 7 to 4 can be arbitrary values and that X= not used.

The timing of reading and writing in this mode is shown in Figure 25 and Table 24.

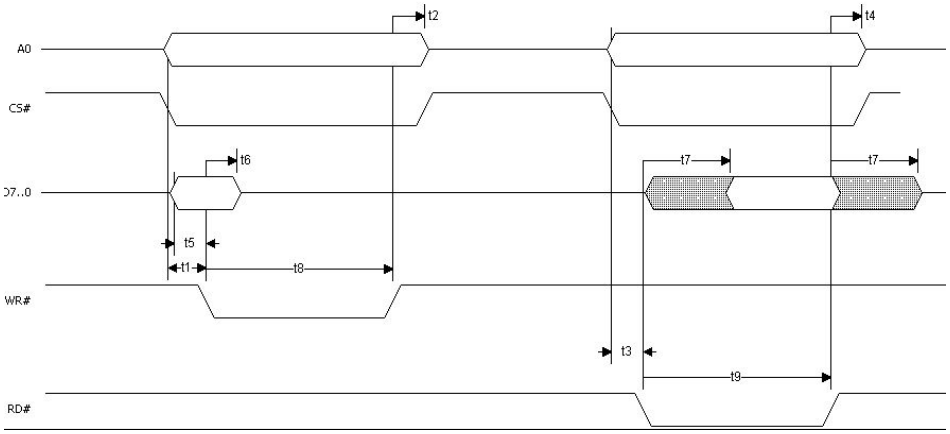


Figure 25 - CPU-Style FIFO Interface Operation Signal Waveforms

Data Bit	Nom	Max	Units	Comment
t1	5		Ns	A0/CS# setup time to WR#
t2	5		Ns	A0/CS# hold time after WR# inactive
t3	5		Ns	A0/CS# setup time to RD#
t4	5		Ns	A0/CS# hold time after RD# inactive
t5	5		Ns	D to WR# 36active setup time
t6	5		Ns	D hold time after WR# inactive
t7	1	14	ns	RD# to D
t8	30		ns	WR# active pulse width
t9	30		ns	RD# active pulse width

Table 24 - CPU-Style FIFO Interface Operation Signal Timing

An example of the CPU-style FIFO interface connection is shown in Figure 26.

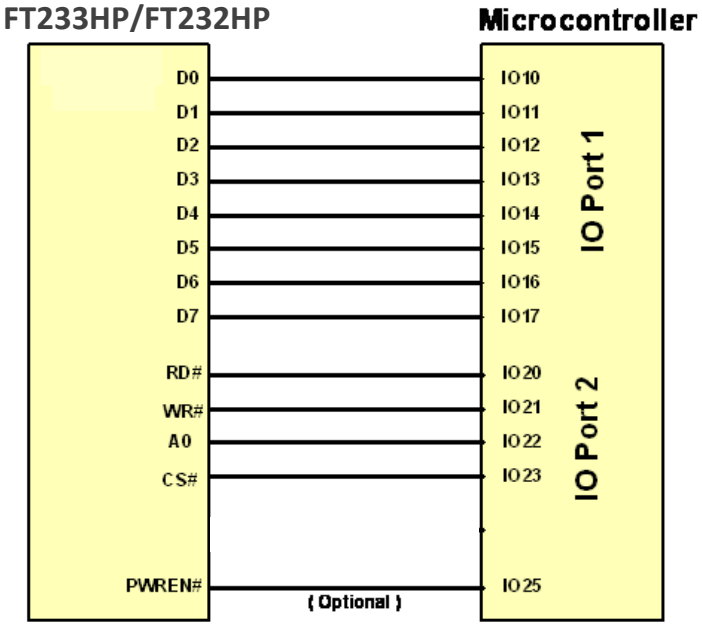


Figure 26 - CPU-Style FIFO Interface Example

4.11 RS232 UART Mode LED Interface Description

When configured in UART mode the FT233HP/FT232HP has two IO pins dedicated to controlling LED status indicators, one for transmitted data the other for received data. When data is being transmitted or received the respective pins drive from tristate to low in order to provide indication on the LEDs of data transfer. A digital one-shot timer is used so that even a small percentage of data transfer is visible to the end user.

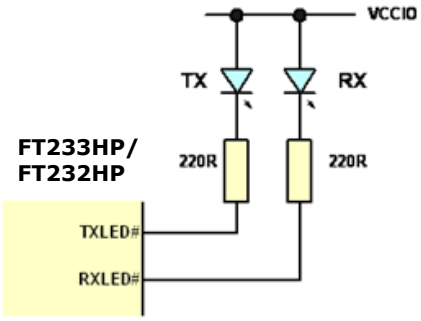


Figure 27 - Dual LED UART Configuration

Figure 27 shows a configuration using two individual LED's – one for transmitted data the other for received data.

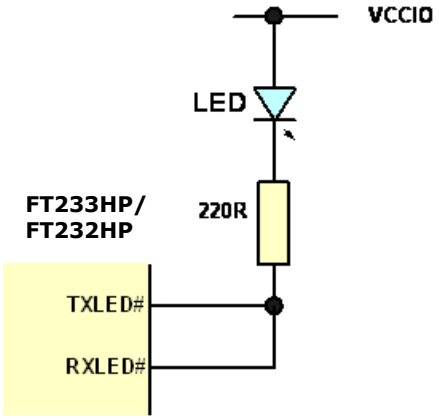


Figure 28 - Single LED UART Configuration

In Figure 28 transmit and receive LED indicators are wire-OR'ed together to give a single LED indicator which indicates any transmit or receive data activity.

Note that the LED's are connected to the same supply as VCCIO.

4.12 Send Immediate/Wake Up (SIWU#)

The SIWU# pin is available in the FIFO modes and in bit-bang mode. The Send Immediate portion is used to flush data from the chip back to the PC. This can be used to force short packets of data back to the PC without waiting for the latency timer to expire.

To avoid overrunning, this mechanism should only be used when a process of sending data to the chip has been stopped. The data transfer is flagged to the USB host by the falling edge of the SIWU# signal. The USB host will schedule the data transfer on the next USB packet.

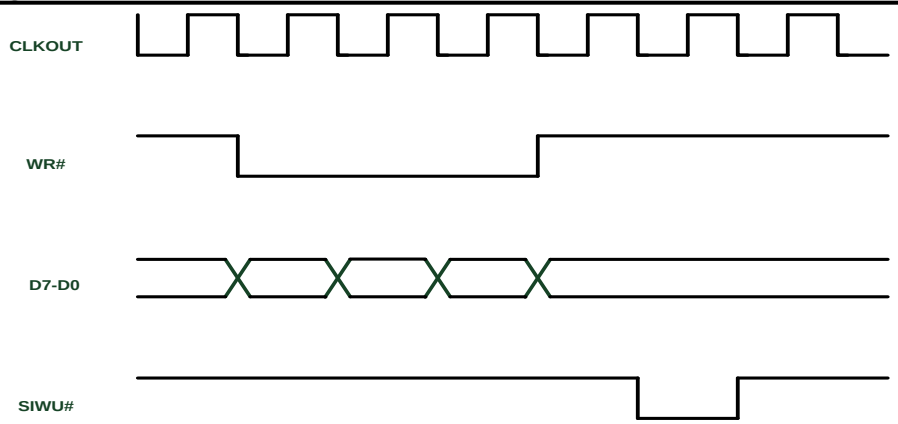


Figure 29 - Using SIWU#

When the pin is being used for a Wake-Up function to wake up a sleeping PC a 20ms negative pulse on this pin is required. When the pin is used to immediately flush the buffer (Send Immediate) a 250ns negative pulse on this pin is required.

Notes:

1. When using remote wake-up, ensure the resistors are pulled-up in suspend. Also ensure peripheral designs do not allow any current sink paths that may partially power the peripheral.
2. A peripheral is allowed to draw up to 2.5mA in suspend.
3. If a Pull-down is enabled, the FT233HP/FT232HP will not wake up from suspend when using SIWU#
4. In UART mode the RI# pin acts as the wake-up pin.

4.13 FT233HP/FT232HP Mode Selection

The FT233HP/FT232HP defaults to asynchronous serial interface (UART) mode of operation.

After a reset the required mode is determined by the contents of the external EEPROM which can be programmed using FT_Prog.

The EEPROM contents determine if the FT233HP/FT232HP device is configured as FT233HP/FT232HP asynchronous serial interface, FT245 FIFO interface, CPU-style FIFO interface, FT1248 or Fast Serial Interface.

Following a reset, the EEPROM is read and the FT233HP/FT232HP configured for the selected mode. After device enumeration, the ***FT_SetBitMode*** command (refer to D2XX_Programmers_Guide) can be sent to the USB driver to switch the selected interface into other modes – asynchronous bit-bang, synchronous bit-bang or MPSSE – if required.

When in FT245 FIFO mode, the ***FT_SetBitMode*** command can be used to select Synchronous FIFO (***FT_SetBitMode*** = 0x40). Note that FT245 FIFO mode must be configured in the EEPROM before selecting the Synchronous FIFO mode.

The drive strength selection, slew rate and Schmitt input function can also be configured in the EEPROM.

The MPSSE can be configured directly using the D2XX commands. The D2XX_Programmers_Guide is available from the FTDI website. The application note AN_108 – Command Processor for MPSSE and MCU Host Bus Emulation Modes gives further explanation and examples for the MPSSE.

4.14 Modes Configuration

This section summarises what modes are configurable using the external EEPROM or the application software.

	ASYNC Serial UART	STYLE ASYNC 245 FIFO	SYNC 245 PARALLEL FIFO	FT1248	ASYNC Bit-Bang	SYNC Bit-Bang	MPSSE	Fast Serial Interface	CPU-Style FIFO
EEPROM configured	YES	YES	YES	YES	NO	NO	NO	YES	YES
Application Software configured	NO	NO	YES	NO	YES	YES	YES	RESET	NO

Table 25 - Configuration Using EEPROM and Application Software

Note:

1. The Synchronous 245 FIFO mode requires both the EEPROM and application software mode settings
2. The application software can be used to reset the fast serial interface controller

4.15 USB Type-C/Power Delivery 3.0 Controller

4.15.1 PD Controller Description

The FT233HP/FT232HP has a Type-C/PD controller that fully supports the latest USB Type-C and Power Delivery (PD) 3.0 standards enabling support for power negotiation with the ability to sink or source current to a USB host device. There are two PD ports in the device (FT233HPQ and FT233HPL only), one port support legacy USB 2.0 as well as providing power sink or source capability, and the other port is standalone PD port as a sink which is used to connect to PD power source. Power Delivery function is designed to meet PD2.0/3.0 specification. If the device is configured to be operated in legacy USB2.0 mode it will be backward compatible to FT232H in terms of USB2.0 and its peripheral IOs functions.

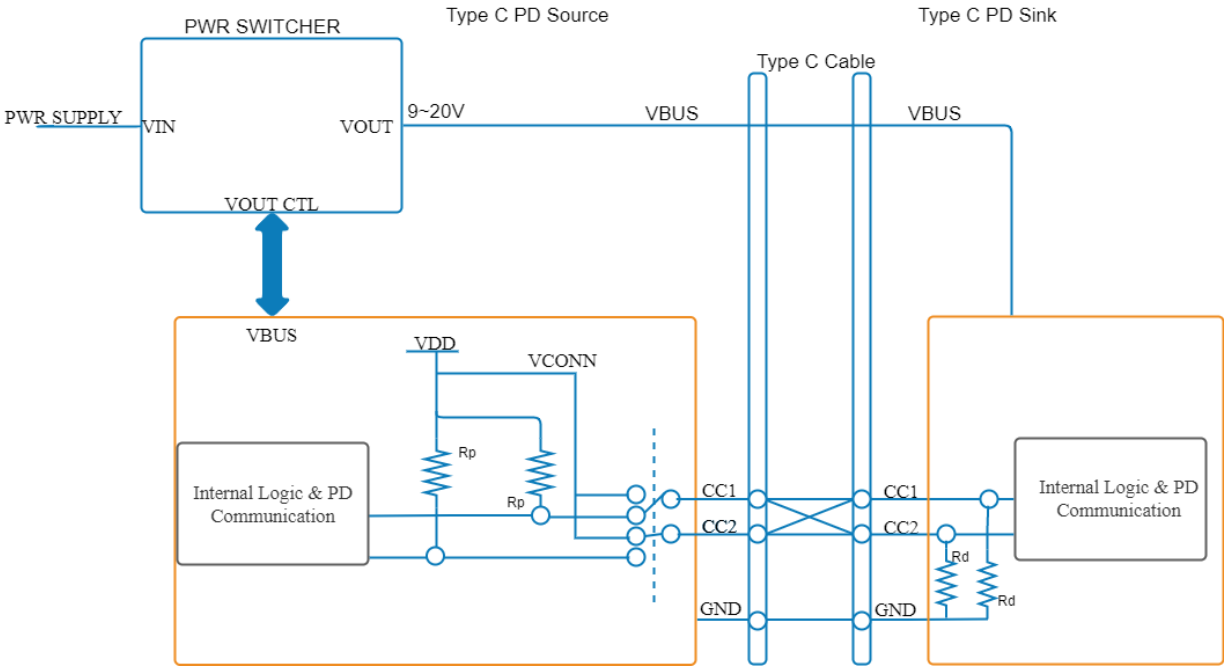


Figure 30 - PD Working Diagram

4.15.2 Features

- PD 3.0 Compliant.
- Physical layer and Policy Engine.
- Initial Sink, with Dual Role Power (Power Role Swap).
- Multiple Configurable Power Profiles.
- Supports up to 20V3A power profile.
- Charge through Support.
- Cable Attach and Orientation Detection.
- Supports 1.5A and 3A cables in Type-C legacy mode (NON-PD Mode).
- Profile Selection indication through GPIOs when operating In Sink Mode.
- Supports External MCU to take over the control.
- 8 bit register interface for a low speed processor, or optional I2C port
- Integrated Chapter 6 protocol reduces required MPU response time to 10mS.
- K code recognition/coding, preamble, CRC, etc offloaded from processor.
- VCONN 200mA protected driver switches
- Single 12MHz clock + 32KHz low power clock.
- Slew rate limited driving of CC cable lines drive to 1.1V and 300nS linear transition time.

4.15.3 AC timing on GPIO pins

Best case transition time with 5pF load		Worst case transition time with 15pF load	
Rise(ns)	Fall(ns)	Rise(ns)	Fall(ns)
1.2	1.1	6.0	6.5

Table 26 - AC Timing on GPIO Pins

4.15.4 GPIO Timing for PD Operation

GPIOs are used as a power profile indicator as well as power supply controllers. When operating as a Sink, GPIO pins are used for LOAD_EN* and ISET*.

Depending on the kind of profile negotiated, the appropriate ISET* GPIO will go high followed by LOAD_EN* pin.

The timing between this ISET* going high to LOAD_EN* can be as up to 12.5uS.

When operating as a Source, GPIO pins are used as power supply controller. During Source operation, the initial voltage will be 5V and then depending on the profile setting; the PD controller can negotiate a higher voltage. Switching from 5V to higher Voltage or vice versa is controlled by switching GPIOs. 5V could be controlled by one Pin whereas each higher Voltage is controlled by a different pin.

For example, Table 27 shows a sample GPIO states for 3 different voltage cases.

	5v	9V	20V
PS_EN*	HIGH	HIGH	HIGH
GPIO_9v*	LOW	HIGH	LOW
GPIO_20v*	LOW	LOW	HIGH

Table 27 - Example GPIO States for Power Control

In this case 5V to 9V or 5v to 20V is just an additional GPIO pin going high. In this case the timing does not matter. However, in the scenario, when the profile changes from 9V to 20V, there is one GPIO going low whereas another one going high. In this case the delay between one pin going low to another pin going high can be up to 12.5uS.

*: These five signals can be configured by software GPIOs setting but also corresponding to board design.

4.15.5 PD Voltage Parameter

Based on USB Type-C specification, during initialization when Source connects to Sink, both are in the unattached state. Source firstly detects the Sink's pull down on CC then enters attached state, Source turns on VBUS and VCONN. So USB Type-C specification requests voltage parameters shown below:

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable / adapter(vRa)	0.00V	0.15V	0.20V
Sink(vRd)	0.25V	1.50V	1.60V
No connect (vOPEN)	1.65V		

Table 28 - CC Voltage on Source Side - Default USB

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable / adapter(vRa)	0.00V	0.35V	0.40V
Sink(vRd)	0.45V	1.50V	1.60V
No connect (vOPEN)	1.65V		

Table 29 - CC Voltage on Source Sid - 1.5A @ 5V

	Minimum Voltage	Maximum Voltage	Threshold
Powered cable / adapter(vRa)	0.00V	0.75V	0.80V
Sink(vRd)	0.85V	2.45V	2.60V
No connect (vOPEN)	2.75V		

Table 30 - CC Voltage on Source Side - 3A @ 5V

To better achieve USB Type-C specification requests, we suggest to use a Schottky Diode to isolate DCDC power from Vcc_PD and PD1_Vconn of FT233HP/FT232HP in order to guarantee the expected voltage parameters. The capacitance between Vcc_PD/PD1_Vconn and ground should not be more than 1uF to avoid the slow rise up of CC line due to the leakage through Vcc_PD and PD1_Vconn to the capacitor. The equivalent circuit is shown below:

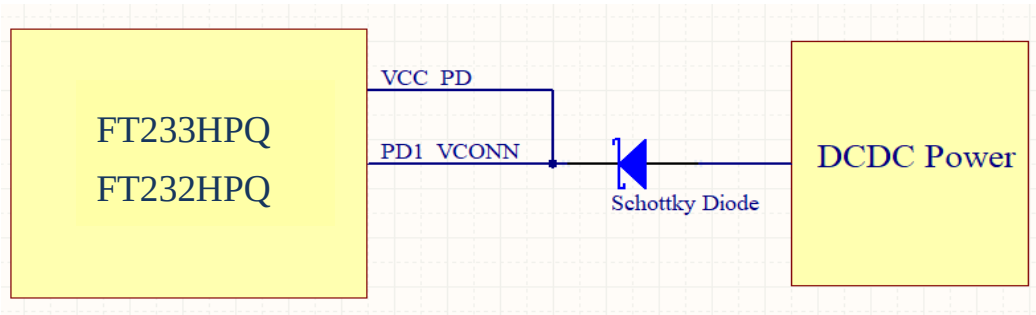


Figure 31 - Schottky Diode Equivalent Circuit

Recommended schottky diode parameters:

$V_{(R)}$	I_F	V_F (Forward Voltage)
-30V(max)	≤ 5A	≤ 0.3V

Table 31 - Schottky Diode Recommended Characteristics

5 Devices Characteristics and Ratings

5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT233HP/FT232HP devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these values may cause permanent damage to the device.

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Operating Temperature (Power Applied)	-40°C to 85°C	Degrees C
MTTF FT233HP/FT232HP	3710058.938	Hours
VCORE Supply Voltage	-0.3 to +2.0	V
VCCIO IO Voltage	-0.3 to +4.0	V
DC Input Voltage – USBDP and USBDM	-0.5 to +3.63	V
DC Input Voltage – High Impedance Bi-directional (ACBUS and ADBUS powered from VCCIO)	-0.3 to +5.8	V
DC Input Voltage – PD1_CC1, PD1_VCONN, PD1_SVBUS, PD1_CC2, PD2_CC1, PD2_SVBUS, PD2_CC2	-0.5 to (VCC_PD + 0.5)	V
DC Input Voltage - VPP	-0.5 to 1.85	V
DC Input Voltage - FSOURCE	-0.5 to 3.7	V
DC Output Current – Outputs	16	mA

Table 32 - Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

5.2 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCORE	VCC Core Operating Supply Voltage	1.08	1.20	1.32	V	
VCCIO*	VCCIO Operating Supply Voltage	2.97	3.30	3.63	V	
VREGIN	VREGIN Voltage regulator Input	3.00	3.30	3.60	V	
VREGOUT	Voltage regulator Output	1.08	1.20	1.32	V	
Ireg	Regulator Current		21.11	150	mA	VREGIN +3.3V and data transfer with 12Mbps
Icc1s	VREGIN Suspend Supply Current		1.64		mA	USB Suspend
I_vccio	VCC_IO operating supply current		0.87		mA	UART Data transfer at 12Mbps
I_vcc_pd	VCC_PD suspend supply current		209		uA	PD suspend

Table 33 - Operating Voltage and Current

Note: Failure to connect all VCCIO pins of the device will have unpredictable behaviour.

The I/O pins are +3.3v cells, which are +5V tolerant (except the USB PHY pins).

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.4	3.26	VCCIO	V	Ioh = +/-2mA I/O Drive strength* = 4mA
		2.4	3.28	VCCIO	V	I/O Drive strength* = 8mA
		2.4	3.285	VCCIO	V	I/O Drive strength* = 12mA
		2.4	3.29	VCCIO	V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0.1	0.4	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0.05		V	I/O Drive strength* = 8mA
			0.04		V	I/O Drive strength* = 12mA
			0.03		V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold			0.8	V	LVTTL
Vih	Input High Switching Threshold	2.0			V	LVTTL
Vt	Switching Threshold		1.5		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage	0.8	1.1		V	
Vt+	Schmitt trigger positive going threshold voltage		1.6	2.0	V	
Rpu	Input pull-up resistance**	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	-10	+/-1	10	µA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	µA	Vin = 5.5 or 0V

Table 34 - I/O Pin Characteristics VCCIO = +3.3V (except USB PHY pins)

* The I/O drive strength and slow slew-rate are configurable in the EEPROM.
** The voltage pulled up to is VCCIO-0.9V in the worst case.

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC_USB	PHY Operating Supply Voltage	3.0	3.3	3.6	V	3.3V I/O
I_vcc_usb	PHY Operating Supply Current	---	22.7	---	mA	Uart Data transfer at 12Mbps
I_vcc_usb (susp)	PHY Suspend Supply Current	---	0.2	---	mA	USB Suspend

Table 35 - PHY Operating Voltage and Current

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
USB2.0 Transceiver (HS)						
VHSOI	High-speed idle level output voltage (Differential)	-10		10	mV	
VHSOL	High-speed low level output voltage (Differential)	-10		10	mV	
VHSOH	High-speed high level output voltage (Differential)	-360		400	mV	
VCHIRPJ	Chirp-J output voltage (Differential)	700		1100	mV	
VCHIRPK	Chirp-K output voltage (Differential)	-900		-500	mV	
USB 1.1 Transceiver (FS)						
Voh	Output Voltage High	2.8	-	3.6	V	
Vol	Output Voltage Low	0	-	0.3	V	
Vil	Input low Switching Threshold		-	0.8	V	
Vih	Input High Switching Threshold	2.0	-		V	

Table 36 - PHY I/O Pin Characteristics

5.3 ESD Tolerance

ESD protection for FT233HP/FT232HP IO's

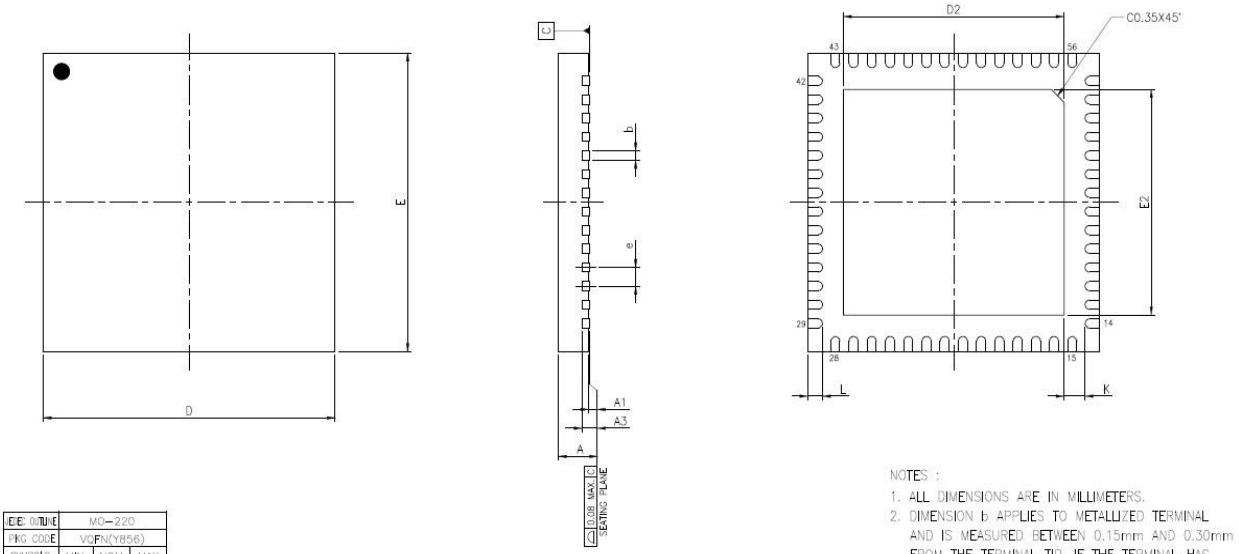
Parameter	Reference	Minimum	Typical	Maximum	Units
Machine Mode (MM)	JEDEC EIA/JESD22-A115C, Class B		±200V		V
Charge Device Model (CDM)	ANSI/ESDA/JEDEC JS-002, JEDEC JESD22-C101F Class-C2		±500V		V
Latch-up	JEDEC STANDARD EIA/JESD78E, Trigger Class-II		±200mA		mA

Table 37 - ESD Tolerance

6 Package Parameters

The FT233HP/FT232HP is available in three different packages. The FT232HPQ is the QFN-56 option, the FT233HPL is LQFP-64 package and the FT233HPQ is the QFN-64 package option.

6.1 FT232HPQ, QFN-56 Package Dimensions



JEDEC OUTLINE	MO-220		
PKG CODE	VQFN(Y856)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.20	0.25	0.30
D	8.00 BSC.		
E	8.00 BSC.		
e	0.50 BSC.		
L	0.30	0.40	0.50
K	0.20	—	—

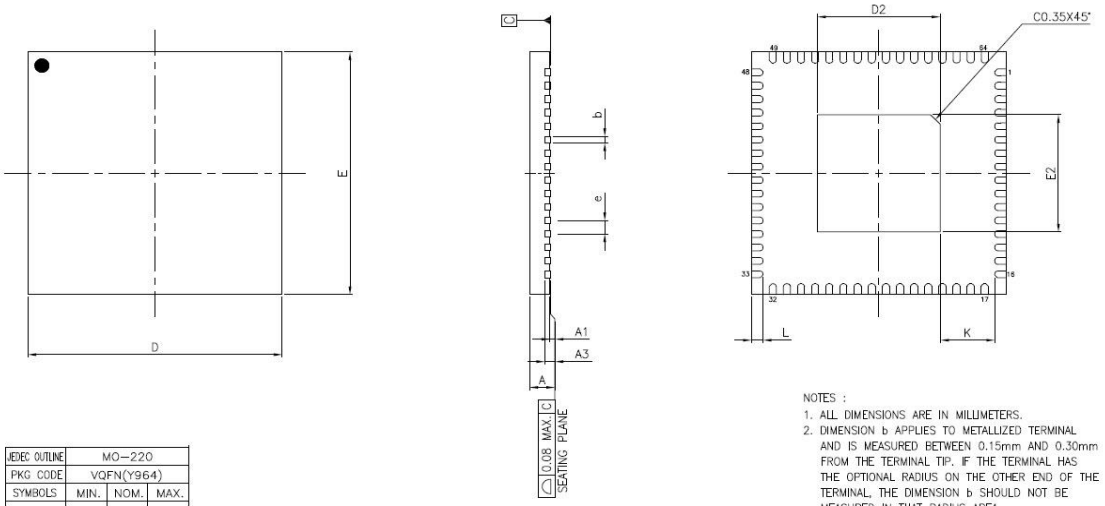
PAD SIZE	D2			E2			L			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
240X240* ML	5.85	5.90	5.95	5.85	5.90	5.95	0.30	0.40	0.50	V	X	(W)VLLD-2

NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

"*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元請參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

Figure 32 - 56 Pin QFN Package Details

6.2 FT233HPQ, QFN-64 Package Dimensions



NOTES :
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

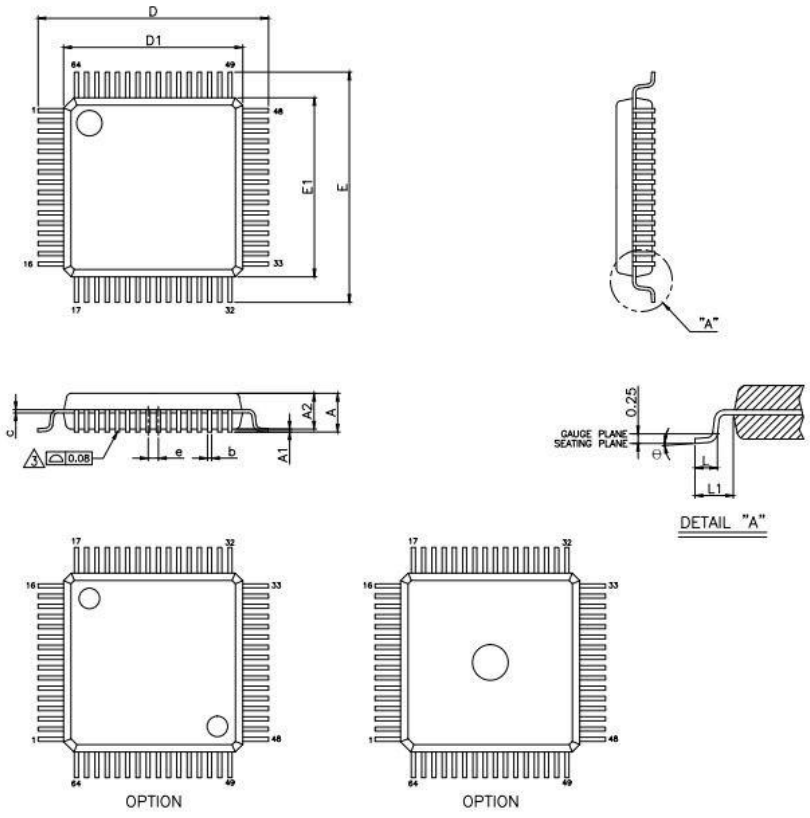
JEDEC OUTLINE	MO-220		
PKG CODE	VQFN(Y964)		
SYMBOLS	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3	0.203 REF.		
b	0.18	0.25	0.30
D	9.00 BSC		
E	9.00 BSC		
e	0.50 BSC		
K	0.20	—	—

PAD SIZE	D2			E2			L			LEAD FINISH		JEDEC CODE
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	Pure Tin	PPF	
179X17* MIL	4.30	4.35	4.40	4.30	4.35	4.40	0.35	0.40	0.45	V	X	N/A

"*"表示汎用字元,此汎用字元可能被其它不同字元所取代,實際的字元應參照bonding diagram所示.
"*" is an universal character, which means maybe replaced by specific character, the actual character please refers to the bonding diagram.

Figure 33 - 64 Pin QFN Package Details

6.3 FT233HPL, LQFP-64 Package Dimensions



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	—	—	1.60
A1	0.05	—	0.15
A2	1.35	1.40	1.45
b	0.13	0.18	0.23
c	0.09	—	0.20
D	9.00 BSC		
D1	7.00 BSC		
e	0.40 BSC		
E	9.00 BSC		
E1	7.00 BSC		
L	0.45	0.60	0.75
L1	1.00 REF		
θ	0°	3.5°	7°

NOTES:
1.JEDEC OUTLINE : MS-026 BBD
2.DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3.DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.

Figure 34 - 64 Pin LQFP Package Details

7 FT233HP/FT232HP Configuration

7.1 Oscillator Configuration

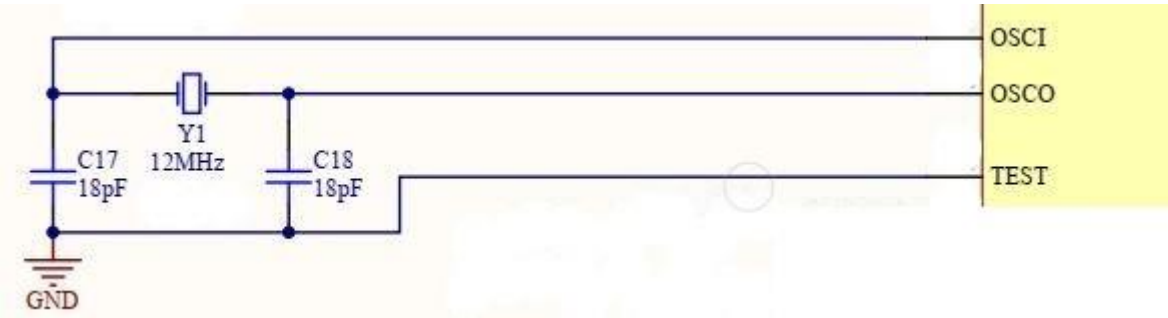


Figure 35 - Recommended FT233HP/FT232HP Crystal Oscillator Configuration

Figure 35 illustrates how to connect the FT233HP/FT232HP with a 12MHz ± 0.003% crystal. In this case loading capacitors should be added between OSCI, OSCO and GND as shown. A value of 18pF is shown as the capacitor in the example – this will be good for many crystals, but it is recommended to select the loading capacitor value based on the manufacturer's recommendations wherever possible. It is recommended to use a parallel cut type crystal.

It is also possible to use a 12 MHz oscillator with the FT233HP/FT232HP. In this case the output of the oscillator would drive OSCI, and OSCO should be left unconnected. The oscillator must have a CMOS output drive capability.

Item / Type	7B	7B(T)
Frequency Tolerance (at 25 ℃)	± 30 ppm	± 10 ppm
Frequency Stability Over Operating Temperature Range	± 30 ppm	± 10 ppm
Shunt Capacitance (C0)	5 pF Max. (2 pF typical)	
Drive Level	1 ~ 200 µW (100 µW typical)	
Load Capacitance	10 pF, 16 pF, 20 pF, or specify	6 pF, 9 pF,10 pF,12 pF,16 pF

Table 38 - Crystal Characteristics

7.2 PD Configuration

Figure 36 illustrates the application example of bus power configuration for PD. The device gets the power either from PD1 or PD2. In this application, the FT233HP requires that the VBUS is regulated down to +3.46V (using LDO) to supply VCCIO, VCC_USB and VREGIN.

VREGIN is the +3.46V input to the on chip +1.2V regulator. The output of the on chip LDO regulator drive the FT233HP core supply (Vcore).

Schotkky diode is added between +3.46V and VCC_PD/PD1_VCONN to prevent CC leakage during the initial attach when the chip is not yet fully powered up.

The GPIOs are used to drive the load switch as well as controlling power level of the voltage regulator according to the negotiated PD profiles.

Please refer to the UMFT233HPEV Evaluation Module Datasheet for more details on the PD configuration in various user scenario.

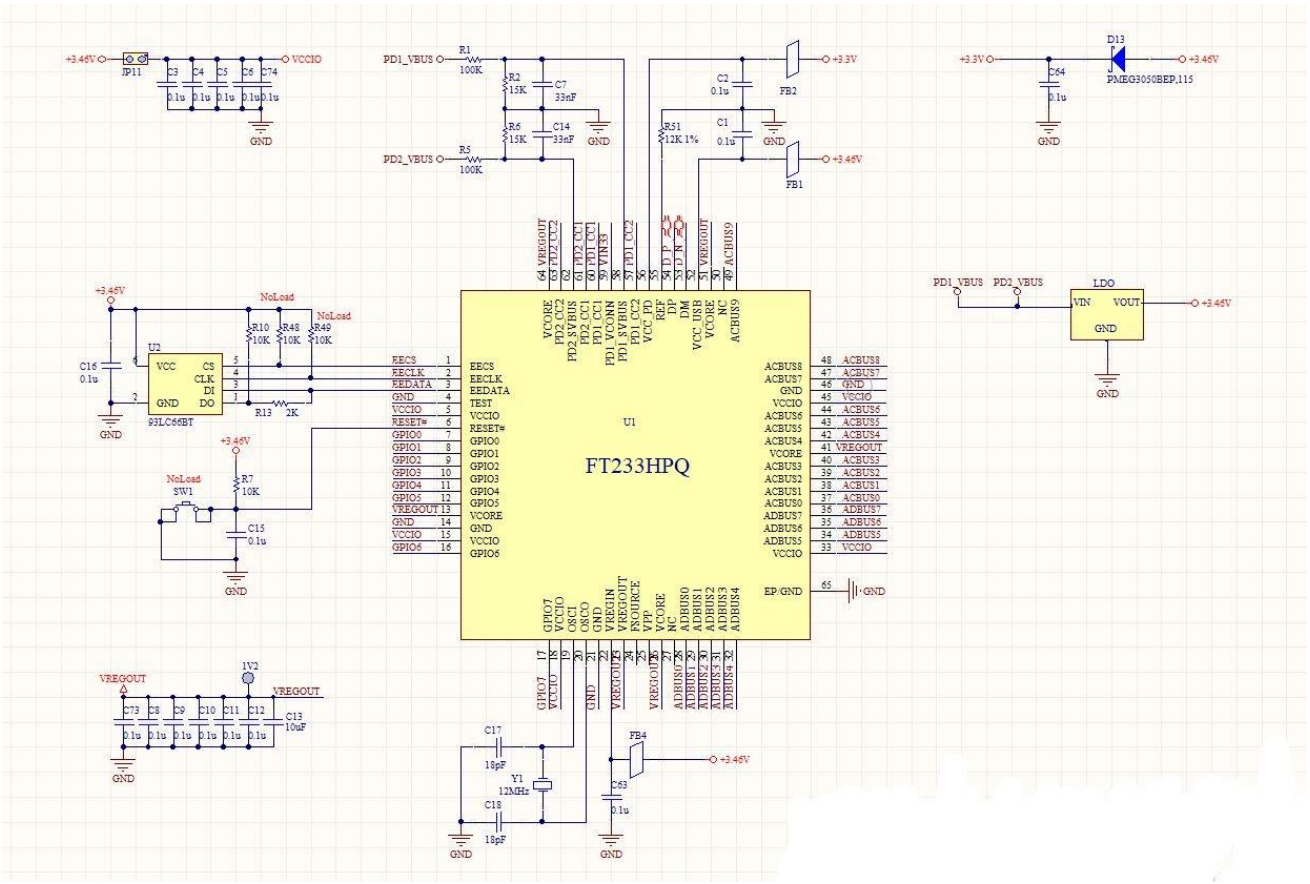


Figure 36 - Bus Powered PD Configuration Diagram

8 EEPROM Configuration

If an external EEPROM is fitted (93LC66) it can be programmed over USB using FT_PROG. The EEPROM must be 16 bits wide and capable of working at a VCC supply of +3.0 to +3.6 volts.

Adding an external EEPROM allows selecting the TXDEN for RS485 mode when asynchronous serial interface has been selected.

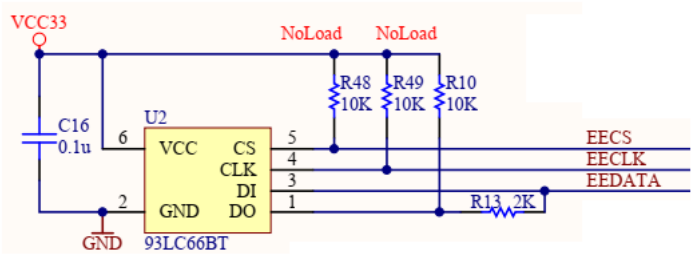


Figure 37 - EEPROM Interface

The external EEPROM can also be used to customise the USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT233HP/FT232HP for OEM applications. Other parameters controlled by the EEPROM include Remote Wake Up, Soft Pull Down on Power-Off, I/O pin drive strength and TXDEN selection.

If no EEPROM is connected (or the EEPROM is blank), the FT233HP/FT232HP uses its built-in default VID (0403), PID (6044/6045) Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor.

8.1 Default EEPROM Configuration

The external EEPROM (if it's fitted) can be programmed over USB using FT_PROG. This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process. Users who do not have their own USB Vendor ID but who would like to use a unique Product ID in their design can apply to FTDI for a free block of unique PIDs.

Contact FTDI support for this service.

Parameter	Value	Notes
USB Vendor ID (VID)	0403h	FTDI default VID (hex)
USB Product ID (PID)	6044h 6045h	FTDI default PID (hex) for FT233HP FTDI default PID (hex) for FT232HP
bcd Device	0x3200 0x3300	for FT233HP for FT232HP
Serial Number Enabled?	Yes	
Serial Number	See Note	None
Pull down I/O Pins in USB Suspend	Disabled	Enabling this option will make the device pull down on the UART interface lines when in USB suspend mode (PWREN# is high).
Manufacturer Name	FTDI	
Product Description	RS232-HS	
Max Bus Power Current	500mA	
Power Source	Bus Powered	
Device Type	FT233HP FT232HP	for FT233HP for FT232HP
USB Version	0200h	Returns USB 2.0 device description to the host.
Remote Wake Up	Disabled	Taking RI# low will wake up the USB host controller from suspend in approximately 20 ms. If enabled.

Parameter	Value	Notes
Hardware Interface	UART	Allows the user to select the hardware mode of the device. Options include RS232 UART, 245 FIFO, CPU 245, OPTO Isolate and FT1248.
FT1248 Settings	00h	FT1248 can be configured to set Clock Polarity High; Bit Order LSB and Flow Control Not Selected.
Suspend ACBus7 Low	Disabled	Enters low power state on ACBus7.
High Current I/Os	Disabled	Enables the high drive level on the UART and ACBUS I/O pins.
Load VCP Driver	Enabled	Makes the device load the VCP driver interface for the device.
ACBUS0	TriSt-PU	Default configuration of ACBUS0 – Input pulled up
ACBUS1	TriSt-PU	Default configuration of ACBUS1 – Input pulled up
ACBUS2	TriSt-PU	Default configuration of ACBUS2 – Input pulled up
ACBUS3	TriSt-PU	Default configuration of ACBUS3 – Input pulled up
ACBUS4	TriSt-PU	Default configuration of ACBUS4 – Input pulled up
ACBUS5	TriSt-PU	Default configuration of ACBUS5 – Input pulled up
ACBUS6	TriSt-PU	Default configuration of ACBUS6 – Input pulled up
ACBUS7	TriSt-PD	Default configuration of ACBUS7 – Input pulled down
ACBUS8	TriSt-PU	Default configuration of ACBUS8 – Input pulled up
ACBUS9	TriSt-PU	Default configuration of ACBUS9 – Input pulled up

Table 39 - Default Configuration with a blank/no EEPROM

8.2 PD Configuration and Default values

Refer to AN_448_FT4233HP_FT2233HP_FT233HP_Configuration_Guide for FT233HP Power Delivery configuration and Default values.

Refer to AN_551_FT4232HP_FT2232HP_FT232HP_Configuration_Guide for FT232HP Power Delivery configuration and Default values.

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Distributor and Sales Representatives

Please visit the Sales Network page of the FTDI Web site for the contact details of our distributor(s) and sales representative(s) in your country.

Appendix A – References

Document References

AN_108 – Command Processor for MPSSE and MCU Host Bus Emulation Modes
AN_110 – Programmers Guide for High Speed FTCJTAG DLL
AN_113 – Interfacing FT2232H Hi-Speed Devices to I2C Bus
AN_114 – Interfacing FT2232H Hi-Speed Devices to SPI Bus
AN_117 – User Guide For libMPSSE – I2C
AN_129 – Interfacing FT2232H Hi-Speed Devices to a JTAG TAP
AN_135 – MPSSE Basics
AN_178 – User Guide For libMPSSE – SPI
AN 411 - FTx232H MPSSE I2C Master Example in C#
AN 355 - FT232H MPSSE Example - I2C Master Interface with Visual Basic
AN 448 FT4233HP FT2233HP FT233HP Configuration Guide
AN 449 FT4233HP FT2233HP FT4232HP FT2232HP DCDC Power Delivery
AN 551 FT4232HP FT2232HP FT232HP Configuration Guide
AN_167 FT1248 Parallel Serial Interface Basics
FT_PROG
TN_167 FTDI FIFO Basics
AN_120 Aliasing VCP Baud Rates
TN_104 – Guide to Debugging Customers Failed Driver Installation
MPSSE Example Projects (I2C Master, SPI Master, JTAG)
Evaluation Modules

Acronyms and Abbreviations

Terms	Description
CPU	Central Processing Unit
EEPROM	Electrically Erasable Programmable Read Only Memory
ESD	Electrostatic Discharge
FIFO	First In First Out
I2C	Inter-Integrated Circuit
LDO	Low Drop Out
LED	Light Emitting Diode
LSB	Least Significant Bit First
LQFP	Low Profile Quad Flat Pack
MPSSE	Multi- Protocol Synchronous Serial Engines
PD	Power Delivery
QFN	Quad Flat Non-leaded package
SPI	Serial Peripheral Interface
TTL	Transistor-Transistor Logic
USB	Universal Serial Bus
UART	Universal Asynchronous Receiver / Transmitter
UTMI	Universal Transceiver Macrocell Interface
VCP	Virtual COM Ports

Appendix B – List of Figures and Tables

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