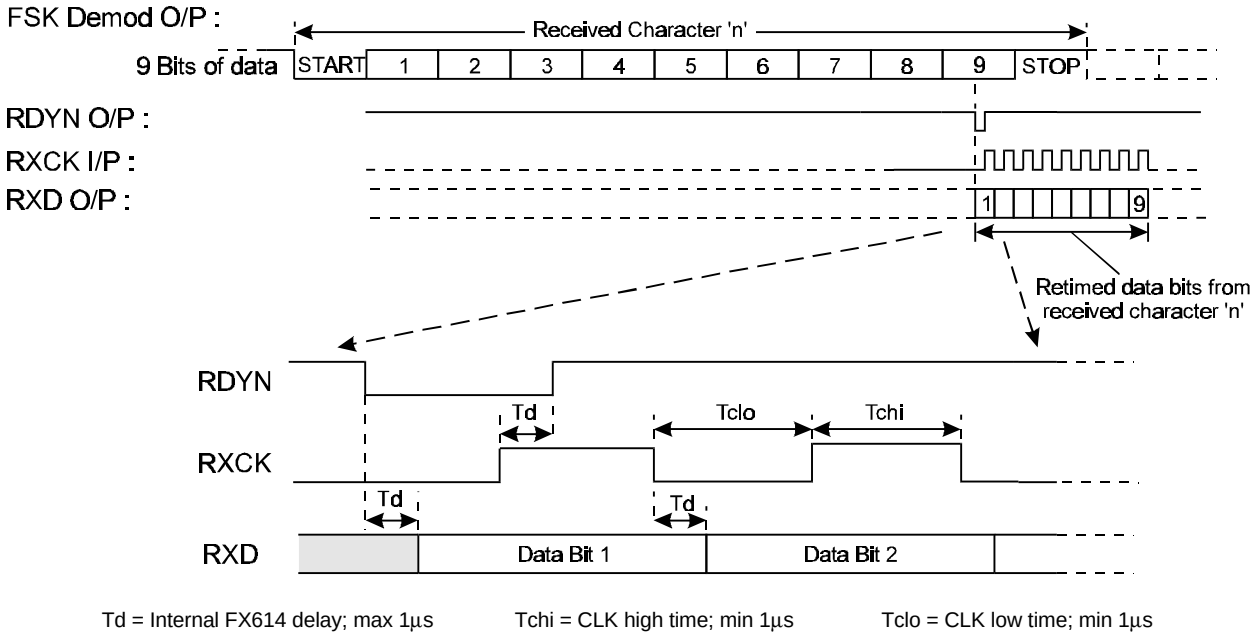

Figure 6a FSK Operation with Rx Data Retiming

Note that, if enabled, the Data Retiming block may interpret speech or other signals as random characters.

If the Data Retiming facility is not required, the CLK input to the FX614 should be kept high at all times. The asynchronous data from the FSK Demodulator will then be connected directly to the RXD output pin, and the RDYN output will not be activated by the FSK signal. This case is illustrated by the example in Figure 6b.

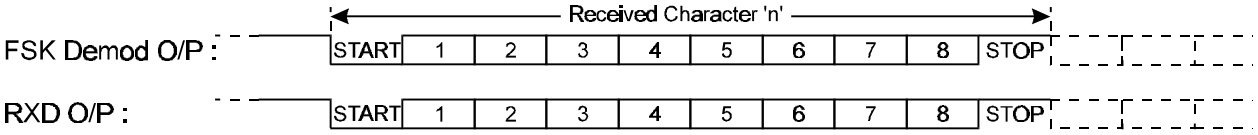

Figure 6b FSK Operation without Rx Data Retiming (CLK always high)

1.5.9 Tx Data Retiming

The Data Retiming block, when enabled in 1200bits/sec transmit mode, requires the controlling µC to load one bit at a time into the device by a pulse applied to the CLK input. The timing of this pulse is not critical and it may easily be generated by a simple software loop. This facility removes the need for a UART in the µC without incurring an excessive software overhead.

The Tx re-timing circuit consists of two 1-bit registers in series, the input of the first is connected to the TXD pin and the output of the second feeds the FSK modulator. The second register is clocked by an internally generated 1200Hz signal and when this occurs the CLK input is sampled. If the CLK input is high the TXD pin directly controls the FSK modulator, if the CLK input is low the FSK modulator is controlled by the output of the second register and the RDYN pin is pulled low. The RDYN output is reset by a high level on the CLK input pin. A low to high change on the CLK input pin will latch the data from the TXD input pin into the first register ready for transfer to the second register when the internal 1200Hz signal next occurs.