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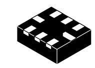
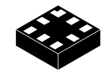
Dual Supply, 2-Bit Voltage Translator / Isolator for I^2C Applications

FXMAR2102

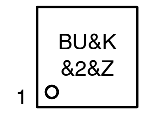


UQFN8, 1.4x1.2, 0.4P
CASE 523AS



UQFN8 1.6X1.6, 0.5P
CASE 523AY

MARKING DIAGRAM



BU = Device Code
&K = 2–Digits Lot Run Traceability Code
&2 = 2–Digit Date Code
&Z = Assembly Plant Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 13 of this data sheet.

Description

The FXMAR2102 is a high–performance configurable dual–voltage–supply translator for bi–directional voltage translation over a wide range of input and output voltages levels. The FXMAR2102 also works in a push– pull environment.

It is intended for use as a voltage translator between I^2C–Bus compliant masters and slaves. Internal 10 kΩ pull–up resistors are provided.

The device is designed so the A port tracks the V_{CCA} level and the B port tracks the V_{CCB} level. This allows for bi–directional A/B–port voltage translation between any two levels from 1.65 V to 5.5 V. V_{CCA} can equal V_{CCB} from 1.65 V to 5.5 V. Either V_{CC} can be powered–up first. Internal power–down control circuits place the device in 3–state if either V_{CC} is removed.

The two ports of the device have automatic direction–sense capability. Either port may sense an input signal and transfer it as an output signal to the other port.

Features

- Bi–Directional Interface between Any Two Levels: 1.65 V to 5.5 V
- No Direction Control Needed
- Internal 10 kΩ Pull–Up Resistors
- System GPIO Resources Not Required when OE Tied to V_{CCA}
- I^2C Bus Isolation
- A/B Port V_{OL} = 175 mV (Typical), V_{IL} = 150 mV, I_{OL} = 6 mA
- Open–Drain Inputs / Outputs
- Works in Push Pull Environment
- Accommodates Standard–Mode and Fast–Mode I^2C–Bus Devices
- Supports I^2C Clock Stretching & Multi–Master
- Fully Configurable: Inputs and Outputs Track V_{CC}
- Non–Preferential Power–Up; Either V_{CC} Can Power–Up First
- Outputs Switch to 3–State if Either V_{CC} is at GND
- Tolerant Output Enable: 5 V
- Packaged in 8–Terminal Leadless MicroPak™ (1.6 mm x 1.6 mm) and Ultrathin MLP (1.2 mm x 1.4 mm)
- ESD Protection Exceeds:
  - B Port: 8 kV HBM ESD (vs. GND & vs. V_{CCB})
  - All Pins: 4 kV HBM ESD (per JESD22–A114)
  - 2 kV CDM (per JESD22–C101)

BLOCK DIAGRAM

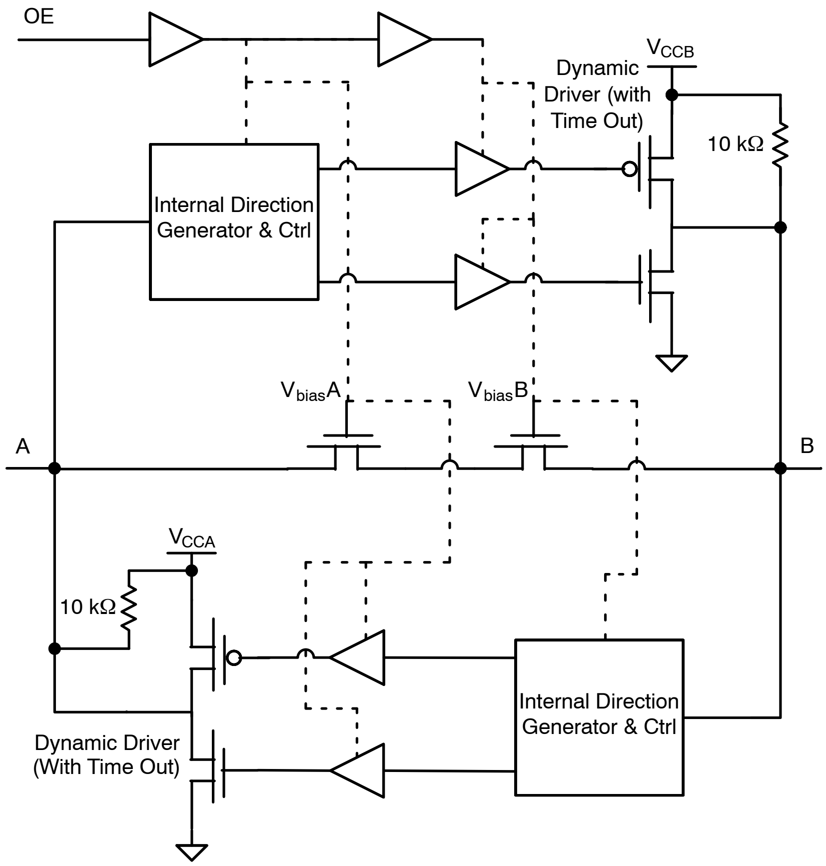


Figure 1. Block Diagram, 1 of 2 Channels

PIN CONFIGURATION

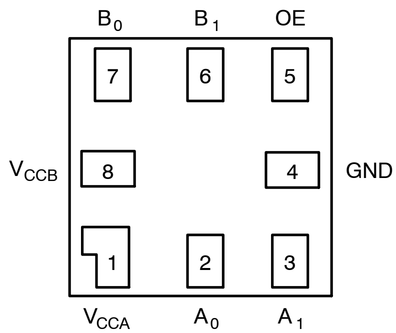


Figure 2. MicroPak (Top−Through View)

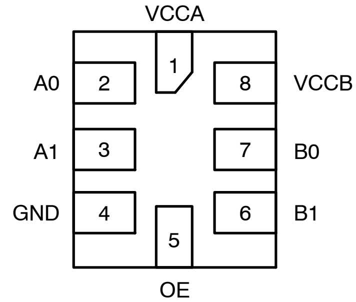


Figure 3. UMLP (Top−Through View)

PIN DEFINITIONS

Pin No.	Name	Description
1	V_{CCA}	A−Side Power Supply
2, 3	A_0, A_1	A−Side Inputs or 3−State Outputs
4	GND	Ground
5	OE	Output Enable Input
6, 7	B_1, B_0	B−Side Inputs or 3−State Outputs
8	V_{CCB}	B−Side Power Supply

TRUTH TABLE

Control	Outputs
OE (Note 1)	
LOW Logic Level	3−State
HIGH Logic Level	Normal Operation

1. If the OE pin is driven LOW, the FXMAR2102 is disabled and the A_0, A_1, B_0, and B_1 pins (including dynamic drivers) are forced into 3−state and all four 10 kΩ internal pull−up resisters are decoupled from their respective V_{CC}.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Unit
V_{CCA}, V_{CCB}	Supply Voltage		–0.5	7.0	V
V_{IN}	DC Input Voltage	A Port	–0.5	7.0	
		B Port	–0.5	7.0	
		Control Input (OE)	–0.5	7.0	
V_O	Output Voltage (Note 2)	A_n Outputs 3–State	–0.5	7.0	V
		B_n Outputs 3–State	–0.5	7.0	
		A_n Outputs Active	–0.5	V_{CCA} + 0.5 V	
		B_n Outputs Active	–0.5	V_{CCB} + 0.5 V	
I_{IK}	DC Input Diode Current	At $V_{IN} < 0$ V	–	–50	mA
I_{OK}	DC Output Diode Current	At $V_O < 0$ V	–	–50	mA
		At $V_O > V_{CC}$	–	+50	
I_{OH} / I_{OL}	DC Output Source/Sink Current		–50	+50	mA
I_{CC}	DC V_{CC} or Ground Current per Supply Pin		–	±100	mA
P_D	Power Dissipation	At 400 KHz	–	0.129	mW
T_{STG}	Storage Temperature Range		–65	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, B–Port Pins	–	8	kV
		Human Body Model, All Pins (JESD22–A114)	–	4	
		Charged Device Mode, JESD22–C101	–	2	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. I_O absolute maximum rating must be observed.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CCA}, V_{CCB}	Power Supply Operating		1.65	5.50	V
V_{IN}	Input Voltage (Note 3)	A–Port	0	5.5	V
		B–Port	0	5.5	
		Control Input (OE)	0	V_{CCA}	
Θ_{JA}	Thermal Resistance	8–Lead MicroPak	–	279	°C/W
		8–Lead Ultrathin MLP	–	302	
T_A	Free Air Operating Temperature		–40	+85	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. All unused inputs and I/O pins must be held at V_{CCI} or GND. V_{CCI} is the V_{CC} associated with the input side.

FUNCTIONAL DESCRIPTION

Power−Up / Power−Down Sequencing

FXM translators offer an advantage in that either V_{CC} may be powered up first. This benefit derives from the chip design. When either V_{CC} is at 0 V, outputs are in a high−impedance state. The control input (OE) is designed to track the V_{CCA} supply. A pull−down resistor tying OE to GND should be used to ensure that bus contention, excessive currents, or oscillations do not occur during power−up/−down. The size of the pull−down resistor is based upon the current−sinking capability of the device driving the OE pin.

The recommended power−up sequence is:

1. Apply power to the first V_{CC}.
2. Apply power to the second V_{CC}.
3. Drive the OE input HIGH to enable the device.

The recommended power−down sequence is:

1. Drive OE input LOW to disable the device.
2. Remove power from either V_{CC}.
3. Remove power from the other V_{CC}.

NOTE:

4. Alternatively, the OE pin can be hardwired to V_{CCA} to save GPIO pins. If OE is hardwired to V_{CCA}, either V_{CC} can be powered up or down first.

APPLICATION CIRCUIT

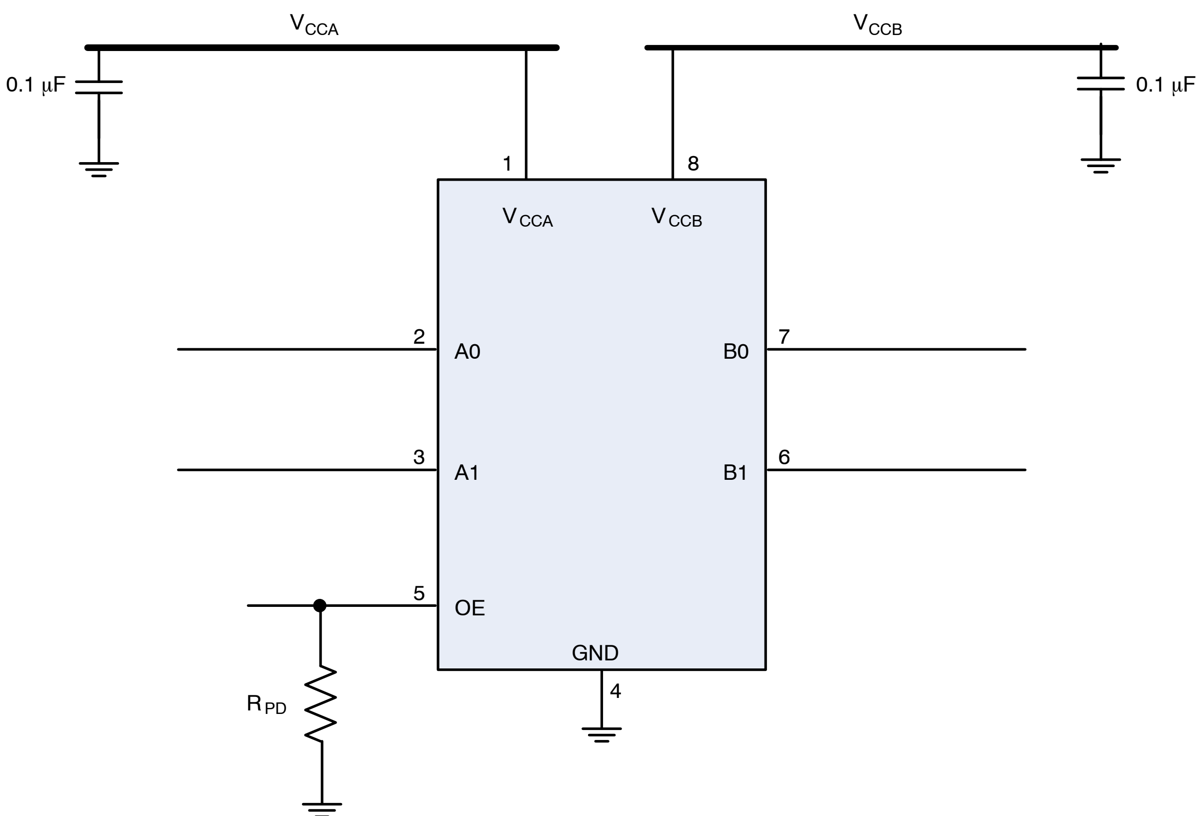


Figure 4. Application Circuit

APPLICATION NOTES

The FXMAR2102 has open−drain I/Os and includes a total of four 10 kΩ internal pull−up resistors (R_{PU}) on each of the four data I/O pins, as shown in Figure 4. If a pair of data I/O pins (A_n/B_n) is not used, both pins should disconnected, eliminating unwanted current flow through the internal RPUs. External RPUs can be added to the I/Os to reduce the total RPU value, depending on the total bus capacitance. The designer is free to lower the total pull−up resistor value to meet the maximum I^2C edge rate per the I^2C specification (*UM10204 rev. 03, June 19, 2007*). For example, according to the I^2C specification, the maximum edge rate (30% − 70%) during Fast Mode (400 kbit/s) is 300 ns. If the bus capacitance is approaching the maximum 400 pF, a lower total R_{PU} value helps keep the rise time below 300 ns (Fast Mode). Likewise, the I^2C specification also specifies a minimum Serial Clock Line High Time of 600 ns during Fast Mode (400 kHz). Lowering the total RPU also helps increase the SCL High Time. If the bus capacitance approaches 400 pF, it may make sense to use the FXMA2102, which does not contain internal RPUs. Then calculate the ideal external R_{PU} value.

NOTE:
5. Section 7.1 of the I^2C specification provides an excellent guideline for pull−up resistor sizing.

Theory of Operation

The FXMAR2102 is designed for high−performance level shifting and buffer / repeating in an I^2C application. Figure 1 shows that each bi−directional channel contains two series−Npassgates and two dynamic drivers. This hybrid architecture is highly beneficial in an I^2C application where auto−direction is a necessity.

For example, during the following three I^2C protocol events:

- Clock Stretching
- Slave's ACK Bit (9th bit = 0) following a Master's Write Bit (8th bit = 0)
- Clock Synchronization and Multi−Master Arbitration

The bus direction needs to change from master−to−slave to slave−to−master without the occurrence of an edge. If there is an I^2C translator between the master and slave in these examples, the I^2C translator must change direction when both A and B ports are LOW. The Npassgates can accomplish this task very efficiently because, when both A and B ports are LOW, the Npassgates act as a low−resistive short between the A and B ports.

Due to I^2C's open−drain topology, I^2C masters and slaves are not push/pull drivers. Logic LOWs are "pulled down" (Isink), while logic HIGHs are "let go" (3−state). For example, when the master lets go of SCL (SCL always comes from the master), the rise time of SCL is largely determined by the RC time constant, where R = RPU and C = the bus capacitance. If the FXMAR2102 is attached to the master [on the A port] and there is a slave on the B port, the Npassgates act as a low−resistive short between both ports until either of the port's $V_{CC}/2$ thresholds are reached. After the RC time constant has reached the $V_{CC}/2$ threshold of either port, the port's edge detector triggers both dynamic drivers to drive their respective ports in the LOW−to−HIGH (LH) direction, accelerating the rising edge. The resulting rise time resembles the scope shot in Figure 5. Effectively, two distinct slew rates appear in rise time. The first slew rate (slower) is the RC time constant of the bus. The second slew rate (much faster) is the dynamic driver accelerating the edge.

If both the A and B ports of the translator are HIGH, a high−impedance path exists between the A and B ports because both the Npassgates are turned off. If a master or slave device decides to pull SCL or SDA LOW, that device's driver pulls down (I_{sink}) SCL or SDA until the edge reaches the A or B port $V_{CC}/2$ threshold. When either the A or B port threshold is reached, the port's edge detector triggers both dynamic drivers to drive their respective ports in the HIGH−to−LOW (HL) direction, accelerating the falling edge.

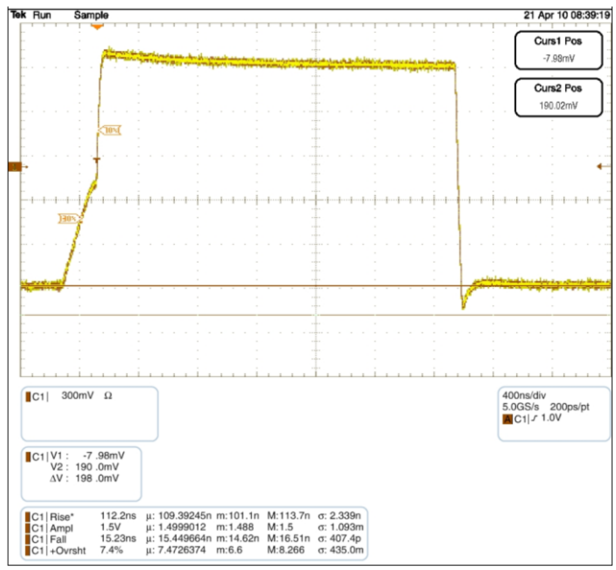


Figure 5. Waveform C: 600 pF, Total R_{PU}: 2.2 kΩ

V_{OL} vs. I_{OL}

The I^2C specification mandates a maximum V_{IL} (I_{OL} of 3 mA) of $V_{CC} \cdot 0.3$ and a maximum V_{OL} of 0.4 V. If there is a master on the A port of an I^2C translator with a V_{CC} of 1.65 V and a slave on the I^2C translator B port with a V_{CC} of 3.3 V, the maximum V_{IL} of the master is (1.65 V x 0.3) 495 mV. The slave could legally transmit a valid logic LOW of 0.4 V to the master.

If the I^2C translator's channel resistance is too high, the voltage drop across the translator could present a V_{IL} to the master greater than 495 mV. To complicate matters, the I^2C specification states that 6 mA of I_{OL} is recommended for bus capacitances approaching 400 pF. More I_{OL} increases the voltage drop across the I^2C translator. The I^2C application benefits when I^2C translators exhibit low V_{OL} performance.

Figure 6 depicts typical FXMAR2102 V_{OL} performance vs. the competition, given a 0.4 V V_{IL}.

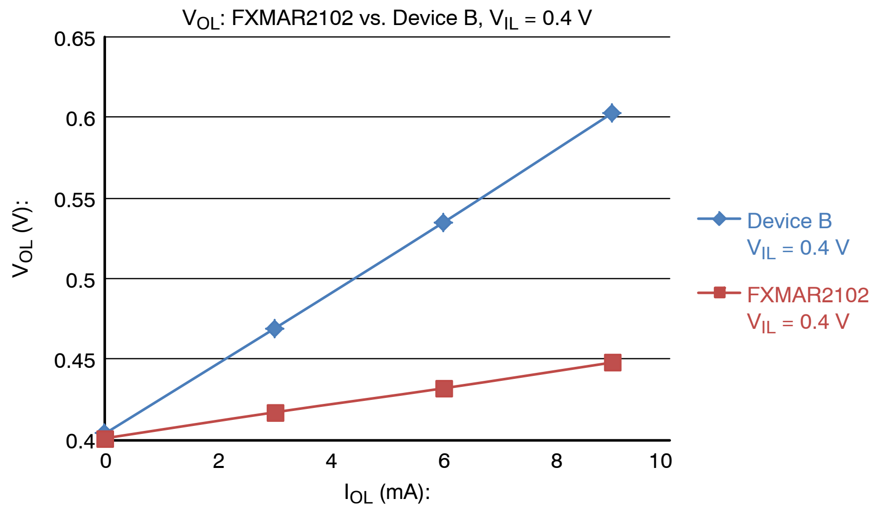


Figure 6. Device Comparison

I^2C–Bus Isolation

The FXMAR2102 supports I^2C–Bus isolation for the following conditions:

- Bus isolation if bus clear
- Bus isolation if either V_{CC} goes to ground

Bus Clear

Because the I^2C specification defines the minimum SCL frequency of DC, the SCL signal can be held LOW forever; however, this condition shuts down the I^2C bus. The I^2C specification refers to this condition as "Bus Clear". In Figure 7; if slave #2 holds down SCL forever, the master and slave #1 are not able to communicate because the FXMAR2102 passes the SCL stuck–LOW condition from slave #2 to slave #1 and as the master. However, if the OE pin is pulled LOW (disabled), both ports (A and B) are 3–stated. This results in the FXMAR2102 isolating slave #2 from the master and slave #1, allowing full communication between the master and slave #1.

V_{CC} to GND

If slave #2 is a camera that is suddenly removed from the I^2C bus, resulting in V_{CCB} transitioning from a valid V_{CC} (1.65 V – 5.5 V) to 0 V; the FXMAR2102 automatically forces SCL and SDA on both its A and B ports into 3–state. Once V_{CCB} has reached 0 V, full I^2C communication between the master and slave #1 remains undisturbed.

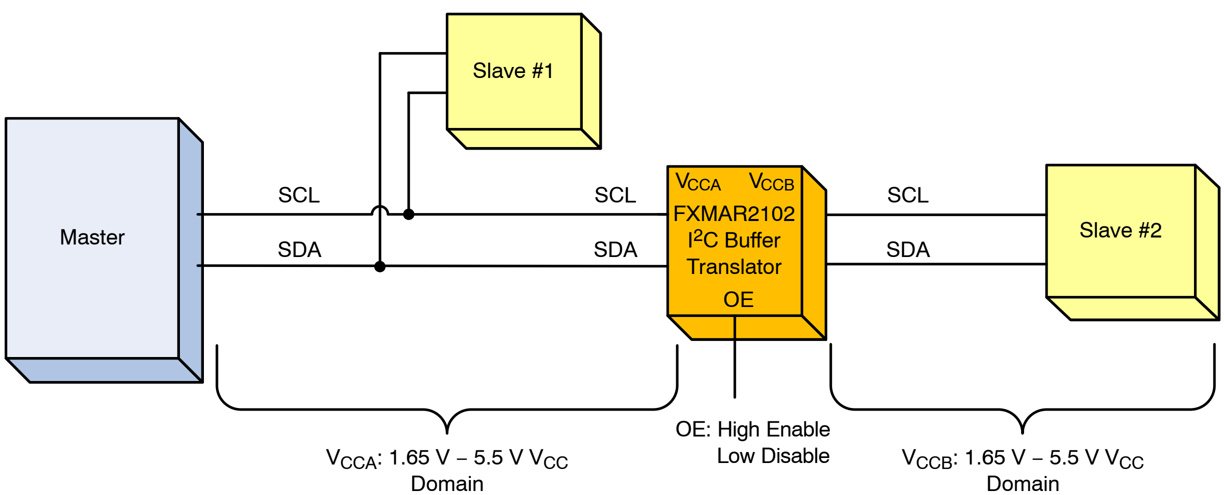


Figure 7. Bus Isolation

DC ELECTRICAL CHARACTERISTICS (T_A = −40°C to +85°C)

Symbol	Parameter	Condition		V_{CCA} (V)	V_{CCB} (V)	Min	Typ	Max	Unit
V_{IHA}	High Level Input Voltage A	Data Inputs A_n		1.65 – 5.50	1.65 – 5.50	V_{CCA} – 0.4	–	–	V
		Control Input OE		1.65 – 5.50	1.65 – 5.50	0.7 x V_{CCA}	–	–	
V_{IHB}	High Level Input Voltage B	Data Inputs B_n		1.65 – 5.50	1.65 – 5.50	V_{CCB} – 0.4	–	–	V
V_{ILA}	Low Level Input Voltage A	Data Inputs A_n		1.65 – 5.50	1.65 – 5.50	–	–	0.4	V
		Control Input OE		1.65 – 5.50	1.65 – 5.50	–	–	0.3 x V_{CCA}	
V_{ILB}	Low Level Input Voltage B	Data Inputs B_n		1.65 – 5.50	1.65 – 5.50	–	–	0.4	V
V_{OL}	Low Level Output Voltage	V_{IL} = 0.15 V		1.65–5.50	1.65–5.50	–	–	0.4	V
		I_{OL} = 6 mA					–		
I_L	Input Leakage Current	Control Input OE, V_{IN} = V_{CCA} or GND		1.65 – 5.50	1.65 – 5.50	–	–	±1.0	μA
I_{OFF}	Power−Off Leakage Current	A_n	V_{IN} or V_O = 0 V to 5.5 V	0	5.50	–	–	±2.0	μA
		B_n	V_{IN} or V_O = 0 V to 5.5 V	5.50	0	–	–	±2.0	
I_{OZ}	3−State Output Leakage (Note 7)	A_n, B_n	V_O = 0 V to 5.5 V, OE = V_{IL}	5.50	5.50	–	–	±2.0	μA
		A_n	V_O = 0 V to 5.5 V, OE = Don't Care	5.50	0	–	–	±2.0	
		B_n	V_O = 0 V to 5.5 V, OE = Don't Care	0	5.50	–	–	±2.0	
$I_{CCA/B}$	Quiescent Supply Current (Note 8, 9)	V_{IN} = V_{CCI} or Floating, I_O = 0		1.65 – 5.50	1.65 – 5.50	–	–	5.0	μA
I_{CCZ}	Quiescent Supply Current (Note 8)	V_{IN} = V_{CCI} or GND, I_O = 0, OE = V_{IL}		1.65 – 5.50	1.65 – 5.50	–	–	5.0	μA
I_{CCA}	Quiescent Supply Current (Note 7)	V_{IN} = 5.5 V or GND, I_O = 0, OE = Don't Care, B_n to A_n		0	1.65 – 5.50	–	–	–2.0	μA
				1.65 – 5.50	0	–	–	2.0	
I_{CCB}	Quiescent Supply Current (Note 7)	V_{IN} = 5.5 V or GND, I_O = 0, OE = Don't Care, A_n to B_n		1.65 – 5.50	0	–	–	–2.0	μA
				0	1.65 – 5.50	–	–	2.0	
R_{PU}	Resistor Pull−up Value	VCCA & VCCB Sides		1.65–5.50	1.65 – 5.50	–	10	–	Ω

6. This table contains the output voltage for static conditions. Dynamic drive specifications are given in Dynamic Output Electrical Characteristics.
7. "Don't Care" indicates any valid logic level.
8. V_{CCI} is the V_{CC} associated with the input side.
9. Reflects current per supply, V_{CCA} or V_{CCB}.

DYNAMIC OUTPUT ELECTRICAL CHARACTERISTICS

OUTPUT RISE / FALL TIME (Note 10) (Output load: C_L = 50 pF, R_{PU} = NC, push / pull driver, and T_A = −40°C to +85°C.)

Symbol	Parameter	V_{CCO} (Note 11)				Unit
		4.5 to 5.5 V	3.0 to 3.6 V	2.3 to 2.7 V	1.65 to 1.95 V	
		Typ	Typ	Typ	Typ	
t_{rise}	Output Rise Time; A Port, B Port (Note 12)	3	4	5	7	ns
t_{fall}	Output Fall Time; A Port, B Port (Note 13)	1	1	1	1	ns

10. Output rise and fall times guaranteed by design simulation and characterization; not production tested.
11. V_{CCO} is the V_{CC} associated with the output side.
12. See Figure 12.
13. See Figure 13.

DYNAMIC OUTPUT ELECTRICAL CHARACTERISTICS

MAXIMUM DATA RATE (Note 14) (Output load: C_L = 50 pF, R_{PU} = NC, push / pull driver, and T_A = −40°C to +85°C.)

V_{CCA}	Direction	V_{CCB}				Unit
		4.5 to 5.5 V	3.0 to 3.6 V	2.3 to 2.7 V	1.65 to 1.95 V	
		Minimums				
4.5 V to 5.5 V	A to B	50	50	40	30	MHz
	B to A	50	50	40	40	
3.0 V to 3.6 V	A to B	50	50	40	19	MHz
	B to A	50	50	40	40	
2.3 V to 2.7 V	A to B	40	40	30	19	MHz
	B to A	40	40	30	30	
1.65 V to 1.95 V	A to B	40	40	30	19	MHz
	B to A	30	30	19	19	

14. F−toggle guaranteed by design simulation; not production tested.

AC CHARACTERISTICS (Note 15) (Output load: C_L = 50 pF, R_{PU} = NC, push / pull driver, and T_A = −40°C to +85°C.)

Symbol	Parameter	V_{CCB}								Unit
		4.5 to 5.5 V		3.0 to 3.6 V		2.3 to 2.7 V		1.65 to 1.95 V		
		Typ	Max	Typ	Max	Typ	Max	Typ	Max	
V_{CCA} = 4.5 to 5.5 V										
t_{PLH}	A to B	1	3	1	3	1	3	1	3	ns
	B to A	1	3	2	4	3	5	4	7	
t_{PHL}	A to B	2	4	3	5	4	6	5	7	ns
	B to A	2	4	2	5	2	6	5	7	
t_{PZL}	OE to A	4	5	6	10	5	9	7	15	ns
	OE to B	3	5	4	7	5	8	10	15	
t_{PLZ}	OE to A	65	100	65	105	65	105	65	105	ns
	OE to B	5	9	6	10	7	12	9	16	
t_{skew}	A Port, B Port (Note 16)	0.50	1.50	0.50	1.00	0.50	1.00	0.50	1.00	ns
V_{CCA} = 3.0 to 3.6 V										
t_{PLH}	A to B	2.0	5.0	1.5	3.0	1.5	3.0	1.5	3.0	ns
	B to A	1.5	3.0	1.5	4.0	2.0	6.0	3.0	9.0	
t_{PHL}	A to B	2.0	4.0	2.0	4.0	2.0	5.0	3.0	5.0	ns
	B to A	2.0	4.0	2.0	4.0	2.0	5.0	3.0	5.0	
t_{PZL}	OE to A	4.0	8.0	5.0	9.0	6.0	11.0	7.0	15.0	ns
	OE to B	4.0	8.0	6.0	9.0	8.0	11.0	10.0	14.0	
t_{PLZ}	OE to A	100	115	100	115	100	115	100	115	ns
	OE to B	5	10	4	8	5	10	9	15	
t_{skew}	A Port, B Port (Note 16)	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns
V_{CCA} = 2.3 to 2.7 V										
t_{PLH}	A to B	2.5	5.0	2.5	5.0	2.0	4.0	1.0	3.0	ns
	B to A	1.5	3.0	2.0	4.0	3.0	6.0	5.0	10.0	
t_{PHL}	A to B	2.0	5.0	2.0	5.0	2.0	5.0	3.0	6.0	ns
	B to A	2.0	5.0	2.0	5.0	2.0	5.0	3.0	6.0	
t_{PZL}	OE to A	5.0	10.0	5.0	10.0	6.0	12.0	9.0	18.0	ns
	OE to B	4.0	8.0	4.5	9.0	5.0	10.0	9.0	18.0	
t_{PLZ}	OE to A	100	115	100	115	100	115	100	115	ns
	OE to B	65	110	65	110	65	115	12	25	
t_{skew}	A Port, B Port (Note 16)	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns
V_{CCA} = 1.65 to 1.95 V										
t_{PLH}	A to B	4	7	4	7	5	8	5	10	ns
	B to A	1.0	2.0	1.0	2.0	1.5	3.0	5.0	10.0	
t_{PHL}	A to B	5	8	3	7	3	7	3	7	ns
	B to A	4	8	3	7	3	7	3	7	
t_{PZL}	OE to A	11	15	11	14	14	28	14	23	ns
	OE to B	6	14	6	14	6	14	9	16	
t_{PLZ}	OE to A	75	115	75	115	75	115	75	115	ns
	OE to B	75	115	75	115	75	115	75	115	
t_{skew}	A Port, B Port (Note 16)	0.5	1.5	0.5	1.0	0.5	1.0	0.5	1.0	ns

15. AC characteristics are guaranteed by design and characterization.
16. Skew is the variation of propagation delay between output signals and applies only to output signals on the same port (A_n or B_n) and switching with the same polarity (LOW−to−HIGH or HIGH−to−LOW) *(see Figure 15)*. Skew is guaranteed; not production tested.

CAPACITANCE (T_A = +25°C.)

Symbol	Parameter	Condition	Typ	Unit
C_{IN}	Input Capacitance Control Pin (OE)	$V_{CCA} = V_{CCB}$ = GND	2.2	pF
$C_{I/O}$	Input/Output Capacitance, A_n, B_n	$V_{CCA} = V_{CCB}$ = 5.0 V, OE = GND	13	pF

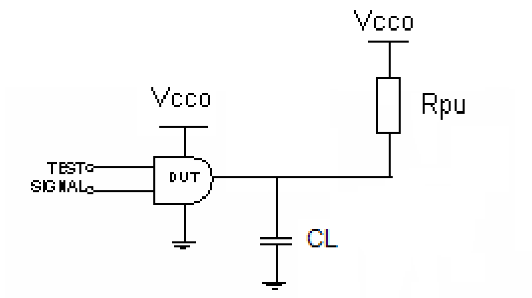


Figure 8. AC Test Circuit

Table 1. PROPAGATION DELAY TABLE (Note 17)

Test	Input Signal	Output Enable Control
t_{PLH}, t_{PHL}	Data Pulses	V_{CCA}
t_{PZL} (OE to A_n, B_n)	0 V	LOW to HIGH Switch
t_{PLZ} (OE to A_n, B_n)	0 V	HIGH to LOW Switch

17. For t_{PZL} and t_{PLZ} testing, an external 2.2 kΩ pull−up resister to V_{CCO} is required in order to force the I/O pins high while OE is Low because when OE is low, the internal 10 kΩ RPUs are decoupled from their respective VCC’s.

Table 2. AC LOAD TABLE

V_{CCO}	C_L	R_L
1.8 ±0.15 V	50 pF	NC
2.5 ±0.2 V	50 pF	NC
3.3 ±0.3 V	50 pF	NC
5.0 ±0.5 V	50 pF	NC

TIMING DIAGRAMS

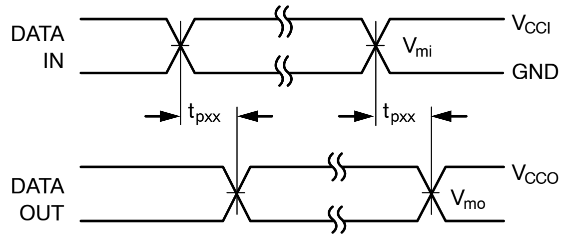


Figure 9. Waveform for Inverting and Non−Inverting Functions (Note 18)

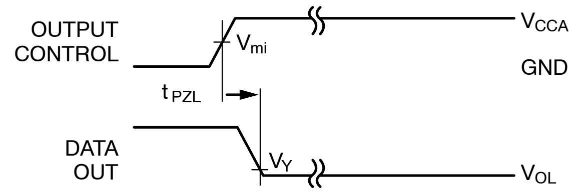


Figure 10. 3−STATE Output Low Enable Time (Note 18)

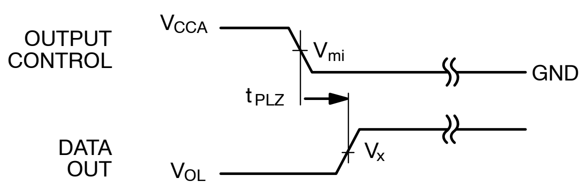


Figure 11. 3−STATE Output High Enable Time (Note 18)

Symbol	V_{CC}
V_{mi} (Note 19)	V_{CCI} / 2
V_{mo}	V_{CCO} / 2
V_{X}	0.5 x V_{CCO}
V_{Y}	0.1 x V_{CCO}

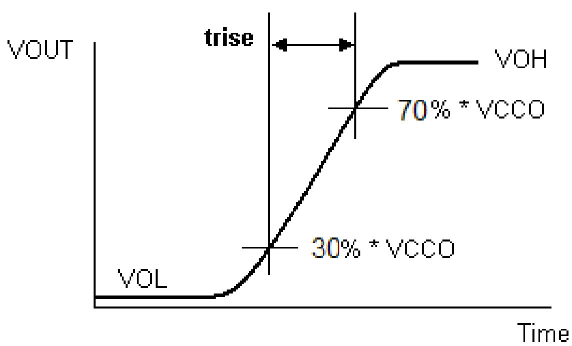


Figure 12. Active Output Rise Time

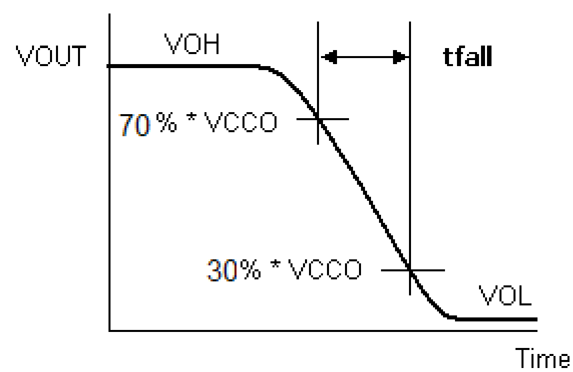


Figure 13. Active Output Fall Time

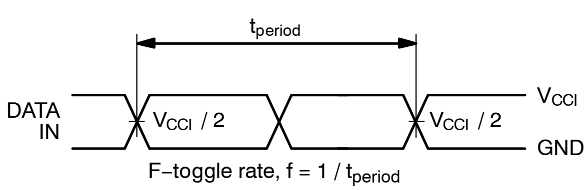


Figure 14. F−Toggle Rate

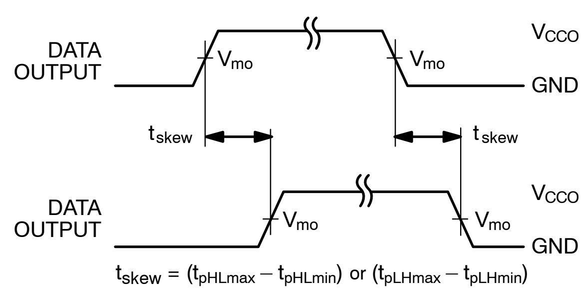


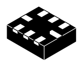
Figure 15. Output Skew Time

NOTES:
18. Input t_R = t_F = 2.0 ns, 10% to 90% at V_{IN} = 1.65 V to 1.95 V;
Input t_R = t_F = 2.0 ns, 10% to 90% at V_{IN} = 2.3 V to 2.7 V;
Input t_R = t_F = 2.5 ns, 10% to 90%, at V_{IN} = 3.0 V to 3.6 V only;
Input t_R = t_F = 2.5 ns, 10% to 90%, at V_{IN} = 4.5 V to 5.5 V only.
19. V_{CCI} = V_{CCA} for control pin OE or V_{mi} = (V_{CCA} / 2).

ORDERING INFORMATION

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method†
FXMAR2102L8X	−40 to +85°C	BU	8−Lead MicroPak, 1.6 mm Wide (Pb−Free)	5000 / Tape & Reel
FXMAR2102UMX			8−Lead Ultrathin MLP, 1.2 mm x 1.4 mm (Pb−Free)	

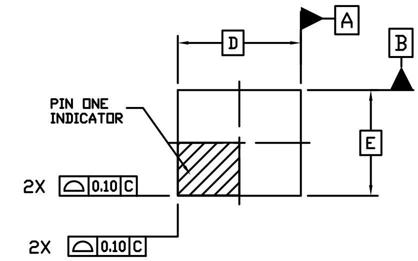
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.



SCALE 4:1

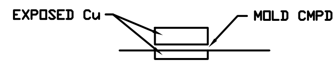
UQFN8, 1.4x1.2, 0.4P
CASE 523AS
ISSUE B

DATE 19 AUG 2021



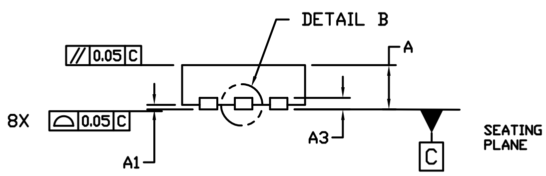
TOP VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.25MM FROM THE TERMINAL TIP.
4. REFER TO SPECIFIC DEVICE DATA SHEET FOR PIN 1 NOTCH LOCATION.

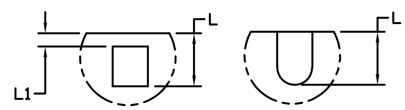


DETAIL B
ALTERNATE CONSTRUCTION

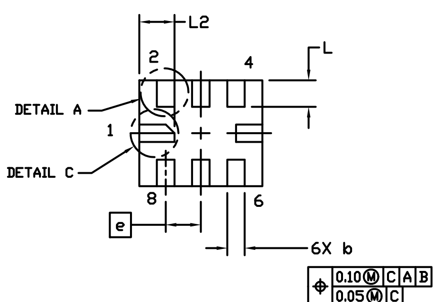
DIM	MILLIMETERS MIN.	MAX.
A	0.45	0.55
A1	0.00	0.05
A3	0.13 REF	
b	0.15	0.25
D	1.40 BSC	
E	1.20 BSC	
e	0.40 BSC	
L	0.20	0.40
L1	---	0.15
L2	0.30	0.50



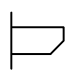
SIDE VIEW



DETAIL A
ALTERNATE CONSTRUCTIONS

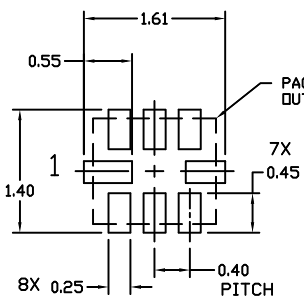


BOTTOM VIEW



DETAIL C
ALTERNATE CONSTRUCTION

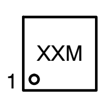
NOTE 4



RECOMMENDED
MOUNTING FOOTPRINT *

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



XX = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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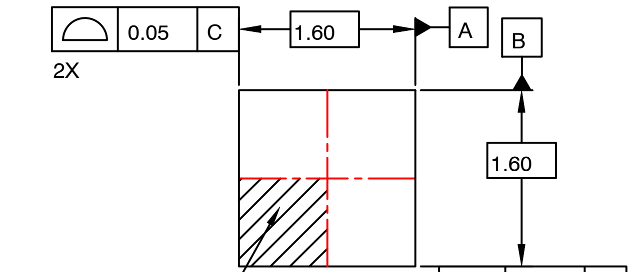
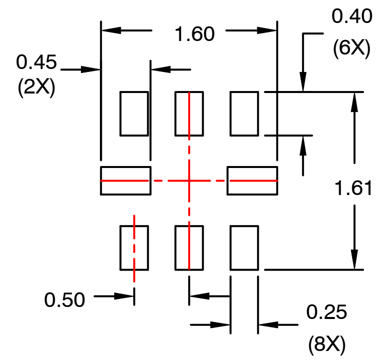
UQFN8 1.6X1.6, 0.5P
CASE 523AY
ISSUE O

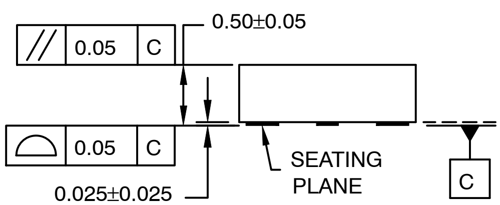
DATE 31 AUG 2016



TOP VIEW



RECOMMENDED
LAND PATTERN



SIDE VIEW

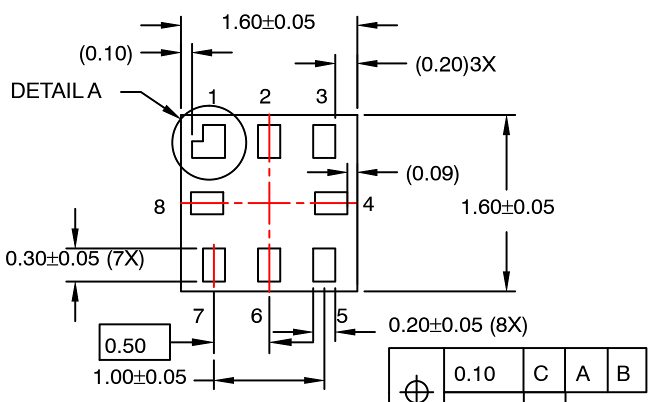
NOTES:

A. PACKAGE CONFORMS TO JEDEC MO−255 VARIATION UAAD.

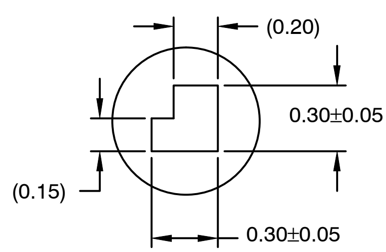
B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.

D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.



BOTTOM VIEW



DETAIL A
SCALE : 2X

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DESCRIPTION:	UQFN8 1.6X1.6, 0.5P	PAGE 1 OF 1