GigaDevice Semiconductor Inc.

GD30WS8662x
Linear Charger for Wearable Application

Datasheet

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- TWS earbuds charging case
- Headsets and hearing aids
- Low battery applications such as smart watches and fitness accessories
- Patient monitors and portable medical equipment

3 General description

The GD30WS8662x is a highly integrated Li-ion charger IC for wearable and IoT applications. The IC integrates a high accuracy linear charger of programmable charging current (up to 456mA). The device also includes power path management and high input protection functions. A low quiescent current, low noise LDO capable of delivering 50mA load current is also implemented internally.

The device integrates advanced power path management and control that allows the device to provide power to the system while charging the battery even with poor adapters. The dynamic power path management is able to automatically balance the currents delivered to the system and battery charging. A high voltage and over current protection circuit is implemented in the IC to protect it from high input voltage as high as 32V.

The GD30WS8662x device supports charge current up to 456mA and supports termination current down to 1mA. The maximum charge current is set at a default of 128mA and is programmable via I^2C. The battery is charged using a standard Li-Ion charge profile with three phases: pre-charge, constant current and constant voltage regulation.

The device has several power saving modes to increase battery life whether the product is in storage or in operation.

The versatile features of GD30WS8662x allow for it to best used in wearable applications such as headsets, earbuds and hearing aids, or low battery applications such as smart watches and fitness accessories, or patient monitors and portable medical equipment.

The GD30WS8662x is available in a compact WLCSP-9 1.75mmx1.75mm package.

4 Device overview

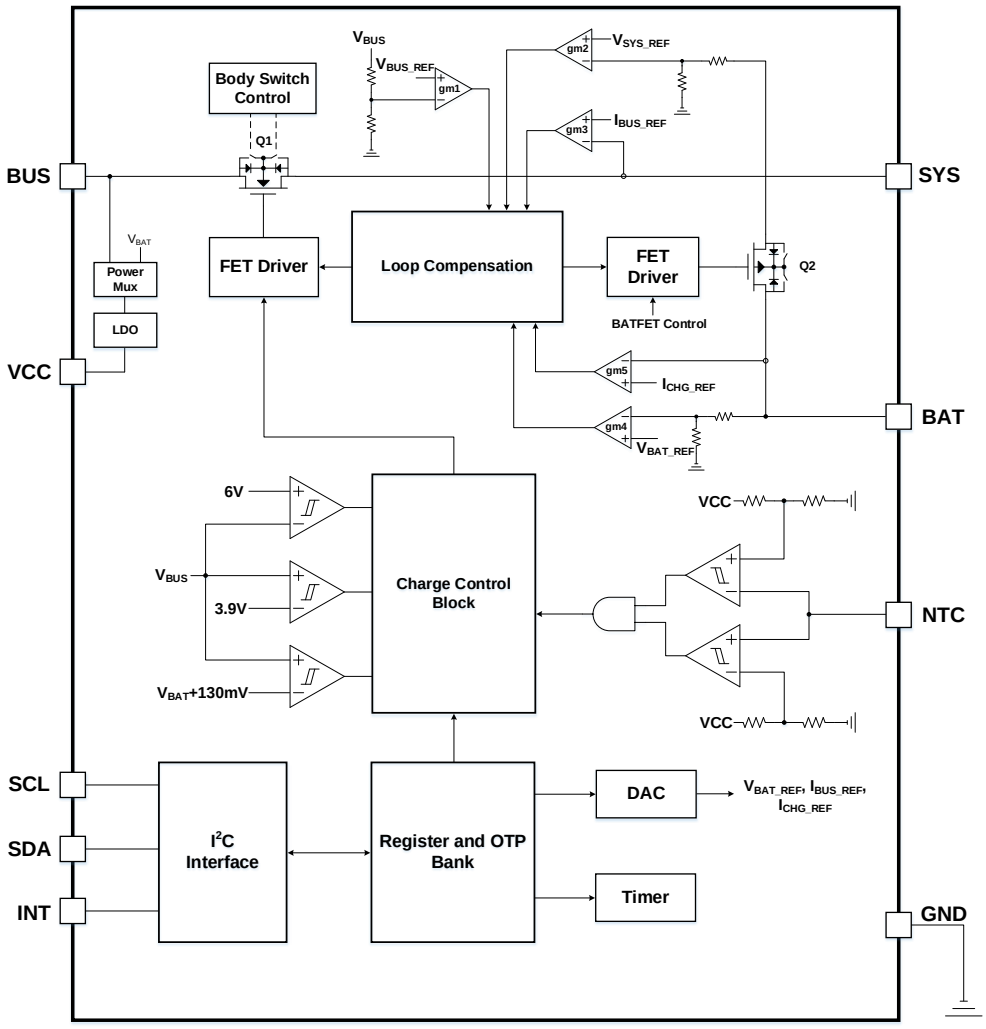
4.1 Device information

Table 4-1 Device Information for GD30WS8662x

Part Number	Package	Function	Description
GD30WS8662x	WLCSP-9 (1.75X1.75)	With I²C Interface	Linear charger for wearable application

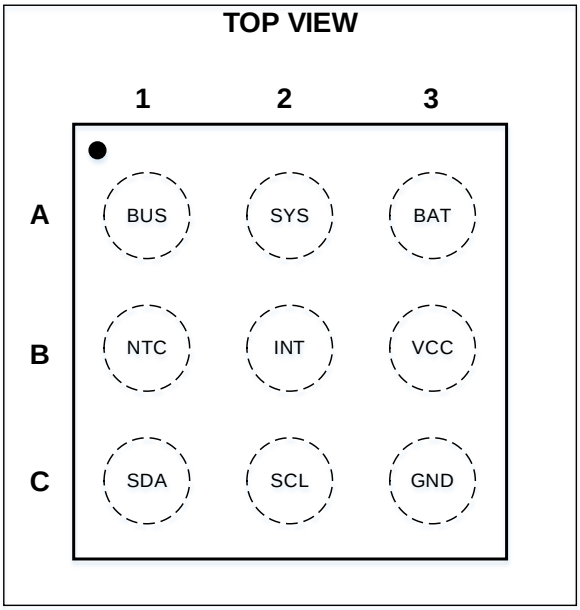
4.2 Block diagram

Figure 4-1 Block Diagram for GD30WS8662x



4.3 Pinout and pin assignment

Figure 4-2 GD30WS8662x WLCSP-9 Pinouts



4.4 Pin definitions

Table 4-2 GD30WS8662x PIN Configuration

Pin Name	Pins	Pin Type	Functions description
BUS	A1	P	**Input power pin**. Power input from BUS or other 5-V voltage source. Connect a ceramic capacitor from BUS to GND as close to IC as possible.
SYS	A2	P	**System power supply**. Connect a ceramic capacitor from SYS to GND as close to IC as possible.
BAT	A3	P	**Battery pin**. Connect to battery positive node. Connect a ceramic capacitor from BAT to GND as close to IC as possible.
NTC	B1	I/O	**Temperature sense input**. Connect a negative temperature coefficient thermistor to NTC. Program the hot and cold temperature window with a resistor divider from VCC to NTC to GND. Charging is suspended when NTC is out of the range. Pull NTC to VCC if NTC function is not used.
INT	B2	I/O	**Open drain interrupt output**. Send charge status and fault interruption to host.
VCC	B3	I/O	**Internal control power supply pin**. LDO output voltage, connect a 1uF ceramic capacitor from VCC to GND.
SCL	C1	I/O	**I²C communication from/to the host controller, clock**.

Pin Name	Pins	Pin Type	Functions description
SDA	C2	O	**I²C communication to the host controller, data**.
GND	C3	G	**Ground**.

Notes:

1. Type: O = Output, I/O = Input or Output, P = Power, G = Ground.

5 Functional description

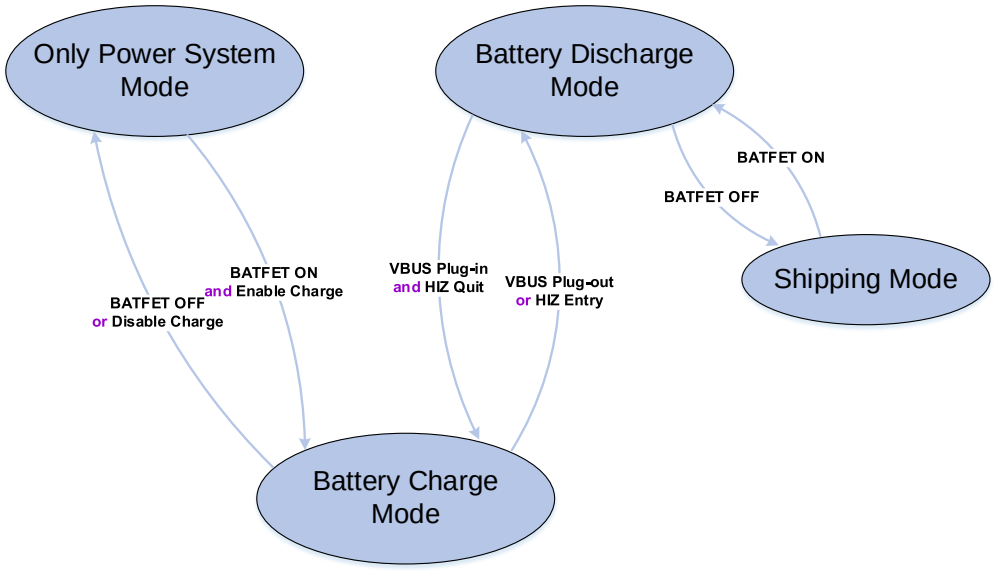
5.1 Power supply

The internal bias circuit of the IC is powered from the higher voltage of either BUS or BAT. When BUS or BAT rises above its respective under-voltage (UVLO) threshold, the sleep comparator, battery depletion comparator, and BATFET(Q2) driver are all active. The I^2C interface is ready for communication, and all register are reset to the default value. The host can access all of the register.

5.2 Operation mode

The GD30WS8662x has three different operation modes: shipping, battery operation and BUS operation mode, as shown in Figure 5-1. The mode of operation is saved in REG04 bit[12:8].

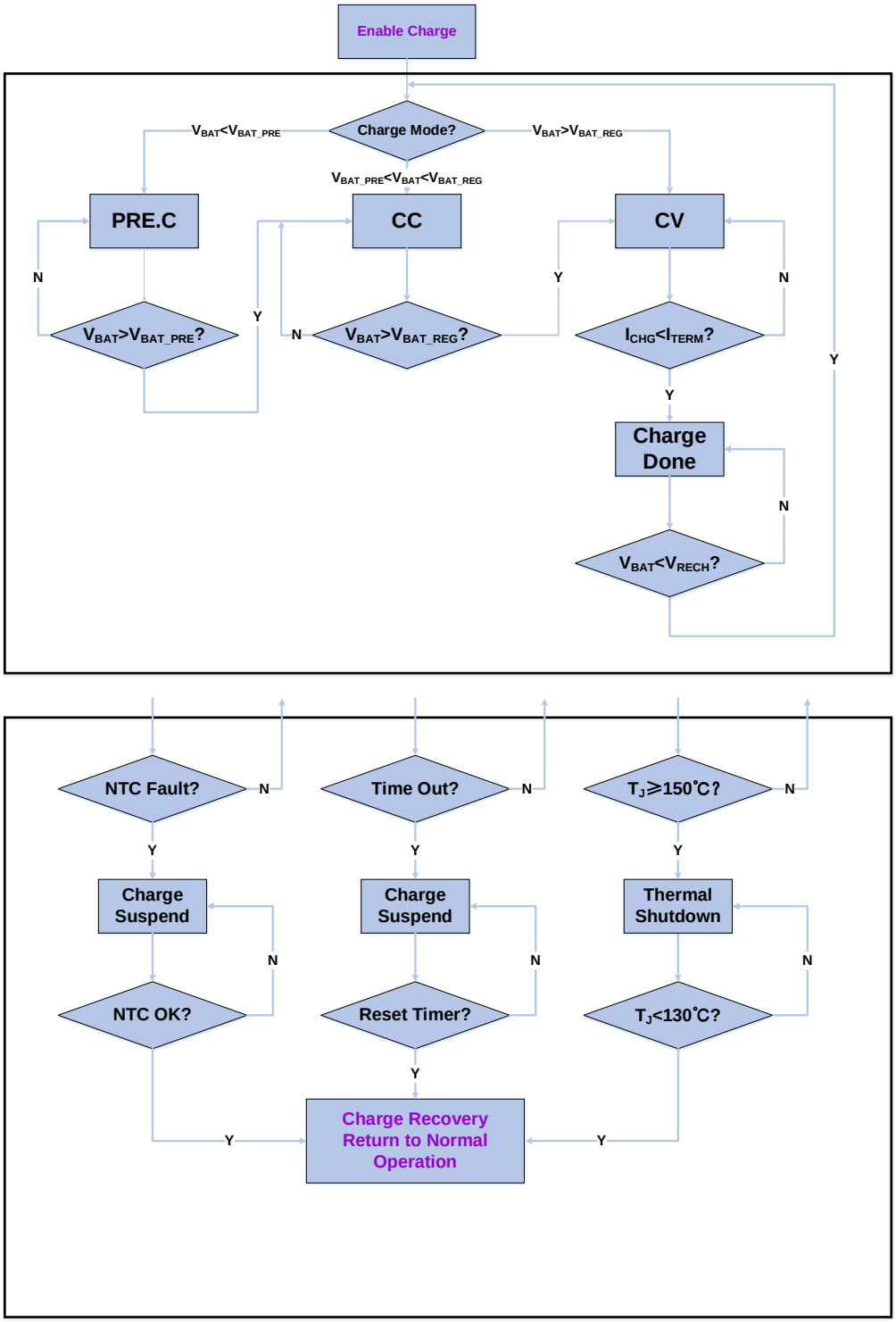
Figure 5-1 GD30WS8662x Operation Modes.



5.3 Battery charge

The GD30WS8662x device integrates a linear charger that allows the battery to be charged with a programmable charge current up to 456mA. In addition to the charge current, other charging parameters can be also programmed through I^2C such as the battery regulation voltage, pre-charge current and termination charge current. The device supports multiple battery regulation voltage regulation settings (V_{REG}) and charge current (I_{CHG}) options to support multiple battery chemistries for single-cell applications**.** A full one-cell linear charger state diagram as shown in Figure 5-2 is implemented in the IC.

Figure 5-2 Battery Charge State Diagram



The GD30WS8662x provide three main charging phases: Pre-charge, Constant current charge and constant voltage charge in Figure 5-3.

Phase 1 (pre-charge): The GD30WS8662x can safely pre-charge the deeply depleted battery until the battery voltage reaches the pre-charge to constant current threshold(V_{BAT_PRE}). The pre-charge current is also programmed through REG01H bit[3:0]. The pre-charge current is equal to 20% of the I_{CC}. The pre-charge current is also programmed

through REG01H bit[3:0]. If V_{BAT_PRE} is not reached before the pre-charge timer (1hr) expires, the charge cycle stop, and a corresponding timeout fault signal is asserted.

Phase 2 (constant-current charge): When the battery voltage exceeds V_{BAT_PRE}, the GD30WS8662x enters a constant current charge phase. The phase charge current can be programmed via REG01H bit[13:8].

Phase 3 (constant-voltage charge): When the battery voltage rises to the battery-full voltage(V_{BAT_REG}) set via REG02H bit [15:10], the charge mode changes from CC mode to CV mode, and the charge current starts decreasing.

Assuming that the termination function EN_TERM is set via REG02H bit[4] = 1, the charge cycle is considered to be completed when the charge current (I_{CHG}) reaches the termination current threshold (I_{TERM}). The charge status is immediately updated to charge done.

The termination charge current threshold (I_{TERM}) can be programmed via REG01H bit[3:0]. If EN_TERM = 0, the termination fuction is disable and all of the above actions are invalid (see Table 5-1).

Table 5-1 Termination Fucnction Selection Table

EN_TERM	After I_{BAT} Reaches I_{TERM} in CV Mode	
	Operation	**Charge status**
0	Keep CV Charge	Charge
1	Charge done	Charge done

Notes:

1. Type: x = Don't Care.

During the entire charging process, the actual charge current may be less than the register setting due to other loop regulations, such as dynamic power management (DPM) regulation (input voltage, input current) or thermal regulation.

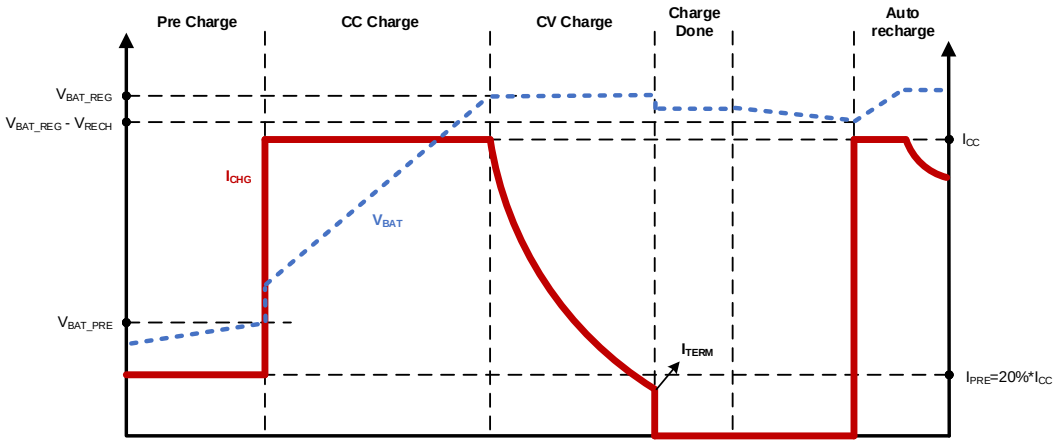
A new charge cycle starts when any of the following conditions are valid:

- The input power is recycled.
- Battery charging is enabled via the I^2C.
- Auto-recharge kick in.

Under the following conditions:

- No termistor fault at NTC.
- No safety timer fault.
- No battery over-voltage event.
- BATFET is not forced off.

Figure 5-3 Battery Charge Cycle and Charge Parameters



The charger input has back to back blocking FETs to prevent reverse current flow from BAT to BUS. They also integrate control circuitry regulating the input current and prevents excessive currents from being drawn from the input power supply for more reliable operation.

5.4 Auto recharge

When the battery is fully charged and charging is terminated, the battery may be discharged due to system consumption or self-discharge. When the battery voltage is discharge below the recharge threshold and V_{BUS} is still in the operating range, the GD30WS8662x begins another new charging cycle automatically without having to restart a charging cycle manually. The auto-recharge function is valid only when EN_TERM = 1.

5.5 Battery discharge

If the battery is connected and the input source is missing, the BATFET is fully on when V_{BAT} is above the V_{BAT_UVLO} threshold. The 100mΩ BATFET minimizes conduction loss during discharge. The quiescent current of the GDWS8662x is as low as 6.5uA in this mode. The low R_{DS_ON} and low I_Q help extend the running time of the battery.

5.6 Power path management and battery supplyment

The GD30WS8662x employs a pass-through power path structure with the BATFET to decouple the system from the battery. This allows for separate control between the system and the battery. The system is given the priority to start up, even with a deeply discharged or missing battery. When the input power is available, even with a depleted battery, the system voltage is always regulated to V_{SYS_REG} by the integrated LDOFET. The direct power structure consists of a frontend LDOFET between BUS and SYS and a BATFET between SYS and BAT. The LDOFET and BATFET can be controlled by the I^2C (see Table 5-2).

Table 5-2 FET Control Via I²C

FET ON/OFF Changed by control	Hi-Z Mode and Charge Control	
	Set EN_HIZ to 1	Set CEB to 0
LDOFET	ON	x
BATFET (Charging)	x	ON
BATFET (discharging)	x	x

Notes:

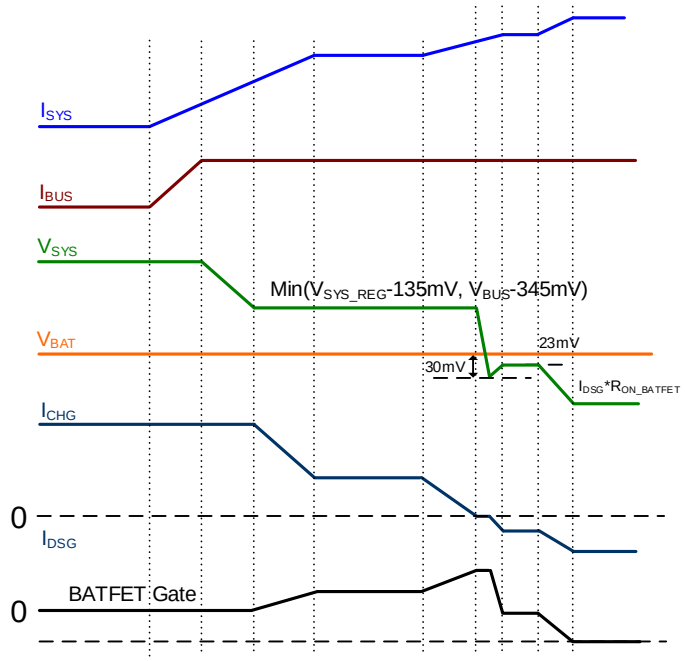
1. Type: x = Don't Care.

For the system voltage control, when the input voltage is higher than V_{SYS_REG}, the system voltage is regulated to V_{SYS_REG}. When the input voltage is lower than V_{SYS_REG}, the LDOFET is fully on with input current limit.V_{SYS_REG} can be programmed through REG03H bit[3:0].

The charge current is reduced to keep the input current or input voltage in regulation when DPM occurs. If the charge current is reduced to zero and the input source is still overloaded due to a heavy system load, the system voltage begins decreasing. Once the system voltage drops to 30mV below the battery voltage, the GD30WS8662x enters battery supplement mode, and the ideal diode mode is enabled. The BATFET is regulated to keep V_{BAT} - V_{SYS} at 23mV when I_{DSG} (supplement current) * R_{ON_BATFET} is lower than 23mV. In the case that I_{DSG} * R_{ON_BATFET} is higher than 23mV, the BATFET is fully turned on to maintain the ideal forward voltage. When the system load decreases, once V_{SYS} is higher than V_{BAT} + 23mV, the ideal diode mode is disabled. Figure 5-4 Dynamic Power Management and Battery Supplement Operation Profile.

When V_{BUS} is not available, the GD30WS8662x operates in discharge mode, and the BATFET is always fully on to reduce loss.

Figure 5-4 Dynamic Power Management and Battery Supplement Operation Profile



5.7 Internal control power supply (LDO)

The integrated LDO not only provides the supply voltage for the IC and also is capable of supplying output up to 50mA current through VCC.

5.8 Interrupt to host (INT)

The GD30WS8662x also has an alert mechanism that can output an interrupt signal via INT to notify the system of the operation by outputting a 256us low-state INT pluse. All of the below events can trigger an INT output.

- Good input source detected (PG_STAT)
- Charge completed
- Charging status change
- Fault in REG04H (watchdog timer fault, thermal fault, safety timer fault, battery OVP fault, NTC fault)

When fault occurs, the GD30WS8662x sends out an INT pulse and latches the fault state in REG04H. After the GD30WS8662x exits the fault state, the fault bit is reset to 0 after the host reads REG04H. The NTC fault bit is not latched and always reports the current thermistor conditions.

The INT signal can be masked when the corresponding control bit is set in REG03H bit[12:8]. When an INT condition is masked, this means that the INT pin signal (and register bit) will not trigged when the corresponding condition occurs. Masking INTs is useful when writing software code to avoid unnecessary interruptions due to these events.

5.9 NTC battery temperature

NTC allows the GD30WS8662x to sense the battery temperature using the thermistor (usually available in the battery pack) to ensure a safe operating environment for the battery. Connect appropriately valued resistors from VCC to NTC to ground. The resistor divider works with a thermistor connected from NTC to ground. The NTC voltage is determined by the resistor divider whose divide ratio depends on the temperature. The GD30WS8662x sets a pre-determined upper and lower bound of the divide ratio for NTC cold and NTC hot internally.

In the GD30WS8662x, the I²C default setting is PCB_OTP. This function can be changed through the I²C (see Table 5-3).

Table 5-3 NTC Function Selection Table

I²C Control		Function
EN_NTC	EN_PCB_OTP	
0	x	Disable
1	1	NTC
1	0	PCB_OTP

Notes:

1. Type: x = Don't Care.

When PCB_OTP is selected and the NTC voltage is lower than the NTC hot threshold, both the LDOFET(Q1) and BATFET are off. The PCB_OTP fault also sets the NTC_FAULT status (REG04H bit[1]) to 1 to show the fault. Operation resumes once the NTC voltage is higher than the NTC hot threshold.

The NTC function works only in charge mode. Once the NTC voltage falls out of this divide ratio, the temperature is outside of the safe operating range, and the GD30WS8662x stops charging and report it on the status bits. Charging resumes automatically after the temperature falls back into the safe range.

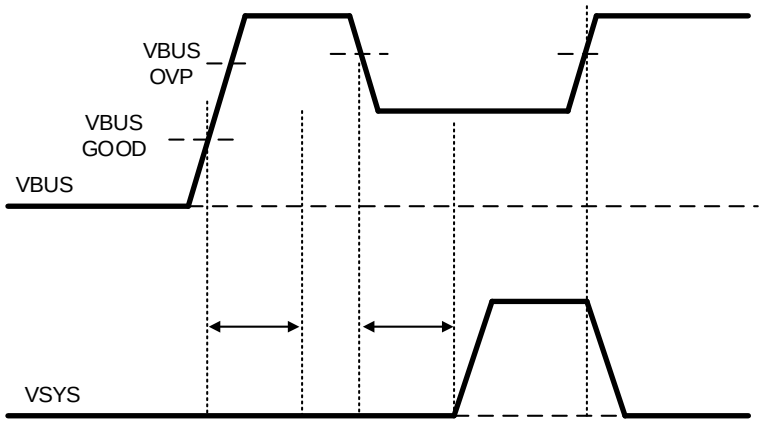
5.10 System protection

5.10.1 Input OVP and UVLO protection

The GD30WS8662x has an input over-voltage protection (OVP) threshold and input UVLO threshold. Once the input voltage is out of its normal range, the LDOFET is turned off immediately.

When the input voltage is identified as a good source, a immunity timer becomes active. If the input power is normal until the immunity timer expires, the system start up. Otherwise, Q1 remains off (see Figure 5-5).

Figure 5-5 Input Power Detection Operation Profile



5.10.2 Battery OVP protection

The GD30WS8662x is designed with a built-in battery over-voltage limit (about 130mV higher than V_{BAT_REG}). When a battery over-voltage event occurs, the GD30WS8662x suspends charging immediately and asserts a fault.

5.10.3 Over-discharge current protection

The GD30WS8662x has an over-discharge current protection in discharge mode and supplement mode. Once IDSG exceeds the programmable discharge current limit (2A default), the BATFET turns off after a 60μs delay. The GD30WS8662x enters hiccup mode as part of the over-current protection (OCP). The discharge current limit can be programmed high to 3.2A through the I^2C. If the discharge current goes high and reaches the internal fixed current limit (about 3.7A), the BATFET turns off and begins hiccup mode immediately. Similarly, when the battery voltage falls below the programmable V_{BAT_UVLO} threshold (2.76V default), the BATFET turns off to prevent an over-discharge.

5.10.4 Short-circuit protection

The GD30WS8662x features SYS node short-circuit protection (SCP) for both the BUS to SYS path and the BAT to SYS path.

The system voltage is monitored continuously. If V_{SYS} is lower than 1.5V, system SCP for both the BUS to SYS path and the BAT to SYS path is active. I_{DSG} decreases to half of the original value.

For the BUS to SYS path, once I_{BUS} is over the protection threshold, both the LDOFET and BATFET are turned off immediately, and the GD30WS8662x enters hiccup mode. Otherwise, the maximum current limit is not reached. When V_{SYS} is lower than 1.5V and the setting input current limit is reached, the hiccup mode also starts after a 60μs delay. The hiccup mode interval is 800μs.

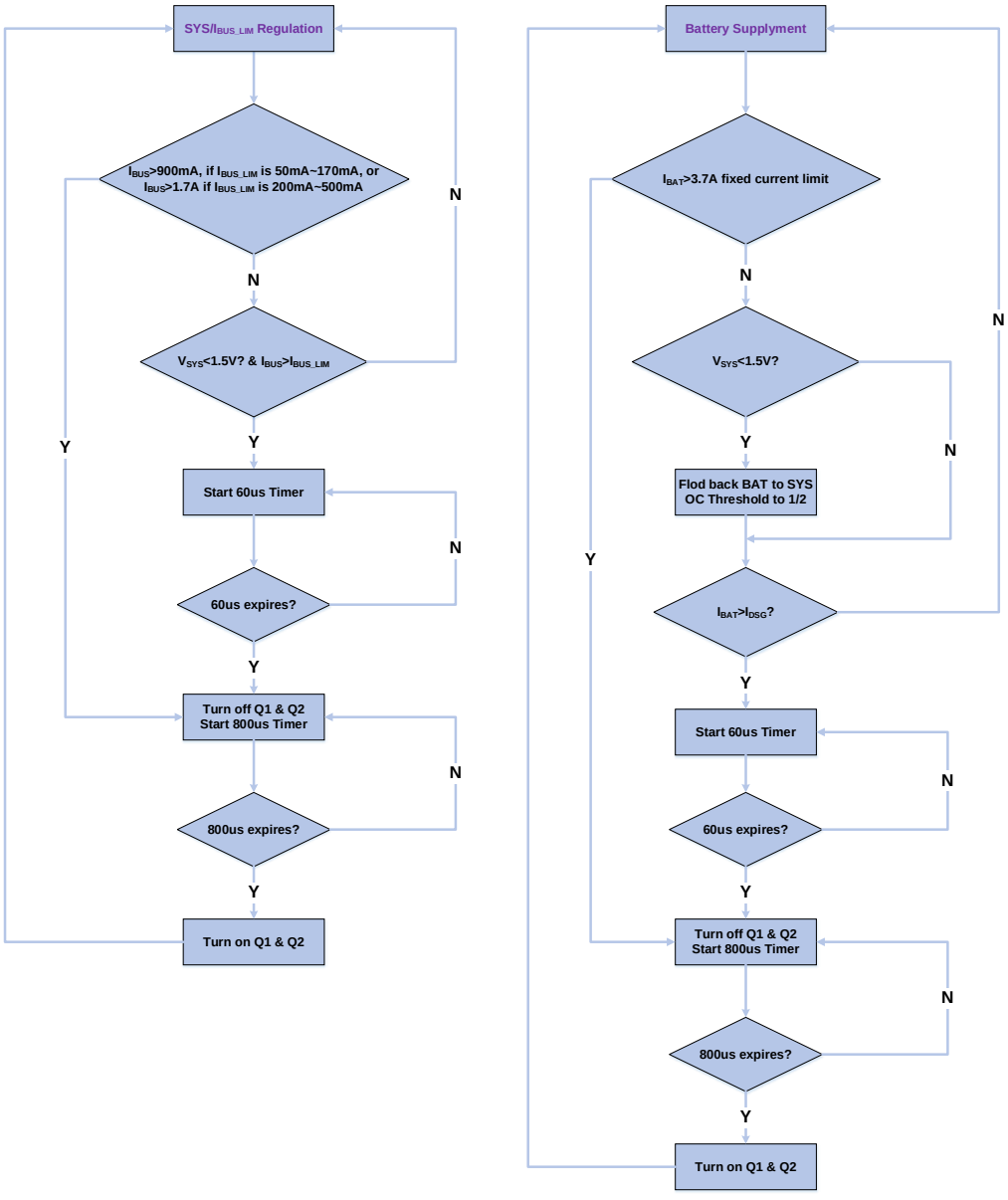
For the BAT to SYS path, once IBAT is over the 3.7A protection threshold, both the LDOFET and BATFET are turned off immediately, and the GD30WS8662x enters hiccup mode. When

the battery discharge current limit threshold is reached, hiccup mode starts after a 60μs delay. The hiccup mode interval is 800μs.

Particularly, if a system short-circuit occurs when both the input and battery are present, the protection mechanism of both paths works. The faster one of the two dominates the hiccup operation.

For details, please refer to the flow chart shown in Figure 5-6.

Figure 5-6 System Short-Circuit Protection



5.10.5 Over temperature protection

The GD30WS8662x monitors the internal junction temperature continuously to maximize power delivery and avoid overheating the chip. When the internal junction temperature reaches the preset limit of T_{J_REG} (120°C default), the IC starts to reduce the charge current to prevent higher power dissipation. The multiple thermal regulation thresholds from

60~120°C help the system design meet the thermal requirements in different applications. The junction temperature regulation threshold can be set via REG03H bit[5:4]. When the junction temperature reaches 150°C, both Q1 and Q2 turn off.

5.10.6 Safety timer

The GD30WS8662x provides both a pre-charge and constant current charge safety timer to prevent an extended charging cycle due to abnormal battery conditions. The safety timer is 1hr when the battery voltage is lower than V_{BAT_PRE}. The constant current(CC) charge safety timer starts when the battery enters CC charge mode. The CC charge safety timer can be programmed through the I^2C. The safety timer can be disabled via the I^2C.

The following actions can restart the safety timer.

- A new charge cycle is kicked in.
- Write REG00H bit[3] from 1 to 0 (charge disable to enable).
- Write REG00H bit[4] from 1 to 0 (HIZ enable to disable).

5.11 Host mode and default mode

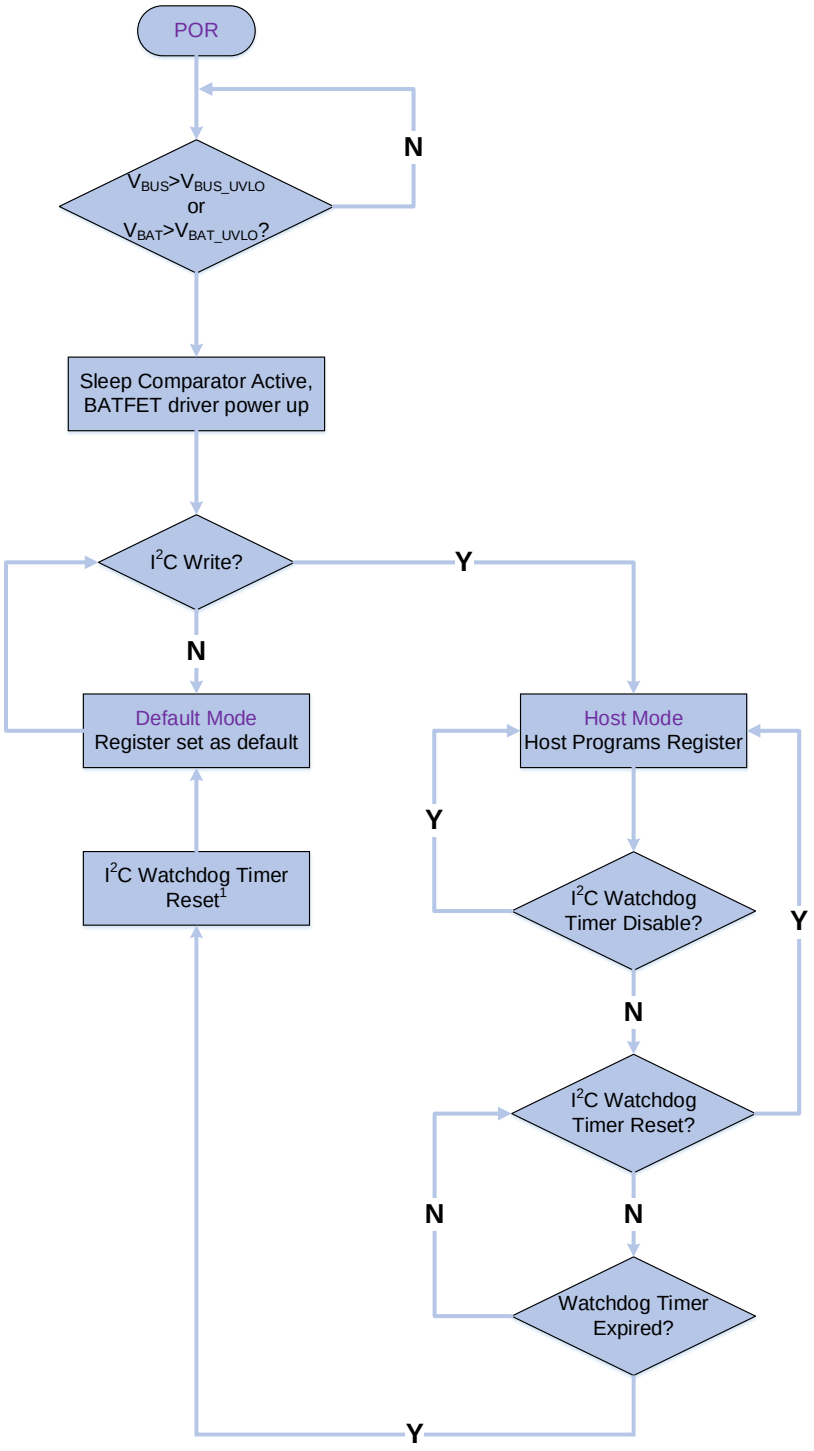
The GD30WS8662x is a host-controlled device. After the power-on reset, the GD30WS8662x starts up in a watchdog timer expiration state or default mode. All registers are in their default settings.

The watchdog timer works in both charge and discharge mode. When the watchdog timer run out, most registers return to the default value (refer to the I^2C Register Map section on 5.14). When the watchdog timer is out in both charge and discharge mode, both the LDOFET and BATFET are turned off. They turn on again automatically after t_{RST_DUR}, which can be programmed by REG00H bit[5].

To save quiescent current during discharge mode, the watchdog timer can be turned off during by setting REG02H bit[7] to 0.

Any write to the GD30WS8662x switches it to host mode. All charge parameters are programmable. If the watchdog timer (REG02H bit[6:5]) is not disabled, the host must reset the watchdog timer regularly by writing 1 to REG01H bit[14] before the watchdog timer expires to keep the device in host mode. Once the watchdog timer expires, the GD30WS8662x goes back to default mode. The watchdog timer limit can also be programmed or disabled by the host control.

Figure 5-7 Host Mode and Default Mode Selection



Notes:

1. Once the watchdog timer expires, the I²C watchdog timer must be reset or will not be valid in the next cycle.

5.12 Shipping mode

In applications where the battery is not removable, it is essential to disconnect the battery from the system for shipping mode or to allow the system power to be reset during the application. The GD30WS8662x provides both shipping mode (shown in Table 5-4) and system reset mode for different applications.

Table 5-4 Shipping Mode Control

Items	Enter Shipping Mode	Exit Shipping Mode	
	Set FET_DIS to 1	INT H to L for 2s	V_{BUS} Plug-In
LDOFET	x	x	On
BATFET(Charging)	Off(t_{SMEN_DGL} later)	On	On(2s later)
BATFET(Discharging)	Off(t_{SMEN_DGL} later)	On	On(2s later)

Notes:

1. Type: x = Don't Care.

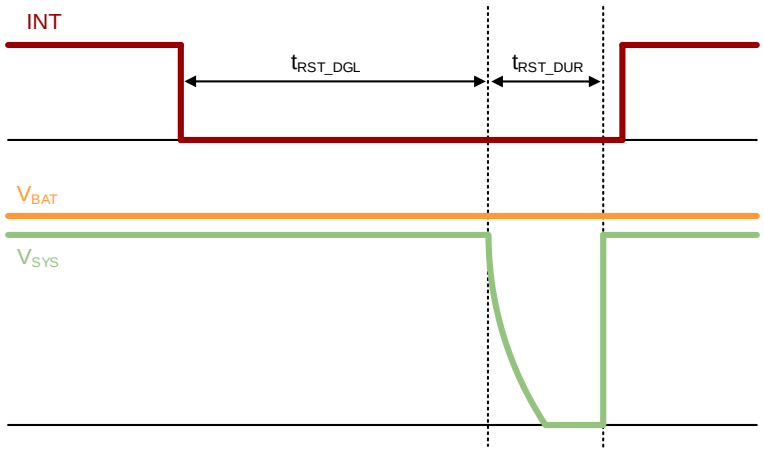
The GD30WS8662x has a register bit for battery disconnection control (FET_DIS). If this bit is set to 1, the GD30WS8662x enters shipping mode after a delay time, which can be programmed by REG04H bit[7:6]. The BATFET turns off, and the FET_DIS bit refreshes to 0 after the BATFET turns off. Pull the INT pin down or plug in the input adapter for 2s to wake the GD30WS8662x up from shipping mode.

The GD30WS8662x can also reuse an INT pin to cut off the path from the battery to the system under the condition needed to reset the system manually. Once the logic at INT is set low for longer than t_{RST_DGL} (which can be programmed by REG00H bit[7:6]), the battery is disconnected from the system by turning off the BATFET. The off state lasts for t_{RST_DUR}, which can be programmed by REG00H bit[5]. Then the BATFET is turned on automatically, and the system is powered by the battery again. During the off period, the INT pin is not limited to be high or low.

When the IC exits shipping mode, only registers that can be reset by the watchdog can be reset.

The GD30WS8662x can reset the system by controlling the INT pin(see Figure 5-8).

Figure 5-8 System Reset Function Operation Profile

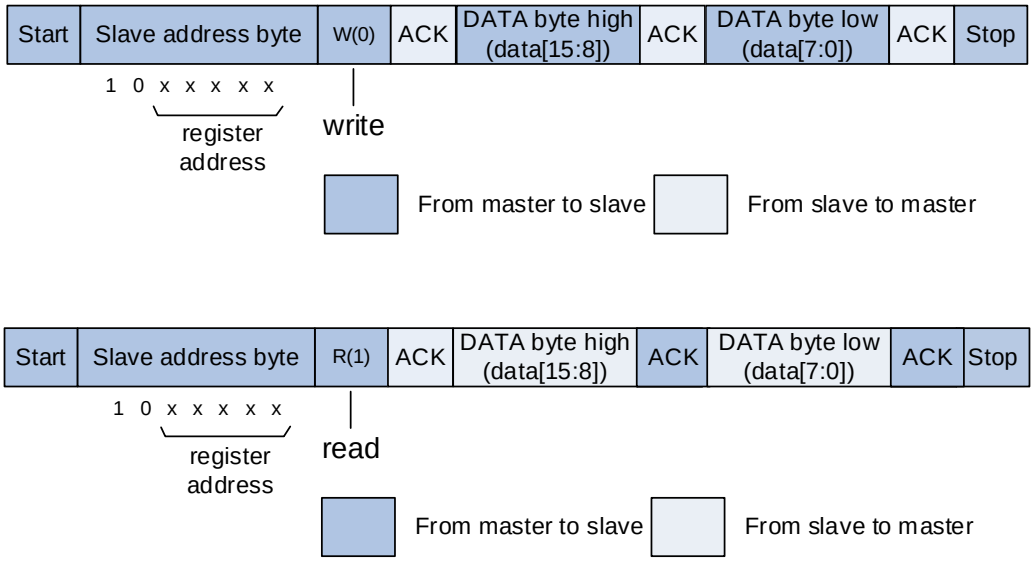


5.13 I²C interface

The I²C (inter-integrated circuit) module provides an I²C interface which is an industry standard two-line serial interface for MCU to communicate with external I²C interface. I²C bus uses two serial lines: a serial data line (SDA), and a serial clock line (SCL).

The I²C interface implements standard I2C protocol with standard-mode (up to 100 kHz) and fast-mode (up to 400 kHz). The I²C interface only supports Slave-mode. The I²C interface receive data on rising SCL and transmit data on falling SCL.

Figure 5-9 Dynamic Power Management and Battery Supplement Operation Profile



The data format is fixed:

8bit function (2'b10 + 5bit(register address), +1bit(1'b0-write, 1'b1-read))

+ 8bit data[15:8]

+ 8bit data[7:0].

5.14 Register map

Table 5-5 GD30WS866x Register Map

Register Name	Address	R/W	Description	Default
REG00H	0x00	r/w	Input source control and Power on configuration register	10011111 10101100
REG01H	0x01	r/w	Charge current control register and Discharge/termination current	00001111 10010001
REG02H	0x02	r/w	Charge voltage control and Charge termination/timer control register	10100011 00111010
REG03H	0x03	r/w	Miscellaneous operation control and System voltage regulation register	11000000 00111001
REG04H	0x04	r/w	System status and Fault register	00100000 00000000

5.14.1 REG00H

Address：0b 00000

Bits	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	VBUS_MIN [3]	1	Y	N	r/w	640mV	Offset: 3.88V Range: 3.88V - 5.08V Default: 4.60V (1001)
14	VBUS_MIN [2]	0	Y	N	r/w	320mV	
13	VBUS_MIN [1]	0	Y	N	r/w	160mV	
12	VBUS_MIN [0]	1	Y	N	r/w	80mV	
11	IBUS_LIM [3]	1	Y	N	r/w	240mA	Offset: 50mA Range: 50mA - 500mA Default: 500mA (1111)
10	IBUS_LIM [2]	1	Y	N	r/w	120mA	
9	IBUS_LIM [1]	1	Y	N	r/w	60mA	
8	IBUS_LIM [0]	1	Y	N	r/w	30mA	
7	tRST_DGL[1]	1	Y	N	r/w	00: 8s 01: 12s	Pull INT low to disconnect the battery. Default: 16s (10)
6	tRST_DGL [0]	0	Y	N	r/w	10: 16s 11: 20s	
5	tRST_DUR	1	Y	Y	r/w	0: 2s 1: 4s	Battery FET is off for a period of time before auto-on Default: 4s (1)
4	EN_HIZ1	0	Y	Y	r/w	0: Disable 1: Enable	Default: Disable (0)
3	CEB	1	Y	Y	r/w	0: Charge enable 1: Charge disabled	Charge configuration Default: charge disabled (1)
2	VBAT_UVLO [2]	1	Y	Y	r/w	440mV	Battery UVLO threshold Offset: 2.6V Range: 2.6V - 3.37V

Bits	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
1	VBAT_UVLO [1]	0	Y	Y	r/w	220mV	Default: 3.04V (100)
0	VBAT_UVLO [0]	0	Y	Y	r/w	110mV	

Notes:

1. This bit only controls the on and off function of the LDOFET(Q1).

5.14.2 REG01H

Address：0b 00001

Bits	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	Register Reset	0	Y	N	r/w	0: Keep current setting 1: Reset	Default: Keep current register setting (0)
14	I2C Watchdog Timer Reset	0	Y	N	r/w	0: Normal 1: Reset	Default: Normal (0)
13	ICC [5]	0	Y	Y	r/w	256mA	Constant charge current setting. Offset: 8mA Range: 8mA (000000) - 456mA (111000) Default: 128mA (001111)
12	ICC [4]	0	Y	Y	r/w	128mA	
11	ICC [3]	1	Y	Y	r/w	64mA	
10	ICC [2]	1	Y	Y	r/w	32mA	
9	ICC [1]	1	Y	Y	r/w	16mA	
8	ICC [0]	1	Y	Y	r/w	8mA	
7	IDSG[3]	1	Y	Y	r/w	1600mA	BAT to SYS discharge current limit. Offset: 200mA Range: 400mA - 3.2A Valid range: 0001 - 1111 Default: 2000mA (1001)
6	IDSG[2]	0	Y	Y	r/w	800mA	
5	IDSG[1]	0	Y	Y	r/w	400mA	
4	IDSG[0]	1	Y	Y	r/w	200mA	
3	ITERM [3]	0	Y	Y	r/w	16mA	Termination current. Offset: 1mA Range: 1mA - 31mA Default: 3mA (0001)
2	ITERM [2]	0	Y	Y	r/w	8mA	
1	ITERM [1]	0	Y	Y	r/w	4mA	
0	ITERM [0]	1	Y	Y	r/w	2mA	

5.14.3 REG02H

Address：0b 00002

Bits	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	VBAT_REG [5]	1	Y	Y	r/w	480mV	Battery regulation voltage. Offset: 3.60V Range: 3.60V - 4.545V Default: 4.2V (101000)
14	VBAT_REG [4]	0	Y	Y	r/w	240mV	
13	VBAT_REG [3]	1	Y	Y	r/w	120mV	
12	VBAT_REG [2]	0	Y	Y	r/w	60mV	
11	VBAT_REG [1]	0	Y	Y	r/w	30mV	
10	VBAT_REG [0]	0	Y	Y	r/w	15mV	
9	VBAT_PRE	1	Y	Y	r/w	0: 2.8V 1: 3.0V	Pre-charge to constant charge threshold. Default: 3.0V (1)
8	VRECH	1	Y	Y	r/w	0: 100mV 1: 200mV	Battery recharge threshold (below V_{BAT_REG}). Default: 200mV (1)
7	EN_WD_ DISCHG	0	Y	N	r/w	0: Disable 1: Enable	Watchdog control in discharge mode. Default: Disable (0)
6	WATCHDOG [1]	0	Y	N	r/w	00: Disable timer 01: 40s 10: 80s 11: 160s	I2C watchdog timer limit. Default: 40s (01) If Bit[6:5] = 00, then watchdog timer is disabled regardless of whether bit[7] is set or not.
5	WATCHDOG [0]	1	Y	N	r/w		
4	EN_TERM	1	Y	Y	r/w	0: Disable 1: Enable	Termination setting (controlling the termination is allowed or not). Default: Enable (1)
3	EN_TIMER	1	Y	Y	r/w	0: Disable 1: Enable	Safety timer setting. Default: Enable timer (1)
2	CHG_TMR [1]	0	Y	Y	r/w	00: 3hrs 01: 5hrs 10: 8hrs 11: 12hrs	Constant charge timer. Default: 5hrs (01)
1	CHG_TMR [0]	1	Y	Y	r/w		
0	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD	RSVD

5.14.4 REG03H

Address：0b 00011

Bits	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	EN_NTC	1	Y	Y	r/w	0: Disable 1: Enable	Default: Enable (1)
14	TMR2X_EN	1	Y	Y	r/w	0: Disable 2X extended safety timer during PPM 1: Enable 2X extended safety timer during PPM	Default: Enable (1)
13	FET_DIS (2)	0	Y	N	r/w	0: Enable 1: Turn off	Default: Enable (0)
12	PG_INT_	0	Y	Y	r/w	0: On	Default: On (0)

Bits	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
	Control					1: Off	
11	EOC_INT_ Control	0	Y	Y	r/w	0: On 1: Off	Charge completed INT mask control Default: On (0)
10	CHG STATUS_INT_ Control	0	Y	Y	r/w	0: On 1: Off	Charging status change INT mask control (charging status contain: not charging, pre charge and charge). Default: On (0)
9	NTC_INT_ Control	0	Y	Y	r/w	0: On 1: Off	Default: On (0)
8	BATOVP_INT_ Control	0	Y	Y	r/w	0: On 1: Off	Default: On (0)
7	EN_PCB_OTP	0	Y	Y	r/w	0: Enable 1: Disable	PCB_OTP enable. Default: Enable (0)
6	EN_VBUSLOOP	0	Y	Y	r/w	0: Enable 1: Disable	Default: Enable (0)
5	TJ_REG [1]	1	Y	Y	r/w	00: 60° C 01: 80° C 10: 100° C 11: 120° C	Thermal regulation threshold. Default: 120° C (11)
4	TJ_REG [0]	1	Y	Y	r/w		
3	VSYS_REG [3]	1	Y	Y	r/w	400mV	System voltage regulation. Offset: 4.2V Range: 4.2V - 4.95V Default: 4.65V (1001)
2	VSYS_REG [2]	0	Y	Y	r/w	200mV	
1	VSYS_REG [1]	0	Y	Y	r/w	100mV	
0	VSYS_REG [0]	1	Y	Y	r/w	50mV	

5.14.5 REG04H

Address：0b 00100

Bits	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
15	WATCHDOG_ FAULT	0	Y	N/A	r	0: Normal 1: Watchdog timer expiration	Normal (0)
14	Rev [1]	0	N/A	N/A	r	00: reserved 01:GD30WS8662x 10: reserved 11: reserved	Revision number. Default: (01)
13	Rev [0]	1	N/A	N/A	r		
12	CHG_STAT [1]	0	N/A	N/A	r	00: Not charging 01: Pre charge 10: Charge 11: Charge done	Not charging (00)
11	CHG_STAT [0]	0	N/A	N/A	r		

Bits	Name	POR	Reset by REG_RST	Reset by WTD	R/W	Description	Comment
10	PPM_STAT	0	N/A	N/A	r	0: No PPM 1: In PPM	No PPM (0)
9	PG_STAT	0	N/A	N/A	r	0: Power fail 1: Power good	No power good (0)
8	THERM_STAT	0	N/A	N/A	r	0: No thermal regulation 1: In thermal regulation	Normal (0)
7	EN_SHIPPING_DGL[1]	0	Y	N	r/w	00: 1s 01: 2s 10: 4s 11: 8s	Enter shipping mode deglitch time Default: 1s (00)
6	EN_SHIPPING_DGL[0]	0	Y	N	r/w		
5	VBUS_FAULT	0	N/A	N/A	r	0: Normal 1: VBUS fault (OVP or bad source)	Normal (0)
4	THEM_SD	0	N/A	N/A	r	0: Normal 1: Thermal shutdown	Normal (0)
3	BAT_FAULT	0	N/A	N/A	r	0: Normal 1: Battery OVP	Normal (0)
2	STMR_FAULT	0	N/A	N/A	r	0: Normal 1: Safety timer expiration	Normal (0)
1	NTC_FAULT[1]	0	N/A	N/A	r	0: Normal 1: NTC hot	Normal (0)
0	NTC_FAULT[0]	0	N/A	N/A	r	0: Normal 1: NTC cold	Normal (0)

6 Electrical characteristics

6.1 Absolute maximum ratings

The maximum ratings are the limits to which the device can be subjected without permanently damaging the device. Note that the device is not guaranteed to operate properly at the maximum ratings. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

Table 6-1 Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit
V_{BUS}	Power supply pin from BUS other 5V input	-0.3	7	V
V_{BUS}	Power supply pin from BUS other 5V input, pulsed less than 20us	—	32	V
V_{BAT}	Battery voltage	-0.3	7	V
V_{SYS}	System Voltage	-0.3	7	V
V_{CC}	LDO output voltage and Internal logic voltage (VCC, NTC, INT, SCL, SDA)	-0.3	7	V
T_J	Operating junction temperature,	–40	150	°C
T_{stg}	Storage temperature,	–65	150	°C

6.2 Recommended operation conditions

Table 6-2 Recommended Operation Conditions

Symbol	Parameter	Min	Max	Unit
V_{BUS}	Power supply pin from BUS other 5V input	4.35	5.5	V
V_{BAT}	Battery voltage	—	4.65	V
V_{SYS}	System Voltage	4.2	5	V
V_{CC}	LDO output voltage and Internal logic voltage (VCC, NTC, INT, SCL, SDA)	3.15	—	V
T_J	Operating Junction temperature	–40	+125	°C

Notes:

1. When the GD30WS8662x is in shipping mode, the maximum VCC is max(V_{BUS}, V_{BAT}), and the maximum VCC is 3.45V in other modes.

6.3 Electrical sensitivity

The device is strained in order to determine its performance in terms of electrical sensitivity. Electrostatic discharges (ESD) are applied directly to the pins of the sample. Static latch-up (LU) test is based on the two measurement methods.

Table 6-3 Electrostatic Discharge and Latch-up

Symbol	Parameter	Conditions	Value	Unit
$V_{ESD(HBM)}$	human body model	T_A = 25 °C; JS-001-2017	±2000	V
$V_{ESD(CDM)}$	charge device model	T_A = 25 °C; JS-002-2018	±1000	V
Latch up	I-test	T_A = 25 °C; JESD78E	±200	mA

6.4 Power supplies voltage and current

All parameters are tested at T_A = –40°C to +125°C, V_{BUS} = 5V or V_{BAT} = 5V (unless otherwise noted)

Table 6-4 Power Supplies Voltages and Currents

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{BAT_Q}	Battery quiescent current	VBUS = 5V, CEB = 0, ISYS = 0A, charge done, VBAT = 4.35V	—	15	—	uA
		VBUS = GND, CEB = 1, ISYS = 0A, VBAT = 4.35V, disable PCB_OTP function, not including the current from the external NTC resistor	—	6.5	8.5	μA
		VBUS = GND, CEB = 1, ISYS = 0A, VBAT = 4.35V, enable PCB_OTP function, not including the current from the external NTC resistor	—	14.5	22	uA
$I_{shipping}$	Current in shipping mode	VBAT = 4.5V, VBUS = VSYS = GND, FET_DIS = 1, shipping mode	—	—	200	nA
V_{CC}	VCC regulator voltage	I_{Vcc} = 0 to 50 mA	3.15	3.3	3.45	V

6.5 Logic input characteristics

All parameters are tested at T_A = –40°C to +125°C, V_{BUS} = 4.5 to 5.5 V (unless otherwise noted)

Table 6-5 Logic Input Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	Input logic low voltage	—	0	—	0.8	V
V_{IH}	Input logic high voltage	—	1.5	—	5.5	V
V_{HYS}	Input logic hysteresis	—	100	—	—	mV

6.6 Open drain outputs characteristics

Open drain output pins include INT, SDA.

All parameters are tested at T_A = –40°C to +125°C, V_{BUS} = 4.5 to 5.5 V (unless otherwise noted)

Table 6-6 Open Drain Output Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INT}	Output logic low voltage	I_O = 5 mA	—	—	0.1	V
V_{SDA}	Output logic low voltage	I_O = 5 mA	—	—	0.1	V
I_{OD}	Output high impedance leakage	V_O = 5 V	–2	—	2	μA

6.7 Input source and battery protection

All parameters are tested at V_{BUS} = 5.0V, V_{BAT} = 3.5V, T_A = +25° C (unless otherwise noted)

Table 6-7 Input Source and Battery Protection

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BUS_UVLO}	VBUS under-voltage lockout threshold	VBUS falling	3.62	3.73	3.82	V
	VBUS under-voltage lockout threshold hysteresis	VBUS rising	—	170	—	mV
V_{BUS_OVP}	VBUS over-voltage protection threshold	VBUS rising threshold	5.85	6	6.15	V
	VBUS over-voltage protection threshold hysteresis	—	—	340	—	mV
V_{HDRM}	VBUS vs. battery voltage headroom threshold	VBUS rising vs. battery	80	130	170	mV
	VBUS vs. battery voltage headroom threshold hysteresis	—	—	65	—	mV
V_{BAT_UVLO}	Battery under-voltage lockout threshold	VBAT voltage rising, REG01[2:0] =000	2.5	2.6	2.7	V
		VBAT voltage rising, REG01[2:0] =100	2.94	3.04	3.14	V
		VBAT voltage rising, REG01[2:0] =111	3.27	3.37	3.47	V
	Battery under-voltage threshold hysteresis	VBAT_UVLO = 2.46V	—	140	—	mV
V_{BAT_OVP}	Battery over-voltage protection threshold	Rising, higher than VBAT_REG	—	130	—	mV
	Battery over-voltage protection hysteresis	—	—	65	—	mV

6.8 Power path management

All parameters are tested at V_{BUS} = 5.0V, V_{BAT} = 3.5V, T_A = +25° C (unless otherwise noted)

Table 6-8 Power Path Management

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{SYS\_REG\_ACC}$	Regulated system output voltage accuracy	VBUS = 5.5V, RSYS = 100Ω, ICHG = 0A, REG03[3:0] = 0000, VSYS_REG = 4.2V	-2	—	2	%
		VBUS = 5.5V, RSYS = 100Ω, ICHG = 0A, REG03[3:0] = 1001, VSYS_REG = 4.65V	-2	—	2	%
		VBUS = 5.5V, RSYS = 100Ω, ICHG = 0A, REG03[3:0] = 1111, VSYS_REG = 4.95V	-2	—	2	%
I_{BUS_LIM}	VBUS current limit	REG00[11:8] = 0000, IBUS_LIM = 50mA	40	50	60	mA
		REG00[11:8] = 0011, IBUS_LIM = 140mA	125	140	155	
		REG00[11:8] = 1001, IBUS_LIM = 320mA	295	320	345	
		REG00[11:8] = 1111, IBUS_LIM = 500mA	455	500	545	
V_{BUS_MIN}	VBUS minimum voltage regulation	REG00[15:12] = 0000, VBUS_MIN = 3.88V	3.68	3.88	4.18	V
		REG00[15:12] = 1001, VBUS_MIN = 4.60V	4.40	4.60	4.75	
		REG00[15:12] = 1111, VBUS_MIN = 5.08V	4.88	5.08	5.35	
R_{ON_Q1}	BUS to SYS switch on resistance	VBUS = 4.5V, ISYS = 100mA	—	290	—	mΩ
I_{BUS_Q}	VBUS quiescent current	VBUS = 5.5V, EN_HIZ = 0, CEB = 0, charge enable, ICHG = 0A, ISYS = 0A	—	2.1	—	mA
		VBUS = 5.5V, EN_HIZ = 0, CEB = 1, charge disabled	—	1.9	—	
I_{BAT_Q}	Battery quiescent current	VBUS = 5V, CEB = 0, ISYS = 0A, charge done, VBAT = 4.35V	—	15	—	uA
		VBUS = GND, CEB = 1, ISYS = 0A, VBAT = 4.35V, disable PCB_OTP	—	6.5	8.5	

		function, not including the current from the external NTC resistor				
		VBUS = GND, CEB = 1, ISYS = 0A, VBAT = 4.35V, enable PCB_OTP function, not including the current from the external NTC resistor	—	14.5	22	
		VBAT = 4.5V, VBUS = VSYS = GND, FET_DIS = 1, shipping mode	—	—	200	nA
R_{ON_Q2}	B-FET on resistance	VBUS < 2V, VBAT = 3.5V, ISYS = 100mA	—	100	—	mΩ
I_{DSG}	B-FET discharge current limit	REG01[7:4] = 0001, IDSG = 400mA	—	400	—	mA
		REG01[7:4] = 1001, IDSG = 2000mA	—	2000	—	mA
V_{FWD}	Ideal diode forward voltage in supplement mode	50mA discharge current	—	23	—	mV

6.9 Shipping mode

All parameters are tested at V_{BUS} = 5.0V, V_{BAT} = 3.5V, T_A = +25° C (unless otherwise noted)

Table 6-9 Shipping Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{SMEN_DGL}	Enter shipping mode deglitch time	REG03[13] is set from 0 to 1, REG04[7:6] = 00	—	1	—	s
t_{SMEX_DGL}	Exit shipping mode by INT or BUS plug-in	INT is pulled low	—	2	—	s

6.10 Auto-reset mode

All parameters are tested at V_{BUS} = 5.0V, V_{BAT} = 3.5V, T_A = +25° C (unless otherwise noted)

Table 6-10 Auto-Reset Mode

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{RST_DGL}	Reset by INT	REG00H[7:6] = 00	—	8	—	s
	—	REG00H[7:6] = 10	—	16	—	
t_{RST_DUR}	BFET off lasting time	REG00H[5] = 0	—	2	—	s
	—	REG00H[5] = 1	—	4	—	

6.11 Battery charger

All parameters are tested at V_{BUS} = 5.0V, V_{BAT} = 3.5V, T_A = +25° C (unless otherwise noted)

Table 6-11 Battery Charger

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT_REG}	Battery charge voltage regulation	REG02[15:10] = 000000, V_{BAT_REG} = 3.6V	3.582	3.6	3.618	V
		REG02[15:10] = 101000, V_{BAT_REG} = 4.2V	4.188	4.2	4.212	
		REG02[15:10] = 110010, V_{BAT_REG} = 4.38V	4.358	4.38	4.44	
		REG02[15:10]= 111110, V_{BAT_REG} = 4.53V	4.522	4.53	4.568	
I_{CC}	Constant current	REG01[13:8] = 001111, I_{CC} = 128mA	113	128	137	mA
		REG01[13:8] = 111000, I_{CC} = 456mA	424	456	488	
T_{J_REG}	Junction temperature regulation(1)	Thermal_Limit = 120°C	—	120	—	°C
I_{PRE}	Pre-charge current	—	—	20% *I_{CC}	—	
I_{TERM}	Charge termination current threshold	REG01[3:0] = 0000, I_{TERM} = 1mA	—	0.95	—	mA
		REG01[3:0] = 0001, I_{TERM} = 3mA	—	3.05	—	
		REG01[3:0] = 0101, I_{TERM} = 11mA	—	11	—	
		REG01[3:0] = 0101, I_{TERM} = 31mA	—	31	—	
V_{BAT_PRE}	Pre-charge to constant current charge threshold	V_{BAT} rising, REG02[9] = 1, V_{BAT_PRE} = 3.0V	2.9	3	3.1	V
	Pre-charge to constant current charge threshold hysteresis	—	—	320	—	mV
V_{RECH}	Battery auto-recharge voltage threshold	Below VBAT_REG, REG02[8] = 0	55	100	145	mV
		Below VBAT_REG, REG02[8] = 1	155	200	245	

6.12 Thermal protection

All parameters are tested at V_{BUS} = 5.0V, V_{BAT} = 3.5V, T_A = +25° C (unless otherwise noted)

Table 6-12 Thermal Protection

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{J_SHDN}	Thermal shutdown threshold (1)	—	—	150	—	°C
	Thermal shutdown hysteresis (1)	—	—	20	—	°C
I_{NTC}	NTC output current	CEB = 0, NTC = 3V	-1	0	1	uA
V_{COLD}	NTC cold temp rising threshold	As a percentage of VCC	63	65	67	%
	NTC cold temp rising	—	—	60	—	mV

	threshold hysteresis					
V_{HOT}	NTC hot temp falling threshold	As a percentage of VCC	31	33	35	%
	NTC hot temp falling threshold hysteresis	—	—	70	—	mV
V_{HOT_PCB}	NTC hot temp falling threshold for PCB_OTP	As a percentage of VCC	30	32	35	%
	NTC hot temp falling threshold hysteresis for PCB_OTP	—	—	90	—	mV

6.13 Watchdog timer

All parameters are tested at V_{BUS} = 5.0V, V_{BAT} = 3.5V, T_A = +25° C (unless otherwise noted)

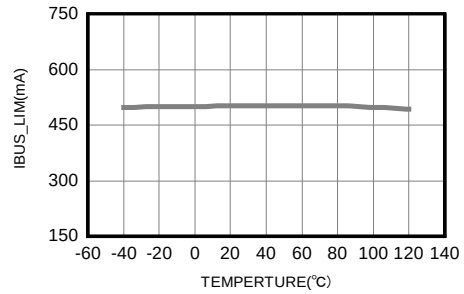
Table 6-13 Watchdog Timer

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{WDT}	Watchdog timer	REG0[6:5] = 11	—	160	—	s

Notes:

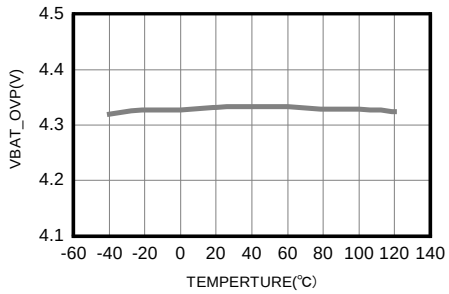
1. Guaranteed by design.

6.14 Typical Characteristics



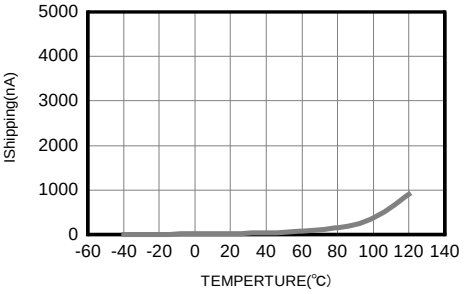
V_{BUS}=5.2V I_{BUS_MIN}=500mA

Figure 1. Bus Current Limit



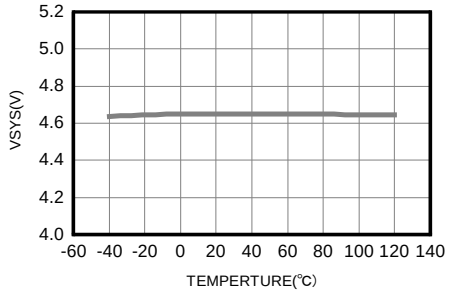
V_{BUS}=5.2V V_{BAT_REG}=4.2V

Figure 2. Battery OVP Voltage



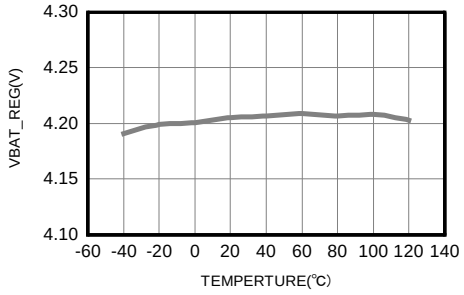
V_{BUS}=0V V_{SYS}=0V V_{BAT}=4.5V

Figure 3. Battery Current under Shipping Mode



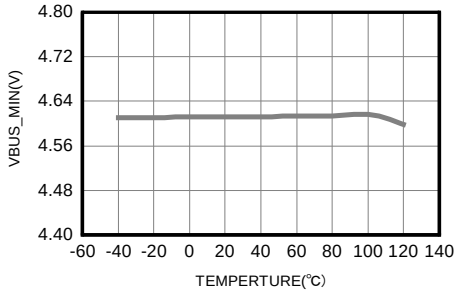
V_{BUS}=5.2V V_{BAT}=0V V_{SYS_REG}=4.65V

Figure 4. System Regulation Volatge



V_{BUS}=5.2V V_{BAT_REG}=4.2V

Figure 5. Battery Regulation Voltage



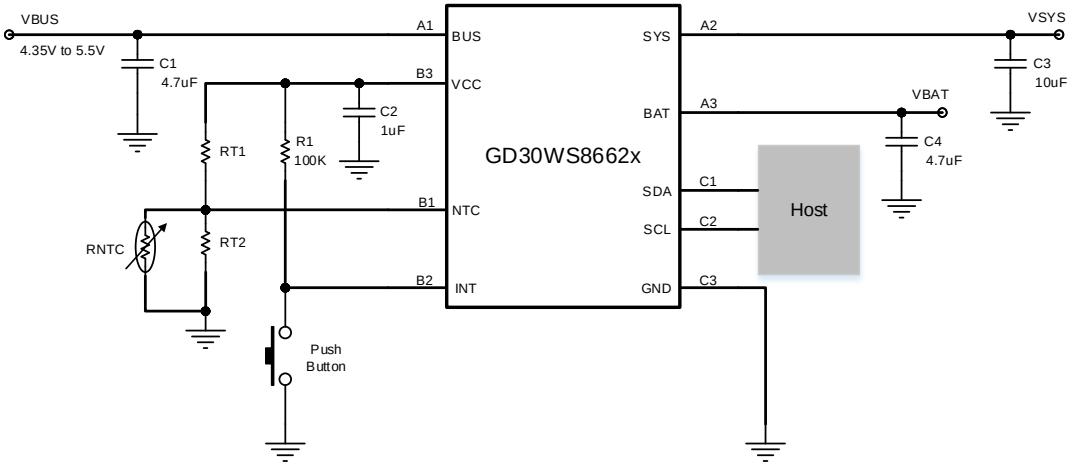
V_{BUS}=5.2V V_{BAT}=0V V_{BUS_MIN}=4.6V

Figure 6. Bus Minimum Voltage

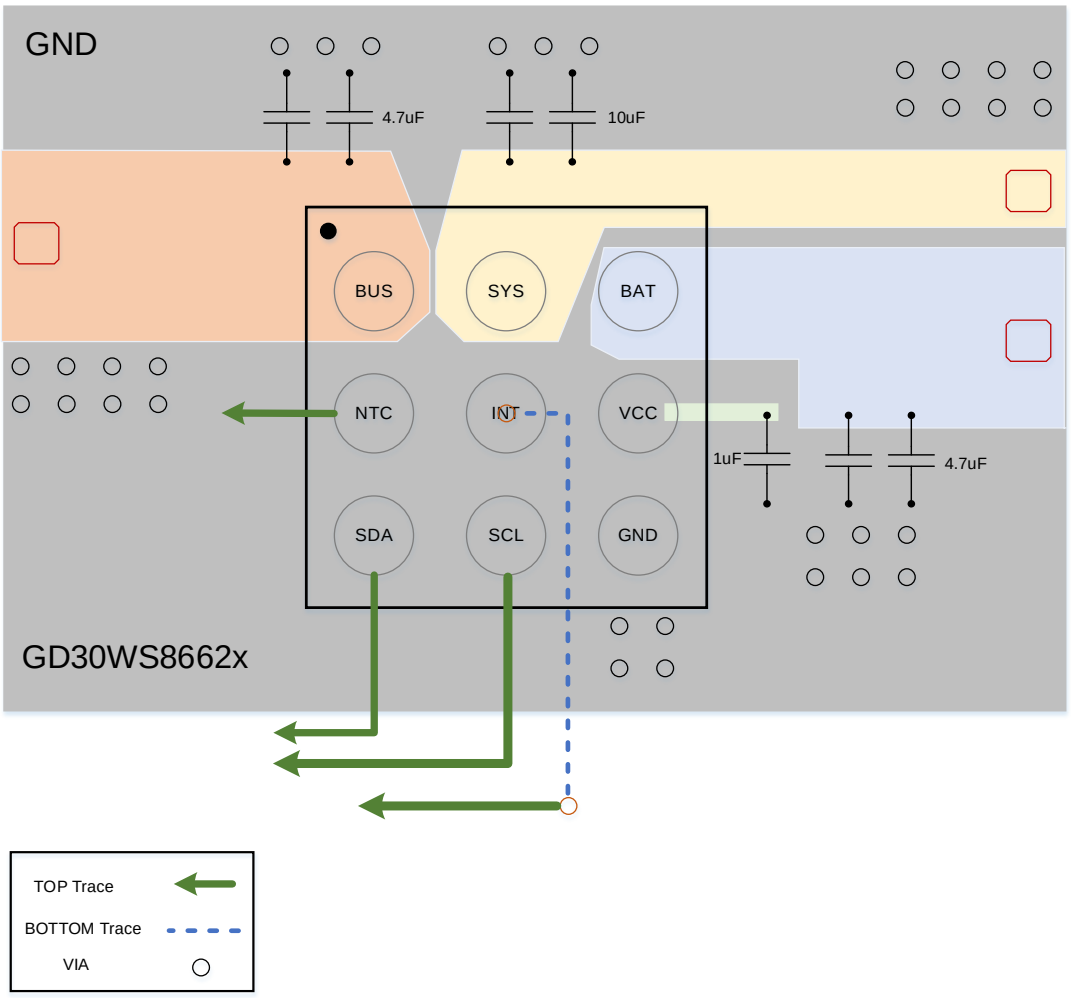
7 Typical application circuit

Figure 7-1 Typical GD30WS8662x Application Circuit

In this application, the GD30WS8662x is used to single-cell battery charging for wireless wearables.



8 Layout guideline



Notes:

1) Place the bypass capacitors as close to the IC as possible to ensure the smallest input inductance and ground impedance.
2) Place the PCB trace connecting the capacitor between VCC and GND very close to the IC.
3) Place the I^2C wire in parallel.
4) Place via in the INT pin and route from the bottom layer.

9 Package information

9.1 WLCSP-9 package outline and dimensions

Figure 9-1 WLCSP-9 Package Outline

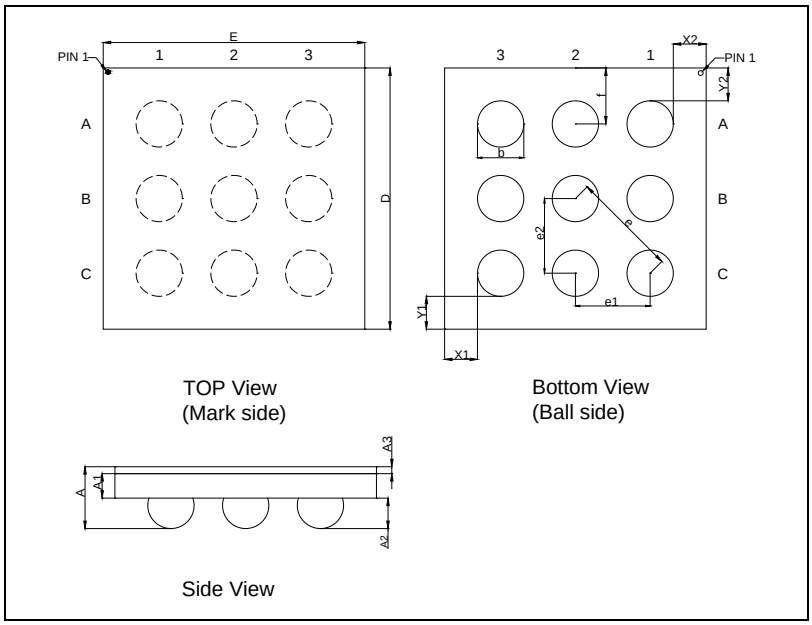
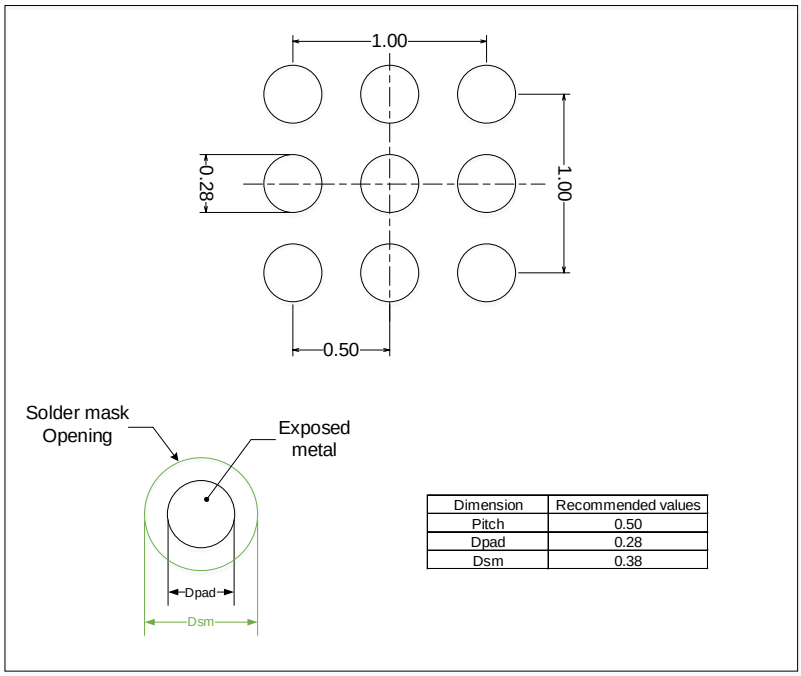


Table 9-1 WLCSP-9 Dimensions (in mm)

Symbol	Min	Typ	Max
A	0.55	0.6	0.65
A1	0.295	0.325	0.355
A2	0.23	0.25	0.27
A3	—	0.025	—
b	0.28	0.31	0.34
D	1.73	1.75	1.77
E	1.73	1.75	1.77
e	—	0.707	—
e1	—	0.5	—
e2	—	0.5	—
f	—	0.375	—
X1	—	0.22	—
X2	—	0.22	—
Y1	—	0.22	—
Y2	—	0.22	—

(Original dimensions are in millimeters)

Figure 9-2 WLCSP-9 recommended footprint



Dimension	Recommended values
Pitch	0.50
Dpad	0.28
Dsm	0.38

(All dimensions are in millimeters)

9.2 Thermal characteristics

Thermal resistance is used to characterize the thermal performance of the package device, which is represented by the Greek letter "Θ". For semiconductor devices, thermal resistance represents the steady-state temperature rise of the chip junction due to the heat dissipated on the chip surface.

Θ_{JA}: Thermal resistance, junction-to-ambient.

Θ_{JB}: Thermal resistance, junction-to-board.

Θ_{JC}: Thermal resistance, junction-to-case.

Ψ_{JB}: Thermal characterization parameter, junction-to-board.

Ψ_{JT}: Thermal characterization parameter, junction-to-top center.

$\Theta_{JA} = (T_J - T_A)/P_D$

$\Theta_{JB} = (T_J - T_B)/P_D$

$\Theta_{JC} = (T_J - T_C)/P_D$

Where, T_J = Junction temperature.

T_A = Ambient temperature

T_B = Board temperature

T_C = Case temperature which is monitoring on package surface

P_D = Total power dissipation

Θ_{JA} represents the resistance of the heat flows from the heating junction to ambient air. It is an indicator of package heat dissipation capability. Lower Θ_{JA} can be considerate as better overall thermal performance. Θ_{JA} is generally used to estimate junction temperature.

Θ_{JB} is used to measure the heat flow resistance between the chip surface and the PCB board.

Θ_{JC} represents the thermal resistance between the chip surface and the package top case. Θ_{JC} is mainly used to estimate the heat dissipation of the system (using heat sink or other heat dissipation methods outside the device package).

Table 9-2 Package Thermal Characteristics(1)

Symbol	Condition	Package	Value	Unit
Θ_{JA}	Natural convection, 2S2P PCB	WLCSP9	69.16	°C/W
Θ_{JB}	Cold plate, 2S2P PCB	WLCSP9	15.25	°C/W
Θ_{JC}	Cold plate, 2S2P PCB	WLCSP9	13.16	°C/W
Ψ_{JB}	Natural convection, 2S2P PCB	WLCSP9	RSVD	°C/W
Ψ_{JT}	Natural convection, 2S2P PCB	WLCSP9	RSVD	°C/W

(1) Thermal characteristics are based on simulation, and meet JEDEC specification.

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10 Ordering information

Table 10-1 Part order code for GD30WS8662x

Ordering Code	Package	Package Type	Packing Type	MOQ	Temperature Operating Range
GD30WS8662DYTR	WLCSP-9 (1.75X1.75)	Green	Tape&Reel	3000	Industrial -40°C to +125°C

11 Revision history

Table 11-1 Revision history

Revision No.	Description	Date
1.0	Initial	Mar.30, 2022
1.1	1.Section *4.1* Part Order Code is modified to Part Number. 2.The Package description in section *4.1* is modified to WLCSP-9(1.75X1.75). 3.Chapter *10 Ordering information* added information on Packing Type(Tape&Reel) and MOQ(3000).	Jun.08, 2022