GD9Fx1GxF2A

DATASHEET

1G-bit 2K+128BPageSize

Contents

1. FEATURES

◆Single level cell technology

◆ONFI 1.0 Compatible

◆Power Supply Voltage
- VCC = 1.7 ~ 1.95v(GD9FS)
- VCC = 2.7 ~ 3.6v (GD9FU)

◆Memory Cell Organization
- Page size:
  X8: 2K + 128bytes
  X16: 1K + 64words
- Block size:
  X8: 128K + 8K bytes
  X16: 64K + 4K words
- Plane size: 1024 blocks
- Device size: 1024 blocks

◆Page Read / Program time
- Random Read Time (tR): 25us Max.
- Sequential Access Time
  3.3v Device: 25ns Min.
  1.8v Device:45ns Min.
- Page Program(tPROG): 300us Typ.

◆Block Erase time
- Block Erase Time(tBERS): 3ms Typ.

◆Number of Valid Blocks
- Min 1004 blocks
- Max 1024 blocks

◆Operating Current
- Read(25ns cycle): 15mA
- Program(Typ): 15mA
- Erase(Typ): 15mA
- Standby(Max):50uA (CMOS)

◆Reliability
- P/E cycles with ECC: 100K
- Data retention: 10 Years

◆ECC Requirement
- 4bit/512 bytes

◆Operating Temperature
- Industrial: -40C ~ 85C
- Industrial: -40C ~ 105C

◆Chip Enable Don’t Care Option

◆Security
- OTP area
- Non-volatile protection

◆Package
- TSOPI 48 (12mm x 20mm)
- FBGA63 (9mm x 11mm)
- FBGA48 (6mm x 8mm)

2. GENERAL DESCRIPTION

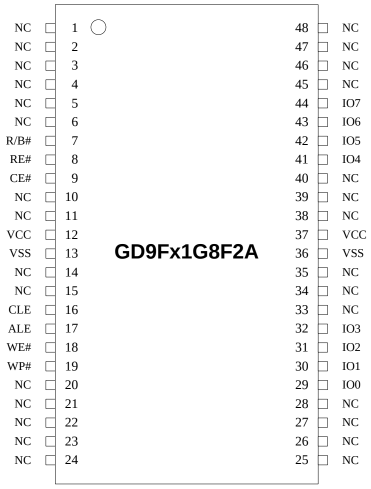
GigaDevice GD9Fx1G8F2A and GD9Fx1G6F2A are 1Gbit with spare 64Mbit capacity. A program operation can be performed in typical tPROG on the 2176-byte page and an erase operation can be performed in typical tBERS on a 128K+8K-bytes block. Data in the data page can be read out at tRC cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. GD9Fx1G8F2A and GD9Fx1G6F2A's provide extended reliability of 100K program/erase cycles with ECC (Error Correcting Code).

2.1 Product List

PART NUMBER	ORGANIZATION	VCC RANGE	PACKAGE	Temperature
GD9FU1G8F2AMG	128M x 8bit	2.7v ~ 3.6v	TSOP(I)-48	Industrial -40~85/-40~105
GD9FU1G6F2AMG	64M x 16bit	2.7v ~ 3.6v	TSOP(I)-48	Industrial -40~85/-40~105
GD9FU1G8F2ALG	128M x 8bit	2.7v ~ 3.6v	FBGA-63	Industrial -40~85/-40~105
GD9FU1G6F2ALG	64M x 16bit	2.7v ~ 3.6v	FBGA-63	Industrial -40~85/-40~105
GD9FU1G8F2ADG	128M x 8bit	2.7v ~ 3.6v	FBGA-48	Industrial -40~85/-40~105
GD9FU1G6F2ADG	64M x 16bit	2.7v ~ 3.6v	FBGA-48	Industrial -40~85/-40~105
GD9FS1G8F2AMG	128M x 8bit	1.7v ~ 1.95v	TSOP(I)-48	Industrial -40~85/-40~105
GD9FS1G6F2AMG	64M x 16bit	1.7v ~ 1.95v	TSOP(I)-48	Industrial -40~85/-40~105
GD9FS1G8F2ALG	128M x 8bit	1.7v ~ 1.95v	FBGA-63	Industrial -40~85/-40~105
GD9FS1G6F2ALG	64M x 16bit	1.7v ~ 1.95v	FBGA-63	Industrial -40~85/-40~105
GD9FS1G8F2ADG	128M x 8bit	1.7v ~ 1.95v	FBGA-48	Industrial -40~85/-40~105
GD9FS1G6F2ADG	64M x 16bit	1.7v ~ 1.95v	FBGA-48	Industrial -40~85/-40~105

3. PACKAGE

3.1 TSOPI-48



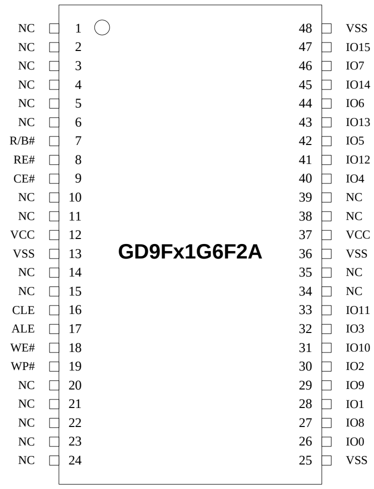


Figure 1-a: GD9Fx1G8F2AMG package figures **Figure 1-b: GD9Fx1G6F2AMG package figures**

3.2 FBGA-63

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			WP#	ALE	VSS	CE#	WE#	R/B#		
D			NC	RE#	CLE	NC	NC	NC		
E			NC	NC	NC	NC	NC	NC		
F			NC	NC	NC	NC	NC	NC		
G			NC	VCC(1)	NC	IO13	IO15	NC		
H			IO8	IO0	IO10	IO12	IO14	VCC		
J			IO9	IO1	IO11	VCC	IO5	IO7		
K			VSS	IO2	IO3	IO4	IO6	VSS		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

GD9Fx1G6F2A

	1	2	3	4	5	6	7	8	9	10
A	NC	NC							NC	NC
B	NC								NC	NC
C			WP#	ALE	VSS	CE#	WE#	R/B#		
D			NC	RE#	CLE	NC	NC	NC		
E			NC	NC	NC	NC	NC	NC		
F			NC	NC	NC	NC	NC	NC		
G			NC	VCC(1)	NC	NC	NC	NC		
H			NC	IO0	NC	NC	NC	VCC		
J			NC	IO1	NC	VCC	IO5	IO7		
K			VSS	IO2	IO3	IO4	IO6	VSS		
L	NC	NC							NC	NC
M	NC	NC							NC	NC

GD9Fx1G8F2A

Figure 2_a: 63-FBGA x16 device ball location figures **Figure 2_b: 63-FBGA x8 device ball location figures**

Note:

1. Ball G4 can be either connected to VCC or NC.

3.3 FBGA-48

	1	2	3	4	5	6
A	WP#	ALE	VSS	CE#	WE#	R/B#
B	NC	RE#	CLE	NC	NC	NC
C	NC	NC	NC	NC	NC	NC
D	NC	NC	NC	NC	NC	NC
E	NC	NC	NC	IO13	IO15	NC
F	IO8	IO0	IO10	IO12	IO14	VCC
G	IO9	IO1	IO11	VCC	IO5	IO7
H	VSS	IO2	IO3	IO4	IO6	VSS

Figure 3_a: 48-FBGA x16 device ball location figures

	1	2	3	4	5	6
A	WP#	ALE	VSS	CE#	WE#	R/B#
B	NC	RE#	CLE	NC	NC	NC
C	NC	NC	NC	NC	NC	NC
D	NC	NC	NC	NC	NC	NC
E	NC	NC	NC	NC	NC	NC
F	NC	IO0	NC	NC	NC	VCC
G	NC	IO1	NC	VCC	IO5	IO7
H	VSS	IO2	IO3	IO4	IO6	VSS

Figure 3_b: 48-FBGA x8 device ball location figures

4. BLOCK DIAGRAM

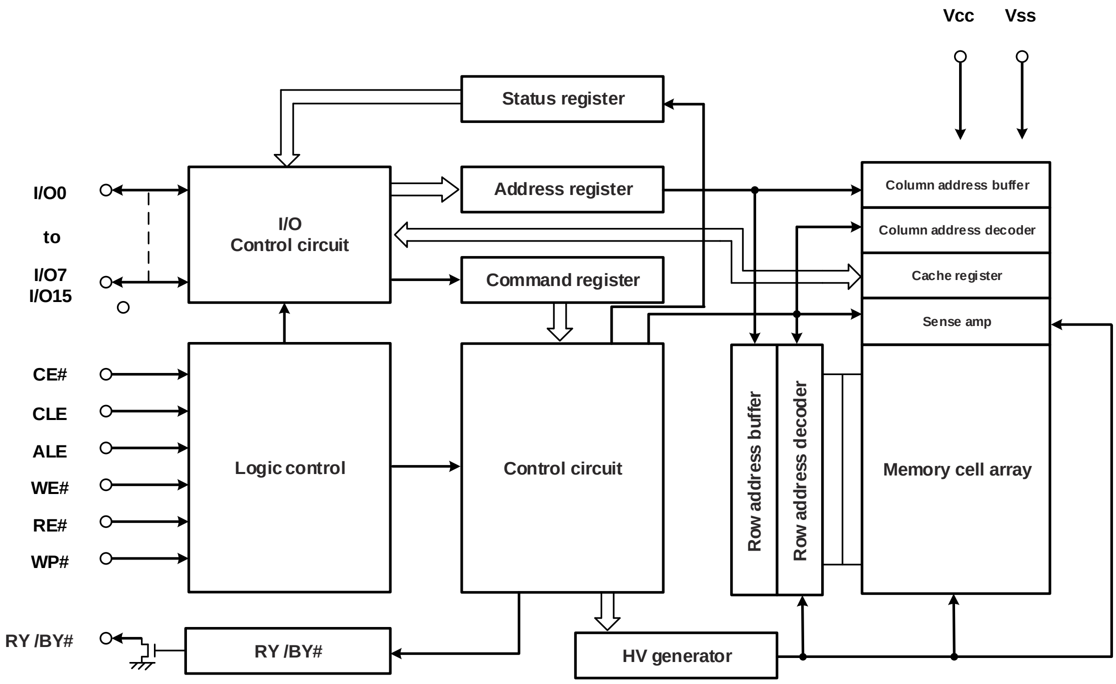


Figure 4: Block Diagram figures

4.1 PIN DESCRIPTION

Signal Name	Input/ Output	Description
R/B#	**O**	Ready/Busy: Open drain output to indicate the target status, low to indicate that one or more operations are in progress.
RE#	**I**	Read Enable: Enables serial data output, active low.
CE#	**I**	Chip Enable: When high and the target is in the ready state, the target goes into a low-power standby state. When low, the target is selected.
CLE	**I**	Command Latch Enable: Enable signal to load a command into the target on the rising edge of WE#, active high.
ALE	**I**	Address Latch Enable: Enable signal to load an address into the target on the rising edge of WE#, active high.
WE#	**I**	Write Enable: Data, Commands, and Addresses are latched on the rising edge of WE#.
WP#	**I**	Write Protect: Low to disable Flash array program and erase operations.
IO0 ~ IO7	**I/O**	I/O Port, bits 0-7: 8-bit wide bidirectional port for transferring address, command, and data to and from the device.
IO8 ~ IO15	**I/O**	I/O Port, bits 8-15: Upper 8 bits for the 16-bit wide bidirectional port used to transfer data to and from the device.
VCC	**I**	Power: Power supply to the device.
VSS	**I**	Ground: Power supply ground.
NC	**-**	No Connection: Lead is not internally connected.

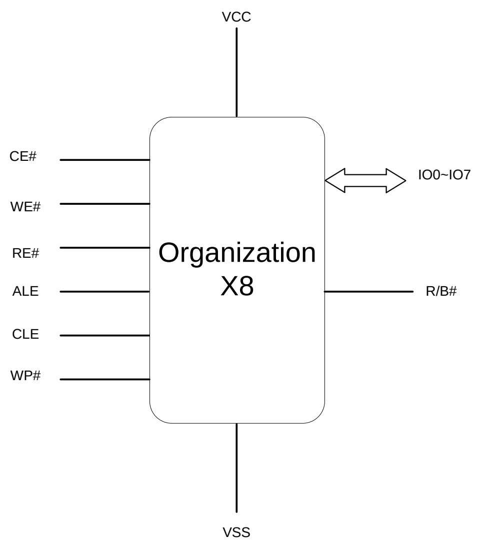


Figure 5_a: GD9Fx1G8F2A figures

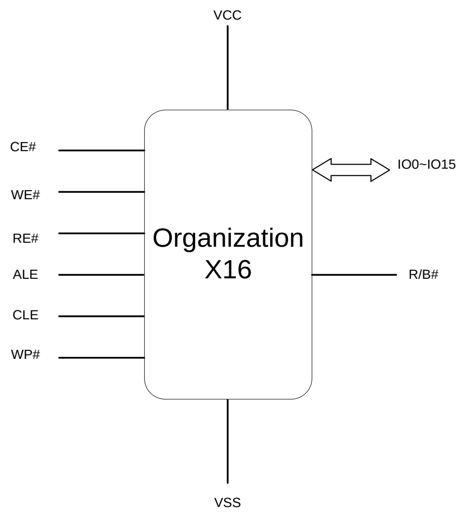


Figure 5_b: GD9Fx1G6F2A figures

5. ARRAY ORGANIZATION

Each device has	Each block has	Each page has	
1G			
128M+8M	128K+8K	2K+128	bytes
1024 x 64	64	-	pages
1024	-	-	blocks

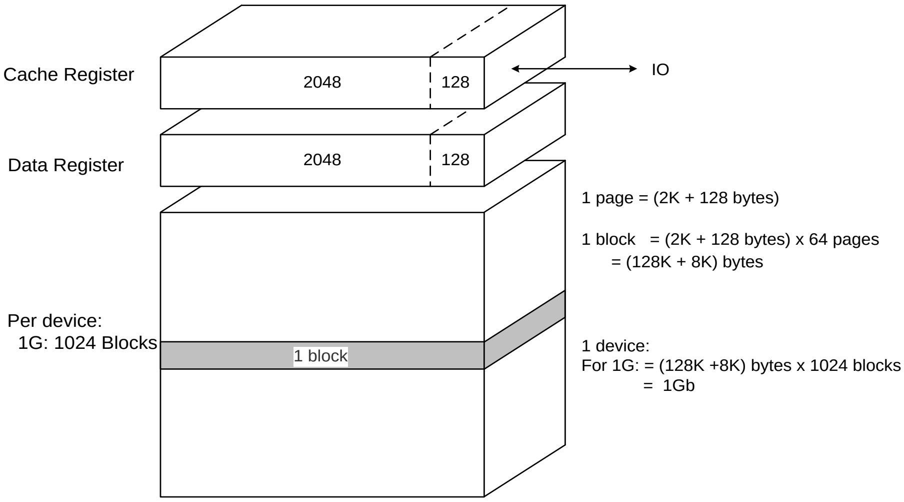


Figure 6: Array Organization figures

5.1 Addressing (X8)

Bus Cycle	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	A11	L	L	L	L
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27

A0-A11: column address in the page
A12-A17: page address in the block
A18-A27: block address

5.2 Addressing (X16)

Bus Cycle	IO0	IO1	IO2	IO3	IO4	IO5	IO6	IO7
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7
2nd Cycle	A8	A9	A10	L	L	L	L	L
3rd Cycle	A11	A12	A13	A14	A15	A16	A17	A18
4th Cycle	A19	A20	A21	A22	A23	A24	A25	A26

A0-A10: column address in the page
A11-A16: page address in the block
A17-A26: block address

5.3 Factory Defect Mapping

The Flash array is not presumed to be pristine, and a number of defects that makes the blocks unusable may be present. Invalid blocks shall be sorted out from normal blocks by software.

5.3.1. Device Requirements

If a block is defective, the manufacturer shall mark the block as defective by setting the Defective Block Marking, as shown in Figure of "Area marked in first or last page of block indicating defect", of the last page of the defective block to a value of non-FFh. The Defective Block Marking is located on the first byte of user data area or the first byte of spare data area in the pages within a block.

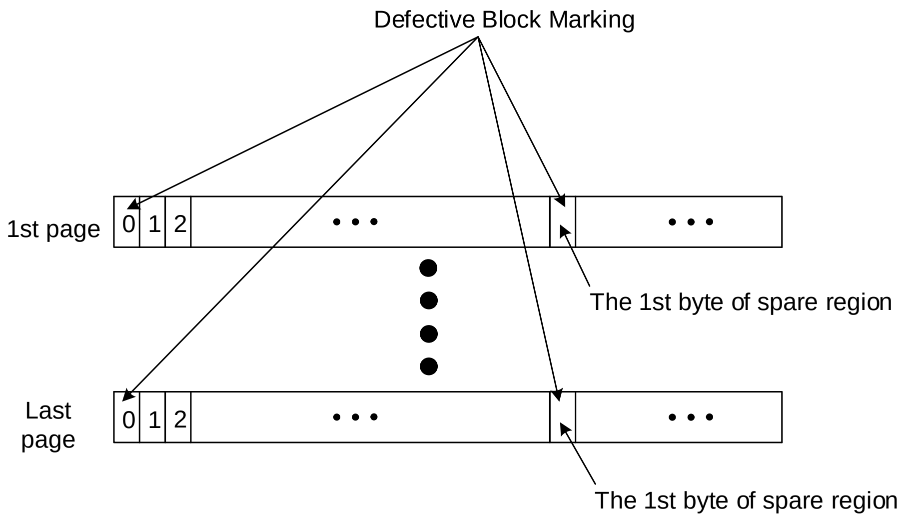


Figure 7. Area marked in first or last page of block indicating defect sequential figures

5.3.2. Host Requirements

The host shall not erase or program blocks marked as defective by the manufacturer, and any attempt to do so yields indeterminate results.

Figure of “Flow chart to create initial invalid block table” outlines the flow chart how to create an initial invalid block table. It should be performed by the host to create the initial bad block table prior to performing any erase or programming operations on the target. The 1st byte of both main and spare region in non-defective blocks are read FFh with ECC enabled on the controller. A defective block is indicated by the majority of bits being read non-FFh in the Defective Block Marking location of either the first page or last page of the block. The host shall check the Defective Block Marking location of both the first and last past page of each block to verify the block is valid prior to any erase or program operations on that block.

NOTE: Over the lifetime use of a NAND device, the Defective Block Marking of defective blocks may encounter read disturbs that cause bit changes. The initial defect marks by the manufacturer may change value over the lifetime of the device, and are expected to be read by the host and used to create a bad block table during initial use of the part.

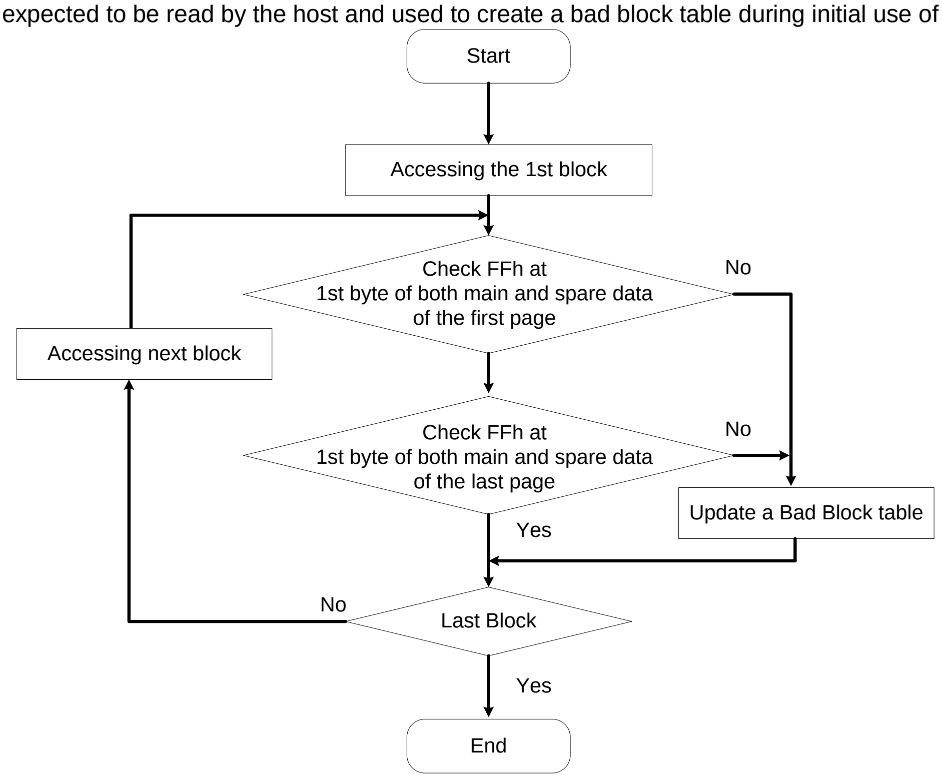


Figure 8: flow chart to create initial invalid block table sequential figures

6. COMMAND SET

Function	1st	2nd	3rd	4th	During busy
Page read	00H	30H	--	--	no
Read for copy-back	00H	35H	--	--	no
Random data output	05H	E0H	--	--	no
Cache read start	31H	--	--	--	no
Cache read random	00H	31H	--	--	no
Cache read end	3FH	--	--	--	no
Read id	90H	--	--	--	no
Read status register	70H	--	--	--	yes
Page program start / Cache program end	80H	10H	--	--	no
Random data input	85H	--	--	--	no
Copy back program	85H	10H	--	--	no
Cache program start	80H	15H	--	--	no
Block erase	60H	D0H	--	--	no
Reset	FFH	--	--	--	yes
Page re-program	8BH	10H	--	--	no
Read parameter page	ECH	--	--	--	no
Read unique ID	EDH	--	--	--	no

Note: 1. read status, read ID are always output on IO [7:0].

7. BUS OPERATION

The bus on the device is multiplexed. Data I/O, addresses, and commands all share the same pins. I/O [15:8] are used only for data in the x16 configuration. Addresses and commands are always supplied on I/O [7:0].

The command sequence typically consists of a COMMAND LATCH cycle, address input cycles, and one or more data cycles, either READ or WRITE.

There are several standard bus operations that control the device. These are Command Input, Address Input, Data Input, Data Output, Write Protect, and Standby.

CLE	ALE	CE#	WE#	RE#	WP#	MODE
H	L	L	Rising	H	X	Command input for read mode
L	H	L	Rising	H	X	Address input (4 cycles) for read mode
H	L	L	Rising	H	H	Command input for write mode
L	H	L	Rising	H	H	Address input (4 cycles) for write cycle
L	L	L	Rising	H	H	Data input
L	L	L	H	Falling	X	Sequential read and data output
L	L	L	H	H	X	During read(busy)
X	X	X	X	X	H	During program/Erase(busy)
X	X	X	X	X	L	Write protect
X	X	H	X	X	0V / VCC	Standby

Notes:

1. X can be VIL or VIH. H = Logic level HIGH. L = Logic level LOW.
2. WP# should be biased to CMOS high or CMOS low for stand-by mode.
3. WE# and RE# during Read Busy must be keep on high to prevent unplanned command/address/data input or to avert unintended data out. In this time, only Reset and Read Status can be input to the device.

7.1 Command Input Cycle

Command Input bus operation is used to give a command to the memory device. Commands are accepted with Chip Enable low, Command Latch Enable High, Address Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high.

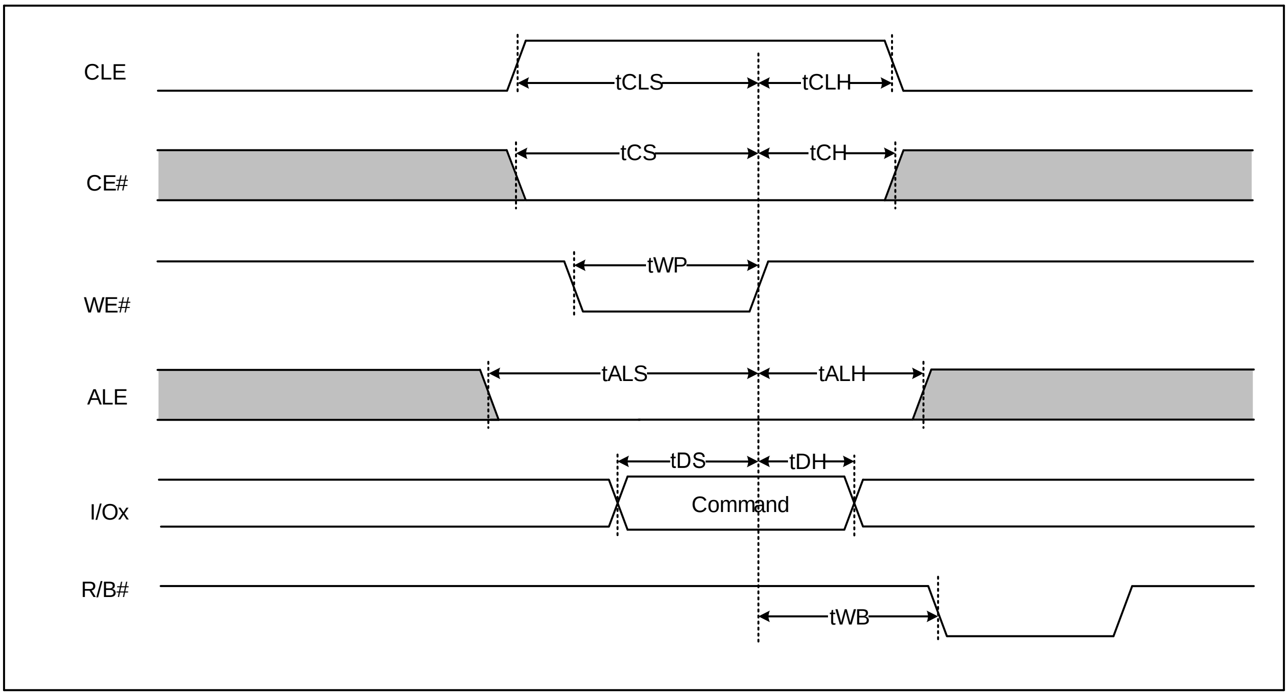


Figure 9: Command Input Cycle figures

7.2 Address Input Cycle

Address Input bus operation allows the insertion of the memory address. Addresses are accepted with Chip Enable low, Address Latch Enable High, Command Latch Enable low and Read Enable High and latched on the rising edge of Write Enable. Moreover for commands that starts a modify operation (write/erase) the Write Protect pin must be high.

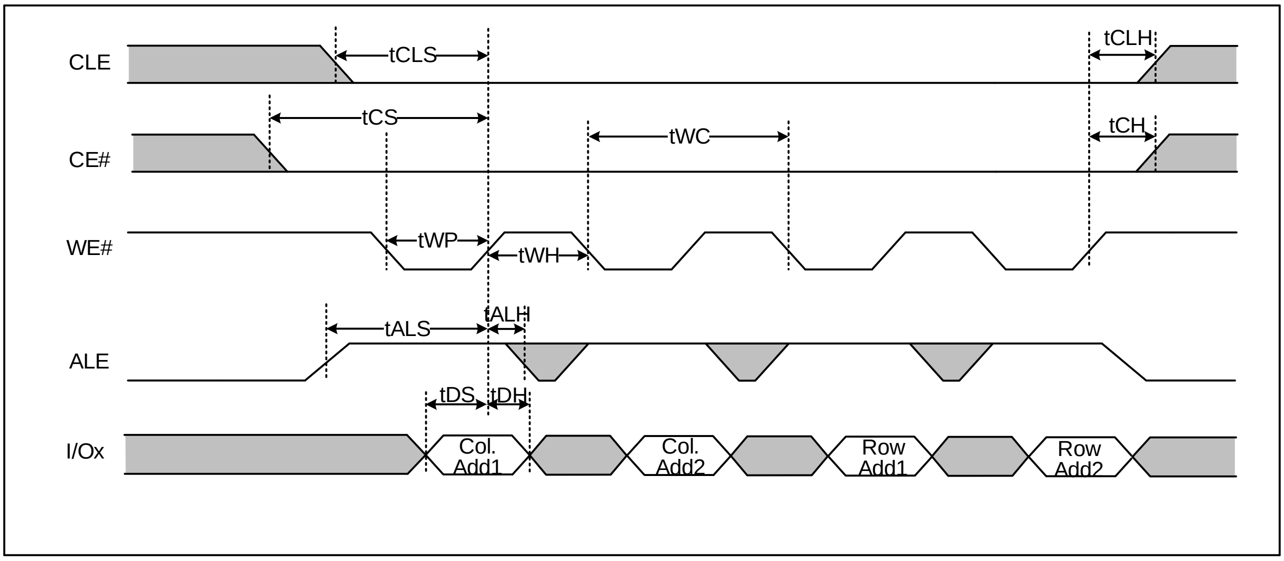


Figure 10: Address Input Cycle figures

7.3 Data Input Cycle

Data Input bus operation allows to feed to the device the data to be programmed. The data insertion is serially and timed by the Write Enable cycles. Data are accepted only with Chip Enable low, Address Latch Enable low, Command Latch Enable low, Read Enable High, and Write Protect High and latched on the rising edge of Write Enable.

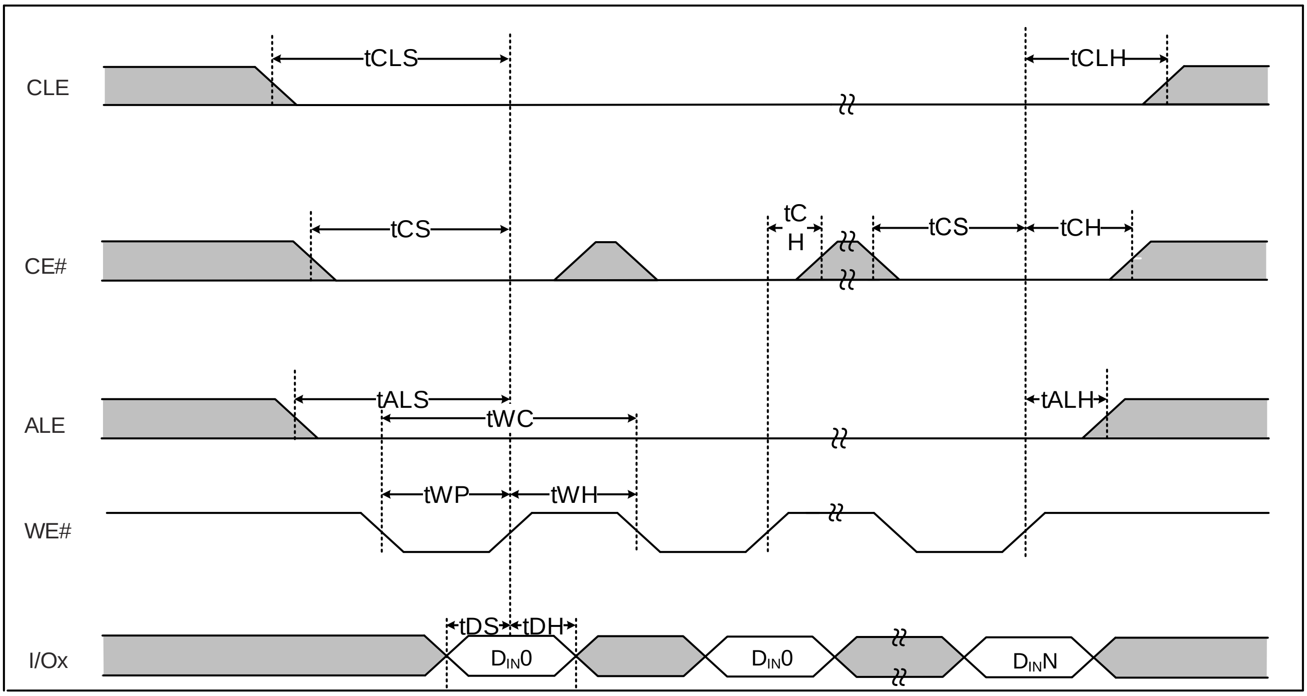


Figure 11: Data Input Cycle figures

7.4 Data Output Cycle

Data Output bus operation allows to output data from the device. The data output cycle is serially and timed by the Read Enable cycles. Data output may be used with CE# don't care. However, if CE# don't care is used tCEA and tCOH timing requirements shall be met by the host.

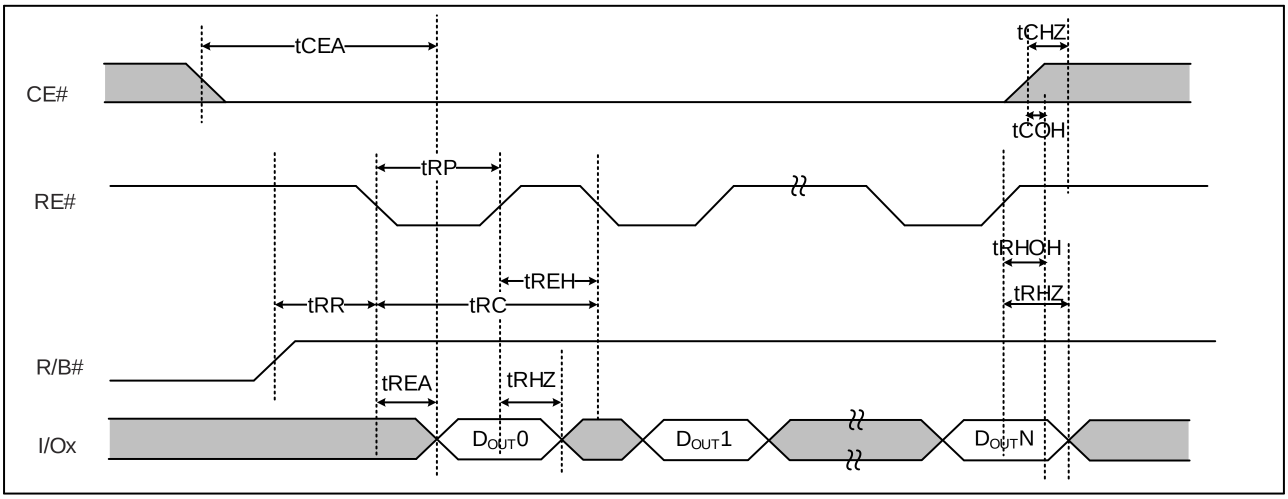


Figure 12_a: Data Output Cycle figures

If the host side uses a sequential access time (tRC) of less than 30ns, the data can be latched on the next falling edge of RE# as the waveform of EDO (Extended data output) mode.

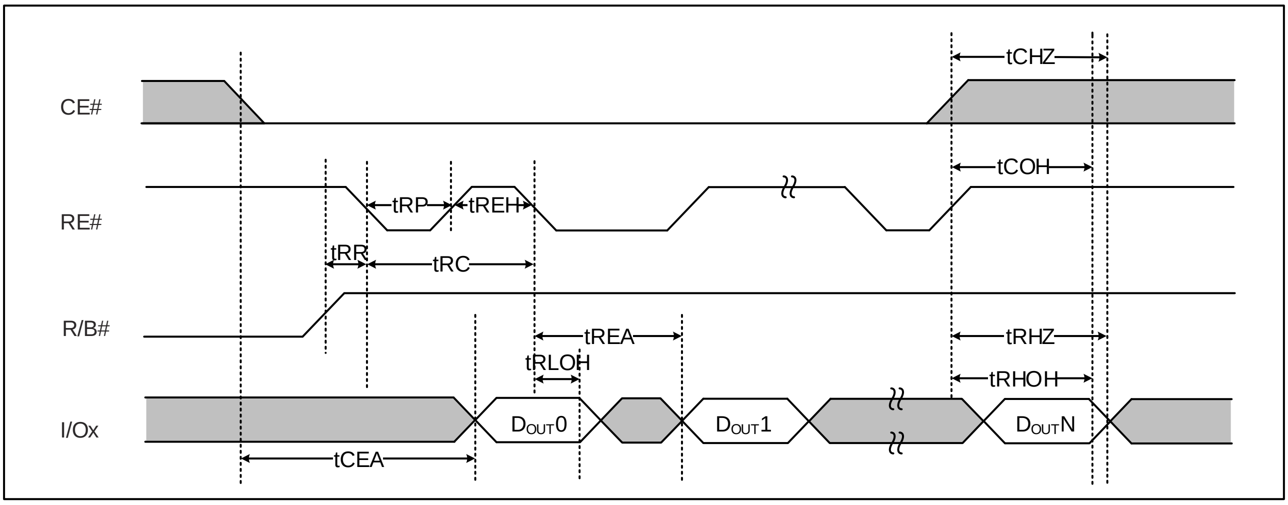


Figure 12_b: Data Output Cycle figures

7.5 Write Protect

The Erase and Program Operations are automatically reset when WP# goes Low. The operations are enabled and disabled as follows.

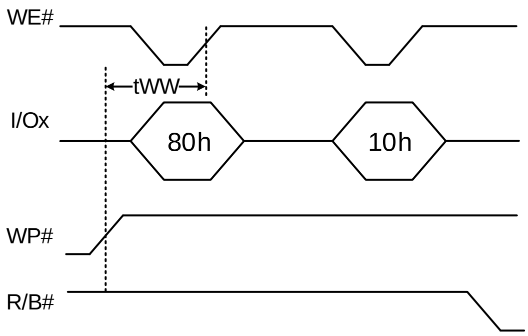


Figure 13_a: Write Protect Disable with program figures

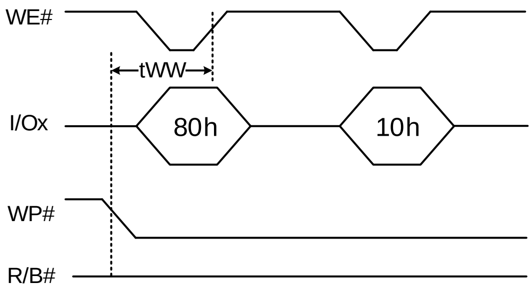


Figure 13_b: Write Protect Enable with program figures

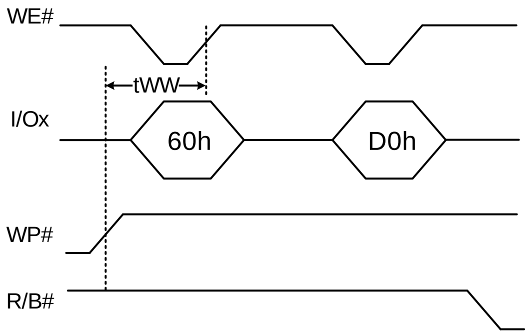


Figure 13_c: Write Protect Disable with erase figures

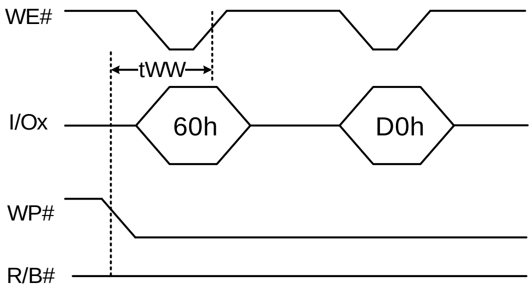


Figure 13_d: Write Protect Enable with erase figures

8. OPERATION DESCRIPTION

8.1 Page Read Operation

8.1.1 Common Page Read (00H-30H)

Read is initiated by writing 00H-30H to the command register along with four address cycles. The 2176 bytes of data within the selected page are transferred to the data registers. The system controller can detect the completion of this data transfer (tR) by analyzing the output of R/B# pin. Once the data in a page is loaded into the data registers, they may be read out in tRC by sequentially pulsing RE#. The repetitive high to low transitions of the RE# clock make the device output the data starting from the selected column address up to the last column address.

After the last data has been read out, CE# may be pulled up for some time to end the read operation, while during the RE# toggle cycle, CE# may be don't care when RE# is high. The CE# Don't Care feature may simplify the system interface, which allows controller to directly download the code from flash device, and the CE# transitions will not stop the read operation during the latency time.

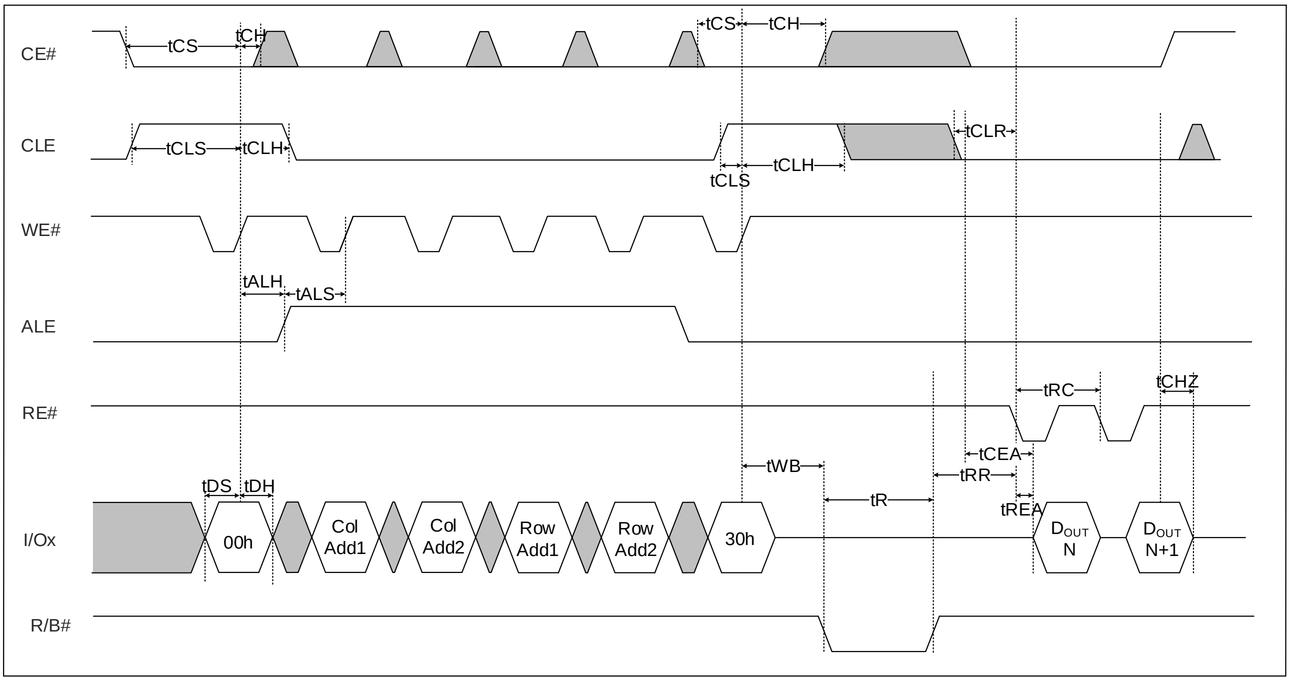


Figure 14: Common Page Read figures

8.1.2 Random Data Output (05H-E0H)

The device may output random data in a page instead of the consecutive sequential data by writing random data output command (05H-E0H). The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page Change Read Column shall only be issued when the device is in a read idle condition.

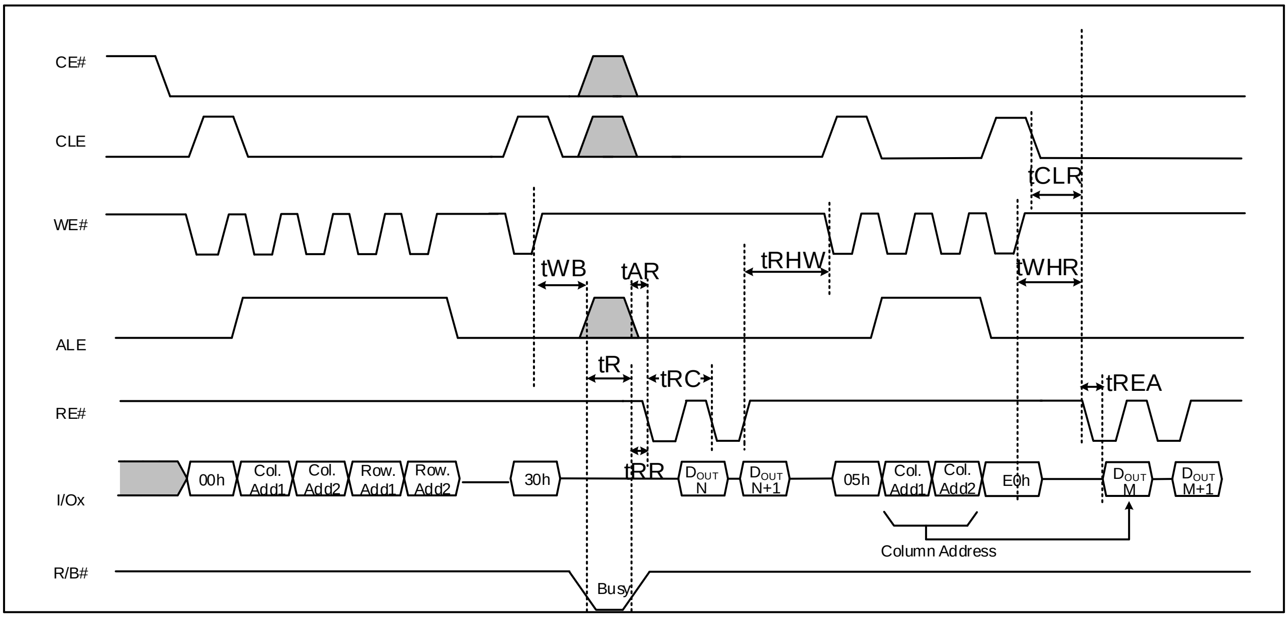


Figure 15: Random Data Output figures

8.1.3 Cache Read Operation (31H/3FH)

The Cache Read function permits a page to be read from the page register while another page is simultaneously read from the Flash array. A Read Page command shall be issued prior to the initial sequential or random Read Cache command in a read cache sequence. A Read Cache command shall be issued prior to a Read Cache End (3FH) command being issued. The Cache Read function may be issued after the Read function is complete. The host may enter the address of the next page to be read from the Flash array. Data output always begins at column address 00H. If the host does not enter an address to retrieve, the next sequential page is read, when the Read Cache function is issued. After the operation is begun R/B# is set to one (ready) and the host may begin to read the data from the previous Read or Read Cache function. Issuing an additional Read Cache function copies the data most recently read from the array into the page register. When no more pages are to be read, the final page is copied into the page register by issuing the 3FH command.

The host may begin to read data from the page register when R/B# is set to one (ready). When the 31H and 3FH commands are issued, R/B# shall be cleared to zero (busy) until the page has finished being copied from the Flash array.

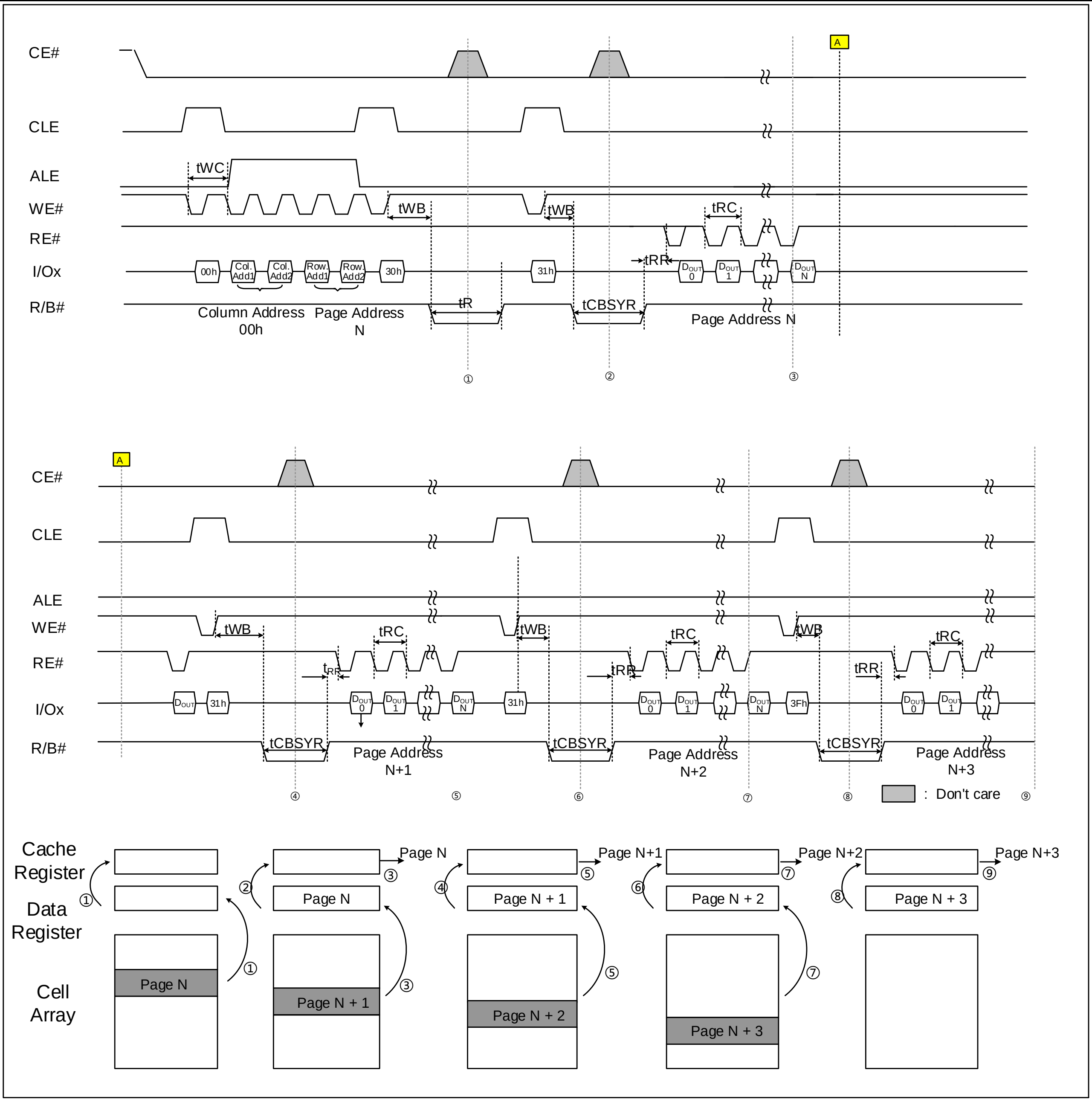


Figure 16: Cache Read Operation figures

Note:

C1-C2 : Column address of the page to retrieve. C1 is the least significant byte.

R1-R2 : Row address of the page to retrieve. R1 is the least significant byte.

D0-Dn : Data bytes/words read from page requested by the original Read or the previous cache operation.

8.2 Page Program Operation

8.2.1 Common Page Program (80H-10H)

The device is programmed basically on a page basis, but it does allow multiple partial pages programming of a word or consecutive bytes up to 2,176 in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed 4 times for main array (1time/512byte) and 4 times for spare array (1time/16byte). The addressing must be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 2,176 bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell.
The serial data loading period begins by inputting the Serial Data Input command (80h), followed by the four cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded.
The Page Program Confirm command (10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be issued to read the status register.
The command register remains in Read Status command mode until another valid command is written to the command register.

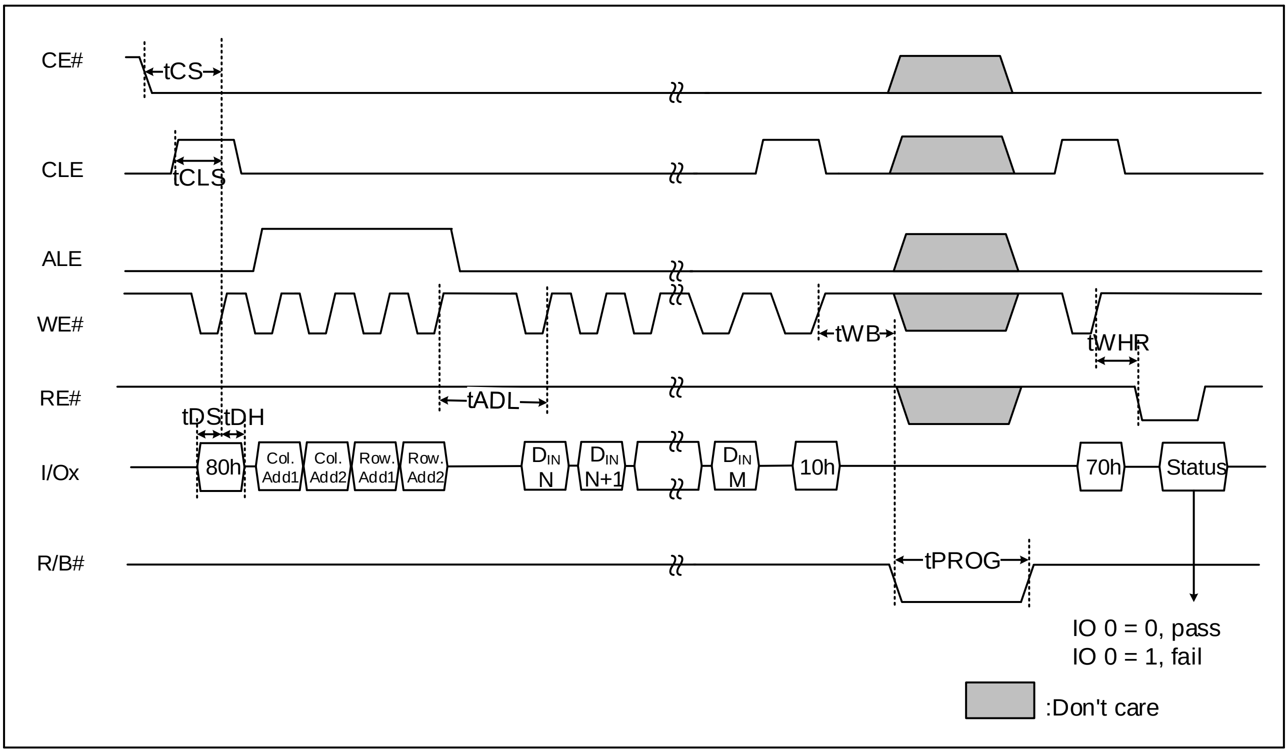


Figure 17: Common Page Program figures

8.2.2 Page Program Operation with Random Data Input (85H-10H)

The device supports random data input in a page. The column address of next data, which will be entered, may be changed to the address which follows random data input command (85H). Random data input may be operated multiple times regardless of how many times it is done in a page.

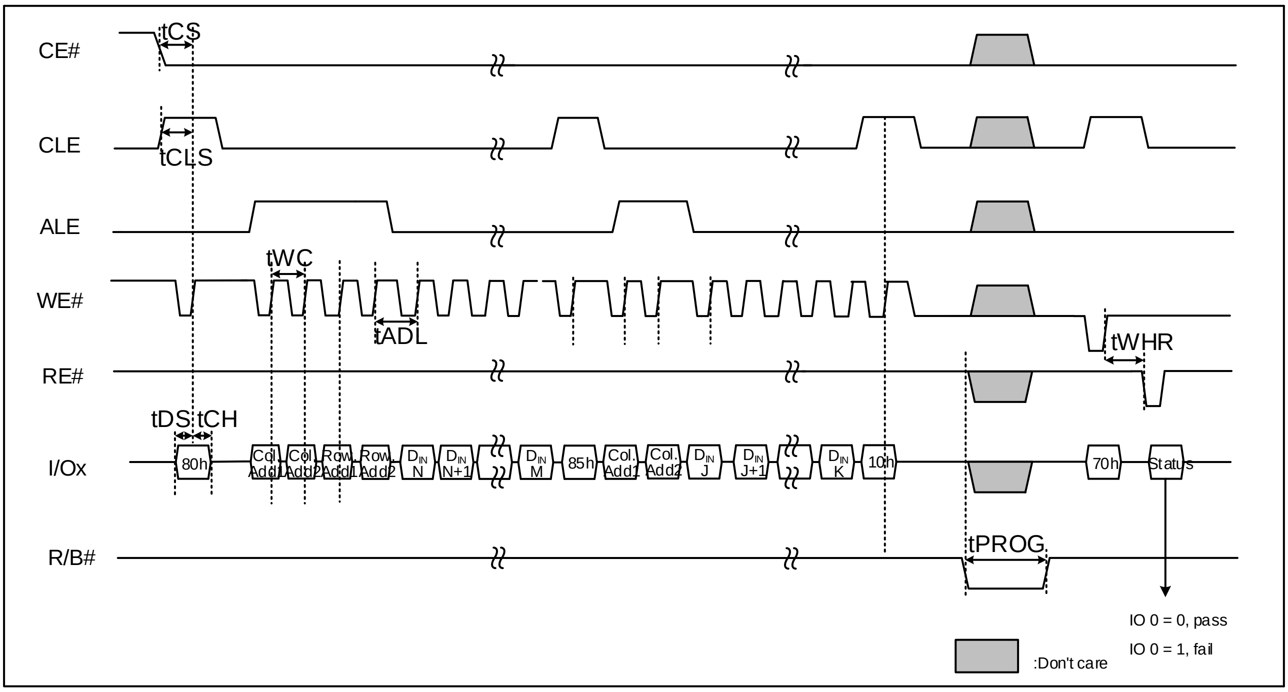


Figure 18: Page Program Operation with Random Data Input figures

8.2.3 Page Re-program (8BH-10H)

It was also highlighted that page program may result in a fail, which can be detected by Read Status Register. In this event, it implements the innovative feature of “page re-program”. This command allows the re-programming of the same pattern of the (failed) page into another memory location. The command sequence initiates with re-program setup (8BH), followed by the four cycle address inputs of the target page. If the target pattern for the destination page is not changed compared to the page, the program confirm can be issued (10H) without any data input cycle.

On the other hand, if the pattern bound for the target page is different from that of the previous page, data in cycles can be issued before program confirm “10H”

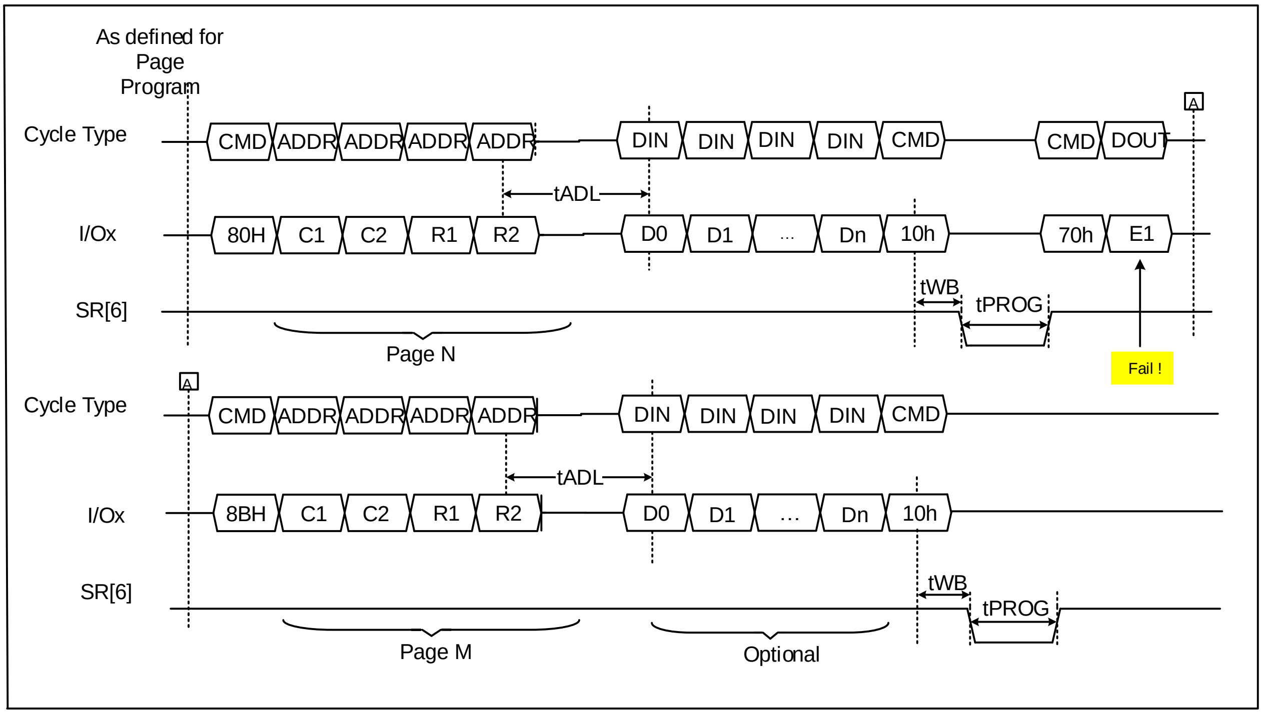


Figure 19: Page Re-program figures

8.2.4 Cache Program Operation (80H-15H)

Cache Program is an extension of Page Program, which is executed with one page data registers, and is available only within a block. Since the device has one page of cache memory, serial data input may be executed while data stored in data register are programmed into memory cell.

After writing the first set of data up to one page into the selected cache registers, Cache Program command (15H) instead of actual Page Program (10H) is inputted to make cache registers free and to start internal program operation. To transfer data from cache registers to data registers, the device remains in Busy state for a short period of time (tCBSYW) and has its cache registers ready for the next data-input while the internal programming gets started with the data loaded into data registers. Read Status command (70H) may be issued to find out when cache registers become ready by polling the Cache-Busy status bit (I/O 6). Pass/fail status of only the previous page is available upon the return to Ready state. When the next set of data is loaded with the Cache Program command, tCBSYW is affected by the progress of pending internal programming. The programming of the cache registers is initiated only when the pending program cycle is finished and the data registers are available for the transfer of data from cache registers. The status bit (I/O5) for internal Ready/Busy may be polled to identify the completion of internal programming. If the system monitors the progress of programming only with R/B#, the last page of the target programming sequence must be programmed with actual Page Program command (10H).

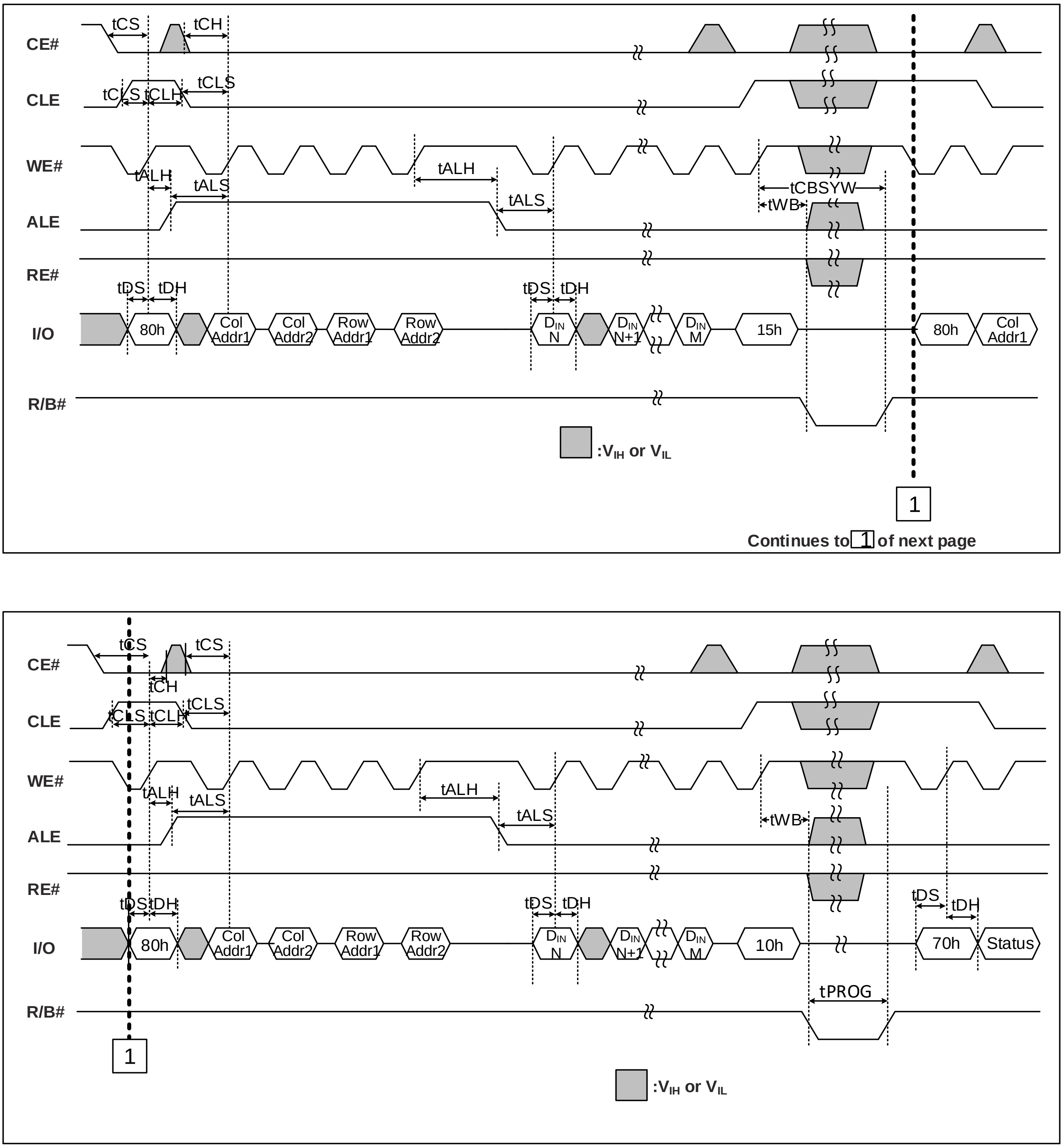


Figure 20: Cache Program Operation figures

8.2.5 Copy-Back Program with Random Data Input (00H-35H-85H-10H)

The copy-back program is configured to quickly and efficiently rewrite data stored in one page without utilizing an external memory. Since the time-consuming cycles of serial access and re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block is also needed to be copied to the newly assigned free block. The operation for performing a copy-back program is a sequential execution of page-read without serial access and copying-program with the address of destination page. A read operation with “35h”command and the address of the source page moves the wholepage bytes data into the internal data buffer. As soon as the device returns to Ready state, optional data read-out is allowed by toggling RE#, or Copy Back command (85H) with the address cycles of destination page may be written. The Program Confirm command (10H) is required to actually begin the programming operation. Data input cycle for modifying a portion or multiple distant portions of the source page is allowed. When there is a program-failure at Copy-Back operation, error is reported by pass/fail status. But, if Copy-Back operations are accumulated over time, bit error due to charge loss is not checked by external error detection/correction scheme. Please note that Random Data Input (with/without data) is entered before Program Confirm command (10H) after Random Data output.

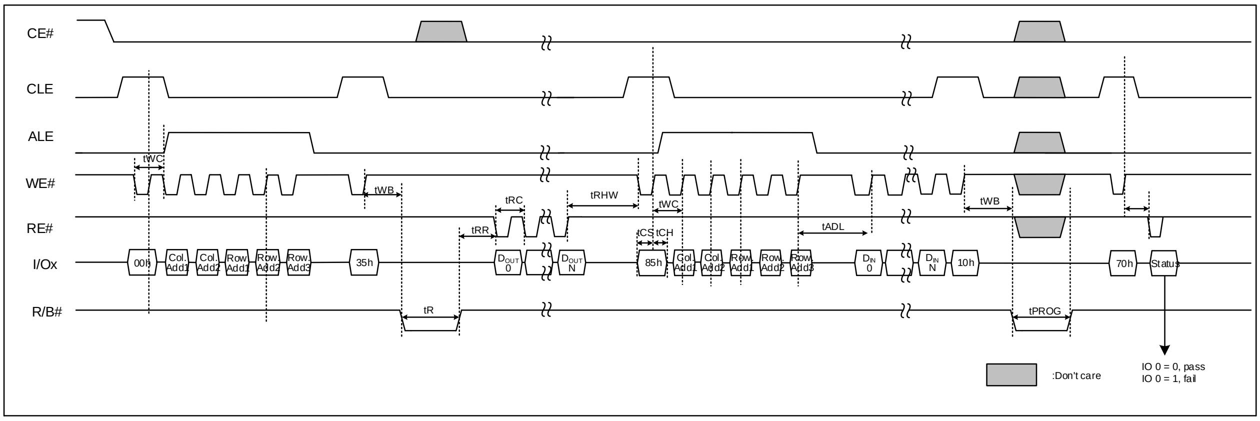


Figure 21: Copy-Back Program with Random Data Input figures

8.3 Block Erase Operation (60H-D0H)

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command (60H). Only address Row Address is valid while Column Addresses ignored. The Erase Confirm command (D0H) following the block address loading initiates the internal erasing process. At the rising edge of WE after the erase confirm command input, the internal write controller handles erase and erase verify. Once the erase process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of an erase by monitoring the R/B output, or the Status bit (I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while erasing is in progress. When the erase operation is completed, the Write Status Bit (I/O 0) may be checked.

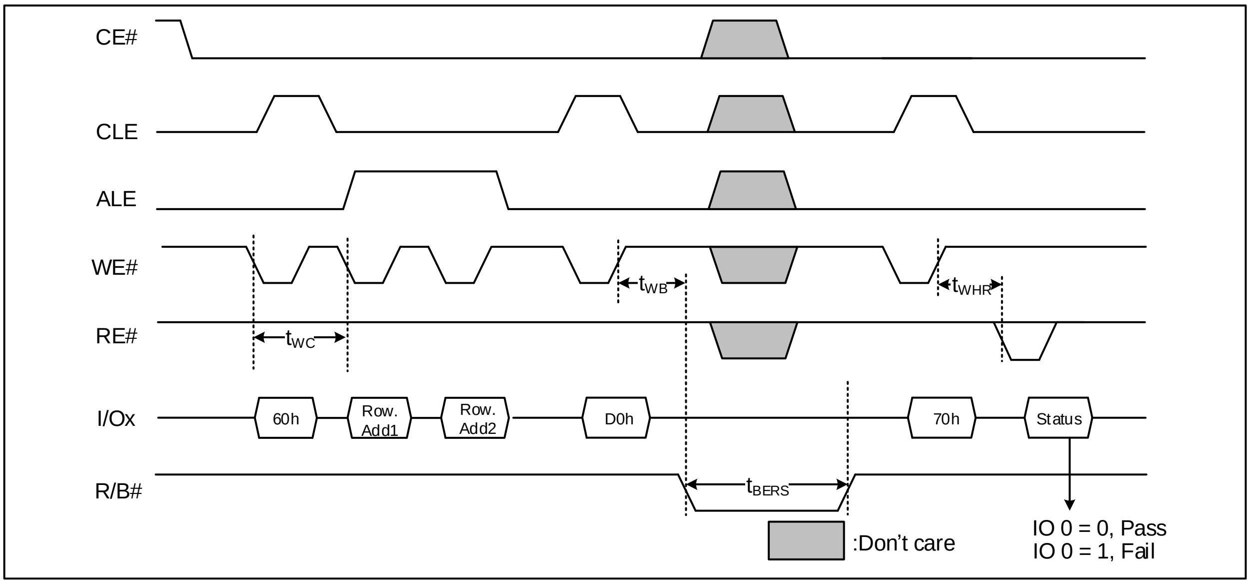


Figure 22: Common Block Erase Operation figures

8.4 Reset (FFH)

The device offers a reset feature, executed by writing FFH to the command register. When the device is in busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when R/B# is high. If the device is already in reset state a new reset command will be accepted by the command register. The R/B# pin transitions to low for tRST after the Reset command is written.

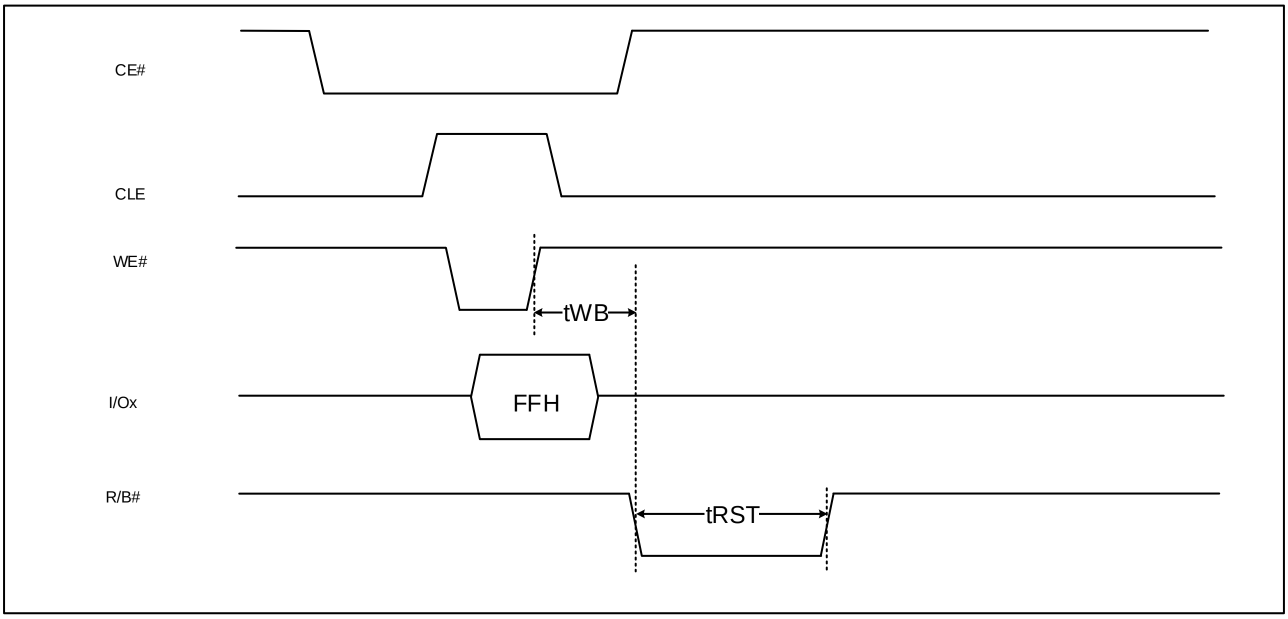


Figure 23: Reset (FFH) figures

8.5 Read Device Information

8.5.1 Read ID and ONFI Signature (90H)

The device contains a product identification mode, initiated by writing 90H to the command register, followed by an address input of 00H. Four read cycles sequentially output the manufacturer code, and the device code and other information, respectively. The command register remains in Read ID mode until further commands are issued to.

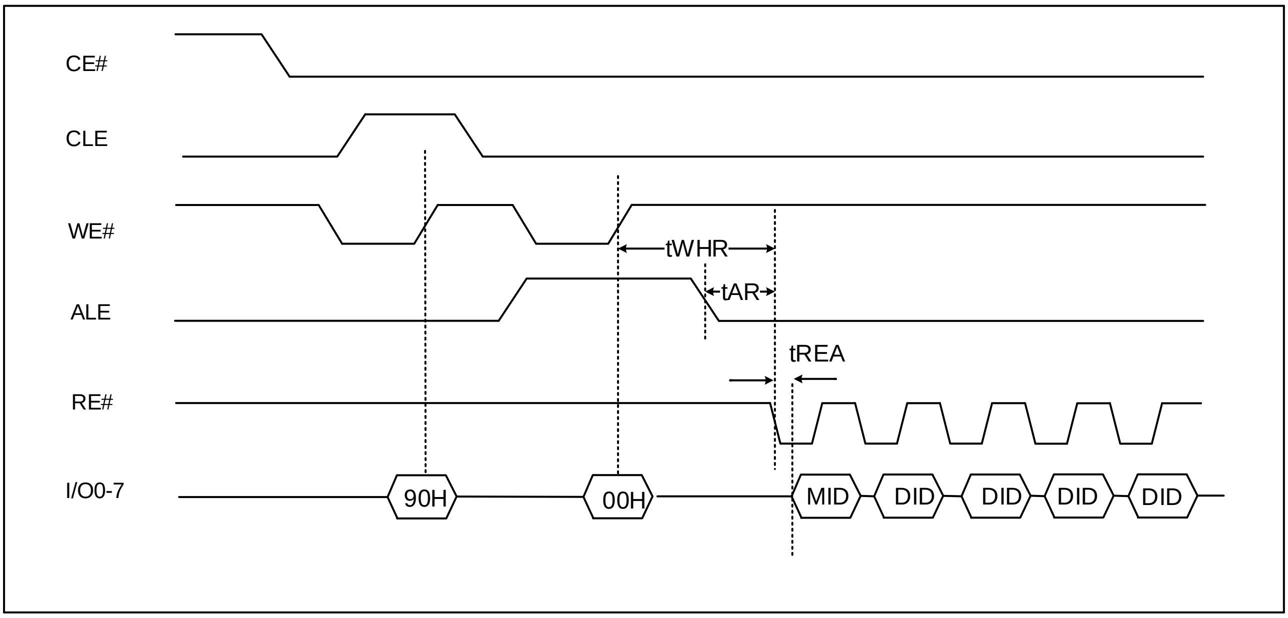


Figure 24: Read ID figures

ID Definition Table

Byte	Description
1st Byte	Manufacturer Code (MID)
2nd Byte	Device Code (DID)
3rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, Interleaved Program, Write Cache
4th Byte	Page size, Block size, Spare size, Organization
5th Byte	ECC & Plane

Read ID Data Table

Part Number	VCC	Bus Width	MID(1st)	DID(2nd)	3rd	4th	5th
GD9FU1G8F2A	3.3v	x8	C8	F1H	80H	1DH	42H
GD9FU1G6F2A	3.3v	x16	C8	C1H	80H	5DH	42H
GD9FS1G8F2A	1.8v	x8	C8	A1H	80H	15H	42H
GD9FS1G6F2A	1.8v	x16	C8	B1H	80H	55H	42H

2rd **Byte of Device Code Description**

2rd Cycle	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
VCC, Bus Width	3.3v 8bits	1	1	1	1				
	3.3v 16bits	1	1	0	0				
	1.8v 8bits	1	0	1	0				
	1.8v 16bits	1	0	1	1				
Memory density	1G					0	0	0	1
	2G					0	0	1	0
	4G					0	0	1	1
	8G					0	1	0	0
	16G					0	1	0	1
	32G					0	1	1	0
	64G					0	1	1	1
	256G					1	0	0	0
	512G					1	0	0	1
	1T					1	0	1	0
	2T					1	0	1	1
	22G					1	1	0	0

3rd Byte of Device Identifier Description

3rd Cycle	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		
Number of Simultaneously Programmed Pages	1			0	0				
	2			0	1				
	4			1	0				
	8			1	1				
Interleaved Program Between Multiple Die	Not Supported		0						
	Supported		1						
Write Cache (Cache Programming)	Not Supported	0							
	Supported	1							

4th Byte of Device Identifier Description

4th Cycle	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
Page Size (without Spare Area)	1KB							0	0
	2KB							0	1
	4KB							1	0
	8KB							1	1
Size of spare area (byte per 512-byte)	16						0		
	32						1		
Serial Access Time	45ns	0				0			
	25ns	0				1			
	Reserved	1				0			
	Reserved	1				1			
Block Size (Without Spare Area)	64KB			0	0				
	128KB			0	1				
	256KB			1	0				
	512KB			1	1				
Organization	x8		0						
	x16		1						

5th Byte of ECC & Plane

5th Cycle	Description	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
ECC Level	1							0	0
	2							0	1
	4							1	0
	8							1	1
Plane Number	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
Plane size	64Mb		0	0	0				
	128Mb		0	0	1				
	256Mb		0	1	0				
	512Mb		0	1	1				
	1Gb		1	0	0				
	2Gb		1	0	1				
	4Gb		1	1	0				
	8Gb		1	1	1				
Internal ECC	ECC disabled	0							
	ECC enabled	1							

To retrieve the ONFI signature, the command 90H together with an address of 20H shall be entered. The ONFI signature is the ASCII encoding of 'ONFI' where 'O' = 4FH, 'N' = 4EH, 'F' = 46H, and 'I' = 49H. Reading beyond four bytes yields indeterminate values.

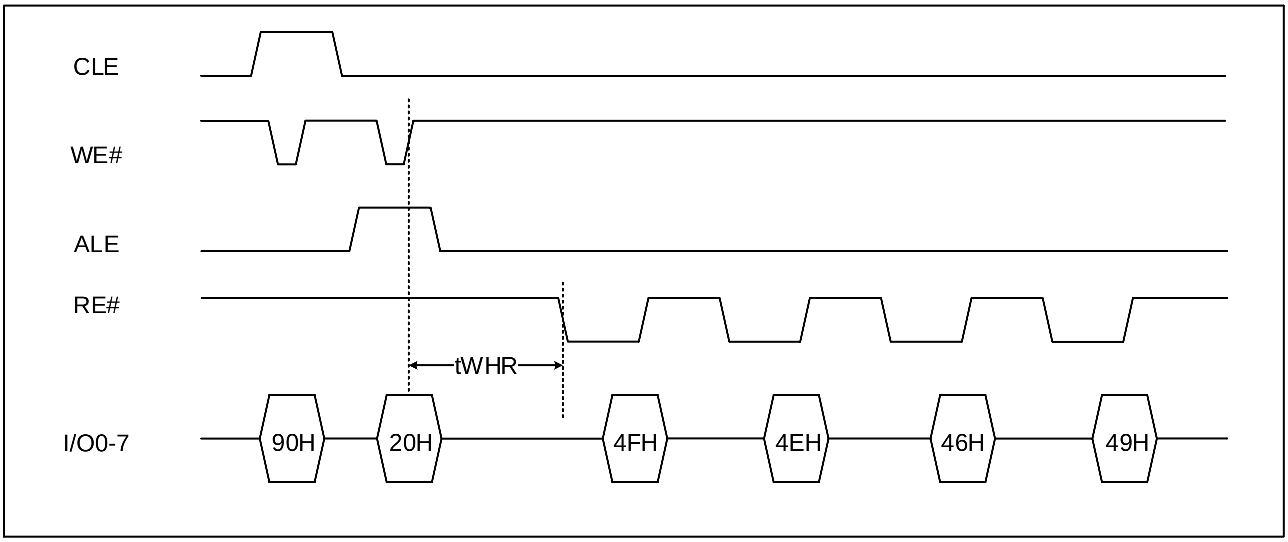


Figure 25: Read ONFI Signature figures

8.5.2 Read Unique ID (EDH)

The Read Unique ID function is used to retrieve the 16 byte unique ID (UID) for the device. The unique ID when combined with the device manufacturer shall be unique.

The UID data may be stored within the Flash array. To allow the host to determine if the UID is without bit errors, the UID is returned with its complement. If the XOR of the UID and its bit-wise complement is all ones, then the UID is valid. To accommodate robust retrieval of the UID in the case of bit errors, sixteen copies of the UID and the corresponding complement shall be stored by the target. For example, reading bytes 32-63 returns to the host another copy of the UID and its complement.

To change the data output location, it is recommended to use the Random Data Out command set (05H-E0H).The Status Read command (70H) can be used to check the completion. To continue the read operation, a following read command (00h) to re-enable the data out is necessary.

Bytes	Value
0-15	UID
16-31	UID complement (bit-wise)

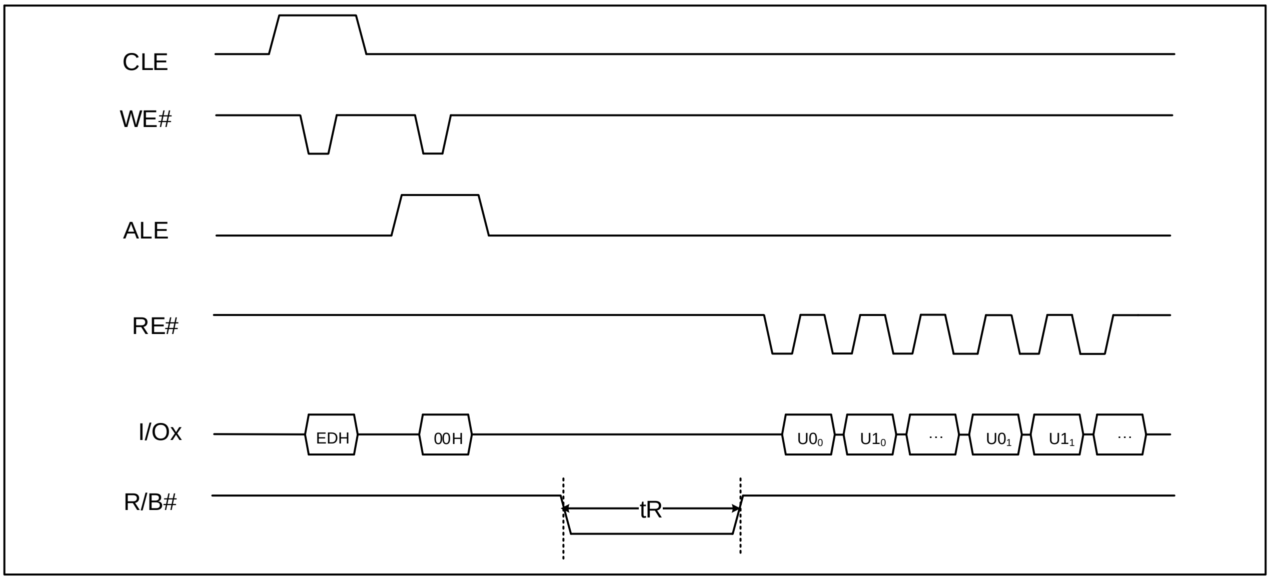


Figure26: Read Unique ID Timing

8.5.3 Read Parameter Page (ECH)

The Read Parameter Page function retrieves the data structure that describes the chip's organization, features, timing-sand other behavioral parameters. This data structure enables the host processor to automatically recognize the NAND Flash configuration of a device. The whole data structure is repeated at least three times. The Random Data Read command (05H-E0H) can be issued during execution of the read parameter page to read specific portion-soft the parameter page. The Read Status command (70H) may be used to check the status of read parameter page during execution. After completion of the Read Status command, 00H is issued by the host on the command line to continue with the data output flow for the Read Parameter Page command.

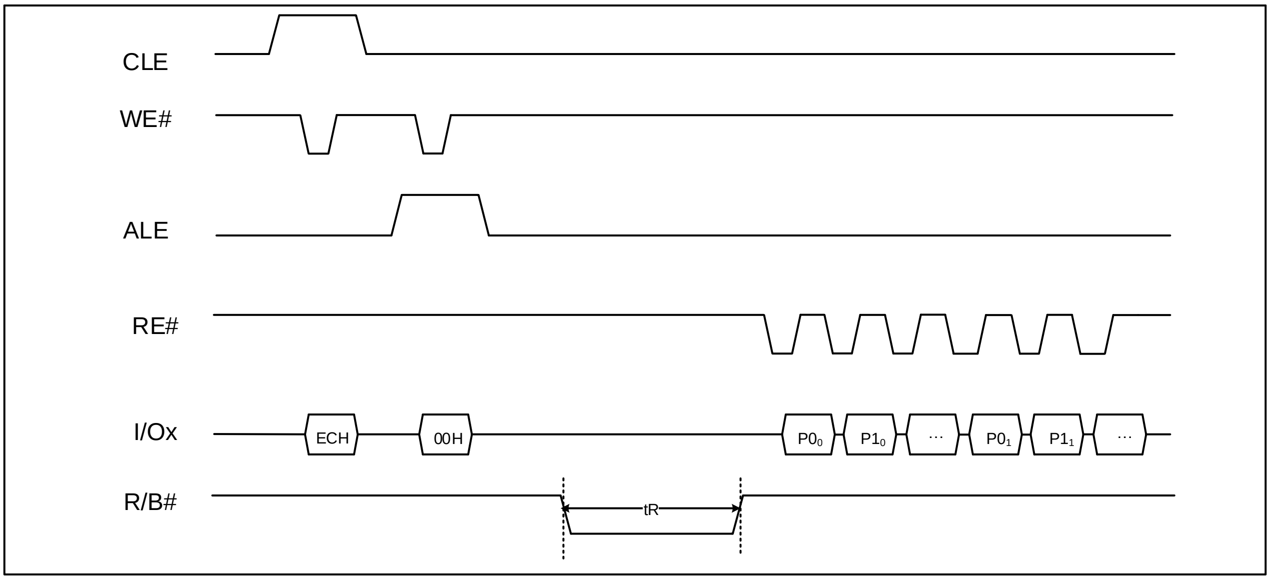


Figure 27: Read Parameter Page figures

Byte	O/M	Description	
0-3	M	Parameter page signature Byte 0: 4FH, “O” Byte 1: 4EH, “N” Byte 2: 46H, “F” Byte 3: 49H, “I”	4FH 4EH 46H 49H
4-5	M	Revision number 2-15 Reserved (0) 1 1 = supports ONFI version 1.0 0 Reserved (0)	02H 00H
6-7	M	Features supported 5-15 Reserved (0) 4 1 = supports odd to even page Copyback 3 1 = supports interleaved operations 2 1 = supports non-sequential page programming 1 1 = supports multiple LUN operations 0 1 = supports 16-bit data bus width	10H(X8)/ 11H(X16) 00H
8-9	M	Optional commands supported 6-15 Reserved (0) 5 1 = supports Read Unique ID 4 1 = supports Copy-back 3 1 = supports Read Status Enhanced 2 1 = supports Get Features and Set Features 1 1 = supports Read Cache Integrity 0 1 = supports Page Cache Program command	33H 00H
10-31		Reserved (0)	00H … 00H
		Manufacturer Information block	
32-43	M	Device manufacturer (12 ASCII characters)“GIGADEVICE ”	47H 49H 47H 41H 44H 45H 56H 49H 43H 45H 20H 20H

<table>
<tr><td>44-63</td><td>M</td><td>Device model (20 ASCII characters)
<table><tr><th>Device Model</th><th>ORGANIZATION</th><th>VCC RANGE</th></tr><tr><td>“GD9FS1G8F2A”</td><td>128M x 8bit</td><td>1.7v ~ 1.95v</td></tr><tr><td>“GD9FS1G6F2A”</td><td>64M x 16bit</td><td>1.7v ~ 1.95v</td></tr><tr><td>“GD9FU1G8F2A“</td><td>128M x 8bit</td><td>2.7v ~ 3.6v</td></tr><tr><td>“GD9FU1G6F2A“</td><td>64M x 16bit</td><td>2.7v ~ 3.6v</td></tr></table></td><td>47H
44H
39H
46H
53H/55H
31H
47H
38H/36H
46H
32H
41H
20H
20H
20H
20H
20H
20H
20H
20H
20H</td></tr>
<tr><td>64</td><td>M</td><td>JEDEC manufacturer ID“C8”</td><td>C8H</td></tr>
<tr><td>65-66</td><td>O</td><td>Date code</td><td>00H
00H</td></tr>
<tr><td>67-79</td><td></td><td>Reserved</td><td>00H
00H
00H</td></tr>
<tr><td></td><td></td><td>Memory organization block</td><td></td></tr>
<tr><td>80-83</td><td>M</td><td>Number of data bytes per page</td><td>00H
08H
00H
00H</td></tr>
<tr><td>84-85</td><td>M</td><td>Number of spare bytes per page</td><td>80H
00H</td></tr>
<tr><td>86-89</td><td>M</td><td>Number of data bytes per partial page</td><td>00H
02H
00H
00H</td></tr>
<tr><td>90-91</td><td>M</td><td>Number of spare bytes per partial page</td><td>20H
00H</td></tr>
<tr><td>92-95</td><td>M</td><td>Number of pages per block</td><td>40H
00H
00H
00H</td></tr>
</table>

96-99	M	Number of blocks per logical unit (LUN)	00H 04H 00H 00H
100	M	Number of logical units (LUNs)	01H
101	M	Number of address cycles 4-7 Column address cycles 0-3 Row address cycles	22H
102	M	Number of bits per cell	01H
103-104	M	Bad blocks maximum per LUN	14H 00H
105-106	M	Block endurance	01H 05H
107	M	Guaranteed valid blocks at beginning of target	01H
108-109	M	Block endurance for guaranteed valid blocks	01H 05H
110	M	Number of programs per page	04H
111	M	Partial programming attributes 5-7 Reserved 4 1 = partial page layout is partial page data followed by partial page spare 1-3 Reserved 0 1 = partial page programming has constraints	00H
112	M	Number of bits ECC correctability	04H
113	M	Number of interleaved address bits 4-7 Reserved (0) 0-3 Number of interleaved address bits	00H
114	O	Interleaved operation attributes 4-7 Reserved (0) 3 Address restrictions for program cache 2 1 = program cache supported 1 1 = no block address restrictions 0 Overlapped / concurrent interleaving support	00H
115-127		Reserved	00H … 00H
		Electrical parameters block	
128	M	I/O capacitance	06H

129-130	M	Timing mode support 6-1 5Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0, shall be 1	07H(3.3V)/ 03H(1.8V) 00H
131-132	O	Program cache timing mode support 6-1 5Reserved (0) 5 1 = supports timing mode 5 4 1 = supports timing mode 4 3 1 = supports timing mode 3 2 1 = supports timing mode 2 1 1 = supports timing mode 1 0 1 = supports timing mode 0,	07H(3.3V)/ 03H(1.8V) 00H
133-134	M	tPROG Maximum page program time (us)	BCH 02H
135-136	M	tBERS Maximum block erase time (us)	10H 27H
137-138	M	tR Maximum page read time (us)	19H 00H
139-140	M	tCCS Minimum Change Column setup time (ns)	3CH 00H
141-163		Reserved	00H
		Vendor block	
164-165	M	Vendor specific Revision number	00H
166-253		Vendor specific	00H
254-255	M	Integrity CRC	
		Redundant parameter pages	
256-511	M	Value of bytes 0-255	
512-767	M	Value of bytes 0-255	
768+	O	Additional redundant parameter pages	

Notes:

1. "O" Stands for Optional, "M" for Mandatory
2. The Integrity CRC (Cycling Redundancy Check) field is used to verify that the contents of the parameters page were transferred correctly to the host. Please refer to ONFI 1.0 specifications for details.
   The CRC shall be calculated using the following 16-bit generator polynomial: *G(X) = X16 + X15 +X2 + 1*, This polynomial in hex may be represented as 8005h.
3. The CRC value shall be initialized with a value of 4F4Eh before the calculation begins. There is no XOR applied to the final CRC value after it is calculated. There is no reversal of the data bytes or the CRC calculated value.

Parameter page CRC value table

Device Model	**ORGANIZATION**	**VCC RANGE**	**CRC value B254/B255**
"GD9FS1G8F2A"	128M x 8bit	1.7v ~ 1.95v	D0H/DBH
"GD9FS1G6F2A"	64M x 16bit	1.7v ~ 1.95v	F8H/18H
"GD9FU1G8F2A"	128M x 8bit	2.7v ~ 3.6v	88H/D5H
"GD9FU1G6F2A"	64M x 16bit	2.7v ~ 3.6v	A0H/16H

8.6 Read Status (70H)

The device contains a Status Register which may be read to find out whether an operation is completed and whether the program or erase operation is completed successfully. After writing 70H command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of CE# or RE#, whichever occurs last. This allows the system to poll the progress of each device in multiple memory connections even when R/B# pins are common-wired. RE# or CE# does not need to be toggled for updated status. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command (00h) should be given before starting read cycles.

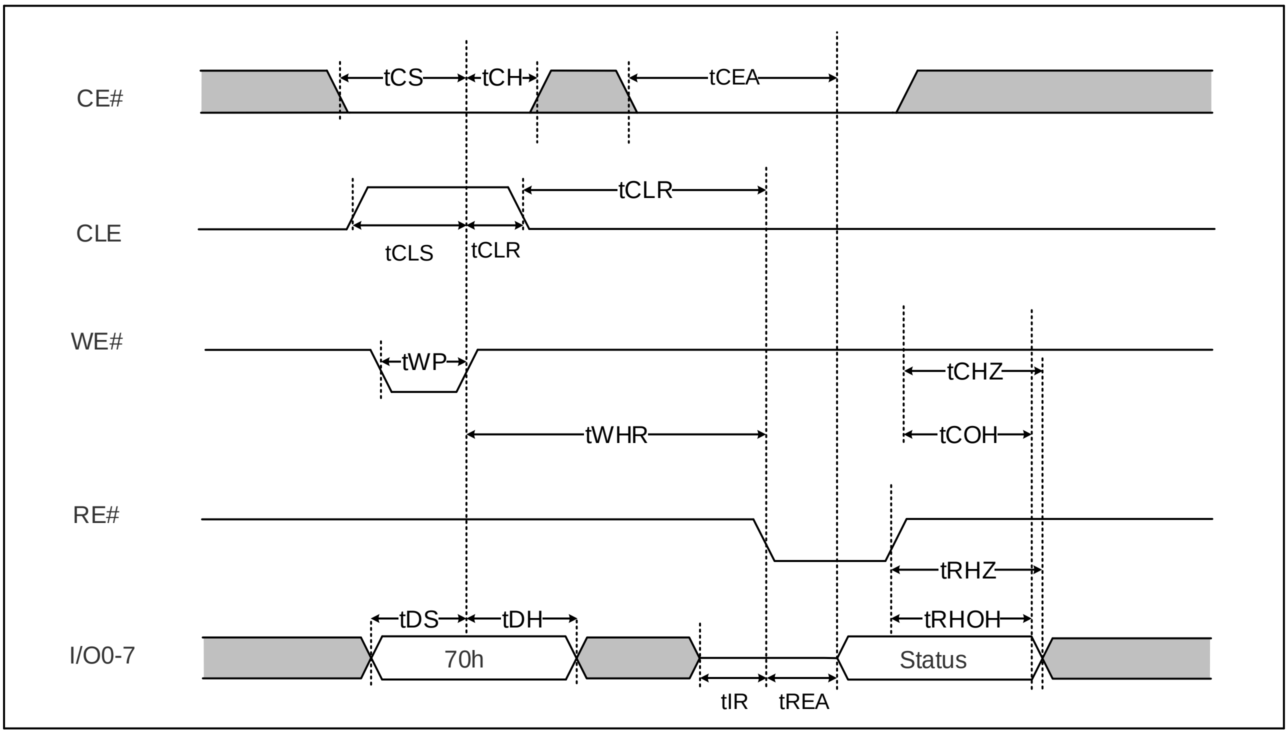


Figure 28: Read Status figures

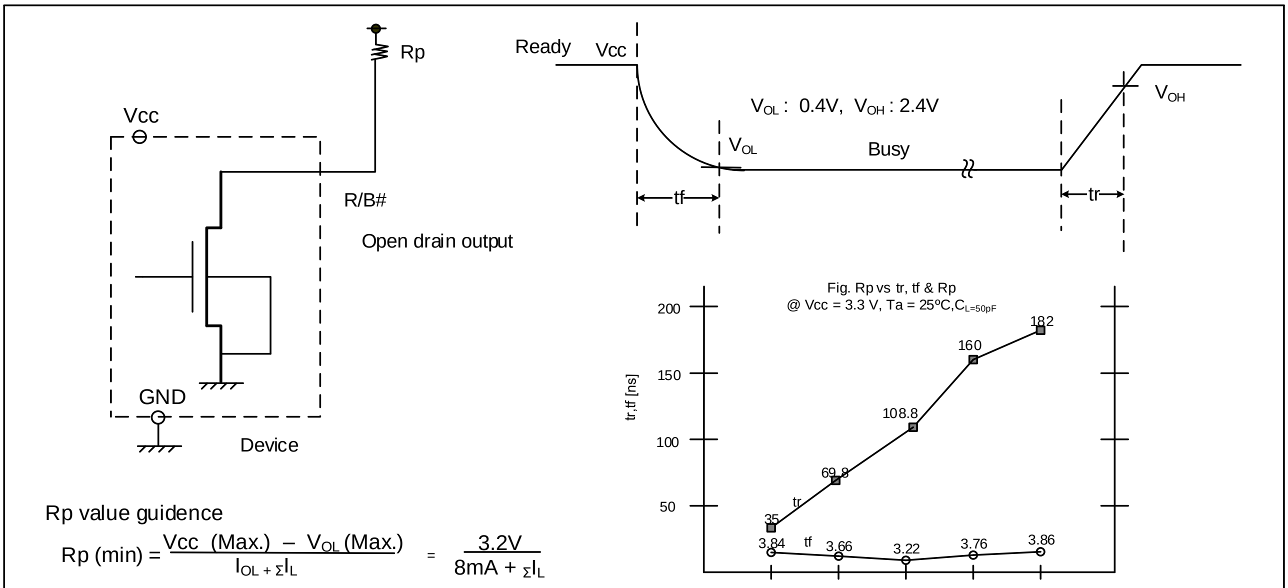
Status Register Definitions

I/O No.	Page Program	Block Erase	Cache Program	Read	Cache Read	Definition
I/O0	Pass/Fail	Pass/Fail	Pass/Fail(N)	-	-	FAIL N Page Pass : 0 Fail : 1
I/O1	-	-	Pass/Fail(N-1)	-	-	FAILC N-1 Page Pass : 0 Fail : 1
I/O2	-	-	-	-	-	Don't Care
I/O3	-	-	-	-	-	Don't Care
I/O4	-	-	-	-	-	Don't Care
I/O5	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	ARDY Ready/Busy for Array Operation Busy : 0 Ready : 1
I/O6	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	Ready/Busy	RDY Ready/Busy Busy : 0 Ready : 1
I/O7	Write Protect	Write Protect	Write Protect	Write Protect	Write Protect	WP# Protected:0 Not Protected:1

Notes:
1. I/O0: This bit is only valid for Program and Erase operations. During Cache Program operations, this bit is only valid when I/O5 is set to 1.
2. I/O1: This bit is only valid for cache program operations. This bit is not valid until after the second 15h command or the 10h command has been transferred in a Cache program sequence.
3. I/O5: If set to one, then there is no array operation in progress. If cleared to zero, then there is a command being processed (I/O6 is cleared to zero) or an array operation in progress.
4. I/O6: When cache operations are in use, then this bit indicates whether another command can be accepted, and I/O5 indicates whether the operation is complete.
5. I/O7: the bit indicates if the block is protected, which include WP# protection and other protection.

8.7 Ready/Busy# (R/B#)

The device has a Ready/Busy output that provides method of indicating the completion of a page program, erase, copy-back and random read completion. The R/B# pin is normally high and goes to low when the device is busy (after a reset, read, program, and erase operation). It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B# outputs to be Or-tied. Because pull-up resistor value is related to tR (R/B#), an appropriate value can be obtained with the following reference below chart. Its value can be determined by the following guidance.



$$Rp(min) = \frac{Vcc\ (Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

Where IL is the sum of the input curmts of all devices tied to the R/B# pin.
Rp(max) is determined by maximum permissible limit of tr

Figure 29: Ready/Busy figures

8.8 Data Protection & Power on/off Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever VCC is below VLKO. WP# pin provides hardware protection and is recommended to be kept at VIL during power-up and power-down. A recovery time of minimum 10us is required before internal circuit gets ready for any command sequences. The two-step command sequence for program/erase provides additional software protection.

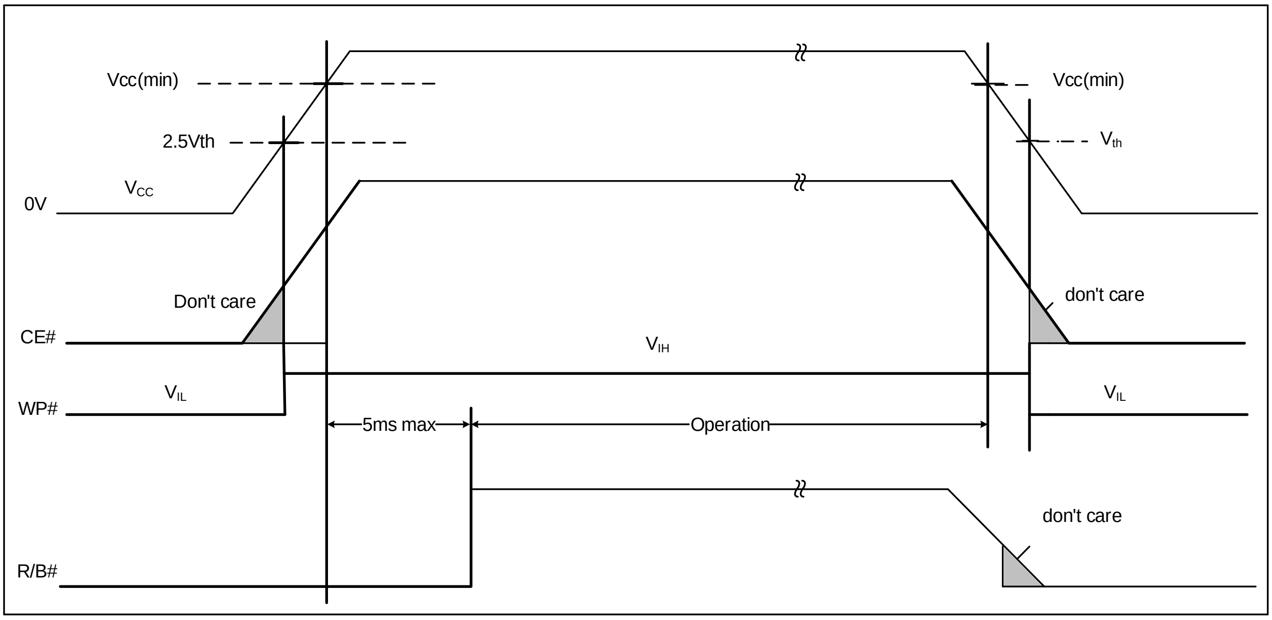


Figure 30_a: Data protection and Power on/off (3.3V Device)

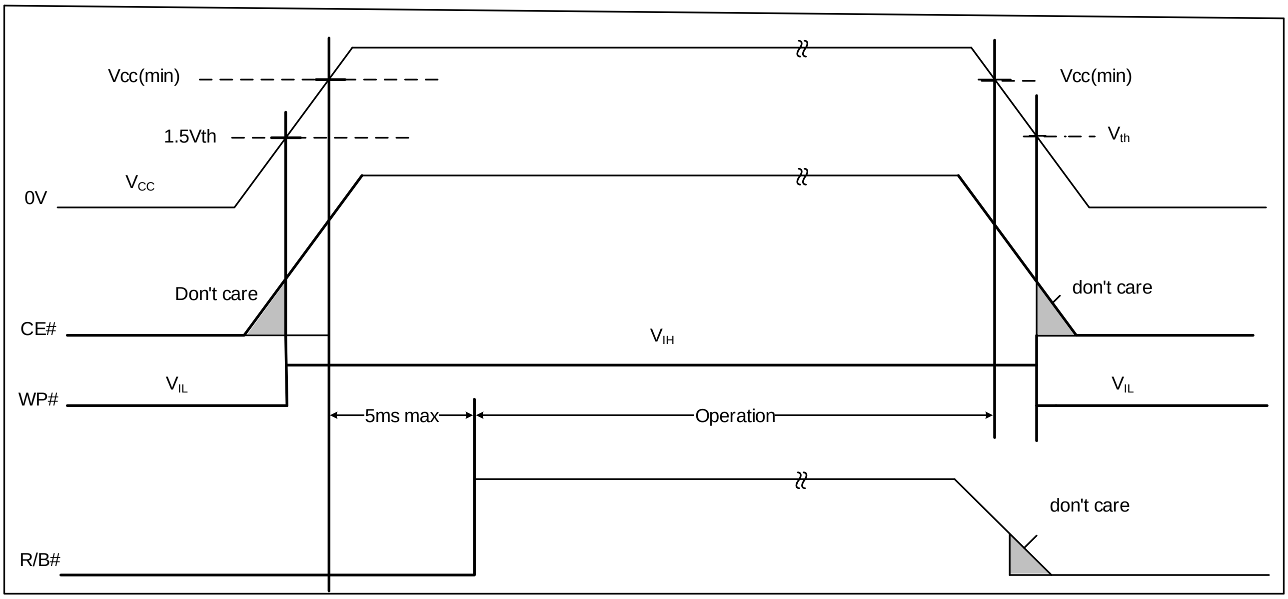


Figure 30_b: Data protection and Power on/off (1.8V Device)

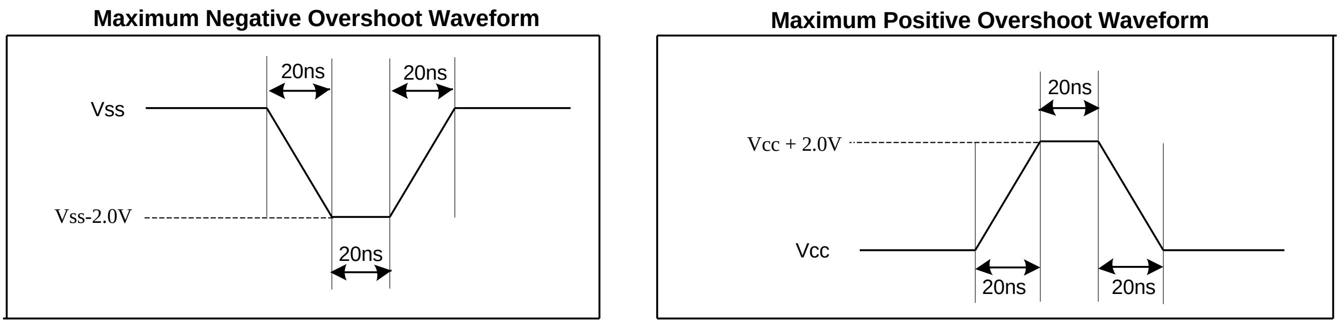
9. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to VSS	VIN/OUT	-0.6 to VCC+0.4	V
	VCC(3.3V)	-0.6 to + 4.0	
	VCC(1.8V)	-0.6 to + 2.5	
Temperature Under Bias	TBIAS	-50 to +125	°C
Storage Temperature	TSTG	-65 to +150	°C

Notes:

1. Minimum DC voltage is -0.6V on input/output pins.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Figure 31: Input Test Waveform and Measurement Level



10. VALID BLOCKS

	Min	Typ	Max	Unit
Valid Block Number	1004		1024	Blocks

Notes:

1. The 1st block is guaranteed to be a valid block with ECC at the time of shipment.
2. Invalid blocks are one that contains one or more bits. The device may contain invalid blocks upon shipment.

11. DC CHARACTERISTICS

(T=-40℃~85℃/-40℃~105℃, VCC=1.7~2.0V)

Parameter		Symbol	Test Conditions	1.7v ~ 1.95v			Unit
				Min	Typ.	Max	
Power on reset current		ICC0	FFh command after power on			50	mA
Operating Current	Page Read with Serial Access	ICC1	tRC=Min, CE#=VIL, IOUT=0mA	-	15	30	mA
	Program	ICC2	-	-	15	30	
	Erase	ICC3	-	-	15	30	
Standby Current (CMOS)		ISB	CE#=VCC-0.2, WP#=0V/VCC	-	10	50	μA
Input Leakage Current		ILI	VIN=0 to VCC(max)	-	-	±10	
Output Leakage Current		ILO	VOUT=0 to VCC(max)	-	-	±10	
Input High Voltage		VIH	-	0.8xVCC	-	VCC+0.3	V
Input Low Voltage		VIL	-	-0.3	-	0.2xVCC	
Output High Voltage Level		VOH	IOH=-400μA	VCC-0.3	-	-	
Output Low Voltage Level		VOL	IOL=2.1mA	-	-	0.4	
Output Low Current(R/B#)		IOL(R/B#)	VOL=0.45V	3	4	-	mA
erase/program lockout voltage		VLKO			1.5		V

(T=-40℃~85℃/-40℃~105℃, VCC=2.7~3.6V)

Parameter		Symbol	Test Conditions	2.7v ~ 3.6v			Unit
				Min	Typ.	Max	
Power on reset current		ICC0	FFh command after power on			50	mA
Operating Current	Page Read with Serial Access	ICC1	tRC=Min, CE#=VIL, IOUT=0mA	-	15	30	mA
	Program	ICC2	-	-	15	30	
	Erase	ICC3	-	-	15	30	
Standby Current (CMOS)		ISB	CE#=VCC-0.2, WP#=0V/VCC	-	10	50	μA
Input Leakage Current		ILI	VIN=0 to VCC(max)	-	-	±10	
Output Leakage Current		ILO	VOUT=0 to VCC(max)	-	-	±10	
Input High Voltage		VIH	-	0.8xVCC	-	VCC+0.3	V
Input Low Voltage		VIL	-	-0.3	-	0.2xVCC	
Output High Voltage Level		VOH	IOH=-400μA	VCC-0.3	-	-	
Output Low Voltage Level		VOL	IOL=2.1mA	-	-	0.4	
Output Low Current(R/B#)		IOL(R/B#)	VOL=0.45V	8	10	-	mA
erase/program lockout voltage		VLKO			1.9		V

Note: Value guaranteed by design and/or characterization, not 100% tested in production.

12. AC CHARACTERISTICS

12.1 Test Condition

(TA=-40℃~85℃/-40℃~105℃ VCC=1.7V~1.95V /2.7V~3.6V)

Parameter	GD9FS1G8F2A/GD9FU1G8F2A
Input Pulse Levels	0V to VCC
Input Rise and Fall Times	5ns
Input and Output Timing Levels	VCC/2
Output Load	1 TTL GATE and CL=30fF

12.2 Capacitance (TA=25°C, F=1.0MHz)

Parameter	Symbol	Test condition	Min	Max	Unit
Input/Output Capacitance	CI/O	VIL=0V	-	6	pF
Input Capacitance	CIN	VIN=0V	-	8	pF

Notes: Capacitance is periodically sampled and not 100% tested.

12.3 AC Timing Characteristics

Parameter	Symbol	3.3V		1.8V		
		Min	Max	Min	Max	
CE# setup time	tCS	15	-	15	-	ns
CE# hold time	tCH	5	-	5	-	ns
CLE setup time	tCLS	12	-	12	-	ns
CLE Hold time	tCLH	5	-	5	-	ns
ALE setup time	tALS	12	-	12	-	ns
ALE hold time	tALH	5	-	5	-	ns
Data setup time	tDS	12	-	12	-	ns
Data hold time	tDH	5	-	5	-	ns
Write cycle time	tWC	25	-	45	-	ns
WE# pulse width	tWP	12	-	22	-	ns
WE# high hold time	tWH	10	-	15	-	ns
Address to data loading time	tADL	70	-	70	-	ns
WE# high to busy	tWB	-	100	-	100	ns
Ready to WE# low	tRW	20	-	20	-	ns
Ready to RE# low	tRR	20	-	20	-	ns
CLE to RE# delay	tCLR	10	-	10	-	ns
ALE to RE# delay	tAR	10	-	10	-	ns
Read cycle time	tRC	25	-	45	-	ns
RE# pulse width	tRP	12	-	22	-	ns
RE# high hold time	tREH	10	-	15	-	ns
RE# access time	tREA	-	20	-	30	ns
CE# access time	tCEA	-	25	-	45	ns
RE# high to output high Z	tRHZ	-	100	-	100	ns
CE# high to output high Z	tCHZ	-	50	-	50	ns
CE# high to ALE or CLE Don’t care	tCSD	10	-	10	-	ns
CE# high to output hold	tCOH	15	-	15	-	ns
RE# high to output hold	tRHOH	15	-	15	-	ns
RE# low to output hold	tRLOH	3	-	3	-	ns
Output Hi-Z to RE# Low	tIR	0	-	0	-	ns
CE# low to RE# low	tCR	10	-	10	-	ns
RE# high to WE# low	tRHW	100	-	100	-	ns
WE# high to RE# low	tWHR	60	-	60	-	ns
Write protect time	tWW	100	-	100	-	ns

Note: 1. Typical value at T_A = 25℃.

2. Value guaranteed by design and/or characterization, not 100% tested in production.

12.4 Performance Characteristics

Parameter		Symbol	Min	Typ.	Max	Unit
Data transfer from cell to register		tR			25	us
Program Time		tPROG	-	300	700	μs
Read Cache busy time		tCBSYR		5	tR	μs
Cache Program short busy time		tCBSYW		5	700	μs
Number of Partial Program Cycles in the Same Page		NOP	-	-	4	cycles
Block Erase Time		tBERS	-	3	10	ms
Device resetting time	Read	tRST			10	us
	Program				20	us
	Erase				500	us

Note: 1.Typical value is measured at Vcc=3.3V, TA=25℃(3.3V Device) or Vcc=1.8 V, TA=25℃(1.8V Device).

2.Value guaranteed by design and/or characterization, not 100% tested in production.

13. PACKAGE INFORMATION

13.1 TSOPI-48

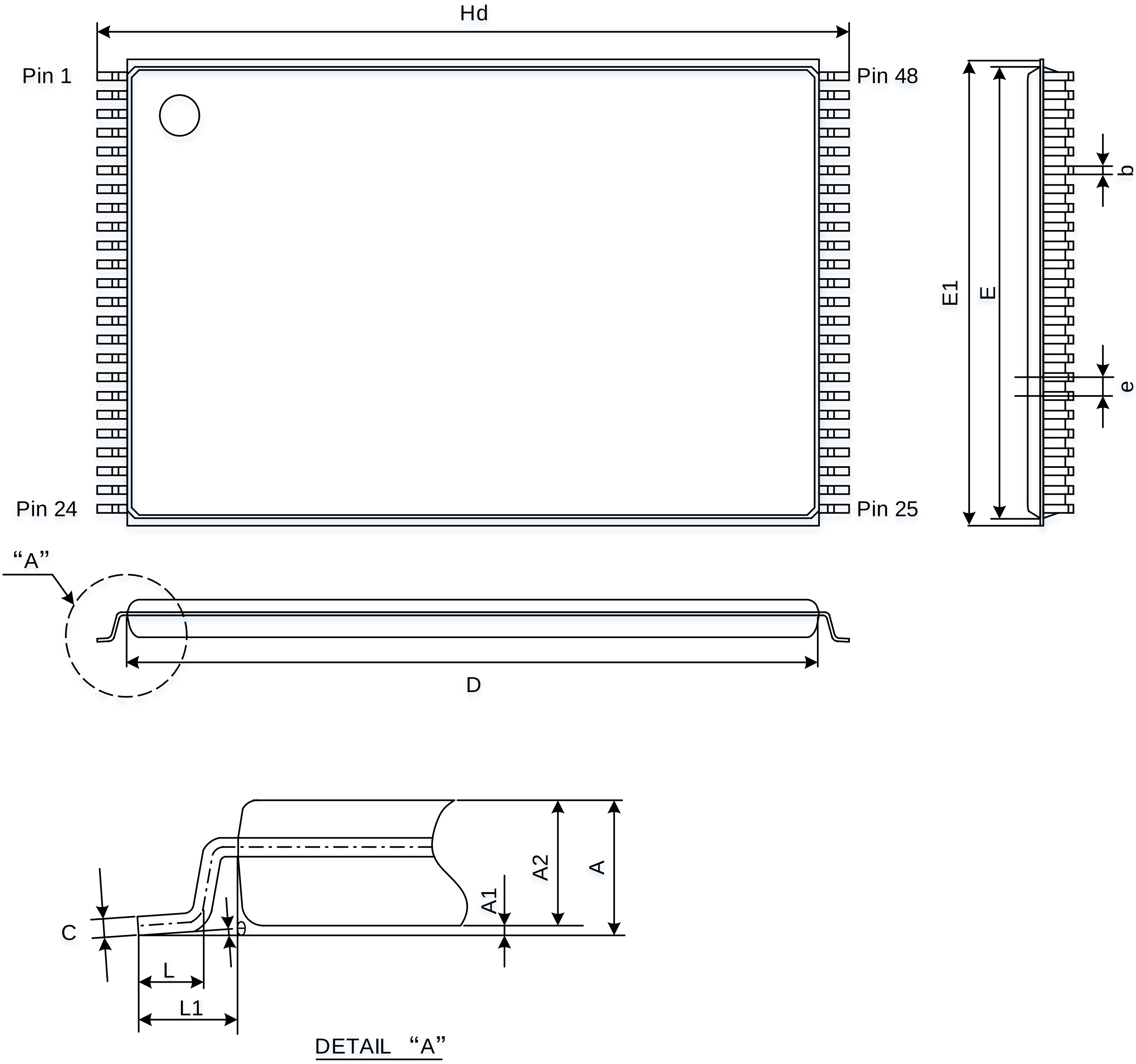


Figure 32: TSOPI-48 figures

Dimensions

Symbol / Unit		A	A1	A2	b	D	Hd	E	E1	e	L	L1	θ
mm	Min	-	0.05	0.90	0.14	18.30	19.80	11.90	-	0.50	0.425	0.60	0
	Nom	-	0.10	1.00	0.22	18.40	20.00	12.00	-		0.525	0.80	-
	Max	1.20	0.15	1.10	0.30	18.50	20.20	12.10	12.40		0.625	1.00	7

Note：

1. Tolerance of the dimension should be ±0.1 unless otherwise specified.
2. Corner radius should be less than ±0.1R unless otherwise specified (excluding outer lead).
3. Tolerance of the angles should be ±0.5 degree unless otherwise specified.
4. The mold surface should have a finish 8±2S without luster.
   Trace of knockout pin and the ahaded portion of detail “A” should be polish surface.
5. Discrepancies between upper and lower molding cavity should be less than 0.05 of the package.
6. Mold flash should be less than 0.2mm.

13.2 FBGA-63

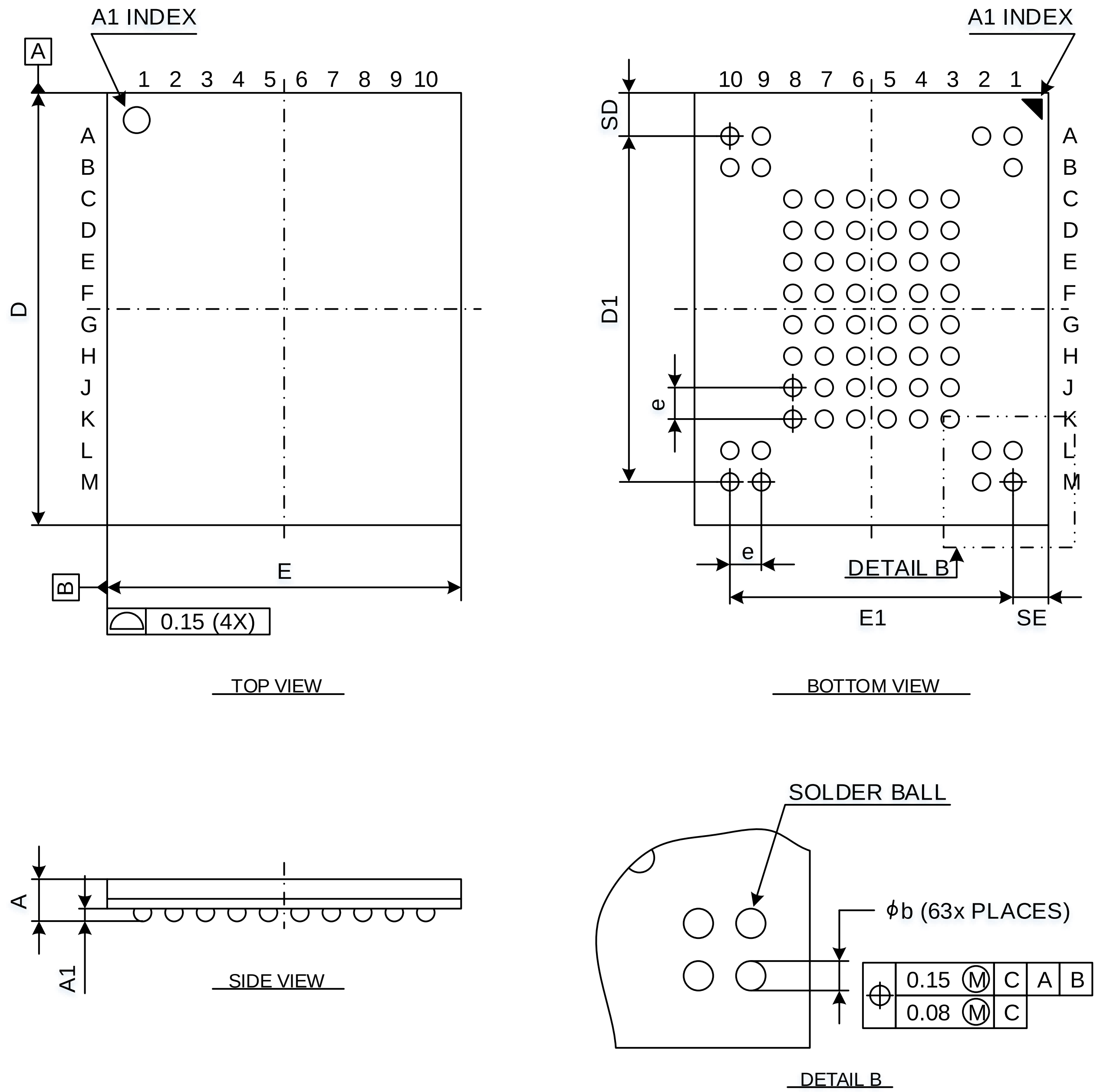


Figure 33: FBGA-63 figures

Dimensions

Symbol / Unit		A	A1	b	E	E1	D	D1	e	SD	SE
mm	Min	-	0.25	0.40	8.90	7.20 BSC	10.90	8.80 BSC	0.80 BSC	1.10 TYP	0.90 TYP
	Nom	-	0.30	0.45	9.00		11.00				
	Max	1.00	0.35	0.50	9.10		11.10				

Note：

1. Controlling dimension: millimeter.
2. Reference document: JEDEC MO-207
3. The diameter of pre-reflow solder ball is ø0.42mm (0.40mm SMO).

13.3 FBGA-48

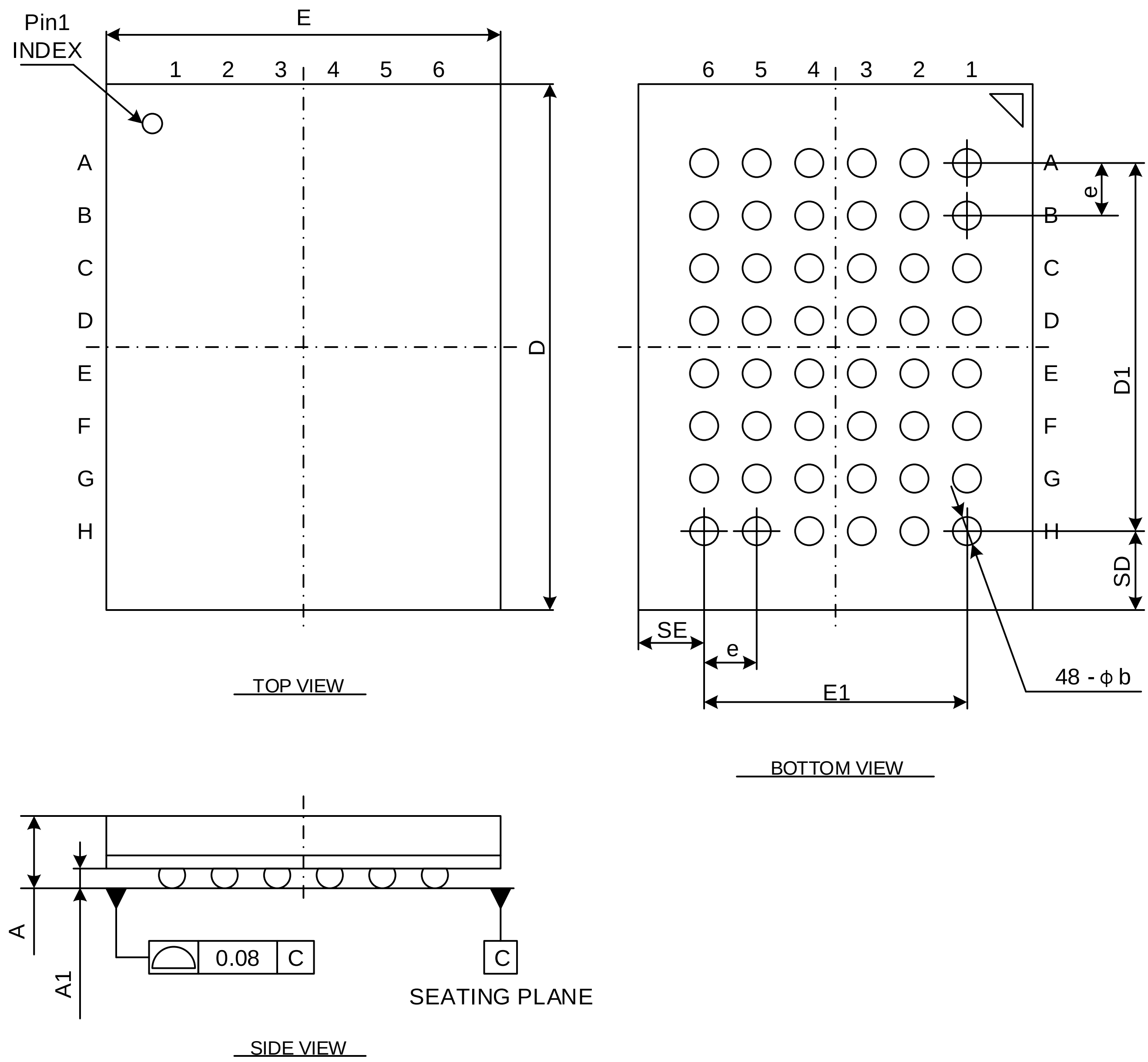


Figure 34: FBGA-48 figures

Dimensions

Symbol / Unit		A	A1	b	E	E1	D	D1	e	SD	SE
mm	Min	-	0.25	0.40	5.90	4.00 BSC	7.90	5.60 BSC	0.80 BSC	1.20 TYP	1.00 TYP
	Nom	-	0.30	0.45	6.00		8.00				
	Max	1.00	0.40	0.50	6.10		8.10				

Note：

1. Controlling dimension: millimeter.

14. Part Numbering Information

GD	9F	U	1G	8	F	2	A	M	G	I
1	2	3	4	5	6	7	8	9	10	11

1. GD

2. Memory Type

9F: Parallel NAND without Internal ECC

3. Power Supply

	V_{CCQ}	V_{CC}
U	2.7v ~ 3.6v	2.7v ~ 3.6v
S	1.7v ~ 1.95v	1.7v ~ 1.95v

4. Density:

1G: 1Gb
2G: 2Gb
4G: 4Gb
8G: 8Gb
AG: 16Gb

5. Organization

8: x8
6: x16

6. NAND Type:

F: SLC, 1Die, 1nCE, 1Rnb
E: SLC; 2Die, 1nCE, 1Rnb
D: SLC; 4Die, 1nCE, 1Rnb

7. Function Mode:

2: Spare size is 128bytes;
3: Spare size is 64bytes;
4: Spare size is 256bytes;

8. Process Generation:

A: A GEN
B: B GEN

9. Package

M: TSOPI-48
L: FBGA-63
W: Wafer
D: FBGA-48

10. Package Material & Packing

G: Lead & Halogen Free
W: Wafer

11. Temperature Grade

I: Industrial (-40C ~ 85℃)
F: Industrial+ (-40C ~ 85℃)
J: Industrial (-40C ~ 105℃)

Note: (1) Industrial+: F grade has implemented additional test flows to ensure higher product quality than I grade.

15. Revision History

Version No.	History Description	Date	Page
1.0	Update parameter page value Update package FBGA-63 information	2016-6-2	
1.1	Change page size from 2K+64 to 2K+128	2016-7-12	
1.2	Add CRC value in parameter page Remove tFEAT parameter Change Device resetting time for read from 5us to 10us Change Device resetting time for read from 10us to 20us Add parameter page CRC value table	2016-11-01	
1.3	Add parameter page CRC arithmetic related description Update CRC table value Update Package information according Package vendor final file.	2016-11-15	
1.4	Update R/B# Resistance figure with Trise and Tfall Update some figure with RD review.	2016-12-14	
1.5	Update Part Numbering Information Add F code at field “Temperature Grade” for Full Function Test for Automotive application and No AECQ	2017-02-27	
1.6	Remove last three code from part number	2017-06-26	
1.7	Change VOL Max. from 0.1 to 0.4 Change ISB Max. from 30 to 50 Change IOL(R/B#) test condition VOL from 0.4V to 0.45V Change description with “The addressing must be done in sequential order in a block” for page program	2017-10-31	
1.8	Add a note of P/E cycles with ECC Delete Commercial Temperature Grade. And add Industrial(J) (-40C ~ 105C) Temperature Grade	2017-11-14	
1.9	Change P/E cycles with ECC from 50k to 100k, and delete note. Delete Industrial+(F):-40C~85C	2017-11-27	
2.0	Change Operating Current Standby (Max.) from 30uA to 50uA Change VOH min from VCC-0.1 to VCC-0.3V Change Parameter page table Byte 105-106 ,108-109,and change CRC Value Change 1.8V tWP and tRP from 12 to 22, Change 1.8V tWH and tREH from 10 to 15 Change tCBSYW and tCBSYR from 3us to 5us Add the figure for Read Unique ID Timing.	2018-4-4	
2.1	Update the tf and tr value in Figure26 :Ready/Busy figures Modify the typo of reliability of program/erase cycles with ECC in chapter 2 Add part numbers of GD9FU1G6F2AMG and GD9FS1G6F2AMG in chapter2.1	2018-5-2	
2.2	Modify the description of Write Protect Add the chapter of 5.3 Factory Defect Mapping	2018-5-17	

2.3	Modify the description of Common Page Program command Modify the sequence diagram of Cache Program Operation command (figure 19)	2018-9-3	
2.4	Update the figures of TSOPI-48 and FBGA-63 packages Add package of FBGA-48	2018-10-11	
2.5	Modify the description of G4 ball in location figures of FBGA-63 package. Modify the description of E2 ball in location figures of FBGA-48 package.	2018-10-25	
2.6	Delete the description of initial power up, the first page of the first block has been read to cache in 8.1.1 Common Page Read. Modify the Total Thickness "A" of BGA63 Modify the Ball Size "b" and Ball thickness "A1" of BGA48. Update Important Notice	2019-4-3	18 50 51 55
2.7	Update Part Number Information	2019-5-15	53
2.8	Add Note of " Value guaranteed by design and/or characterization, not 100% tested in production. Update Figure 22: Common Block Erase Operation figures Modify error description Voltage on any pin relative to VSS VCC:3.3V -0.6~4.0/1.8V -0.6~2.5 Modify error description Voltage on any pin relative to VSS VIN/OUT -0.6 to VCC+0.4 Modify error description three Bytes row address in Figure 16: Cache Read Operation Add Figure 31: Input Test Waveform and Measurement Level	2021-11-01	45/47/48 26 43 43 21 43