GLS55LD040M
PATA NAND Controller

Fact Sheet 01.000
November 2011

Features

- **Industry Standard PATA Bus Interface**
  - Host Interface: 16-bit access
  - Supports up to PIO Mode-4
  - Supports up to Multi-Word DMA Mode-2
  - Supports up to Ultra DMA Mode-6
  - Supports 48-bit Address Feature Set
- **Interface for Standard NAND Flash Media**
  - Flash Media Interface: 8-bit per channel with 1, 2 or 4 channel options
    - Supports up to 16 flash media devices directly
    - Supports up to 64 flash media devices with external decoding logic
  - Supports Single-Level Cell (SLC) or Multi-Level Cell (MLC) flash media
  - Supports 4Kbyte and 8Kbyte program page size
    - Two-plane operation
- **Low Power, 3.3V Host and NAND Flash Media Interface**
- **Low Power Operation**
  - Active mode: 60mA (3.3V) (typical)
  - Sleep mode: 800uA (3.3V) (typical)
- **Power Management Unit**
  - Immediate disabling of unused circuitry without host intervention
  - Zero wake-up latency
- **Expanded Data Protection**
  - Added data security through user-selectable protection zones
- **20-Byte Unique ID for Enhanced Security**
  - Factory Pre-programmed 10-Byte Unique ID
  - User-Programmable 10-Byte ID
- **Programmable, Multi-tasking NAND Flash Media Interface**
- **Firmware Storage in Embedded Flash**
- **Pre-programmed Firmware**
  - Performs self-initialization on first system Power-on
  - Executes industry standard ATA/IDE commands
  - Implements advanced wear-leveling algorithms to substantially increase the longevity of flash media
  - Embedded Flash File System
- **Built-in Hardware ECC**
  - Corrects up to 12 random bits of error per 512-Byte sector; up to 24 random bits of error per 1-Kbyte sector
- **Internal or External System Clock**
- **Multi-tasking Technology enables Fast Sustained Read/Write Performance**
  - MLC NAND
    - Up to 105 MByte/sec Read, 73 MByte/sec Write (external clock)
    - Up to 92 MByte/sec Read, 73 MByte/sec Write (internal clock)
  - SLC NAND
    - Up to 109 MByte/sec Read/Write (external clock)
    - Up to 92 MByte/sec Read, 109 MByte/sec Write (internal clock)
- **Automatic Recognition and Initialization of Flash Media Devices**
  - Seamless integration into a standard SMT manufacturing process
- **Commercial and Industrial Temperature Range**
  - 0°C to 70°C for commercial operation
  - -40°C to 85°C for industrial operation
- **Package**
  - 12mm x 12mm x 1.17mm (maximum height), 145-ball, 0.8mm ball pitch, TFBGA (BZJE)
- **All Devices are RoHS Compliant**

Product Description

The Greenliant PATA NAND Controller is the heart of a high-performance, flash media-based data storage system. The NAND Controller recognizes the control, address and data signals on the ATA/IDE bus and translates them into memory accesses to the standard NAND-type flash media. The GLS55LD040M device supports Single-Level Cell (SLC) and Multi-Level Cell (MLC) flash media. This technology is ideal for solid state mass storage applications offering expanded functionality, flexible capacity scaling capabilities and lower power consumption.

The Greenliant PATA NAND Controller supports standard ATA/IDE protocols with up to PIO Mode-4, Multi-word DMA Mode-2, and Ultra DMA Mode-6 interface. It directly supports up to 16 flash media devices or, through simple decoding logic, supports up to 64 flash media devices.

The PATA NAND Controller uses Embedded Flash memory and is factory pre-programmed with a flash file system. Upon initial power-on, the PATA NAND Controller recognizes attached flash media devices, sets up a bad block table, executes all necessary handshaking routines for flash media support and performs the low level format.

For added manufacturing flexibility, system debug, re-initialization and user customization is accomplished through the ATA/IDE interface.

For confidential information stored in the flash media, the GLS55LD040M provides exceptional security protection. Four password-protected protection zones can be set to Read/Write, Read-only or Hidden (Read-disabled). The NAND Controller also provides a WP#/PD# pin to protect critical information stored in the flash media from unauthorized overwrites.

The GLS55LD040M is available in an industry-standard, 145-ball TFBGA package for easy integration into a surface mount technology manufacturing process.

1.0 GENERAL DESCRIPTION

The GLS55LD040M PATA NAND Controller contains a microcontroller and a flash file system integrated in a TFBGA package. Refer to Figure 2-1 for the PATA NAND Controller block diagram. The controller interfaces with the host system allowing data to be written to and read from the flash media.

1.1 Optimized PATA NAND Controller

The heart of the flash drive is the PATA NAND Controller which translates standard ATA signals into flash media data and control signals. The following components contribute to the PATA NAND Controller's operation.

1.1.1 Microcontroller Unit (MCU)

The 32 bit RISC MCU transfers the ATA/IDE commands into required flash media operations.

1.1.2 Internal Direct Memory Access (DMA)

The PATA NAND Controller uses internal DMA allowing instant data transfer from buffer to flash media. This implementation eliminates microcontroller overhead associated with the traditional, firmware-based approach, thereby increasing the data transfer rate.

1.1.3 Power Management Unit (PMU)

The power management unit controls the power consumption of the PATA NAND Controller. The PMU dramatically reduces the power consumption of the PATA NAND Controller by putting the part of the circuitry that is not in operation into sleep mode. The PMU is designed so that it has zero wake-up latency when using the internal clock.

1.1.4 SRAM Buffer

A contributor to the PATA NAND Controller performance is an SRAM buffer. The buffer optimizes the Host's data transfer from/to and to/from the flash media.

1.1.5 Embedded Flash File System

The embedded flash file system is an integral part of the PATA NANDrive. It contains MCU firmware that performs the following tasks:

1. Translates host side signals into flash media writes and reads
2. Provides advanced flash media wear leveling to spread the flash writes to increase the longevity of flash media
3. Keeps track of data file structures
4. Manages system security for the selected protection zones
5. Stores the data in Flash media upon completion of a Write command. The PATA NAND Controller does not perform Post-Write operations, except for when the Write cache is enabled by the Host command.

1.1.6 Media Interface Block (MIB)

The GLS55LD040M contains two Media Interface Blocks, MIB0 and MIB1. The MIB work independently to transfer data to and from the NAND Flash media. Each MIB controls two 8-bit channels.

Each Media Interface Block has three functions: DMA, ECC and Programmable Multi-tasking NAND Interface.

1.1.7 Programmable, Multi-tasking Interface

The multi-tasking interface enables fast, sustained write performance by allowing multiple Read, Program, and Erase operations to multiple flash media devices. The ease with which the NAND interface can be programmed enables the quick support of new NAND devices.

1.1.8 Error Correction Code (ECC)

The GLS55LD040M utilizes 24-bit, BCH Error detection Code (EDC) and Error Correction Code (ECC) algorithms. The ECC engine can provide, depending on settings, 6 or 12 bits of ECC for each 512-Byte block of data, and 12 or 24 bits of ECC for each 1KByte of data.

The ECC encoding and decoding operations occur during the data transfer.

1.1.9 Serial Communication Interface (SCI)

The Serial Communication Interface (SCI) is designed to provide trace information during debugging processes. To aid in validation, always provide the SCI access to PCB design.

1.1.10 External Clock

The GLS55LD040M supports an external clock interface (XCLKI) that is enabled, or disabled, by the external clock enable (XCLKEN) input signal. With a 4.7K ohm pull-down resistor connected to the XCLKEN pin, and a 6.0 MHz external oscillator or clock source present at the XCLKI input pin, the GLS55LD040M uses the external oscillator as the internal clock reference.

2.0 FUNCTIONAL BLOCKS

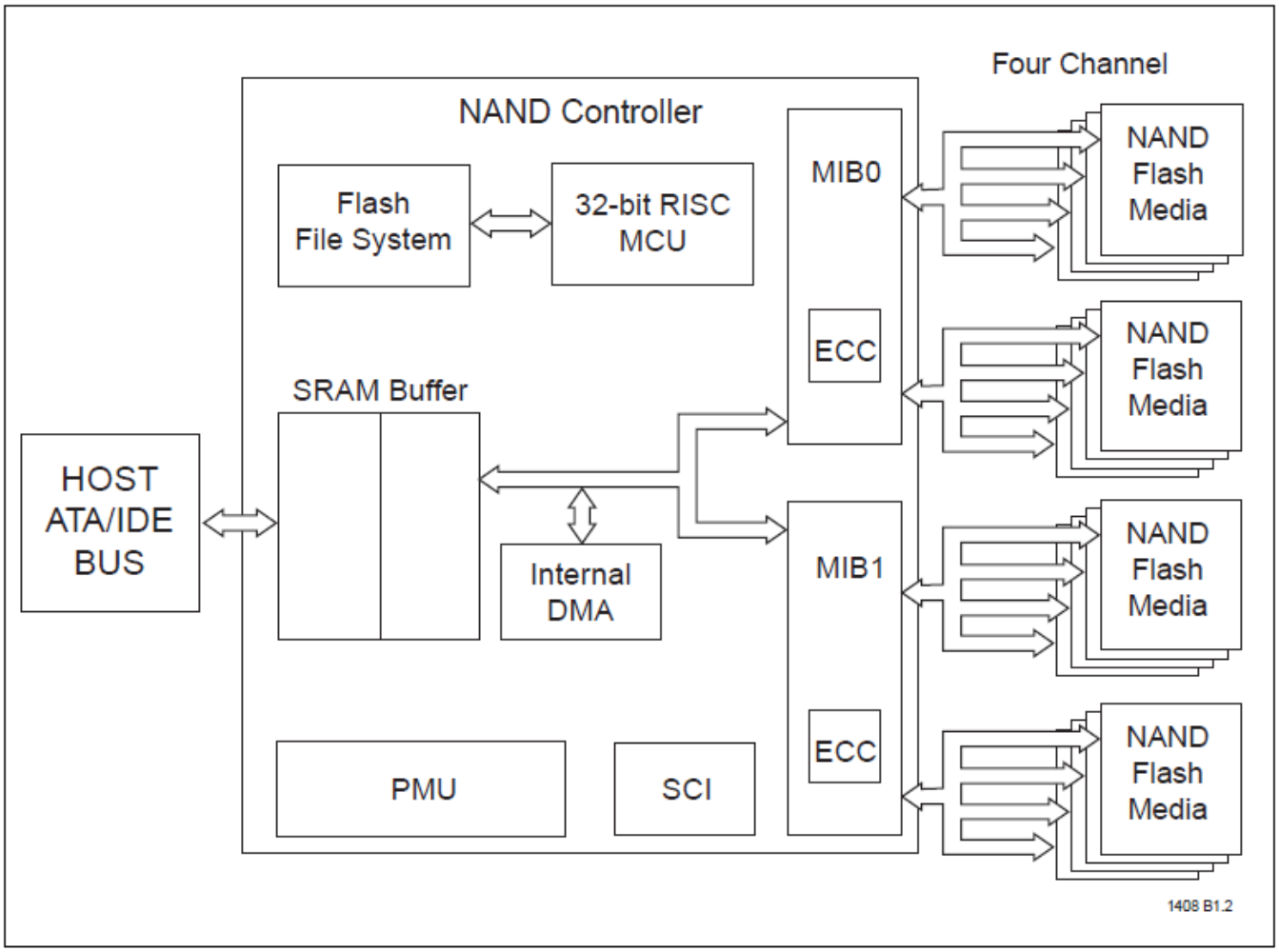


Figure 2-1: PATA NAND Controller Block Diagram

3.0 PIN ASSIGNMENTS

The signal/pin assignments are listed in Table 3-1. Low active signals have a "#" suffix. Pin types are Input, Output, or Input/Output. Signals whose source is the Host are designated as inputs while signals that the PATA NAND Controller sources are outputs. The PATA NAND Controller functions in ATA mode, which is compatible with IDE hard disk drives.

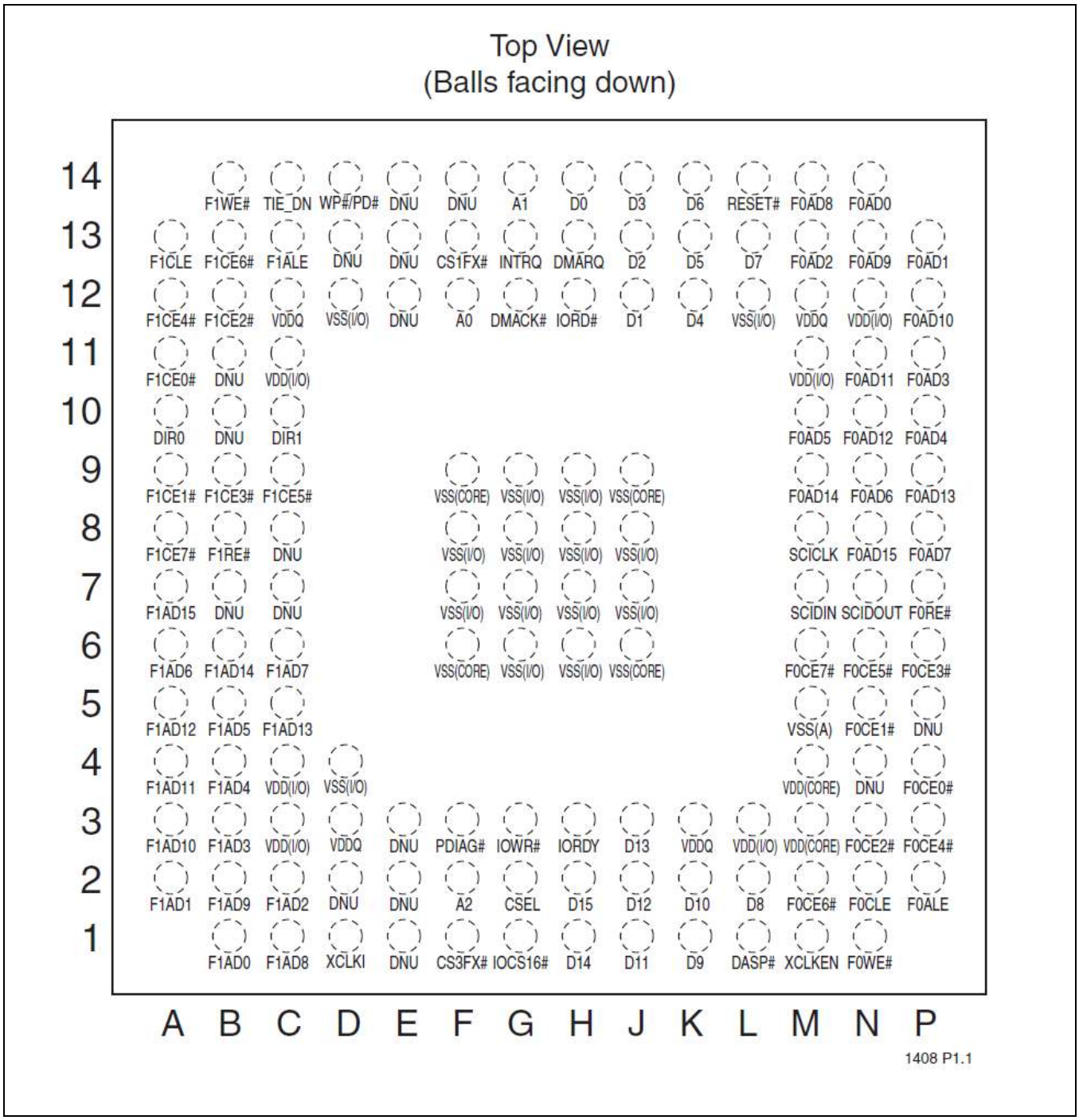


Figure 3-1: Pin Assignments for 145-Ball TFBGA

Table 3-1: Pin Assignments (1 of 4)

Symbol	Pin No. 145-Ball	Pin Type	I/O Type	Name and Functions
Host Side Interface				
A2	F2	I	I1Z	A[2:0] are used to select one of eight registers in the Task File.
A1	G14			
A0	F12			
D15	H2	I/O	I1Z/O2	D[15:0] Data bus
D14	H1			
D13	J3			
D12	J2			
D11	J1			
D10	K2			
D9	K1			
D8	L2			
D7	L13			
D6	K14			
D5	K13			
D4	K12			
D3	J14			
D2	J13			
D1	J12			
D0	H14			
DMACK#	G12	I	I2U	DMA Acknowledge - input from Host
DMARQ	H13	O	O2	DMA Request to Host
CS1FX#	F13	I	I2Z	CS1FX# is the chip select for the task file registers
CS3FX#	F1			CS3FX# is used to select the Alternate Status register and the Device Control register.
CSEL	G2	I	I1U	This internally pulled-up signal is used to configure this device as a Master or a Slave. When this pin is grounded, this device is configured as a Master. When the pin is open, or tied to V_{DDQ}, this device is configured as a Slave. The pin setting should remain the same from Power-on to Power-down.
IORD#	H12	I	I2Z	IORD#: This is an I/O Read Strobe generated by the Host. When Ultra DMA mode is not active, this signal gates I/O data from the device. (This pin supports three functions)
				HDMARDY#: In Ultra DMA mode when DMA Read is active, this signal is asserted by the Host to indicate that the Host is ready to receive Ultra DMA data-in bursts. The Host may negate HDMARDY# to pause an Ultra DMA transfer.
				HSTROBE: When DMA Write is active, this signal is the data-out strobe generated by the Host. Both the rising and falling edges of HSTROBE cause data to be latched by the device. The Host may stop generating HSTROBE edges to pause an Ultra DMA data-out burst.
IOWR#	G3	I	I2Z	IOWR#: This is an I/O Write Strobe generated by the Host. When Ultra DMA mode is not active, this signal is used to clock I/O data into the device. (This pin supports two functions)
				STOP: When Ultra DMA mode protocol is active, the assertion of this signal causes the termination of the Ultra DMA burst

Table 3-1: Pin Assignments (2 of 4)

Symbol	Pin No. 91-Ball	Pin Type	I/O Type	Name and Functions
IORDY	H3	O	O2	IORDY: When in PIO mode, the device is not ready to respond to a data transfer request. This signal is negated to extend the Host transfer cycle from the assertion of IORD# or IOWR#. However, it is never negated by this controller. (This pin supports three functions) DDMARDY#: When Ultra DMA mode DMA Write is active, this signal is asserted by the device to indicate that the device is ready to receive Ultra DMA data-out bursts. The device may negate DDMARDY# to pause an Ultra DMA transfer. DSTROBE: When Ultra DMA mode DMA Write is active, this signal is the data-in strobe generated by the device. Both the rising and falling edges of DSTROBE cause data to be latched by the Host. The device may stop generating DSTROBE edges to pause an Ultra DMA data-in burst.
IOCS16#	G1	O	O3	This output signal is asserted low when the device is indicating a Word data transfer cycle.
INTRQ	G13	O	O2	Ready/Busy or Interrupt Request to the host.
PDIAG#	F3	I/O	I1U/O2	The Pass Diagnostic signal in the Master/Slave handshake protocol.
DASP#	L1	I/O	I1U/O4	The Drive Active/Slave Present signal in the Master/Slave handshake protocol.
RESET#	L14	I	I2U	This input pin is the active low hardware reset from the Host.
Flash Media Interface [1)]				
F0RE#	P7	O	O7	Active Low Flash Media Chip Read [MIB0]
F0WE#	N1			Active Low Flash Media Chip Write [MIB0]
F0CLE	N2	O	O6	Active High Flash Media Chip Command Latch Enable [MIB0]
F0ALE	P2			Active High Flash Media Chip Address Latch Enable [MIB0]
F0AD15	N8	I/O	I3U/O6	Flash Media Chip High Byte Address/Data Bus pins [MIB0]
F0AD14	M9			
F0AD13	P9			
F0AD12	N10			
F0AD11	N11			
F0AD10	P12			
F0AD9	N13			
F0AD8	M14			
F0AD7	P8			Flash Media Chip Low Byte Address/Data Bus pins [MIB0]
F0AD6	N9			
F0AD5	M10			
F0AD4	P10			
F0AD3	P11			
F0AD2	M13			
F0AD1	P13			
F0AD0	N14			
F0CE7#	M6	O	O5	Active Low Flash Media Chip Enable pin [MIB0]
F0CE6#	M2			
F0CE5#	N6			
F0CE4#	P3			
F0CE3#	P6			
F0CE2#	N3			
F0CE1#	N5			
F0CE0#	P4			
F1RE#	B8	O	O7	Active Low Flash Media Chip Read [MIB1]
F1WE#	B14			Active Low Flash Media Chip Write [MIB1]
F1CLE	A13	O	O6	Active High Flash Media Chip Command Latch Enable [MIB1]
F1ALE	C13			Active High Flash Media Chip Address Latch Enable [MIB1]

Table 3-1: Pin Assignments (3 of 4)

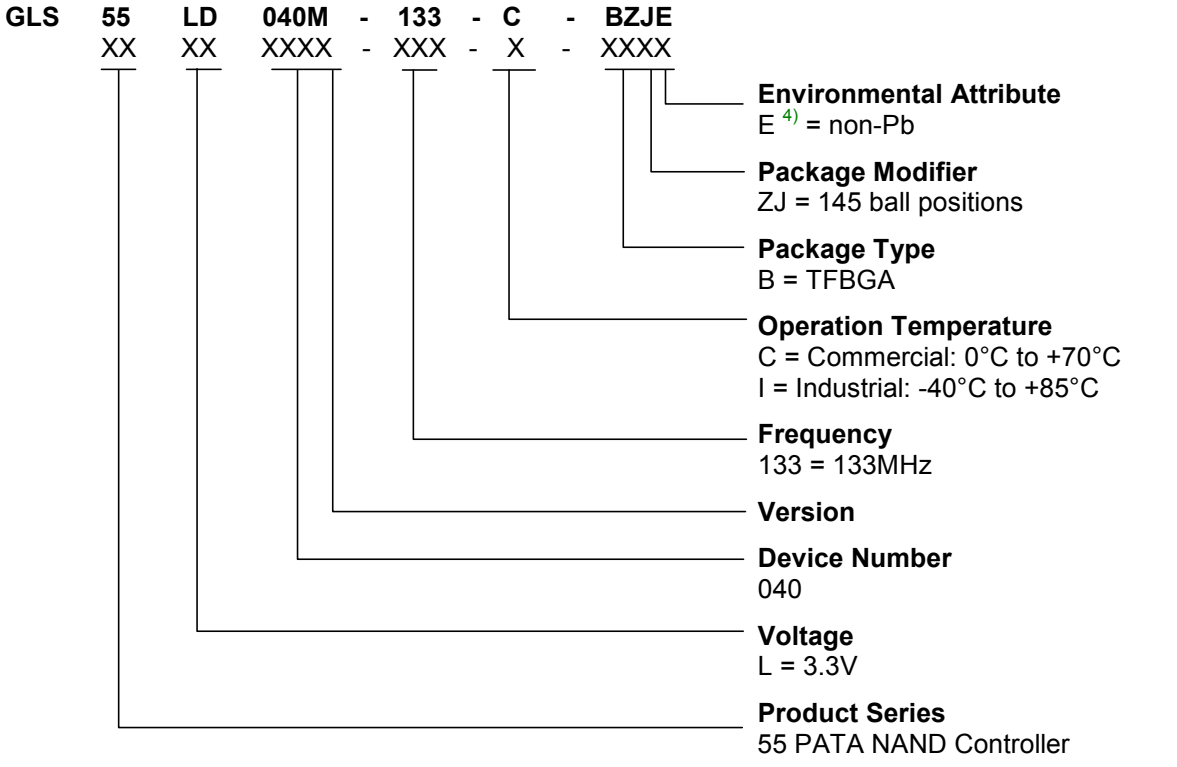
Symbol	Pin No. 91-Ball	Pin Type	I/O Type	Name and Functions
F1AD15	A7	I/O	I3U/O6	Flash Media Chip High Byte Address/Data Bus pins [MIB1]
F1AD14	B6			
F1AD13	C5			
F1AD12	A5			
F1AD11	A4			
F1AD10	A3			
F1AD9	B2			
F1AD8	C1			
F1AD7	C6			Flash Media Chip Low Byte Address/Data Bus pins [MIB1]
F1AD6	A6			
F1AD5	B5			
F1AD4	B4			
F1AD3	B3			
F1AD2	C2			
F1AD1	A2			
F1AD0	B1			
F1CE7#	A8	O	O5	Active Low Flash Media Chip Enable pin [MIB1]
F1CE6#	B13			
F1CE5#	C9			
F1CE4#	A12			
F1CE3#	B9			
F1CE2#	B12			
F1CE1#	A9			
F1CE0#	A11			
DIR0	A10	O	O6	Bus direction of external decoder for MIB0 group of NAND [2)]
DIR1	C10			Bus direction of external decoder for MIB1 group of NAND [2)]
Serial Communication Interface (SCI)				
$SCID_{OUT}$	N7	O	O6	SCI data output. No external pull-up or pull-down resistor should connect to this signal.
$SCID_{IN}$	M7	I	I3U	SCI data input
SCICLK	M8	I	I3D	SCI clock
Miscellaneous				
TIE_DN	C14			Pin needs to be connected to Vss
V_{SS} (IO)	D4, D12, F7, F8, G6, G7, G8, G9, H6, H7, H8, H9, J7, J8, L12	PWR		Ground for I/O
V_{SS} (Core)	F6, F9, J6, J9	PWR		Ground for Core
V_{SS} (A)	M5	PWR		Analog ground
V_{DD} (IO)	C3, C4, C11, L3, M11, N12	PWR		3.3V for Media interface and SCI
V_{DD} (Core)	M3, M4	PWR		V_{DD} (3.3V) Power Supply
V_{DDQ}	C12, D3, K3, M12	PWR		3.3V for Host interface
XCLKEN	M1	O	I3U/O5	External clock enable. Selects the internal or external clock source. The NAND Controller defaults to the internal clock source when XCLKEN is not connected, and XCLKI is connected to Vss. For assistance using external clock source, please contact Greenliant sales.
XCLKI	D1	I	I4Z	External clock input. This pin should not be left unconnected in any mode. When using the default internal clock, connect this pin to GND.

Table 3-1: Pin Assignments (4 of 4)

Symbol	Pin No. 91-Ball	Pin Type	I/O Type	Name and Functions
WP#/PD#	D14	I	I4U	The WP#/PD# pin can be used for either the Write Protect mode or Power-down mode, but only one mode is active at any time. The Write Protect or Power-down modes can be selected through the host command. The Write Protect mode is the factory default setting. This pin accepts only in the 3.3V V_{DD} signal level.
DNU [3)]	B7, B10, B11, C7, C8, D2, D13, E1, E2, E3, E12, E13, E14, F14, N4, P5			Do not use, must be left unconnected.

1) MIB0 and MIB1 operations are mutually exclusive. Do not mix the two groups' signals or FxCE#.
2) To support up to 64 flash media devices.
3) All DNU pins should not be connected.

4.0 Product Ordering Information



4) Environmental suffix "E" denotes non-Pb solder. Greenliant non-Pb solder devices are "RoHS Compliant."

Valid Combinations 5)

PATA NAND Controller Product
GLS55LD040M-133-C-BZJE
GLS55LD040M-133-I-BZJE

5) Valid product combinations are those that are in the mass production or will be in the mass production. Consult your Greenliant sales representative to confirm availability of the valid combinations and to determine availability of new product combinations.

4.1 Packaging Diagram

4.1.1 BZJE Package

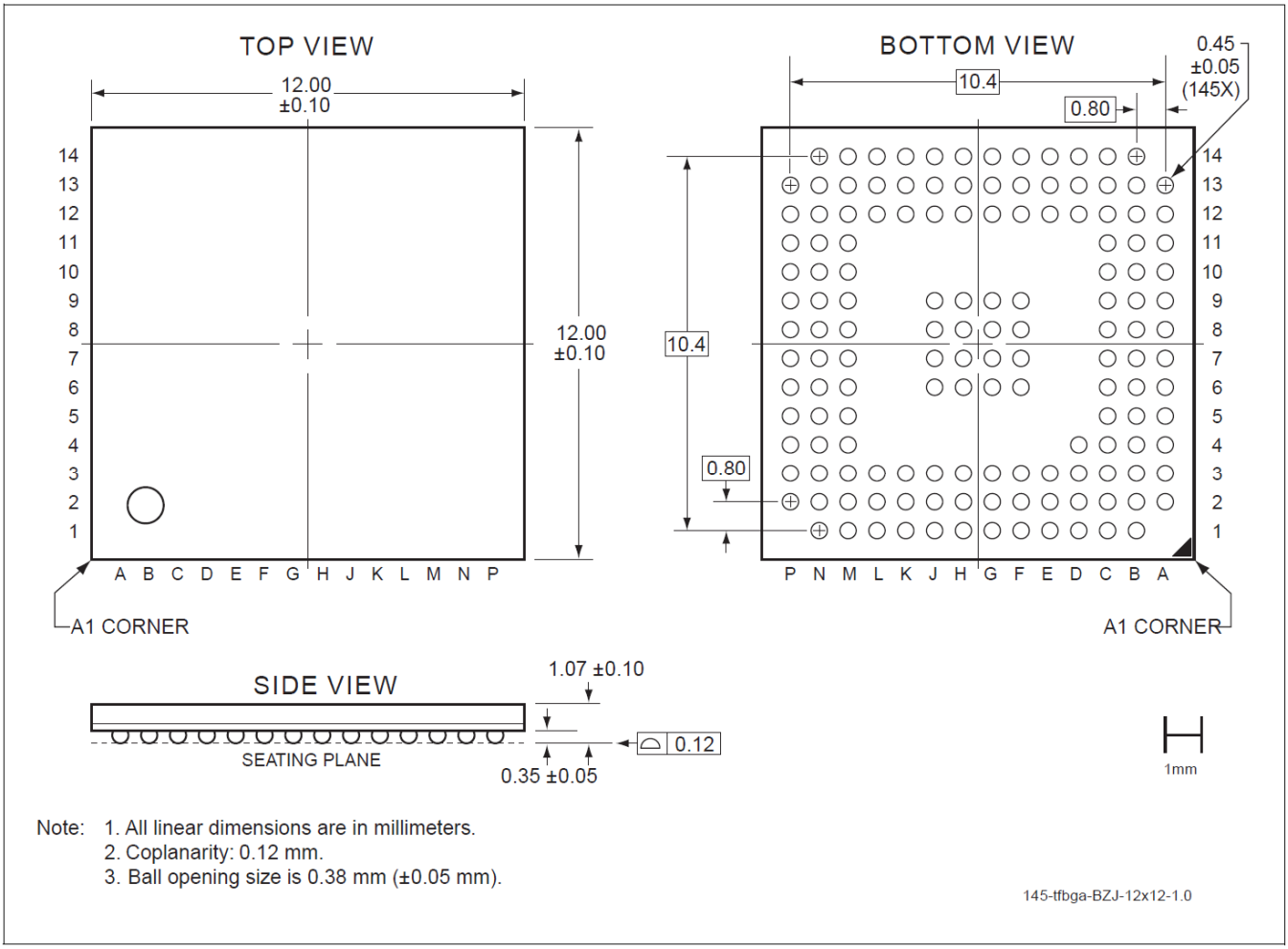


Figure 4-1: PATA NAND Controller 145-Ball, Thin-profile Fine-pitch Ball Grid Array (TFBGA)
Greenliant Package Code: BZJE