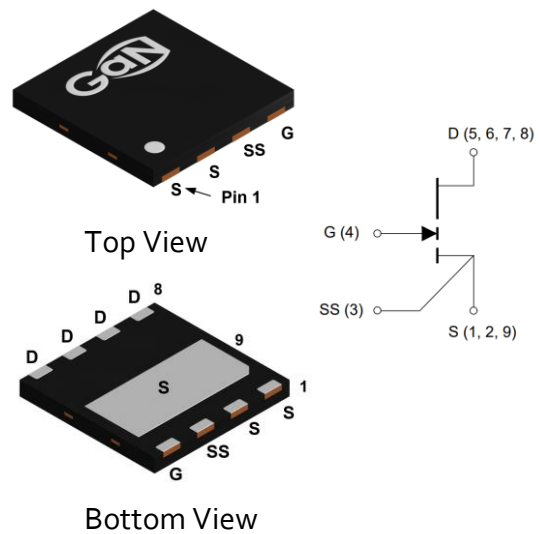


## Features

- 650 V enhancement mode power transistor
- 850 V transient drain-to-source voltage
- Bottom-cooled, 8x8 mm PDFN package
- $R_{DS(on)} = 78 \text{ m}\Omega$
- $I_{D(smax,DC)} = 18 \text{ A} / I_{D(smax,Pulse)} = 35 \text{ A}$
- Simple gate drive requirements (0 V to 6 V)
- Transient tolerant gate drive (-20 V / +10 V)
- High switching frequency (> 1 MHz)
- Fast and controllable fall and rise times
- Reverse conduction capability
- Zero reverse recovery loss
- Source Sense (SS) pin for optimized gate drive
- RoHS 3 (6+4) compliant



## Applications

- Consumer and Industrial Power Supplies
- Power Adapters
- LED Lighting Drivers
- Fast Battery Charging
- Power Factor Correction
- Appliance and Industrial Motor Drives
- Wireless Power Transfer

## Description

The GS-065-018-2-L is a 650V enhancement mode GaN-on-Silicon power transistor. The properties of GaN allow for high current, high voltage breakdown and high switching frequency. GaN Systems innovates with industry leading advancements such as patented **Island Technology®** cell layout which realizes high-current die and high yield. The GS-065-018-2-L is a bottom-side cooled transistor that offers low junction-to-case thermal resistance for demanding high power applications. These features combine to provide very high efficiency power switching.

### Absolute Maximum Ratings ( $T_{case} = 25\text{ °C}$ except as noted)

Parameter	Symbol	Value	Unit
Operating Junction Temperature	$T_J$	-55 to +150	°C
Storage Temperature Range	$T_S$	-55 to +150	°C
Drain-to-Source Voltage	$V_{DS}$	650	V
Drain-to-Source Voltage – transient	$V_{DS(transient)}$	850	V
Gate-to-Source Voltage	$V_{GS}$	-10 to +7	V
Gate-to-Source Voltage – transient (Note 1)	$V_{GS(transient)}$	-20 to +10	V
Continuous Drain Current ( $T_{case} = 25\text{ °C}$ )	$I_{DS}$	18	A
Continuous Drain Current ( $T_{case} = 100\text{ °C}$ )	$I_{DS}$	12	A
Pulse Drain Current (Pulse width 10 $\mu$ s, $V_{GS} = 6\text{ V}$ ) (Note 2)	$I_{DS\ Pulse}$	35	A

(1) For  $\leq 100\ \mu$ s

(2) Defined by product design and characterization. Value is not tested to full current in production.

### Thermal Characteristics (Typical values unless otherwise noted)

Parameter	Symbol	Value	Units
Thermal Resistance (junction-to-case) – bottom side	$R_{\theta JC}$	1.24	°C / W
Thermal Resistance (junction-to-ambient) (Note 3)	$R_{\theta JA}$	36	°C / W
Maximum Soldering Temperature (MSL3 rated)	$T_{SOLD}$	260	°C

(3) Device mounted on 1.6 mm PCB thickness FR4, 4-layer PCB with 2 oz. copper on each layer. The recommendation for thermal via under the thermal pad is 0.3 mm diameter (12 mil) with 0.635 mm pitch (25 mil). The copper layers under the thermal pad and drain pad are 25 x 25 mm<sup>2</sup> each. The PCB is mounted in horizontal position without air stream cooling.

### Ordering Information

Ordering code	Package type	Packing method	Qty	Reel Diameter	Reel Width
GS-065-018-2-L-TR	8x8 mm PDFN	Tape-and-Reel	3000	13" (330 mm)	16 mm
GS-065-018-2-L-MR	8x8 mm PDFN	Mini-Reel	250	7" (180 mm)	16 mm

**Electrical Characteristics** (Typical values at  $T_J = 25\text{ }^\circ\text{C}$ ,  $V_{GS} = 6\text{ V}$  unless otherwise noted)

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Drain-to-Source Blocking Voltage	$V_{(BL)DSS}$	650			V	$V_{GS} = 0\text{ V}$ , $I_{DSS} \leq 35\text{ }\mu\text{A}$
Drain-to-Source On Resistance	$R_{DS(on)}$		78	110	m $\Omega$	$V_{GS} = 6\text{ V}$ , $T_J = 25\text{ }^\circ\text{C}$ $I_{DS} = 5.5\text{ A}$
Drain-to-Source On Resistance	$R_{DS(on)}$		197		m $\Omega$	$V_{GS} = 6\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ $I_{DS} = 5.5\text{ A}$
Gate-to-Source Threshold	$V_{GS(th)}$	1.1	1.7	2.6	V	$V_{DS} = V_{GS}$ , $I_{DS} = 4.8\text{ mA}$
Gate-to-Source Current	$I_{GS}$		110		$\mu\text{A}$	$V_{GS} = 6\text{ V}$ , $V_{DS} = 0\text{ V}$
Gate Plateau Voltage	$V_{plat}$		3.5		V	$V_{DS} = 400\text{ V}$ , $I_{DS} = 18\text{ A}$
Drain-to-Source Leakage Current	$I_{DSS}$		1.2	35	$\mu\text{A}$	$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ $T_J = 25\text{ }^\circ\text{C}$
Drain-to-Source Leakage Current	$I_{DSS}$		42		$\mu\text{A}$	$V_{DS} = 650\text{ V}$ , $V_{GS} = 0\text{ V}$ $T_J = 150\text{ }^\circ\text{C}$
Internal Gate Resistance	$R_G$		1.3		$\Omega$	$f = 5\text{ MHz}$ , open drain
Input Capacitance	$C_{ISS}$		132		pF	$V_{DS} = 400\text{ V}$ $V_{GS} = 0\text{ V}$ $f = 100\text{ kHz}$
Output Capacitance	$C_{OSS}$		34		pF	
Reverse Transfer Capacitance	$C_{RSS}$		0.4		pF	
Effective Output Capacitance Energy Related (Note 4)	$C_{O(ER)}$		58		pF	$V_{GS} = 0\text{ V}$ $V_{DS} = 0\text{ to }400\text{ V}$
Effective Output Capacitance Time Related (Note 5)	$C_{O(TR)}$		90		pF	
Total Gate Charge	$Q_G$		4		nC	$V_{GS} = 0\text{ to }6\text{ V}$ $V_{DS} = 400\text{ V}$
Gate-to-Source Charge	$Q_{GS}$		1.2		nC	
Gate-to-Drain Charge	$Q_{GD}$		1.2		nC	
Output Charge	$Q_{OSS}$		37		nC	$V_{GS} = 0\text{ V}$ , $V_{DS} = 400\text{ V}$
Reverse Recovery Charge	$Q_{RR}$		0		nC	

(4)  $C_{O(ER)}$  is the fixed capacitance that would give the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 V to the stated  $V_{DS}$ .

(5)  $C_{O(TR)}$  is the fixed capacitance that would give the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 V to the stated  $V_{DS}$ .

**Electrical Characteristics cont'd** (Typical values at  $T_J = 25\text{ }^\circ\text{C}$ ,  $V_{GS} = 6\text{ V}$  unless otherwise noted)

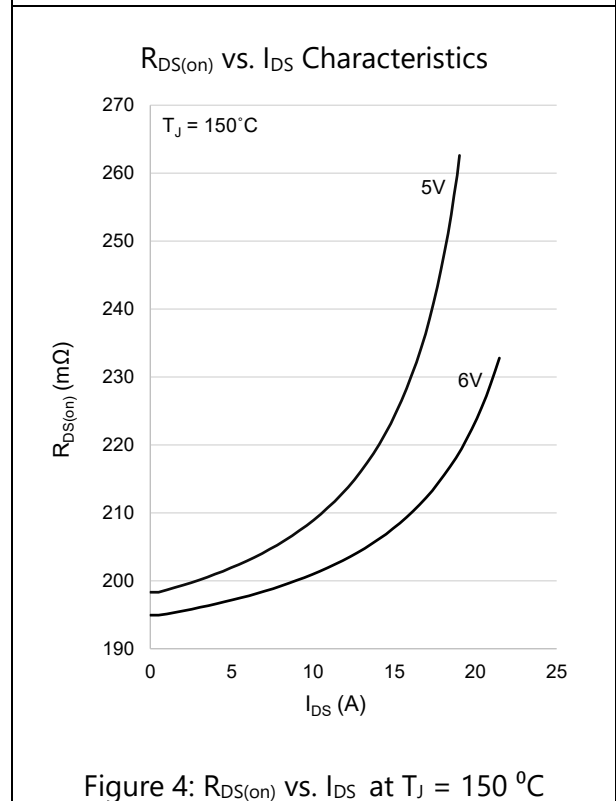
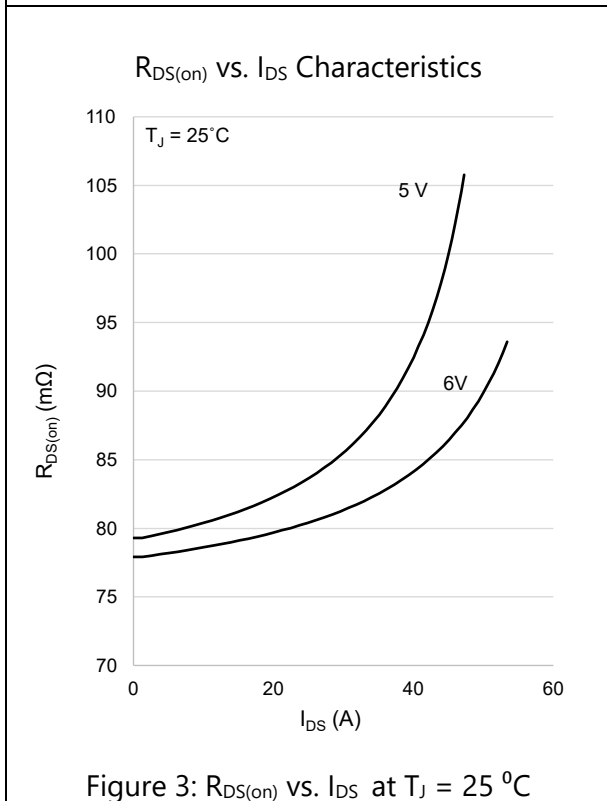
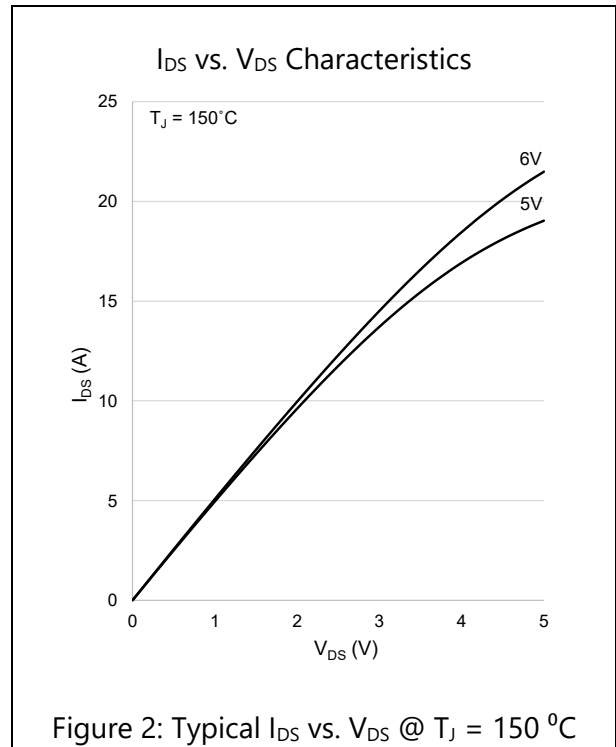
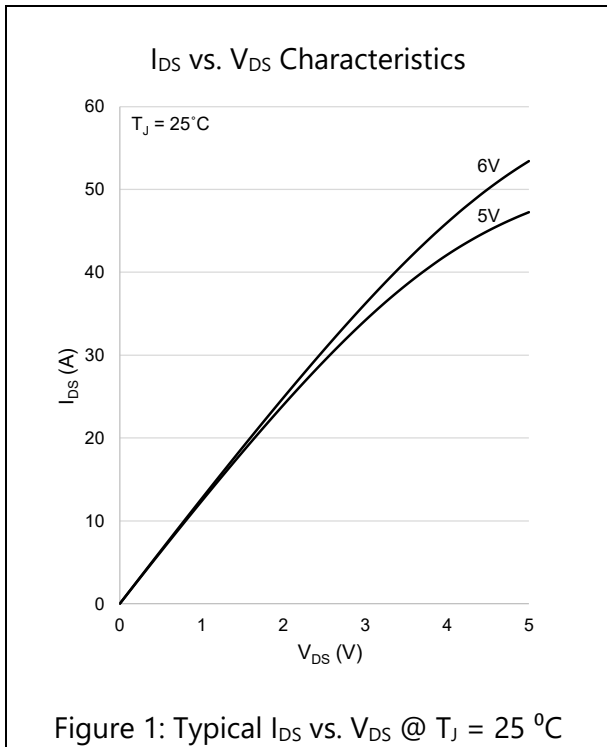
Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Turn-On Delay	$t_{D(on)}$		1.5		ns	$V_{DD} = 400\text{ V}$ , $V_{GS} = +6/-3\text{ V}$ , $I_{DS} = 10\text{ A}$ , $R_{G(on)} = 10\ \Omega$ , $R_{G(off)} = 2\ \Omega$ , $L = 110\ \mu\text{H}$ , $L_P = 12\ \text{nH}$ (Notes 6, 7, 8)
Rise Time	$t_R$		5.0		ns	
Turn-Off Delay	$t_{D(off)}$		2.9		ns	
Fall Time	$t_F$		4.8		ns	
Switching Energy during turn-on	$E_{on}$		16.4		$\mu\text{J}$	
Switching Energy during turn-off	$E_{off}$		7.5		$\mu\text{J}$	
Output Capacitance Stored Energy	$E_{OSS}$		4.6		$\mu\text{J}$	$V_{DS} = 400\text{ V}$ $V_{GS} = 0\text{ V}$ , $f = 100\text{ kHz}$

(6) See Figure 16 for switching test circuit diagram.

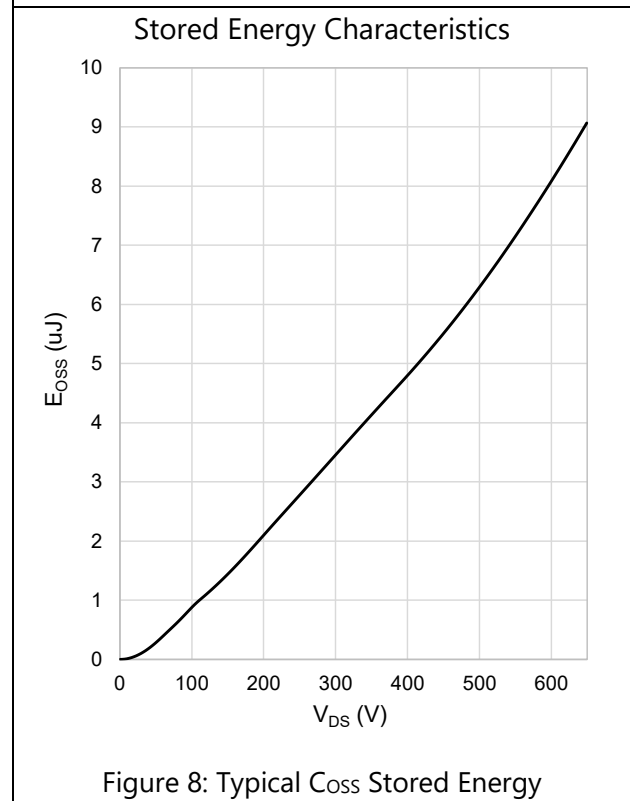
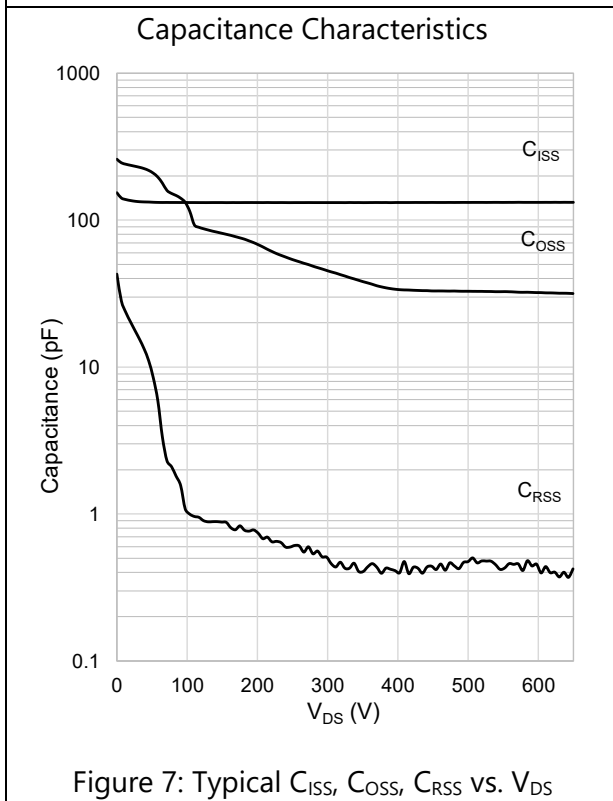
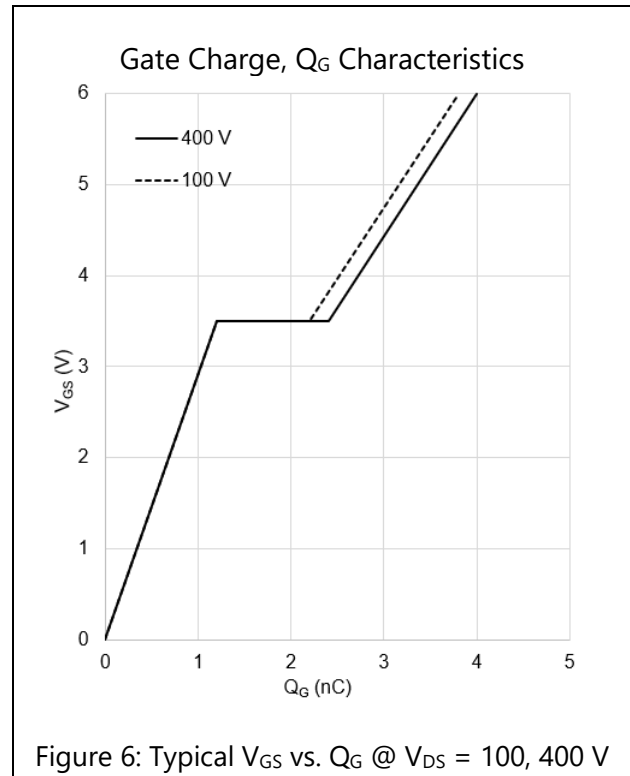
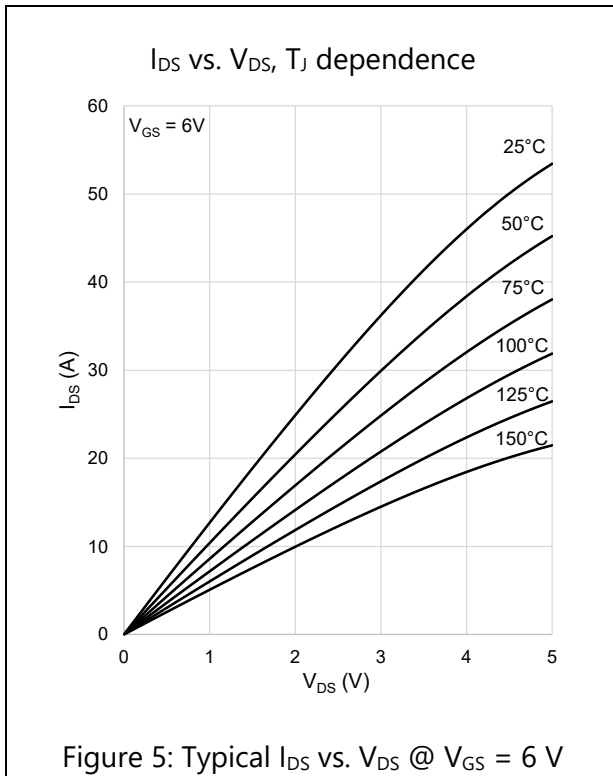
(7) See Figure 17 for switching time definition waveforms.

(8)  $L_P$  = parasitic inductance.

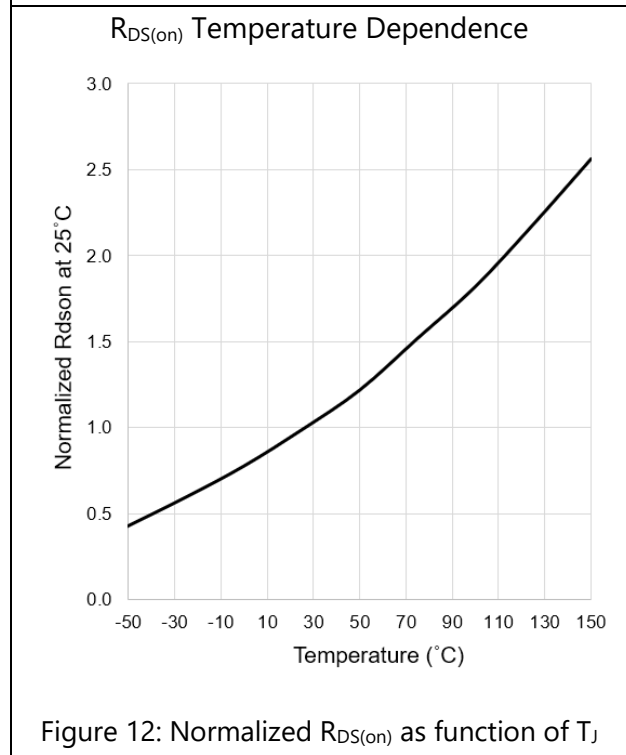
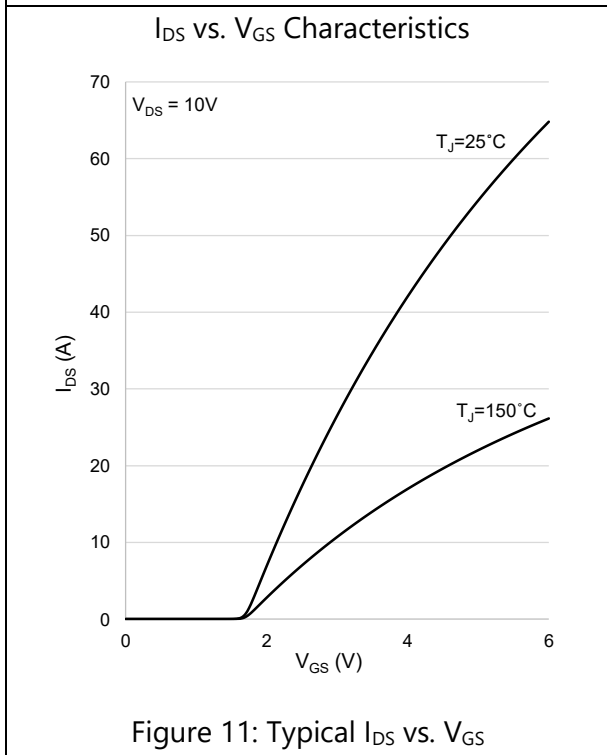
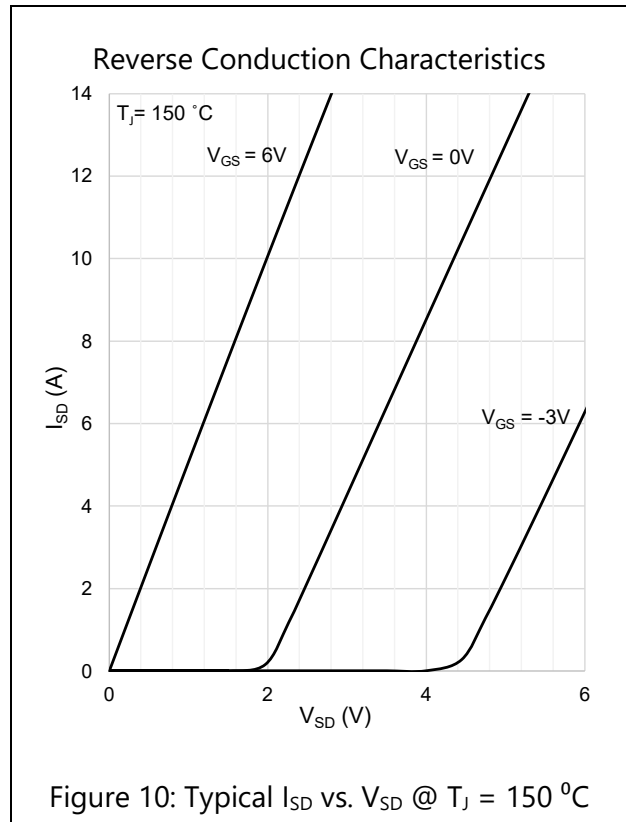
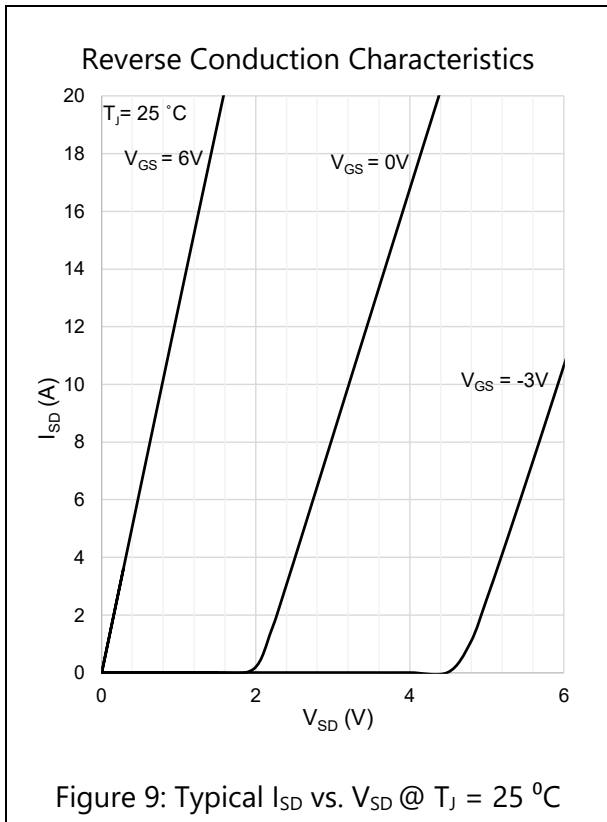
Electrical Performance Graphs



Electrical Performance Graphs



Electrical Performance Graphs



Thermal Performance Graphs

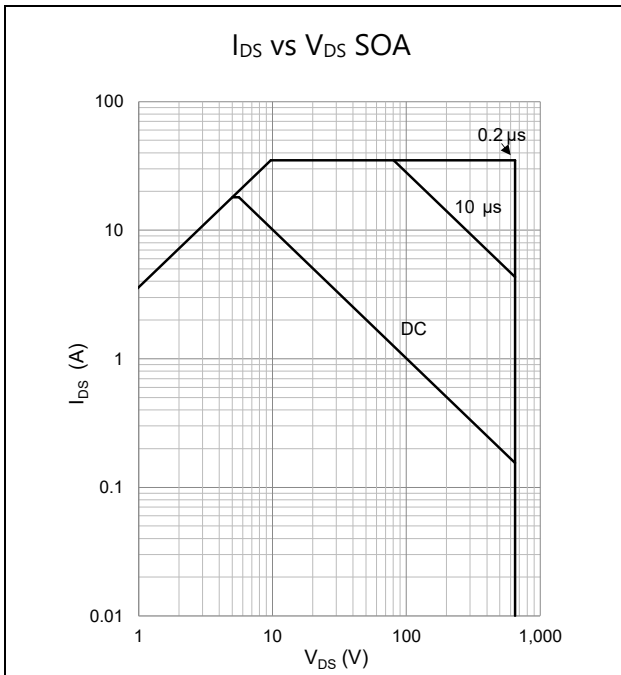


Figure 13: Safe Operating Area @  $T_{case} = 25^{\circ}C$

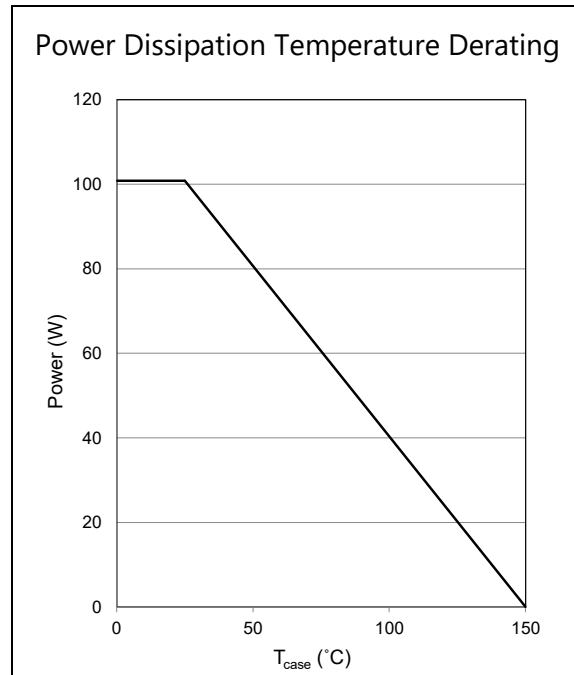


Figure 14: Derating vs. Case Temperature

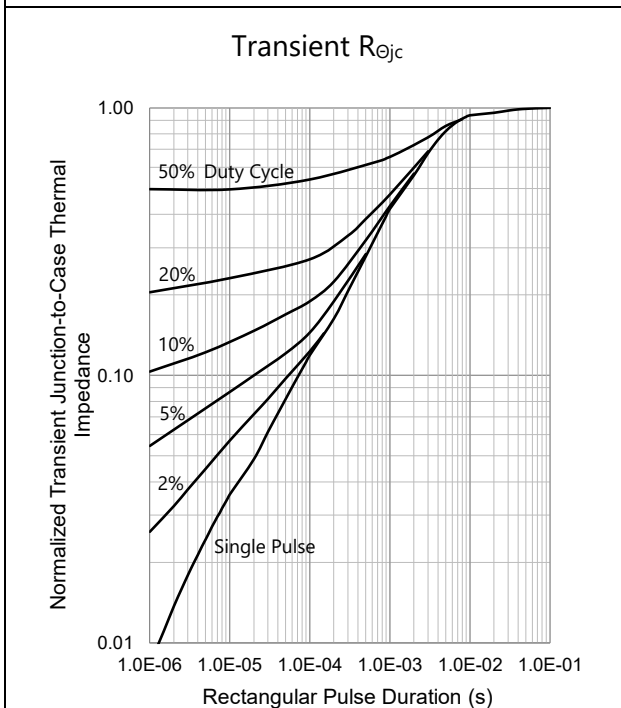


Figure 15: Transient Thermal Impedance (1.00 = Nominal DC thermal impedance)



Test Circuits

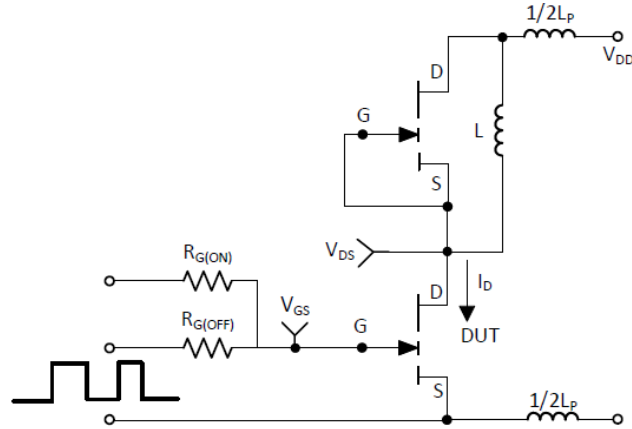


Figure 16: Switching Test Circuit

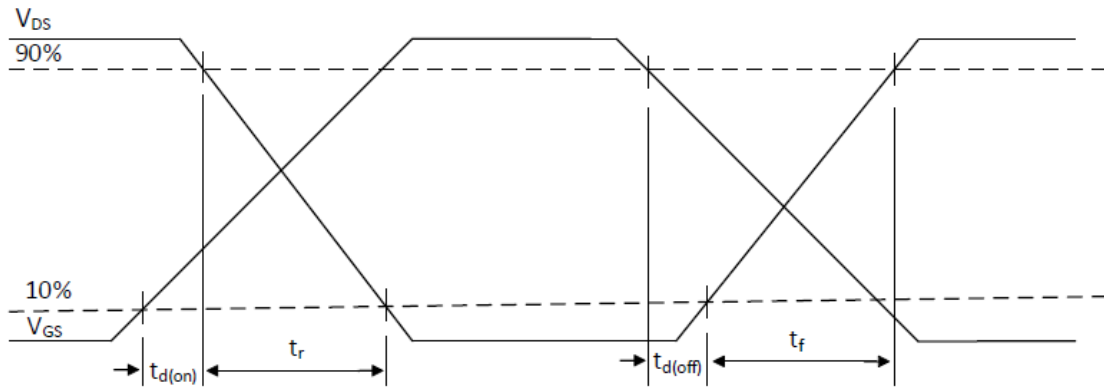


Figure 17: Switching Time Waveforms

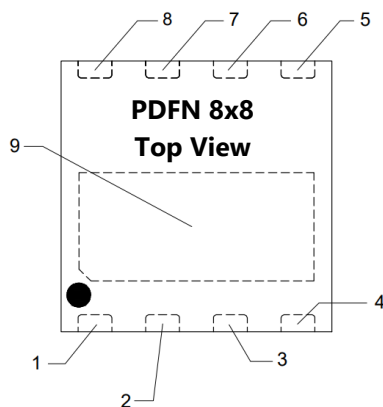
## Application Information

### Pin Configurations

Note that the Pin 1 (Source) is located at the bottom left corner from the top view indicated by the pin 1 marking.

The package features a dedicated Source Sense (SS) pin (3) which enhances the switching performance by eliminating the common source inductance. Source Sensing (or Kelvin Source) can be implemented by using pin 3 (SS) as the gate driver signal ground return.

The thermal pad / Source (Pin 9) is designed to provide a low thermal conduction path to the external main circuit board for optimum heat dissipation. It is internally connected to the die substrate and the Source, which can be used for both thermal and electrical conduction. The Source pin 1 & 2 can also be used together to enhance thermal conductivity, but it is **NOT** recommended to carry main current with only Pin 1 & 2.



Pin	Name	Description
1-2	S	Source
3	SS	Source Sense pin. Used for gate driver kelvin source connection
4	G	Gate
5-8	D	Drain
9	S / TP	Source and thermal pad. Recommend to join pin 1, 2 and 9 together with large copper polygon for optimum thermal dissipation and source connection

### Gate Drive

The recommended gate drive voltage range,  $V_{GS}$ , is 0 V to + 6 V for optimal  $R_{DS(on)}$  performance. Also, the repetitive gate to source voltage, maximum rating,  $V_{GS(AC)}$ , is +7 V to -10 V. The gate can survive non-repetitive transients up to +10 V and - 20 V for pulses up to 100  $\mu$ s. These specifications allow designers to easily use 6.0 V or 6.5 V gate drive settings. At 6 V gate drive voltage, the enhancement mode high electron mobility transistor (E-HEMT) is fully enhanced and reaches its optimal efficiency point. A 5 V gate drive can be used but may result in lower operating efficiency. Inherently, GaN Systems E-HEMT do not require negative gate bias to turn off. Negative gate bias, typically  $V_{GS} = -3$  V, ensures safe operation against the voltage spike on the gate, however it may increase reverse conduction losses if not driven properly. For more details, please refer to the gate driver application note "Gate Driver Circuit Design with GaN E-HEMTs" at [www.gansystems.com](http://www.gansystems.com)

Similar to a silicon MOSFET, an external gate resistor can be used to control the switching speed and slew rate. Adjusting the resistor to achieve the desired slew rate may be needed. Lower turn-off gate resistance,  $R_{G(OFF)}$  is recommended for better immunity to cross conduction. Please see the gate driver application note for more details.

A standard MOSFET driver can be used as long as it supports 6 V for gate drive and the UVLO is suitable for 6 V operation. Gate drivers with low impedance and high peak current are recommended for fast switching speed. GaN Systems E-HEMTs have significantly lower  $Q_G$  when compared to equally sized  $R_{DS(on)}$  MOSFETs, so high speed can be reached with smaller and lower cost gate drivers.

Some non-isolated half bridge MOSFET drivers are not compatible with 6 V gate drive due to their high under-voltage lockout threshold. Also, a simple bootstrap method for high side gate drive may not be able to provide tight tolerance on the gate voltage. Therefore, special care should be taken when you select and use the half bridge drivers. Please see the gate driver application note for more details.

### Parallel Operation

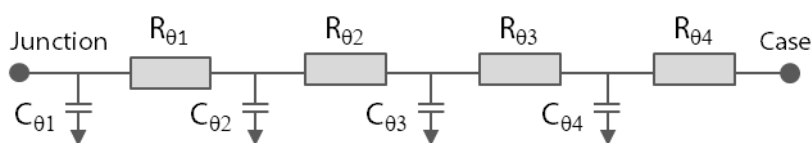
Design wide tracks or polygons on the PCB to distribute the gate drive signals to multiple devices. Keep the drive loop length to each device as short and equal length as possible.

GaN enhancement mode HEMTs have a positive temperature coefficient on-state resistance which helps to balance the current. However, special care should be taken in the driver circuit and PCB layout since the device switches at very fast speed. It is recommended to have a symmetric PCB layout and equal gate drive loop length (star connection if possible) on all parallel devices to ensure balanced dynamic current sharing. Adding a small gate resistor (1-2  $\Omega$ ) on each gate is strongly recommended to minimize the gate parasitic oscillation.

### Thermal Modeling

RC thermal models are available to support detailed thermal simulation using SPICE. The thermal models are created using the Cauer model, an RC network model that reflects the real physical property and packaging structure of our devices. This approach allows our customers to extend the thermal model to their system by adding extra  $R_\theta$  and  $C_\theta$  to simulate the Thermal Interface Material (TIM) or Heatsink.

RC thermal model:



RC breakdown of  $R_{\theta JC}$

$R_\theta$ ( $^{\circ}\text{C}/\text{W}$ )	$C_\theta$ ( $\text{W}\cdot\text{s}/^{\circ}\text{C}$ )
$R_{\theta 1} = 0.080$	$C_{\theta 1} = 1.0\text{E-}04$
$R_{\theta 2} = 0.462$	$C_{\theta 2} = 1.1\text{E-}03$
$R_{\theta 3} = 0.642$	$C_{\theta 3} = 3.2\text{E-}03$
$R_{\theta 4} = 0.051$	$C_{\theta 4} = 7.1\text{E-}01$

For more detail, please refer to Application Note entitled "Modeling Thermal Behavior of GaNPX® and PDFN Packages Using RC Thermal SPICE Models" available at [www.gansystems.com](http://www.gansystems.com)

### Reverse Conduction

GaN Systems enhancement mode HEMTs do not have an intrinsic body diode and there is zero reverse recovery charge. The devices are naturally capable of reverse conduction and exhibit different characteristics depending on the gate voltage. Anti-parallel diodes are not required for GaN Systems transistors as is the case for IGBTs to achieve reverse conduction performance.

On-state condition ( $V_{GS} = +6$  V): The reverse conduction characteristics of a GaN Systems enhancement mode HEMT in the on-state is similar to that of a silicon MOSFET, with the I-V curve symmetrical about the origin and it exhibits a channel resistance,  $R_{DS(on)}$ , similar to forward conduction operation.

Off-state condition ( $V_{GS} \leq 0$  V): The reverse characteristics in the off-state are different from silicon MOSFETs as the GaN device has no body diode. In the reverse direction, the device starts to conduct when the gate voltage, with respect to the drain,  $V_{GD}$ , exceeds the gate threshold voltage. At this point the device exhibits a channel resistance. This condition can be modeled as a "body diode" with slightly higher  $V_F$  and no reverse recovery charge.

If negative gate voltage is used in the off-state, the source-drain voltage must be higher than  $V_{GS(th)} + V_{GS(off)}$  in order to turn the device on. Therefore, a negative gate voltage will add to the reverse voltage drop " $V_F$ " and hence increase the reverse conduction loss.

### Blocking Voltage

The blocking voltage rating,  $V_{(BL)DSS}$ , is defined by the drain leakage current. The hard (unrecoverable) breakdown voltage is approximately 30 % higher than the rated  $V_{(BL)DSS}$ . As a general practice, the maximum drain voltage should be de-rated in a similar manner as IGBTs or silicon MOSFETs. All GaN E-HEMTs do not avalanche and thus do not have an avalanche breakdown rating. The maximum drain-to-source rating is 650 V and does not change with negative gate voltage. GaN Systems tests devices in production with a 850V Drain-to-source voltage pulse to insure blocking voltage margin.

### Packaging and Soldering

The package is a standard PDFN and it can handle at least 3 reflow cycles.

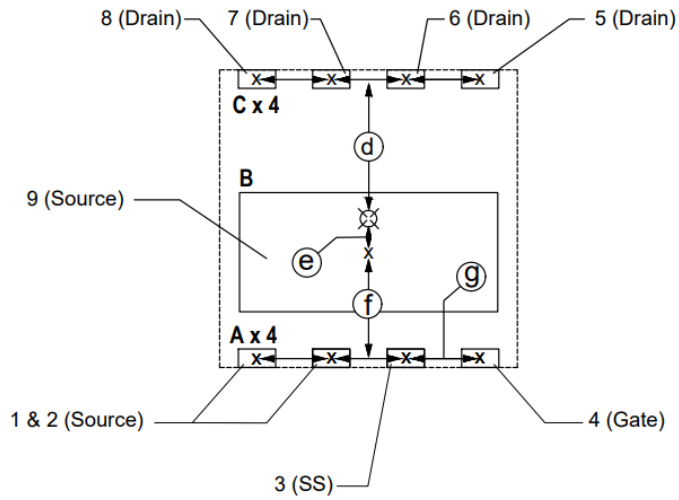
It is recommended to use the reflow profile in IPC/JEDEC J-STD-020 REV D.1 (March 2008)

The basic temperature profiles for Pb-free (Sn-Ag-Cu) assembly are:

- Preheat/Soak: 60 – 120 seconds.  $T_{min} = 150$  °C,  $T_{max} = 200$  °C.
- Reflow: Ramp up rate 3 °C/sec, max. Peak temperature is 260 °C and time within 5 °C of peak temperature is 30 seconds.
- Cool down: Ramp down rate 6 °C/sec max.

Using "No-Clean" soldering paste and operating at high temperatures may cause a reactivation of the "No-Clean" flux residues. In extreme conditions, unwanted conduction paths may be created. Therefore, when the product operates at greater than 100 °C it is recommended to also clean the "No-Clean" paste residues.



Recommended PCB Footprint



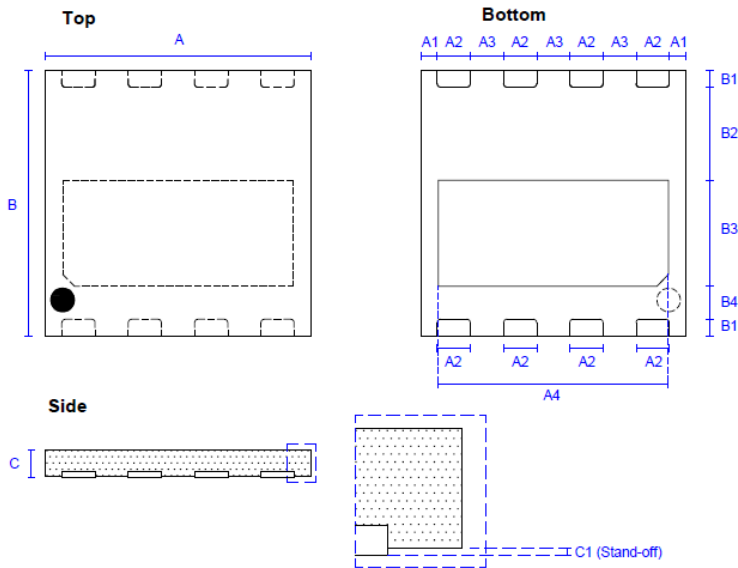
**Pad sizes**

	mm		Inches	
	X (width)	Y (height)	X (width)	Y (height)
<b>A</b>	1.00	0.50	0.039	0.020
<b>B</b>	6.94	3.20	0.273	0.126
<b>C</b>	1.00	0.50	0.039	0.020

	mm	Inches
<b>d</b>	3.75	0.148
<b>e</b>	0.90	0.035
<b>f</b>	2.85	0.112
<b>g</b>	2.00	0.079

-  PCB pad openings
-  Package outline

### Package Dimensions

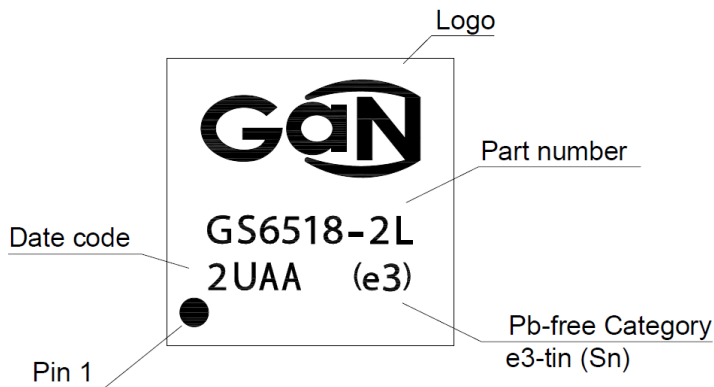


mm			Inches*		
<b>A</b>	8.00	0.315	+/- 0.100 mm	(0.004")	
<b>A1</b>	0.50	0.020	+/- 0.050 mm	(0.002")	
<b>A2</b>	1.00	0.039	+/- 0.100 mm	(0.004")	
<b>A3</b>	1.00	0.039	+/- 0.050 mm	(0.002")	
<b>A4</b>	6.94	0.273	+/- 0.100 mm	(0.004")	
<b>B</b>	8.00	0.315	+/- 0.100 mm	(0.004")	
<b>B1</b>	0.50	0.020	+/- 0.100 mm	(0.004")	
<b>B2</b>	2.80	0.110	+/- 0.100 mm	(0.004")	
<b>B3</b>	3.20	0.126	+/- 0.100 mm	(0.004")	
<b>B4</b>	1.00	0.039	+/- 0.100 mm	(0.004")	
<b>C</b>	0.90	0.033	+/- 0.050 mm	(0.002")	
<b>C1</b>	0.03	0.001	+0.02/-0.03 mm	(0.001")	

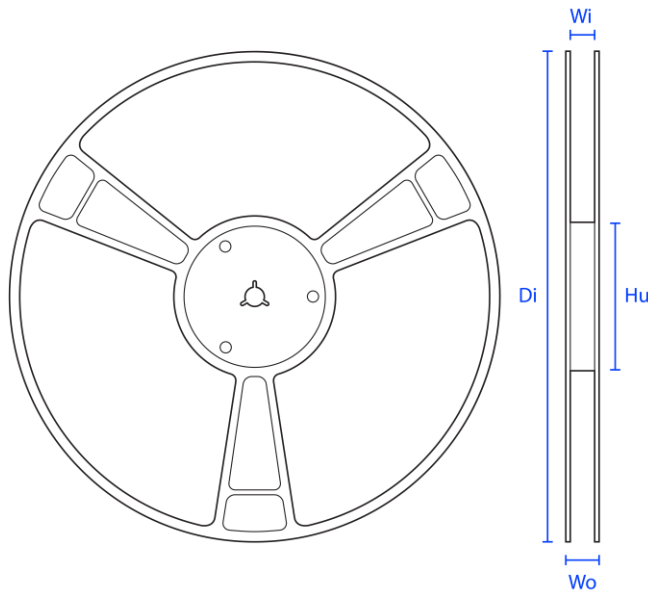
\*Inch measurements are approximate values

Surface Finish: Sn  
Sn: 10-20 um

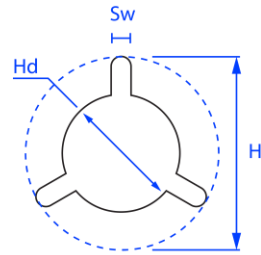
### Part Marking



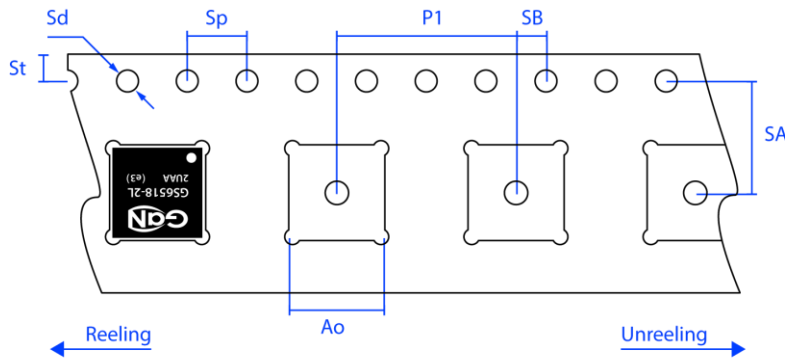
Tape and Reel Information



Dimensions (mm)				
	13 inch reel		7 inch reel	
	Min	Max	Min	Max
Di	328.0	332.0	178.0	180.0
Wo		22.4	Wo	22.4
Wi	16.4	18.4	Wi	16.4
Hu	176.0	178.0	Hu	58.0
H	20.2		H	20.2
Sw	1.5		Sw	1.5
Hd	12.8	13.5	Hd	12.8



Note: Wo and Wi measured at hub



Dimensions (mm)		
	Nominal	Tolerance
P1	12.00	+/- 0.1
W	16.00	+/- 0.3
Ko	1.10	+/- 0.1
Ao	8.30	+/- 0.1
Bo	8.30	+/- 0.1
Sp	4.00	+/- 0.1
Sd	1.55	+/- 0.05
St	1.75	+/- 0.1
SA	7.50	+/- 0.1
SB	2.00	+/- 0.1