

BGA
Commercial Temp
Industrial Temp

256K x 32

8Mb Asynchronous SRAM

8, 10, 12 ns
3.3 V V_{DD}

Features

- Fast access time: 8, 10, 12 ns
- CMOS low power operation: 260/210/180 mA at minimum cycle time
- Single 3.3 V ± 0.3 V power supply
- All inputs and outputs are TTL-compatible
- Byte control
- Fully static operation
- Industrial Temperature Option: -40° to 85°C
- 14 mm x 22 mm, 119-bump, 1.27 mm Pitch Ball Grid Array package
- RoHS-compliant package available

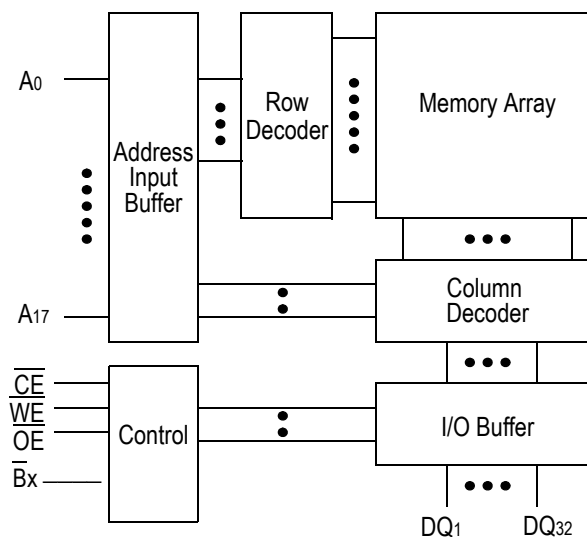
Description

The GS78132A is a high speed CMOS Static RAM organized as 262,144-words by 32-bits. Static design eliminates the need for external clocks or timing strobes. The GS78132A operates on a single 3.3 V power supply, and all inputs and outputs are TTL-compatible. The GS78132A is available in a 14 mm x 22 mm BGA package.

Pin Descriptions

Symbol	Description
A ₀ to A ₁₇	Address input
$\overline{\text{CE}}$	Chip enable input
DQA ₁ TO DQA ₈	Byte A Data input/output
DQB ₁ TO DQB ₈	Byte B Data input/output
DQC ₁ TO DQC ₈	Byte C Data input/output
DQD ₁ TO DQD ₈	Byte D Data input/output
$\overline{\text{B}}_A$	Byte A Byte enable input
$\overline{\text{B}}_B$	Byte B Byte enable input
$\overline{\text{B}}_C$	Byte C Byte enable input
$\overline{\text{B}}_D$	Byte D Byte enable input
$\overline{\text{WE}}$	Write enable input
$\overline{\text{OE}}$	Output enable input
V _{DD}	+3.3 V power supply
V _{SS}	Ground
NC	No connect

Block Diagram



256K x 32 Async SRAM in 119-bump, 14 mm x 22 mm BGA—Top View (Package B)

	1	2	3	4	5	6	7
A	NC	A15	A14	A16	A13	A12	NC
B	$\overline{B_C}$	A11	A10	$\overline{C_E}$	A9	A8	$\overline{B_B}$
C	DQC6	NC	V _{DD} , NC	A17	V _{SS} , NC	NC	DQB6
D	DQC5	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	DQB5
E	DQC4	DQC8	V _{DD}	V _{SS}	V _{DD}	DQB8	DQB4
F	DQC3	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	DQB3
G	DQC2	DQC7	V _{DD}	V _{SS}	V _{DD}	DQB7	DQB2
H	DQC1	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	DQB1
J	V _{DD}	V _{SS}	V _{DD}	V _{SS}	V _{DD}	V _{SS}	V _{DD}
K	DQD1	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	DQA1
L	DQD2	DQD7	V _{DD}	V _{SS}	V _{DD}	DQA7	DQA2
M	DQD3	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	DQA3
N	DQD4	DQD8	V _{DD}	V _{SS}	V _{DD}	DQA8	DQA4
P	DQD5	V _{DD}	V _{SS}	V _{SS}	V _{SS}	V _{DD}	DQA5
R	DQD6	NC	NC	NC	NC	NC	DQA6
T	$\overline{B_D}$	A7	A6	$\overline{W_E}$	A5	A4	$\overline{B_A}$
U	NC	A3	A2	$\overline{O_E}$	A1	A0	NC

Note:

Bumps 3C and 5C are actually NC's but should be wired 3C = V_{DD} and 5C = V_{SS} to assure compatibility with future versions.

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	\overline{BA}	\overline{BB}	\overline{BC}	\overline{BD}	DQA1-A8	DQB1-B8	DQC1-C8	DQD1-D8	Supply Current
H	X	X	X	X	X	X	Not Selected	Not Selected	Not Selected	Not Selected	ISB1, ISB2
L	L	H	L	L	L	L	Read	Read	Read	Read	IDD
			H	L	L	L	High Z	Read	Read	Read	
			L	H	L	L	Read	High Z	Read	Read	
			L	L	H	L	Read	Read	High Z	Read	
			L	L	L	H	Read	Read	Read	High Z	
L	X	L	L	L	L	L	Write	Write	Write	Write	
			H	L	L	L	High Z	Write	Write	Write	
			L	H	L	L	Write	High Z	Write	Write	
			L	L	H	L	Write	Write	High Z	Write	
			L	L	L	H	Write	Write	Write	High	
L	H	H	X	X	X	X	High Z	High Z	High Z	High Z	
L	X	X	H	H	H	H	High Z	High Z	High Z	High Z	

X: "H" or "L"

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{DD}	-0.5 to +4.6	V
Input Voltage	V_{IN}	-0.5 to $V_{DD} + 0.5$ (≤ 4.6 V max.)	V
Output Voltage	V_{OUT}	-0.5 to $V_{DD} + 0.5$ (≤ 4.6 V max.)	V
Allowable power dissipation	PD	1.5	W
Storage temperature	T_{STG}	-55 to 150	°C

Note:

Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation shall be restricted to Recommended Operating Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage for -8/10/12	V_{DD}	3.0	3.3	3.6	V
Input High Voltage	V_{IH}	2.0	—	$V_{DD} + 0.3$	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V
Ambient Temperature, Commercial Range	T_{Ac}	0	—	70	°C
Ambient Temperature, Industrial Range	T_{Ai}	-40	—	85	°C

Notes:

1. Input overshoot voltage should be less than $V_{DD} + 2$ V and not exceed 20 ns.
2. Input undershoot voltage should be greater than -2 V and not exceed 20 ns.

Capacitance

Parameter	Symbol	Test Condition	Max	Unit
Input Capacitance	C_{IN}	$V_{IN} = 0$ V	10	pF
Output Capacitance	C_{OUT}	$V_{OUT} = 0$ V	7	pF

Notes:

1. Tested at $T_A = 25^\circ\text{C}$, $f = 1$ MHz
2. These parameters are sampled and are not 100% tested

DC I/O Pin Characteristics

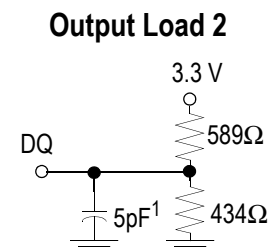
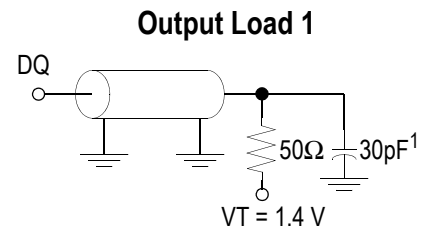
Parameter	Symbol	Test Conditions	Min	Max
Input Leakage Current	I_{IL}	$V_{IN} = 0$ to V_{DD}	-2 μA	2 μA
Output Leakage Current	I_{OL}	Output High Z, $V_{OUT} = 0$ to V_{DD}	-1 μA	1 μA
Output High Voltage	V_{OH}	$I_{OH} = -4$ mA	2.4	
Output Low Voltage	V_{OL}	$I_{OL} = +4$ mA		0.4 V

Power Supply Currents

Parameter	Symbol	Test Conditions	0 to 70°C			-40 to 85°C		
			8 ns	10 ns	12 ns	8 ns	10 ns	12 ns
Operating Supply Current	I_{DD}	$\bar{E} \leq V_{IL}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time $I_{OUT} = 0$ mA	260 mA	210 mA	180 mA	280 mA	230 mA	200 mA
Standby Current	I_{SB1}	$\bar{E} \geq V_{IH}$ All other inputs $\geq V_{IH}$ or $\leq V_{IL}$ Min. cycle time	60 mA	50 mA	50 mA	80 mA	70 mA	70 mA
Standby Current	I_{SB2}	$E \geq V_{DD} - 0.2V$ All other inputs $\geq V_{DD} - 0.2V$ or $\leq 0.2V$	20 mA			40 mA		

AC Test Conditions

Parameter	Conditions
Input high level	$V_{IH} = 2.4$ V
Input low level	$V_{IL} = 0.4$ V
Input rise time	$t_r = 1$ V/ns
Input fall time	$t_f = 1$ V/ns
Input reference level	1.4 V
Output reference level	1.4 V
Output load	Fig. 1 & 2



Notes:

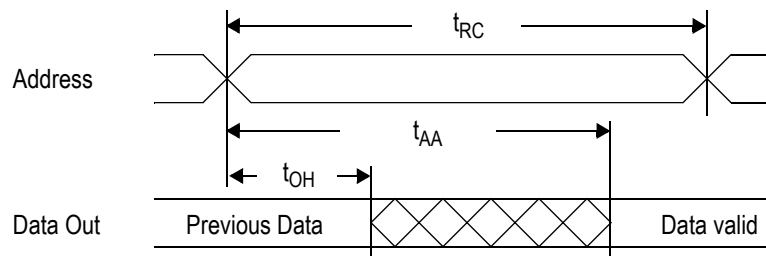
1. Include scope and jig capacitance.
2. Test conditions as specified with output loading as shown in **Fig. 1** unless otherwise noted
3. Output load 2 for t_{LZ} , t_{HZ} , t_{OLZ} and t_{OHZ} .

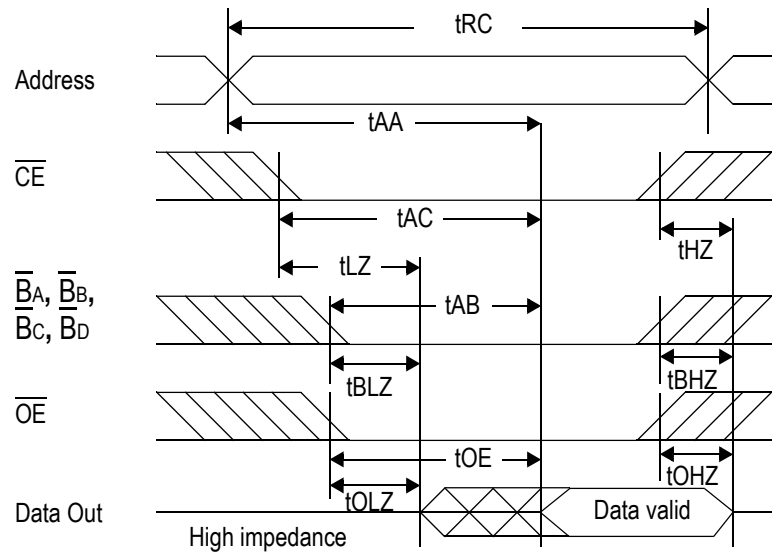
AC Characteristics

Read Cycle

Parameter	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Read cycle time	t_{RC}	8	—	10	—	12	—	ns
Address access time	t_{AA}	—	8	—	10	—	12	ns
Chip enable access time (\overline{CE})	t_{AC}	—	8	—	10	—	12	ns
Output enable to output valid (\overline{OE})	t_{OE}	—	3.5	—	4	—	5	ns
Output hold from address change	t_{OH}	3	—	3	—	3	—	ns
Chip enable to output in low Z (\overline{CE})	t_{LZ}^*	3	—	3	—	3	—	ns
Output enable to output in low Z (\overline{OE})	t_{OLZ}^*	0	—	0	—	0	—	ns
Chip disable to output in High Z (\overline{CE})	t_{HZ}^*	—	4	—	5	—	6	ns
Output disable to output in High Z (\overline{OE})	t_{OHZ}^*	—	3.5	—	4	—	5	ns

Read Cycle 1: $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, $\overline{BA} = \overline{BB} = \overline{BC} = \overline{BD} = V_{IL}$



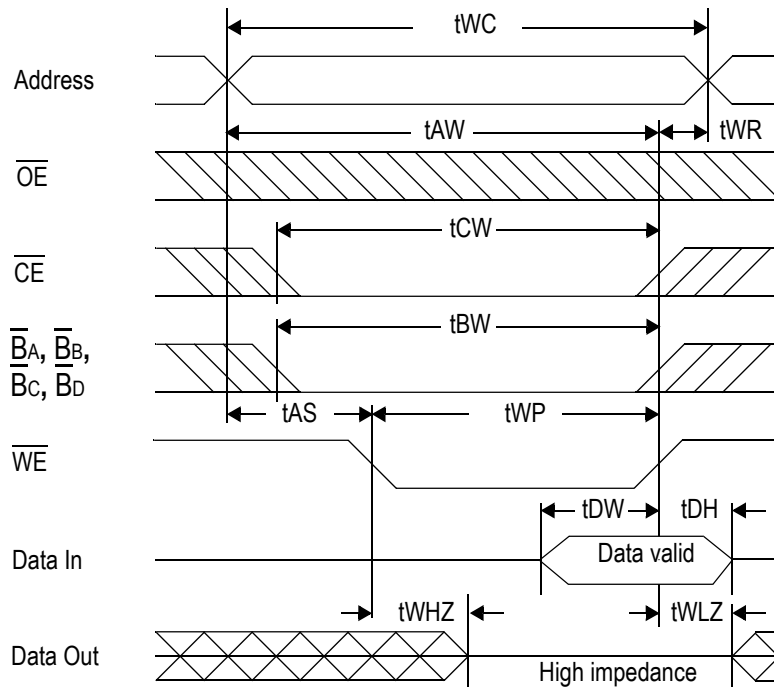
Read Cycle 2: $\overline{WE} = V_{IH}$


* These parameters are sampled and are not 100% tested

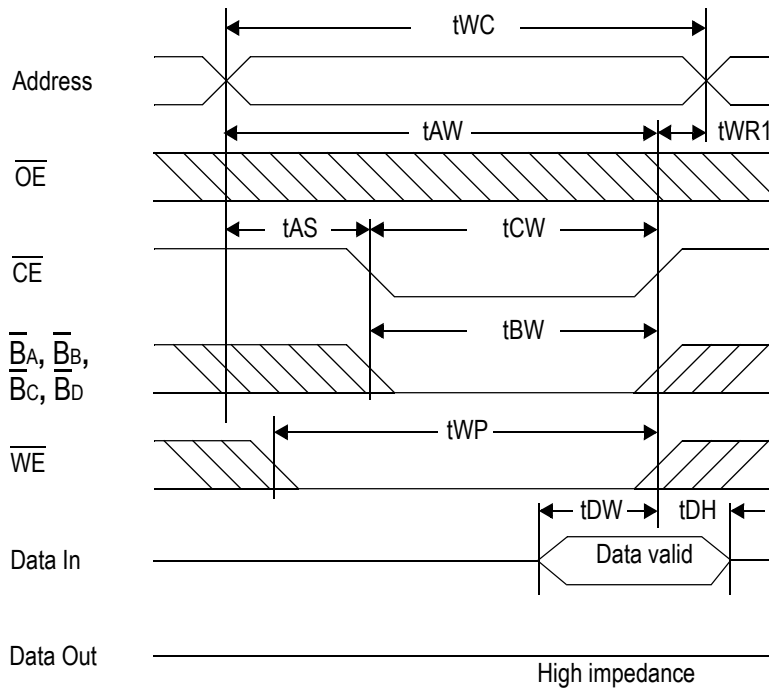
Write Cycle

Parameter	Symbol	-8		-10		-12		Unit
		Min	Max	Min	Max	Min	Max	
Write cycle time	t_{WC}	8	—	10	—	12	—	ns
Address valid to end of write	t_{AW}	5.5	—	7	—	8	—	ns
Chip enable to end of write	t_{CW}	5.5	—	7	—	8	—	ns
Data set up time	t_{DW}	4	—	5	—	6	—	ns
Data hold time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	5.5	—	7	—	8	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time (\overline{WE})	t_{WR}	0	—	0	—	0	—	ns
Write recovery time (\overline{CE})	t_{WR1}	0	—	0	—	0	—	ns
Output Low Z from end of write	t_{WLZ}^*	3	—	3	—	3	—	ns
Write to output in High Z	t_{WHZ}^*	—	3.5	—	4	—	5	ns

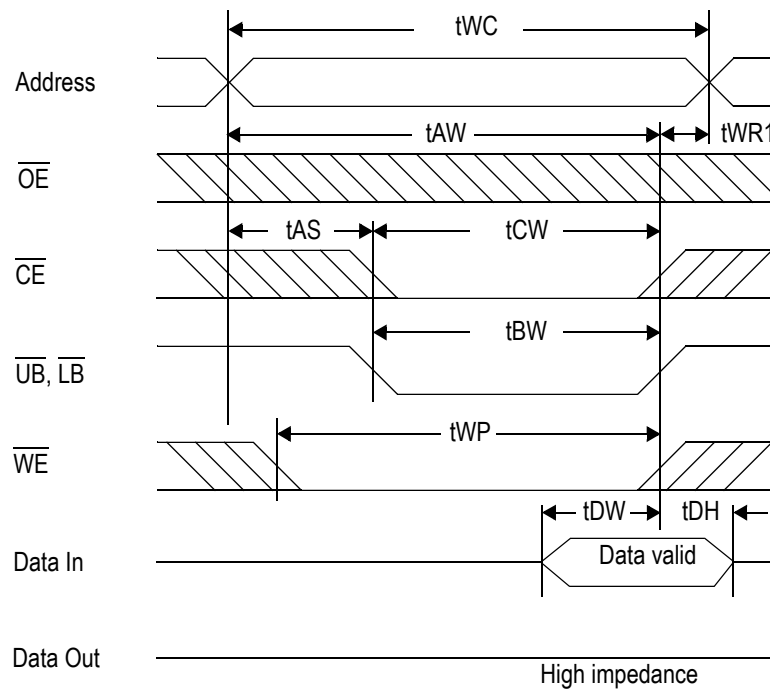
Write Cycle 1: \overline{WE} Controlled



Write Cycle 2: \overline{CE} Controlled

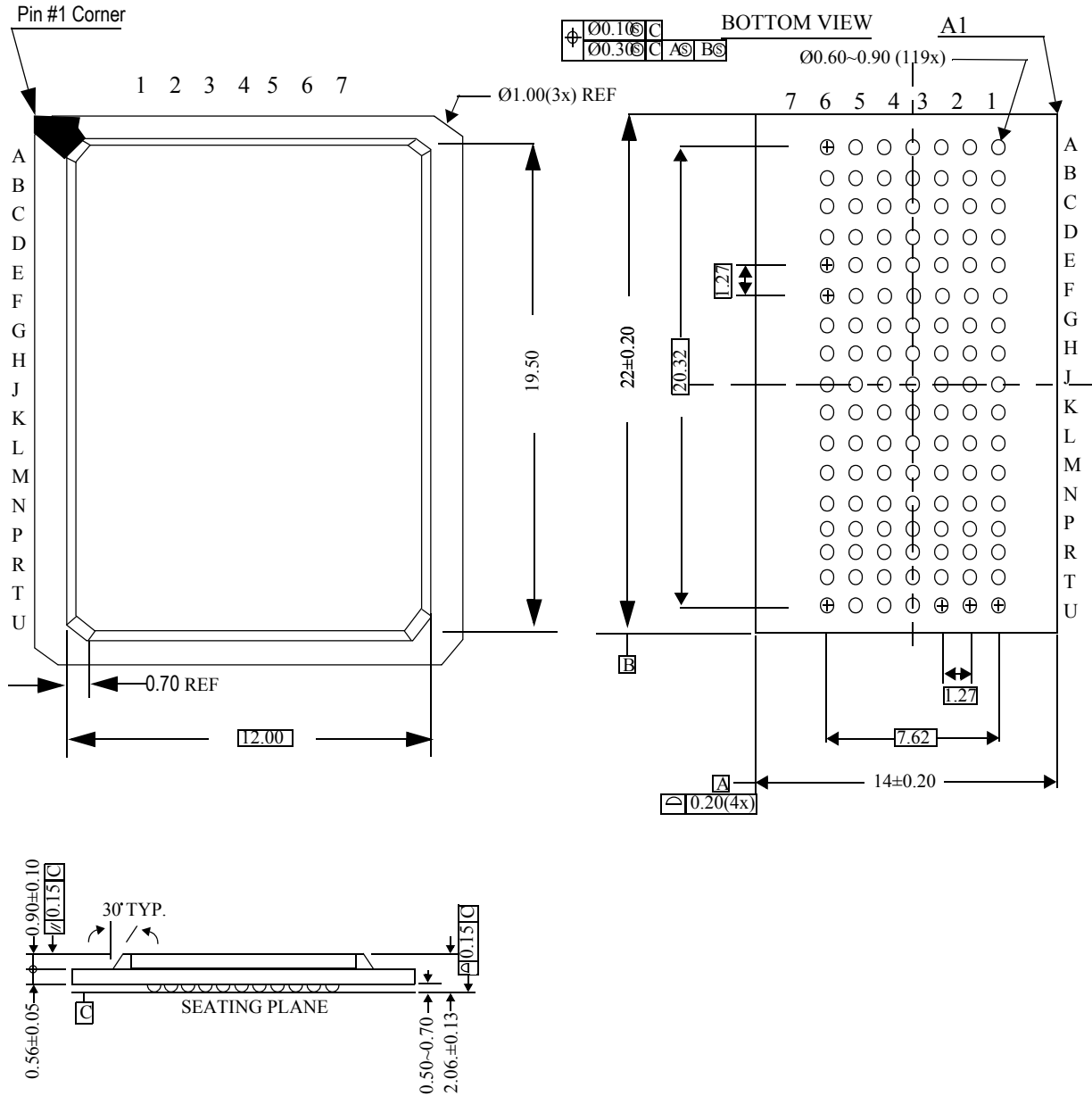


Write Cycle 3: \overline{UB} , \overline{LB} control

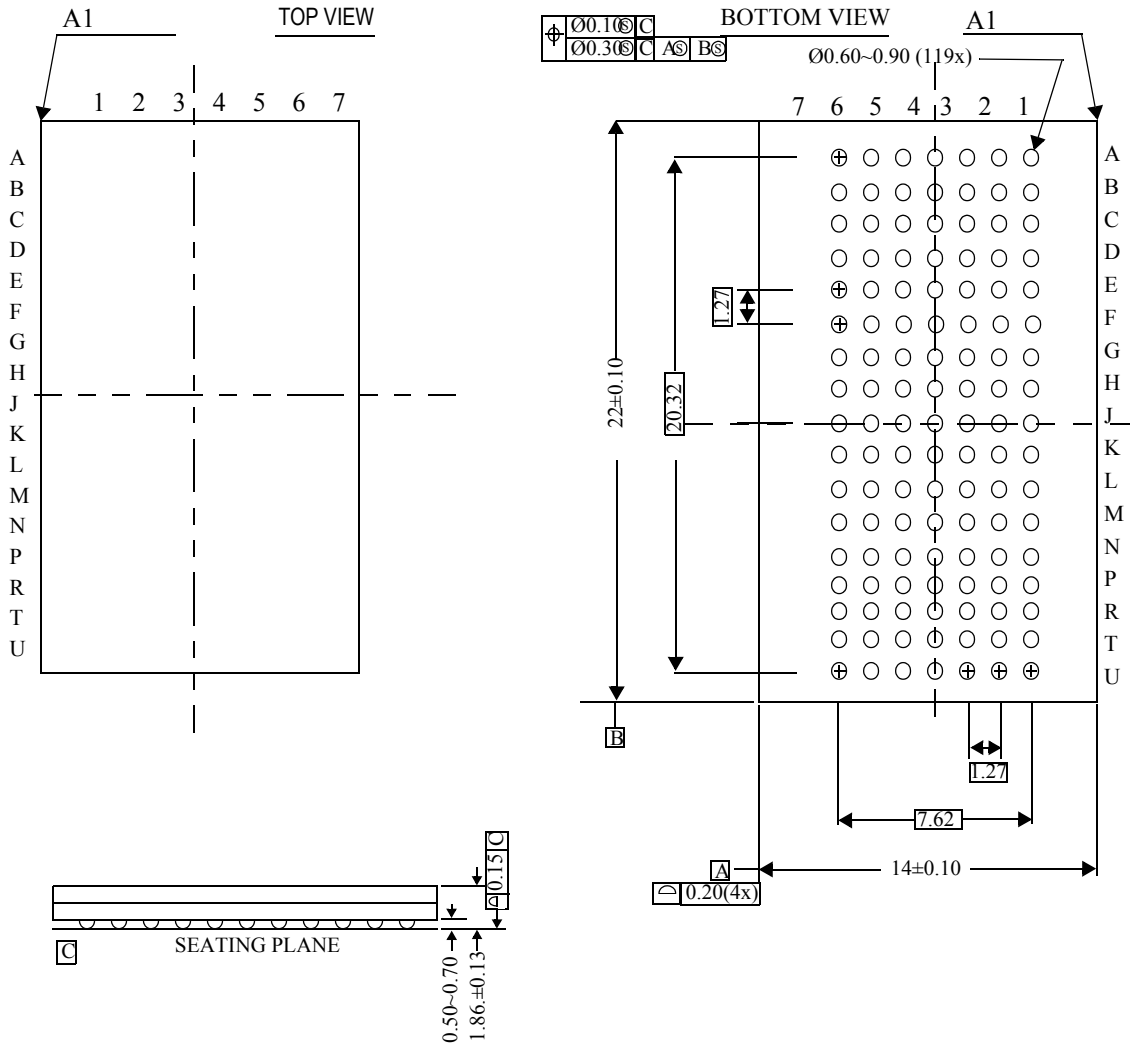


Package Dimensions—119-Bump FPBGA (Package B, Variation 1)

(Date Code: yyww.31)



Package Dimensions—119-Bump FPBGA (Package B, Variation 2)
(Date Code: yyww.3H)



Ordering Information

Part Number¹	Package	Access Time	Temp. Range	Status
GS78132AB-8	119-Bump BGA ²	8 ns	Commercial	
GS78132AB-10	119-Bump BGA ²	10 ns	Commercial	
GS78132AB-12	119-Bump BGA ²	12 ns	Commercial	
GS78132AB-8I	119-Bump BGA ²	8 ns	Industrial	
GS78132AB-10I	119-Bump BGA ²	10 ns	Industrial	
GS78132AB-12I	119-Bump BGA ²	12 ns	Industrial	
GS78132AB-15I	119-Bump BGA ²	15 ns	Industrial	
GS78132AGB-8	RoHS-compliant 119-Bump BGA ²	8 ns	Commercial	
GS78132AGB-10	RoHS-compliant 119-Bump BGA ²	10 ns	Commercial	
GS78132AGB-12	RoHS-compliant 119-Bump BGA ²	12 ns	Commercial	
GS78132AGB-8I	RoHS-compliant 119-Bump BGA ²	8 ns	Industrial	
GS78132AGB-10I	RoHS-compliant 119-Bump BGA ²	10 ns	Industrial	
GS78132AGB-12I	RoHS-compliant 119-Bump BGA ²	12 ns	Industrial	
GS78132AGB-15I	RoHS-compliant 119-Bump BGA ²	15 ns	Industrial	

Notes:

- Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number.
For example: GS78132AB-12T
- Please see pages 9 and 10 for date code information for Variation 1 and Variation 2 of the 119-bump BGA.