165-Bump BGA
Commercial Temp
Industrial Temp

144Mb SigmaDDR™-II+ Burst of 2 SRAM

500 MHz–350 MHz
1.8 V V_{DD}
1.8 V or 1.5 V I/O

Features

- 2.5 Clock Latency
- Simultaneous Read and Write SigmaDDR™ Interface
- JEDEC-standard pinout and package
- Double Data Rate interface
- Byte Write controls sampled at data-in time
- Burst of 2 Read and Write
- On-Die Termination (ODT) on Data (D), Byte Write ($\overline{BW}$), and Clock (K, $\overline{K}$) inputs
- 1.8 V +100/–100 mV core power supply
- 1.5 V or 1.8 V HSTL Interface
- Pipelined read operation
- Fully coherent read and write pipelines
- ZQ pin for programmable output drive strength
- Data Valid Pin (QVLD) Support
- IEEE 1149.1 JTAG-compliant Boundary Scan
- 165-bump, 15 mm x 17 mm, 1 mm bump pitch BGA package
- RoHS-compliant 165-bump BGA package available

SigmaDDR-II™ Family Overview

The GS81302T06/11/20/38E are built in compliance with the SigmaDDR-II+ SRAM pinout standard for Common I/O synchronous SRAMs. They are 150,994,944-bit (144Mb) SRAMs. The GS81302T06/11/20/38E SigmaDDR-II+ SRAMs are just one element in a family of low power, low voltage HSTL I/O SRAMs designed to operate at the speeds needed to implement economical high performance networking systems.

Clocking and Addressing Schemes

The GS81302T06/11/20/38E SigmaDDR-II+ SRAMs are synchronous devices. They employ two input register clock inputs, K and $\overline{K}$. K and $\overline{K}$ are independent single-ended clock inputs, not differential inputs to a single differential clock input buffer.

Each internal read and write operation in a SigmaDDR-II+ B2 RAM is two times wider than the device I/O bus. An input data bus de-multiplexer is used to accumulate incoming data before it is simultaneously written to the memory array. An output data multiplexer is used to capture the data produced from a single memory array read and then route it to the appropriate output drivers as needed. Therefore, the address field of a SigmaDDR-II+ B2 RAM is always one address pin less than the advertised index depth (e.g., the 16M x 8 has an 8M addressable index).

Parameter Synopsis

	-500	-450	-400	-350
tKHKH	2.0 ns	2.2 ns	2.5 ns	2.86 ns
tKHQV	0.45 ns	0.45 ns	0.45 ns	0.45 ns

4M x 36 SigmaDDR-II+ SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	SA	SA	R/$\overline{W}$	$\overline{BW2}$	$\overline{K}$	$\overline{BW1}$	$\overline{LD}$	SA	SA	CQ
B	NC	DQ27	DQ18	SA	$\overline{BW3}$	K	$\overline{BW0}$	SA	NC (288Mb)	NC	DQ8
C	NC	NC	DQ28	V_{SS}	SA	NC	SA	V_{SS}	NC	DQ17	DQ7
D	NC	DQ29	DQ19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	DQ16
E	NC	NC	DQ20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQ15	DQ6
F	NC	DQ30	DQ21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	DQ31	DQ22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ14
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	DQ32	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ13	DQ4
K	NC	NC	DQ23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ12	DQ3
L	NC	DQ33	DQ24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	DQ34	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ11	DQ1
N	NC	DQ35	DQ25	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	DQ10
P	NC	NC	DQ26	SA	SA	QVLD	SA	SA	NC	DQ9	DQ0
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—15 x 17 mm^2 Body—1 mm Bump Pitch

Notes:
1. $\overline{BW0}$ controls writes to DQ0:DQ8; $\overline{BW1}$ controls writes to DQ9:DQ17; $\overline{BW2}$ controls writes to DQ18:DQ26; $\overline{BW3}$ controls writes to DQ27:DQ35
2. Pin B9 is the expansion address.

8M x 18 SigmaDDR-II+ SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	SA	SA	R/$\overline{W}$	$\overline{BW1}$	$\overline{K}$	SA	$\overline{LD}$	SA	SA	CQ
B	NC	DQ9	NC	SA	NC (288Mb)	K	$\overline{BW0}$	SA	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	SA	NC	SA	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	SA	SA	QVLD	SA	SA	NC	NC	DQ0
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—15 x 17 mm^2 Body—1 mm Bump Pitch

Notes:
1. $\overline{BW0}$ controls writes to DQ0:DQ8; $\overline{BW1}$ controls writes to DQ9:DQ17
2. Pin B5 is the expansion address.

16M x 9 SigmaDDR-II+ SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	SA	SA	R/$\overline{W}$	NC	$\overline{K}$	SA	$\overline{LD}$	SA	SA	CQ
B	NC	NC	NC	SA	NC/SA (288Mb)	K	$\overline{BW0}$	SA	NC	NC	DQ4
C	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
D	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ5	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ3
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	NC	DQ6	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ2	NC
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	DQ7	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ1
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
N	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	DQ8	SA	SA	QVLD	SA	SA	NC	NC	DQ0
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—15 x 17 mm^2 Body—1 mm Bump Pitch

Notes:
3. $\overline{BW0}$ controls writes to DQ0:DQ8.
4. Pin B5 is the expansion address.

16M x 8 SigmaDDR-II+ SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	SA	SA	R/$\overline{W}$	$\overline{NW1}$	$\overline{K}$	SA	$\overline{LD}$	SA	SA	CQ
B	NC	NC	NC	SA	NC/SA (288Mb)	K	$\overline{NW0}$	SA	NC	NC	DQ3
C	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
D	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ4	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
F	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
G	NC	NC	DQ5	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ1	NC
K	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
L	NC	DQ6	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ0
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
N	NC	NC	NC	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	DQ7	SA	SA	QVLD	SA	SA	NC	NC	NC
R	TDO	TCK	SA	SA	SA	ODT	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—15 x 17 mm^2 Body—1 mm Bump Pitch

Notes:
1. $\overline{NW0}$ controls writes to DQ0:DQ3; $\overline{NW1}$ controls writes to DQ4:DQ7.
2. Pin B5 is the expansion address.

Pin Description Table

Symbol	Description	Type	Comments
SA	Synchronous Address Inputs	Input	—
R/$\overline{W}$	Synchronous Read/Write	Input	High: Read Low: Write
$\overline{BW0}$–$\overline{BW3}$	Synchronous Byte Writes	Input	Active Low
$\overline{LD}$	Synchronous Load Pin	Input	Active Low
K	Input Clock	Input	Active High
$\overline{K}$	Input Clock	Input	Active Low
TMS	Test Mode Select	Input	—
TDI	Test Data Input	Input	—
TCK	Test Clock Input	Input	—
TDO	Test Data Output	Output	—
V_{REF}	HSTL Input Reference Voltage	Input	—
ZQ	Output Impedance Matching Input	Input	—
MCL	Must Connect Low	—	—
DQ	Data I/O	Input/Output	Three State
$\overline{Doff}$	Disable DLL when low	Input	Active Low
CQ	Output Echo Clock	Output	—
$\overline{CQ}$	Output Echo Clock	Output	—
V_{DD}	Power Supply	Supply	1.8 V Nominal
V_{DDQ}	Isolated Output Buffer Supply	Supply	1.8 V or 1.5 V Nominal
V_{SS}	Power Supply: Ground	Supply	—
QVLD	Q Valid Output	Output	—
ODT	On-Die Termination	Input	Active High
NC	No Connect	—	—

Notes:
1. NC = Not Connected to die or any other pin
2. When ZQ pin is directly connected to V_{DDQ}, output impedance is set to minimum value and it cannot be connected to ground or left unconnected.
3. K and $\overline{K}$ cannot be set to V_{REF} voltage.

Background

Common I/O SRAMs, from a system architecture point of view, are attractive in read dominated or block transfer applications. Therefore, the SigmaDDR-II+ SRAM interface and truth table are optimized for burst reads and writes. Common I/O SRAMs are unpopular in applications where alternating reads and writes are needed because bus turnaround delays can cut high speed Common I/O SRAM data bandwidth in half.

Burst Operations

Read and write operations are "Burst" operations. In every case where a read or write command is accepted by the SRAM, it will respond by issuing or accepting two beats of data, executing a data transfer on subsequent rising edges of K and $\overline{K}$, as illustrated in the timing diagrams. This means that it is possible to load new addresses every K clock cycle. Addresses can be loaded less often, if intervening deselect cycles are inserted.

Deselect Cycles

Chip Deselect commands are pipelined to the same degree as read commands. This means that if a deselect command is applied to the SRAM on the next cycle after a read command captured by the SRAM, the device will complete the two beat read data transfer and then execute the deselect command, returning the output drivers to High-Z. A high on the $\overline{LD}$ pin prevents the RAM from loading read or write command inputs and puts the RAM into deselect mode as soon as it completes all outstanding burst transfer operations.

SigmaDDR-II+ Burst of 2 SRAM Read Cycles

The SRAM executes pipelined reads. The status of the Address, $\overline{LD}$ and R/$\overline{W}$ pins are evaluated on the rising edge of K. The read command ($\overline{LD}$ low and R/$\overline{W}$ high) is clocked into the SRAM by a rising edge of K.

SigmaDDR-II+ Burst of 2 SRAM Write Cycles

The status of the Address, $\overline{LD}$ and R/$\overline{W}$ pins are evaluated on the rising edge of K. The SRAM executes "late write" data transfers. Data in is due at the device inputs on the rising edge of K following the rising edge of K clock used to clock in the write command ($\overline{LD}$ and R/$\overline{W}$ low) and the write address. To complete the remaining beat of the burst of two write transfer, the SRAM captures data in on the next rising edge of $\overline{K}$, for a total of two transfers per address load.

Special Functions

Byte Write and Nybble Write Control

Byte Write Enable pins are sampled at the same time that Data In is sampled. A high on the Byte Write Enable pin associated with a particular byte (e.g., $\overline{BW0}$ controls D0–D8 inputs) will inhibit the storage of that particular byte, leaving whatever data may be stored at the current address at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven High or Low during the data in sample times in a write sequence.

Each write enable command and write address loaded into the RAM provides the base address for a 2-beat data transfer. The x18 version of the RAM, for example, may write 36 bits in association with each address loaded. Any 9-bit byte may be masked in any write sequence.

Nybble Write (4-bit) control is implemented on the 8-bit-wide version of the device. For the x8 version of the device, “Nybble Write Enable” and “$\overline{NWx}$” may be substituted in all the discussion above.

Resulting Write Operation

Byte 1 D0–D8	Byte 2 D9–D17	Byte 3 D0–D8	Byte 4 D9–D17
Written	Unchanged	Unchanged	Written
Beat 1		Beat 2	

Example x18 RAM Write Sequence using Byte Write Enables

Data In Sample Time	$\overline{BW0}$	$\overline{BW1}$	D0–D8	D9–D17
Beat 1	0	1	Data In	Don't Care
Beat 2	1	0	Don't Care	Data In

FLXDrive-II Output Driver Impedance Control

HSTL I/O SigmaDDR-II+ SRAMs are supplied with programmable impedance output drivers. The ZQ pin must be connected to V_{SS} via an external resistor, RQ, to allow the SRAM to monitor and adjust its output driver impedance. The value of RQ must be 5X the value of the desired RAM output impedance. The allowable range of RQ to guarantee impedance matching continuously is between 175Ω and 350Ω. Periodic readjustment of the output driver impedance is necessary as the impedance is affected by drifts in supply voltage and temperature. The SRAM's output impedance circuitry compensates for drifts in supply voltage and temperature. A clock cycle counter periodically triggers an impedance evaluation, resets and counts again. Each impedance evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps.

Input Termination Impedance Control

These SigmaDDR-II+ SRAMs are supplied with programmable input termination on Data (DQ), Byte Write ($\overline{BW}$), and Clock (K, $\overline{K}$) input receivers. Input termination can be enabled or disabled via the ODT pin (6R). When the ODT pin is tied Low (or left floating–the pin has a small pull-down resistor), input termination is disabled. When the ODT pin is tied High, input termination is enabled. Termination impedance is programmed via the same RQ resistor (connected between the ZQ pin and V_{SS}) used to program output driver impedance, and is nominally RQ*0.6 Thevenin-equivalent when RQ is between 175Ω and 250Ω. Periodic readjustment of the termination impedance occurs to compensate for drifts in supply voltage and temperature, in the same manner as for driver impedance (see above).

Notes:

1. When ODT = 1, Byte Write ($\overline{BW}$), and Clock (K, $\overline{K}$) input termination is always enabled. Consequently, $\overline{BW}$, K, $\overline{K}$ inputs should always be driven High or Low; they should never be tri-stated (i.e., in a High-Z state). If the inputs are tri-stated, the input termination will pull the signal to $V_{DDQ}/2$ (i.e., to the switch point of the diff-amp receiver), which could cause the receiver to enter a meta-stable state, resulting in the receiver consuming more power than it normally would. This could result in the device's operating currents being higher.

2. When ODT = 1, DQ input termination is enabled during Write and NOP operations, and disabled during Read operations. Specifically, DQ input termination is disabled 0.5 cycles before the SRAM enables its DQ drivers and starts driving valid Read Data, and remains disabled until 0.5 cycles after the SRAM stops driving valid Read Data and disables its DQ drivers; DQ input termination is enabled at all other times. Consequently, the SRAM Controller should disable its DQ input termination, enable its DQ drivers, and drive DQ inputs (High or Low) during Write and NOP operations. And, it should enable its DQ input termination and disable its DQ drivers during Read operations. Care should be taken during Write or NOP -> Read transitions, and during Read -> NOP transitions, to minimize the time during which one device (SRAM or SRAM Controller) has enabled its DQ input termination while the other device has not yet enabled its DQ driver. Otherwise, the input termination will pull the signal to $V_{DDQ}/2$ (i.e., to the switch point of the diff-amp receiver), which could cause the receiver to enter a meta-stable state, resulting in the receiver consuming more power than it normally would. This could result in the device's operating currents being higher.

Common I/O SigmaDDR-II+ Burst of 2 SRAM Truth Table

K_n	$\overline{LD}$	R/$\overline{W}$	DQ		Operation
			A + 0	A + 1	
↑	1	X	Hi-Z / *	Hi-Z / *	Deselect
↑	0	0	D@K_{n+1}	D@$\overline{K}_{n+1}$	Write
↑	0	1	Q@$\overline{K}_{n+2}$	Q@K_{n+3}	Read

Notes:

1. "1" = input "high"; "0" = input "low"; "V" = input "valid"; "X" = input "don't care".
2. D1 and D2 indicate the first and second pieces of Write Data transferred during Write operations.
3. Q1 and Q2 indicate the first and second pieces of Read Data transferred during Read operations.
4. When On-Die Termination is disabled (ODT = 0), DQ drivers are disabled (i.e., DQ pins are tri-stated) for one cycle in response to NOP and Write commands, 2.5 cycles after the command is sampled.
5. When On-Die Termination is enabled (ODT = 1), DQ drivers are disabled for one cycle in response to NOP and Write commands, 2.5 cycles after the command is sampled. The state of the DQ pins during that time (denoted by "*" in the table above) is determined by the state of the DQ input termination. See the Input Termination Impedance Control section for more information.

Burst of 2 Byte Write Clock Truth Table

$\overline{BW}$	$\overline{BW}$	Current Operation	D	D
K ↑ (t_{n+1})	$\overline{K}$ ↑ ($t_{n+1½}$)	K ↑ (t_n)	K ↑ (t_{n+1})	$\overline{K}$ ↑ ($t_{n+1½}$)
T	T	Write Dx stored if $\overline{BWn}$ = 0 in both data transfers	D1	D2
T	F	Write Dx stored if $\overline{BWn}$ = 0 in 1st data transfer only	D1	X
F	T	Write Dx stored if $\overline{BWn}$ = 0 in 2nd data transfer only	X	D2
F	F	Write Abort No Dx stored in either data transfer	X	X

Notes:
1. "1" = input "high"; "0" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".
2. If one or more $\overline{BWn}$ = 0, then $\overline{BW}$ = "T", else $\overline{BW}$ = "F".

Burst of 2 Nybble Write Clock Truth Table

$\overline{NW}$	$\overline{NW}$	Current Operation	D	D
K ↑ (t_{n+1})	$\overline{K}$ ↑ ($t_{n+1½}$)	K ↑ (t_n)	K ↑ (t_{n+1})	$\overline{K}$ ↑ ($t_{n+1½}$)
T	T	Write Dx stored if $\overline{NWn}$ = 0 in both data transfers	D1	D2
T	F	Write Dx stored if $\overline{NWn}$ = 0 in 1st data transfer only	D1	X
F	T	Write Dx stored if $\overline{NWn}$ = 0 in 2nd data transfer only	X	D2
F	F	Write Abort No Dx stored in either data transfer	X	X

Notes:
1. "1" = input "high"; "0" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".
2. If one or more $\overline{NWn}$ = 0, then $\overline{NW}$ = "T", else $\overline{NW}$ = "F".

x36 Byte Write Enable ($\overline{BWn}$) Truth Table

$\overline{BW0}$	$\overline{BW1}$	$\overline{BW2}$	$\overline{BW3}$	D0–D8	D9–D17	D18–D26	D27–D35
1	1	1	1	Don't Care	Don't Care	Don't Care	Don't Care
0	1	1	1	Data In	Don't Care	Don't Care	Don't Care
1	0	1	1	Don't Care	Data In	Don't Care	Don't Care
0	0	1	1	Data In	Data In	Don't Care	Don't Care
1	1	0	1	Don't Care	Don't Care	Data In	Don't Care
0	1	0	1	Data In	Don't Care	Data In	Don't Care
1	0	0	1	Don't Care	Data In	Data In	Don't Care
0	0	0	1	Data In	Data In	Data In	Don't Care
1	1	1	0	Don't Care	Don't Care	Don't Care	Data In
0	1	1	0	Data In	Don't Care	Don't Care	Data In
1	0	1	0	Don't Care	Data In	Don't Care	Data In
0	0	1	0	Data In	Data In	Don't Care	Data In
1	1	0	0	Don't Care	Don't Care	Data In	Data In
0	1	0	0	Data In	Don't Care	Data In	Data In
1	0	0	0	Don't Care	Data In	Data In	Data In
0	0	0	0	Data In	Data In	Data In	Data In

x18 Byte Write Enable ($\overline{BWn}$) Truth Table

$\overline{BW0}$	$\overline{BW1}$	D0–D8	D9–D17
1	1	Don't Care	Don't Care
0	1	Data In	Don't Care
1	0	Don't Care	Data In
0	0	Data In	Data In

x8 Nybble Write Enable ($\overline{NWn}$) Truth Table

$\overline{NW0}$	$\overline{NW1}$	D0–D3	D4–D7
1	1	Don't Care	Don't Care
0	1	Data In	Don't Care
1	0	Don't Care	Data In
0	0	Data In	Data In

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 2.9	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to V_{DD}	V
V_{REF}	Voltage in V_{REF} Pins	–0.5 to V_{DDQ}	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 2.9 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DDQ} +0.5 (≤ 2.9 V max.)	V
V_{TIN}	Input Voltage (TCK, TMS, TDI)	–0.5 to V_{DDQ} +0.5 (≤ 2.9V max.)	V
I_{IN}	Input Current on Any Pin	+/–100	mA dc
I_{OUT}	Output Current on Any I/O Pin	+/–100	mA dc
T_J	Maximum Junction Temperature	125	°C
T_{STG}	Storage Temperature	–55 to 125	°C

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

Power Supplies

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	1.7	1.8	1.9	V
I/O Supply Voltage	V_{DDQ}	1.4	—	V_{DD}	V
Reference Voltage	V_{REF}	$V_{DDQ}/2 - 0.05$	—	$V_{DDQ}/2 + 0.05$	V

Note:.
The power supplies need to be powered up simultaneously or in the following sequence: V_{DD}, V_{DDQ}, V_{REF}, followed by signal inputs. The power down sequence must be the reverse. V_{DDQ} must not exceed V_{DD}. For more information, read AN1021 SigmaQuad and SigmaDDR Power-Up.

Operating Temperature

Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction Temperature (Commercial Range Versions)	T_J	0	25	85	°C
Junction Temperature (Industrial Range Versions)*	T_J	–40	25	100	°C

Note:
* The part numbers of Industrial Temperature Range versions end with the character "I". Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

Thermal Impedance

Package	Test PCB Substrate	θ JA (C°/W) Airflow = 0 m/s	θ JA (C°/W) Airflow = 1 m/s	θ JA (C°/W) Airflow = 2 m/s	θ JB (C°/W)	θ JC (C°/W)
165 BGA	4-layer	16.4	13.4	12.4	8.6	1.2

Notes:
1. Thermal Impedance data is based on a number of of samples from mulitple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

HSTL I/O DC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
Input Reference Voltage	V_{REF}	V_{DDQ} /2 – 0.05	V_{DDQ} /2 + 0.05	V	—
Input High Voltage	V_{IH1}	V_{REF} + 0.1	V_{DDQ} + 0.3	V	1
Input Low Voltage	V_{IL1}	–0.3	V_{REF} – 0.1	V	1
Input High Voltage	V_{IH2}	0.7 * V_{DDQ}	V_{DDQ} + 0.3	V	2,3
Input Low Voltage	V_{IL2}	–0.3	0.3 * V_{DDQ}	V	2,3

Notes:
1. Parameters apply to K, $\overline{K}$, SA, DQ, R/$\overline{W}$, $\overline{BW}$, $\overline{LD}$ during normal operation and JTAG boundary scan testing.
2. Parameters apply to $\overline{Doff}$, ODT during normal operation and JTAG boundary scan testing.
3. Parameters apply to ZQ during JTAG boundary scan testing only.

HSTL I/O AC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
Input Reference Voltage	V_{REF}	V_{DDQ} /2 – 0.08	V_{DDQ} /2 + 0.08	V	—
Input High Voltage	V_{IH1}	V_{REF} + 0.2	V_{DDQ} + 0.5	V	1,2,3
Input Low Voltage	V_{IL1}	–0.5	V_{REF} – 0.2	V	1,2,3
Input High Voltage	V_{IH2}	V_{DDQ} – 0.2	V_{DDQ} + 0.5	V	4,5
Input Low Voltage	V_{IL2}	–0.5	0.2	V	4,5

Notes:
1. $V_{IH(MAX)}$ and $V_{IL(MIN)}$ apply for pulse widths less than one-quarter of the cycle time.
2. Input rise and fall times myust be a minimum of 1 V/ns, and within 10% of each other.
3. Parameters apply to K, $\overline{K}$, SA, DQ, R/$\overline{W}$, $\overline{BW}$, $\overline{LD}$ during normal operation and JTAG boundary scan testing.
4. Parameters apply to $\overline{Doff}$, ODT during normal operation and JTAG boundary scan testing.
5. Parameters apply to ZQ during JTAG boundary scan testing only.

Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 1.8 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	6	7	pF
Clock Capacitance	C_{CLK}	V_{IN} = 0 V	5	6	pF

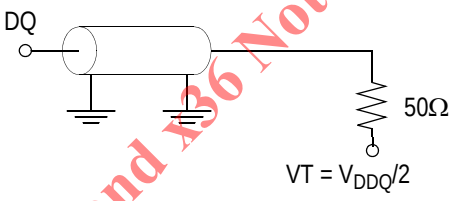
Note:
This parameter is sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	1.25 V
Input low level	0.25 V
Max. input slew rate	2 V/ns
Input reference level	0.75 V
Output reference level	V_{DDQ}/2

Note:
Test conditions as specified with output loading as shown unless otherwise noted.

AC Test Load Diagram



RQ = 250 Ω (HSTL I/O)
V_{REF} = 0.75 V

Input and Output Leakage Characteristics

Parameter	Symbol	Test Conditions	Min.	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–2 uA	2 uA
$\overline{\text{Doff}}$	$I_{IL\overline{DOFF}}$	V_{IN} = 0 to V_{DD}	–2 uA	100 uA
ODT	I_{ILODT}	V_{IN} = 0 to V_{DD}	–2 uA	100 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DDQ}	–2 uA	2 uA

HSTL I/O Output Driver DC Electrical Characteristics

Parameter	Symbol	Min.	Max.	Units	Notes
Output High Voltage	V_{OH1}	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$	V	1, 3
Output Low Voltage	V_{OL1}	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$	V	2, 3
Output High Voltage	V_{OH2}	$V_{DDQ} - 0.2$	—	V	4, 5
Output Low Voltage	V_{OL2}	—	0.2	V	4, 6

Notes:

1. $I_{OH} = (V_{DDQ}/2) / (RQ/5)$ +/– 15% @ $V_{OH} = V_{DDQ}/2$ (for: $175\Omega \le RQ \le 275\Omega$).
2. $I_{OL} = (V_{DDQ}/2) / (RQ/5)$ +/– 15% @ $V_{OL} = V_{DDQ}/2$ (for: $175\Omega \le RQ \le 275\Omega$).
3. Parameter tested with RQ = 250 Ω and V_{DDQ} = 1.5 V
4. $0\Omega \le RQ \le \infty\Omega$
5. I_{OH} = –1.0 mA
6. I_{OL} = 1.0 mA

Operating Currents

Parameter	Symbol	Test Conditions	-500		-450		-400		-350		Notes
			0° to 70°C	–40° to 85°C	0° to 70°C	–40° to 85°C	0° to 70°C	–40° to 85°C	0° to 70°C	–40° to 85°C	
Operating Current (x36): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0 mA Cycle Time ≥ t_{KHKH} Min	1300mA	1310mA	1190mA	1200mA	995mA	1005mA	895mA	905mA	2, 3
Operating Current (x18): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0 mA Cycle Time ≥ t_{KHKH} Min	1070mA	1080mA	1000mA	1010mA	895mA	905mA	800mA	810mA	2, 3
Operating Current (x9): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0 mA Cycle Time ≥ t_{KHKH} Min	1070mA	1080mA	1000mA	1010mA	895mA	905mA	800mA	810mA	2, 3
Operating Current (x8): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0 mA Cycle Time ≥ t_{KHKH} Min	1070mA	1080mA	1000mA	1010mA	895mA	905mA	800mA	810mA	2, 3
Standby Current (NOP): DDR	I_{SB1}	Device deselected, I^{OUT} = 0 mA, f = Max, All Inputs ≤ 0.2 V or ≥ V_{DD} – 0.2 V	315mA	325mA	305mA	315mA	290mA	300mA	275mA	285mA	2, 4

Notes:
1. Power measured with output pins floating.
2. Minimum cycle, I_{OUT} = 0 mA
3. Operating current is calculated with 50% read cycles and 50% write cycles.
4. Standby Current is only after all pending read and write burst operations are completed.

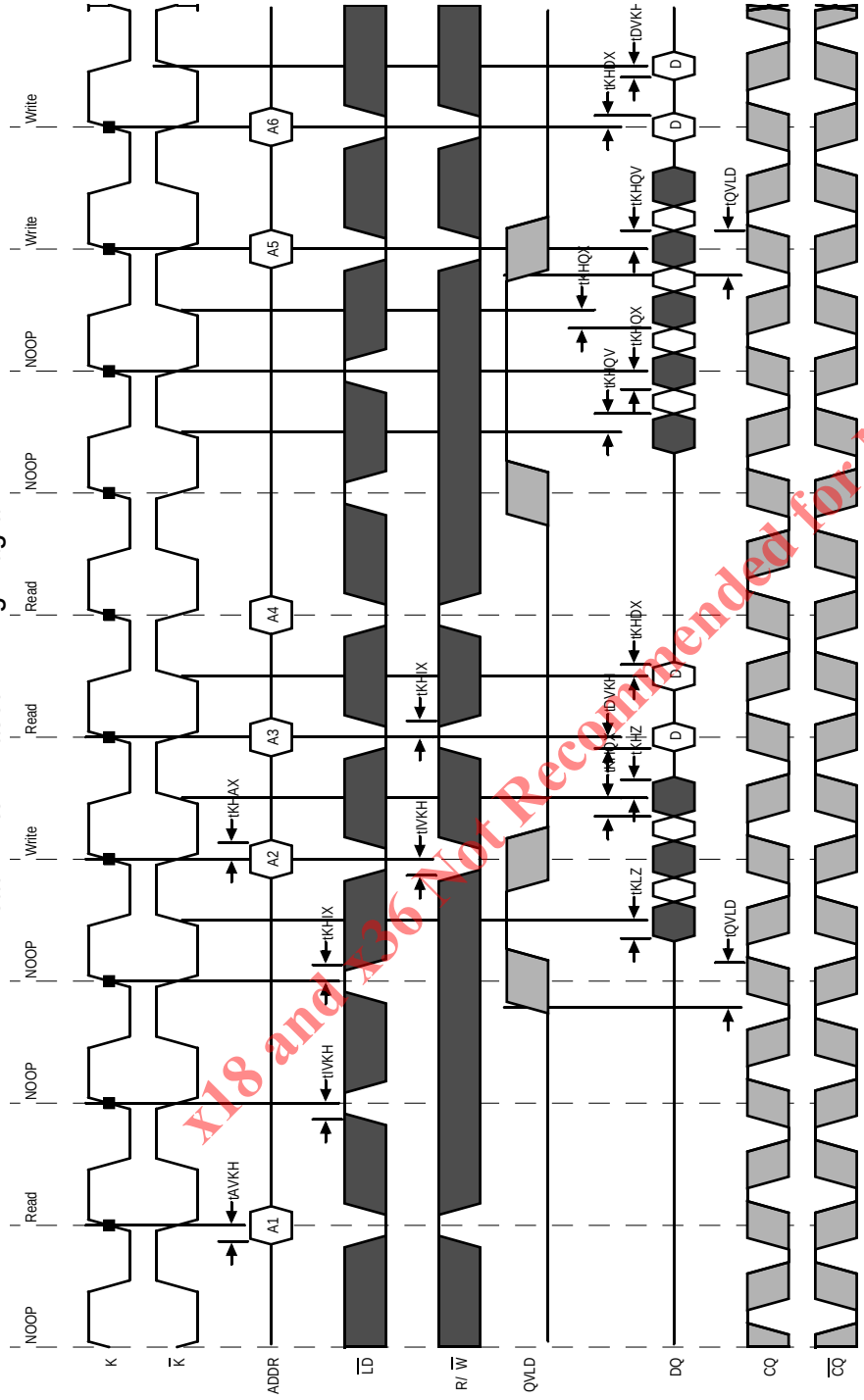
AC Electrical Characteristics

Parameter	Symbol	-500		-450		-400		-350		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock											
K, $\overline{K}$ Clock Cycle Time	t_{KHKH}	2.0	8.4	2.2	8.4	2.5	8.4	2.86	8.4	ns	
tK Variable	t_{KVar}	—	0.15	—	0.15	—	0.2	—	0.2	ns	4
K, $\overline{K}$ Clock High Pulse Width	t_{KHKL}	0.4	—	0.4	—	0.4	—	0.4	—	cycle	
K, $\overline{K}$ Clock Low Pulse Width	t_{KLKH}	0.4	—	0.4	—	0.4	—	0.4	—	cycle	
K to $\overline{K}$ High	$t_{KH\overline{K}H}$	0.85	—	0.94	—	1.06	—	1.23	—	ns	
$\overline{K}$ to K High	$t_{\overline{K}HKH}$	0.85	—	0.94	—	1.06	—	1.23	—	ns	
DLL Lock Time	t_{KLock}	2048	—	2048	—	2048	—	2048	—	cycle	5
K Static to DLL reset	t_{KReset}	30	—	30	—	30	—	30	—	ns	
Output Times											
K, $\overline{K}$ Clock High to Data Output Valid	t_{KHQV}	—	0.45	—	0.45	—	0.45	—	0.45	ns	
K, $\overline{K}$ Clock High to Data Output Hold	t_{KHQX}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	ns	
K, $\overline{K}$ Clock High to Echo Clock Valid	t_{KHCQV}	—	0.45	—	0.45	—	0.45	—	0.45	ns	
K, $\overline{K}$ Clock High to Echo Clock Hold	t_{KHCQX}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	ns	
CQ, $\overline{CQ}$ High Output Valid	t_{CQHQV}	—	0.15	—	0.15	—	0.2	—	0.23	ns	
CQ, $\overline{CQ}$ High Output Hold	t_{CQHQX}	–0.15	—	–0.15	—	–0.2	—	–0.23	—	ns	
CQ, $\overline{CQ}$ High to QLVD	t_{QVLD}	–0.15	0.15	–0.15	0.15	–0.2	0.2	–0.23	0.23	ns	
CQ Phase Distortion	$t_{CQH\overline{CQ}H}$ $t_{\overline{CQ}HCQH}$	0.75	—	0.85	—	1.0	—	1.18	—	ns	
K Clock High to Data Output High-Z	t_{KHQZ}	—	0.45	—	0.45	—	0.45	—	0.45	ns	
K Clock High to Data Output Low-Z	t_{KHQX1}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	ns	
Setup Times											
Address Input Setup Time	t_{AVKH}	0.25	—	0.275	—	0.4	—	0.4	—	ns	1
Control Input Setup Time ($\overline{RW}$, $\overline{LD}$)	t_{IVKH}	0.25	—	0.275	—	0.4	—	0.4	—	ns	2
Control Input Setup Time ($\overline{BWX}$)	t_{IVKH}	0.2	—	0.22	—	0.28	—	0.28	—	ns	3
Data Input Setup Time	t_{DVKH}	0.2	—	0.22	—	0.28	—	0.28	—	ns	
Hold Times											
Address Input Hold Time	t_{KHAX}	0.25	—	0.275	—	0.4	—	0.4	—	ns	1
Control Input Hold Time ($\overline{RW}$, $\overline{LD}$)	t_{KHIX}	0.25	—	0.275	—	0.4	—	0.4	—	ns	2
Control Input Hold Time ($\overline{BWX}$)	t_{KHIX}	0.2	—	0.22	—	0.28	—	0.28	—	ns	3
Data Input Hold Time	t_{KHDX}	0.2	—	0.22	—	0.28	—	0.28	—	ns	

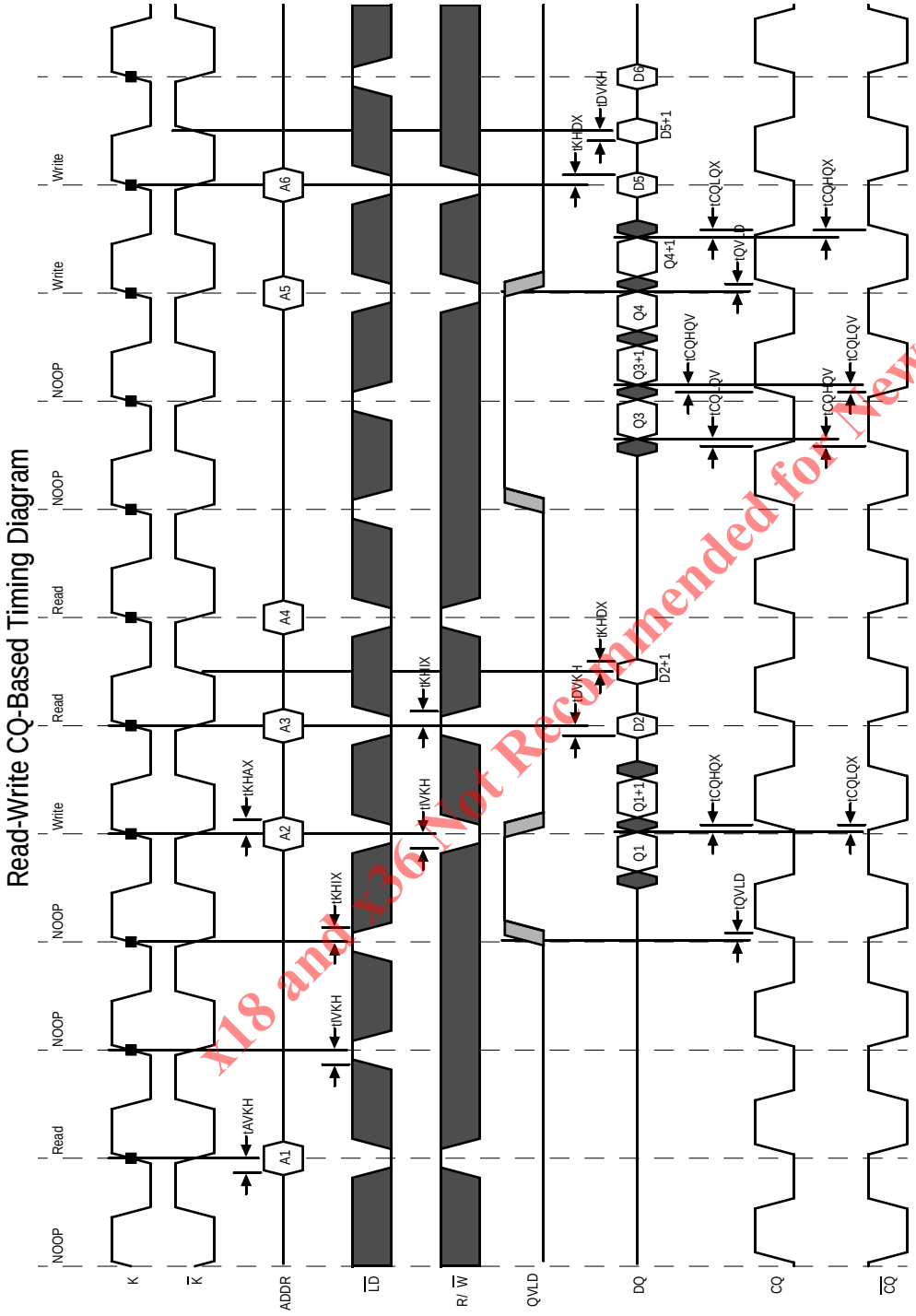
Notes:

1. All Address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control signals are $\overline{RW}$, $\overline{LD}$.
3. Control signals are $\overline{BW0}$, $\overline{BW1}$ and ($\overline{BW2}$, $\overline{BW3}$ for x36).
4. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
5. V_{DD} slew rate must be less than 0.1 V DC per 50 ns for DLL lock retention. DLL lock time begins once V_{DD} and input clock are stable.

Read-Write K-Based Timing Diagram



Read-Write CQ-Based Timing Diagram



JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with V_{DD}. The JTAG output drivers are powered by V_{DD}.

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits.To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either V_{DD} or V_{SS}. TDO should be left unconnected.

JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

JTAG Port Registers

Overview

The various JTAG registers, refered to as Test Access Port or TAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

Bypass Register

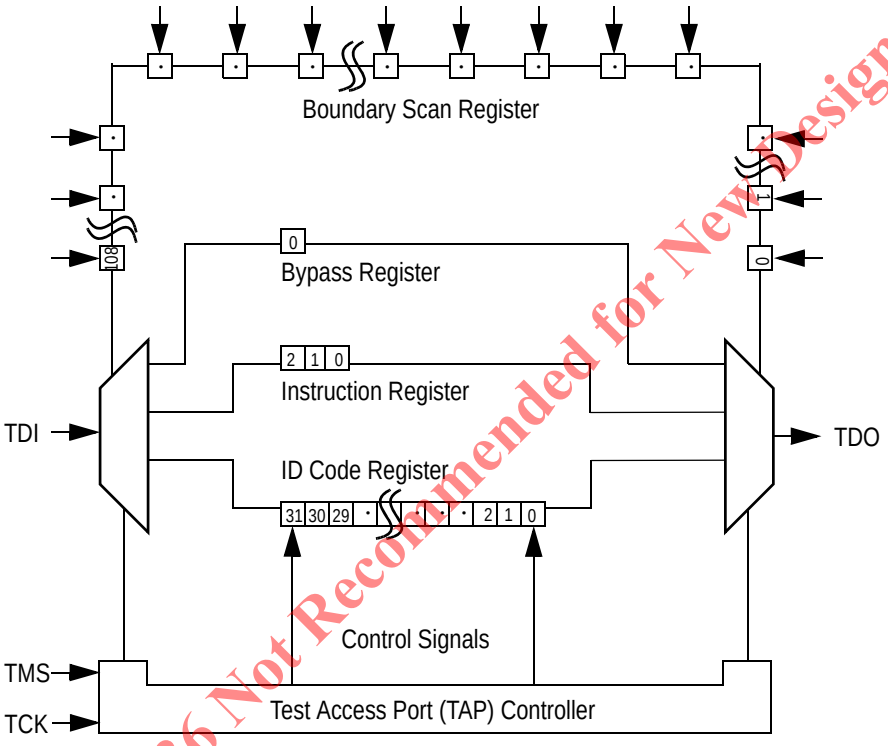
The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan

Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

JTAG TAP Block Diagram



Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Contents

	See BSDL Model																			GSI Technology JEDEC Vendor ID Code										Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	1	1	0	0	1	1

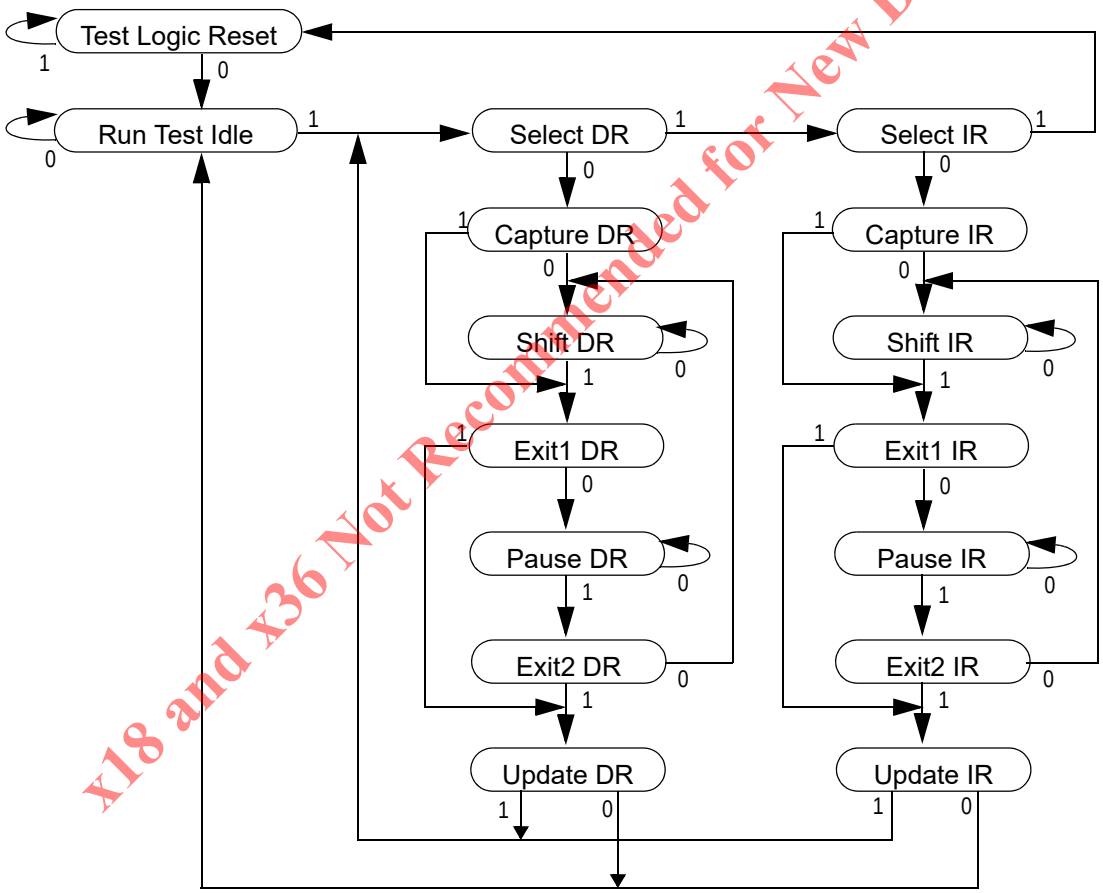
Tap Controller Instruction Set

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG Tap Controller State Diagram



Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time (tTS plus tTH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM's input pins; therefore, the RAM's internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register's contents, in parallel, on the RAM's data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the sate of all the RAM's input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM's output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z.	1
GSI	011	GSI Private Instruction.	1
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI	101	GSI Private Instruction.	1
GSI	110	GSI Private Instruction.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

JTAG Port Recommended Operating Conditions and DC Characteristics

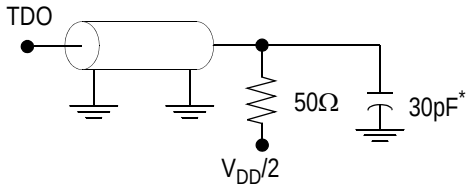
Parameter	Symbol	Min.	Max.	Unit	Notes
Test Port Input Low Voltage	V_{ILJ}	–0.3	0.3 * V_{DD}	V	1
Test Port Input High Voltage	V_{IHJ}	0.7 * V_{DD}	V_{DD} +0.3	V	1
TMS, TCK and TDI Input Leakage Current	I_{INHJ}	–300	1	uA	2
TMS, TCK and TDI Input Leakage Current	I_{INLJ}	–1	100	uA	3
TDO Output Leakage Current	I_{OLJ}	–1	1	uA	4
Test Port Output High Voltage	V_{OHJ}	V_{DD} – 0.2	—	V	5, 6
Test Port Output Low Voltage	V_{OLJ}	—	0.2	V	5, 7
Test Port Output CMOS High	V_{OHJC}	V_{DD} – 0.1	—	V	5, 8
Test Port Output CMOS Low	V_{OLJC}	—	0.1	V	5, 9

Notes:
1. Input Under/overshoot voltage must be –1 V < Vi < V_{DDn} +1 V not to exceed V maximum, with a pulse width not to exceed 20% tTKC.
2. $V_{ILJ} \leq V_{IN} \leq V_{DDn}$
3. 0 V $\leq V_{IN} \leq V_{ILJn}$
4. Output Disable, V_{OUT} = 0 to V_{DDn}
5. The TDO output driver is served by the V_{DD} supply.
6. I_{OHJ} = –2 mA
7. I_{OLJ} = + 2 mA
8. I_{OHJC} = –100 uA
9. I_{OLJC} = +100 uA

JTAG Port AC Test Conditions

Parameter	Conditions
Input high level	V_{DD} – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DD}/2$
Output reference level	$V_{DD}/2$

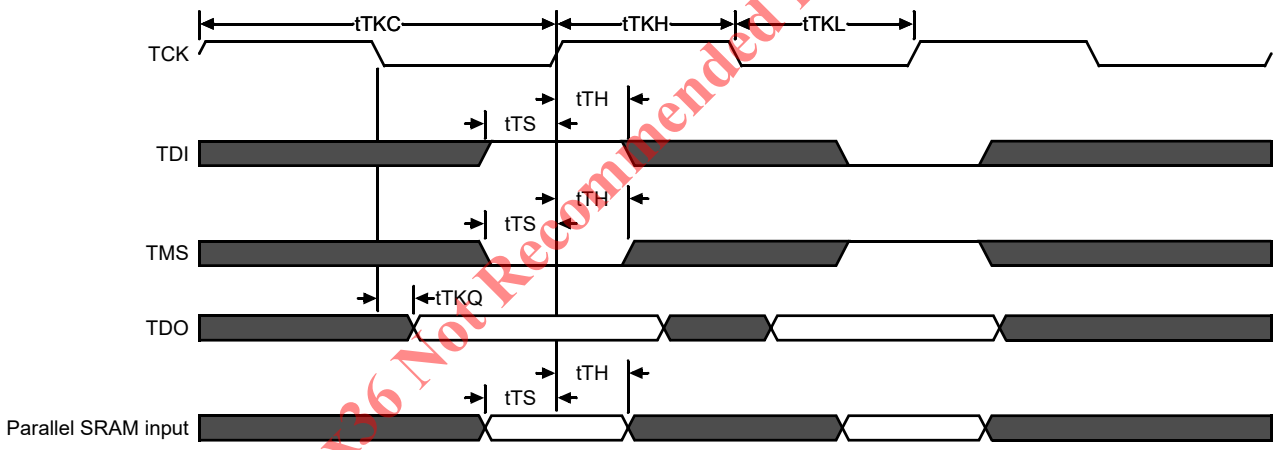
JTAG Port AC Test Load



* Distributed Test Jig Capacitance

Notes:
1. Include scope and jig capacitance.
2. Test conditions as shown unless otherwise noted.

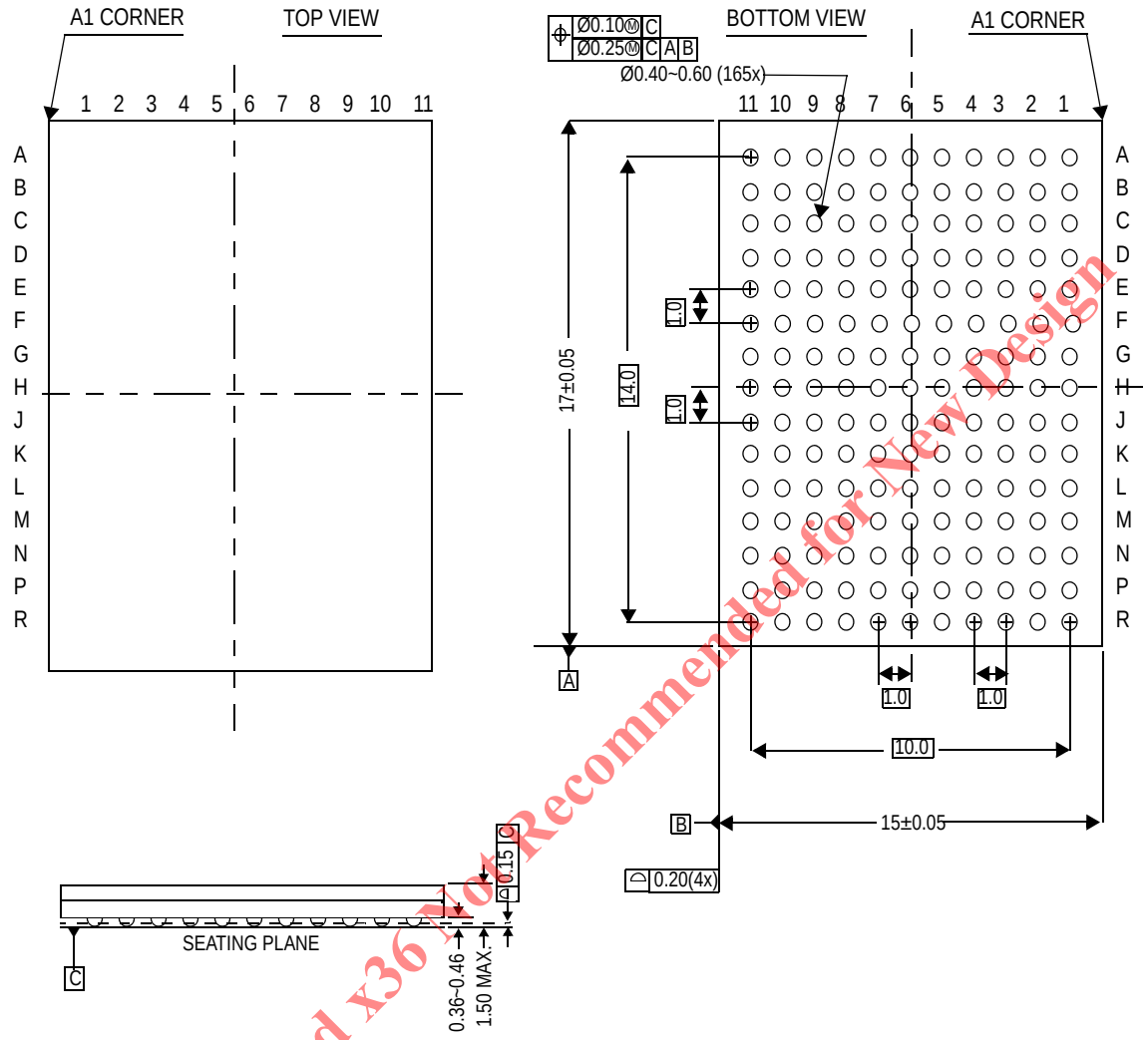
JTAG Port Timing Diagram



JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	tTKC	50	—	ns
TCK Low to TDO Valid	tTKQ	—	20	ns
TCK High Pulse Width	tTKH	20	—	ns
TCK Low Pulse Width	tTKL	20	—	ns
TDI & TMS Set Up Time	tTS	10	—	ns
TDI & TMS Hold Time	tTH	10	—	ns

Package Dimensions—165-Bump FPBGA (Package E)



Ordering Information GSI SigmaDDR-II+ SRAM

Org	Part Number[1]	Type	Package	Speed (MHz)	T_J[2]
16M x 8	GS81302T06E-500	SigmaDDR-II+ SRAM	165-bump BGA	500	C
16M x 8	GS81302T06E-450	SigmaDDR-II+ SRAM	165-bump BGA	450	C
16M x 8	GS81302T06E-400	SigmaDDR-II+ SRAM	165-bump BGA	400	C
16M x 8	GS81302T06E-350	SigmaDDR-II+ SRAM	165-bump BGA	350	C
16M x 8	GS81302T06E-500I	SigmaDDR-II+ SRAM	165-bump BGA	500	I
16M x 8	GS81302T06E-450I	SigmaDDR-II+ SRAM	165-bump BGA	450	I
16M x 8	GS81302T06E-400I	SigmaDDR-II+ SRAM	165-bump BGA	400	I
16M x 8	GS81302T06E-350I	SigmaDDR-II+ SRAM	165-bump BGA	350	I
16M x 8	GS81302T06GE-500	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	500	C
16M x 8	GS81302T06GE-450	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	450	C
16M x 8	GS81302T06GE-400	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	400	C
16M x 8	GS81302T06GE-350	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	350	C
16M x 8	GS81302T06GE-500I	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	500	I
16M x 8	GS81302T06GE-450I	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	450	I
16M x 8	GS81302T06GE-400I	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	400	I
16M x 8	GS81302T06GE-350I	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	350	I
16M x 9	GS81302T11E-500	SigmaDDR-II+ SRAM	165-bump BGA	500	C
16M x 9	GS81302T11E-450	SigmaDDR-II+ SRAM	165-bump BGA	450	C
16M x 9	GS81302T11E-400	SigmaDDR-II+ SRAM	165-bump BGA	400	C
16M x 9	GS81302T11E-350	SigmaDDR-II+ SRAM	165-bump BGA	350	C
16M x 9	GS81302T11E-500I	SigmaDDR-II+ SRAM	165-bump BGA	500	I
16M x 9	GS81302T11E-450I	SigmaDDR-II+ SRAM	165-bump BGA	450	I
16M x 9	GS81302T11E-400I	SigmaDDR-II+ SRAM	165-bump BGA	400	I
16M x 9	GS81302T11E-350I	SigmaDDR-II+ SRAM	165-bump BGA	350	I
16M x 9	GS81302T11GE-500	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	500	C
16M x 9	GS81302T11GE-450	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	450	C
16M x 9	GS81302T11GE-400	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	400	C
16M x 9	GS81302T11GE-350	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	350	C
16M x 9	GS81302T11GE-500I	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	500	I
16M x 9	GS81302T11GE-450I	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	450	I
16M x 9	GS81302T11GE-400I	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	400	I

Notes:

1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS81302T38E-400T.
2. C = Commercial Temperature Range. I = Industrial Temperature Range.

Ordering Information GSI SigmaDDR-II+ SRAM

Org	Part Number[1]	Type	Package	Speed (MHz)	T_J[2]
16M x 9	GS81302T11GE-350I	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	350	I
8M x 18	GS81302T20E-500	SigmaDDR-II+ SRAM	165-bump BGA	500	C
8M x 18	GS81302T20E-450	SigmaDDR-II+ SRAM	165-bump BGA	450	C
8M x 18	GS81302T20E-400	SigmaDDR-II+ SRAM	165-bump BGA	400	C
8M x 18	GS81302T20E-350	SigmaDDR-II+ SRAM	165-bump BGA	350	C
8M x 18	GS81302T20E-500I	SigmaDDR-II+ SRAM	165-bump BGA	500	I
8M x 18	GS81302T20E-450I	SigmaDDR-II+ SRAM	165-bump BGA	450	I
8M x 18	GS81302T20E-400I	SigmaDDR-II+ SRAM	165-bump BGA	400	I
8M x 18	GS81302T20E-350I	SigmaDDR-II+ SRAM	165-bump BGA	350	I
8M x 18	GS81302T20GE-500	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	500	C
8M x 18	GS81302T20GE-450	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	450	C
8M x 18	GS81302T20GE-400	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	400	C
8M x 18	GS81302T20GE-350	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	350	C
8M x 18	GS81302T20GE-500I	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	500	I
8M x 18	GS81302T20GE-450I	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	450	I
8M x 18	GS81302T20GE-400I	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	400	I
8M x 18	GS81302T20GE-350I	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	350	I
4M x 36	GS81302T38E-500	SigmaDDR-II+ SRAM	165-bump BGA	500	C
4M x 36	GS81302T38E-450	SigmaDDR-II+ SRAM	165-bump BGA	450	C
4M x 36	GS81302T38E-400	SigmaDDR-II+ SRAM	165-bump BGA	400	C
4M x 36	GS81302T38E-350	SigmaDDR-II+ SRAM	165-bump BGA	350	C
4M x 36	GS81302T38E-500I	SigmaDDR-II+ SRAM	165-bump BGA	500	I
4M x 36	GS81302T38E-450I	SigmaDDR-II+ SRAM	165-bump BGA	450	I
4M x 36	GS81302T38E-400I	SigmaDDR-II+ SRAM	165-bump BGA	400	I
4M x 36	GS81302T38E-350I	SigmaDDR-II+ SRAM	165-bump BGA	350	I
4M x 36	GS81302T38GE-500	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	500	C
4M x 36	GS81302T38GE-450	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	450	C
4M x 36	GS81302T38GE-400	SigmaDDR-II+ SRAM	RoHS-compliant 165-bump BGA	400	C

Notes:
1. Customers requiring delivery in Tape and Reel should add the character "T" to the end of the part number. Example: GS81302T38E-400T.
2. C = Commercial Temperature Range. I = Industrial Temperature Range.

