165-Bump BGA
Commercial Temp
Industrial Temp

72Mb SigmaDDR-II™ Burst of 2 ECCRAM™

400 MHz–200 MHz
1.8 V V_{DD}
1.8 V and 1.5 V_{DDQ}

Features

- On-Chip ECC with virtually zero SER
- Simultaneous Read and Write SigmaDDR™ Interface
- Common I/O bus
- JEDEC-standard pinout and package
- Double Data Rate interface
- Byte Write Capability
- Burst of 2 Read and Write
- 1.8 V +100/–100 mV core power supply
- 1.5 V or 1.8 V HSTL Interface
- Pipelined read operation with self-timed Late Write
- Fully coherent read and write pipelines
- ZQ pin for programmable output drive strength
- IEEE 1149.1 JTAG-compliant Boundary Scan
- Pin-compatible with 18Mb, 36Mb and 144Mb devices
- 165-bump, 15 mm x 17 mm, 1 mm bump pitch BGA package
- RoHS-compliant 165-bump BGA package available

SigmaDDR™ ECCRAM Overview

The GS8672T18/36BE SigmaDDR-II ECCRAMs are built in compliance with the SigmaDDR-II SRAM pinout standard for Common I/O synchronous SRAMs. They are 75,497,472-bit (72Mb) SRAMs. The GS8672T18/36BE SigmaDDR-II SRAMs are just one element in a family of low power, low voltage HSTL I/O SRAMs designed to operate at the speeds needed to implement economical high performance networking systems.

Clocking and Addressing Schemes

The GS8672T18/36BE SigmaDDR-II SRAMs are synchronous devices. They employ two input register clock inputs, K and $\overline{K}$. K and $\overline{K}$ are independent single-ended clock inputs, not differential inputs to a single differential clock input buffer. The device also allows the user to manipulate the output register clock inputs quasi independently with the C and $\overline{C}$ clock inputs. C and $\overline{C}$ are also independent single-ended clock inputs, not differential inputs. If the C clocks are tied high, the K clocks are routed internally to fire the output registers instead.

Each internal read and write operation in a SigmaDDR-II B2 ECCRAM is two times wider than the device I/O bus. An input data bus de-multiplexer is used to accumulate incoming data before it is simultaneously written to the memory array. An output data multiplexer is used to capture the data produced from a single memory array read and then route it to the appropriate output drivers as needed.

When a new address is loaded into the part, A0 is used to initialize the pointers that control the data multiplexer / de-multiplexer so the ECCRAM can perform "critical word first" operations. From an external address point of view, regardless of the starting point, the data transfers always follow the same sequence {0, 1} or {1, 0} (where the digits shown represent A0).

On-Chip Error Correction Code

GSI's ECCRAMs implement an ECC algorithm that detects and corrects all single-bit memory errors, including those induced by Soft Error Rate (SER) events such as cosmic rays, alpha particles etc. The resulting SER of these devices is anticipated to be <0.002 FITs/Mb — a 5-order-of-magnitude improvement over comparable SRAMs with no On-Chip ECC, which typically have an SER of 200 FITs/Mb or more. SER quoted above is based on reading taken at sea level.

However, the On-Chip Error Correction (ECC) will be disabled if a "Half Write" operation is initiated. See the **Byte Write Contol** section for further information.

Parameter Synopsis

	-400	-333	-300	-250	-200
tKHKH	2.5 ns	3.0 ns	3.3 ns	4.0 ns	5.0 ns
tKHQV	0.45 ns	0.45 ns	0.45 ns	0.45 ns	0.45 ns

2M x 36 SigmaDDR-II SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{\text{CQ}}$	NF (144Mb)	SA	R/$\overline{\text{W}}$	$\overline{\text{BW2}}$	$\overline{\text{K}}$	$\overline{\text{BW1}}$	$\overline{\text{LD}}$	SA	SA	CQ
B	NC	DQ27	DQ18	SA	$\overline{\text{BW3}}$	K	$\overline{\text{BW0}}$	SA	NC	NC	DQ8
C	NC	NC	DQ28	V_{SS}	SA	SA0	SA	V_{SS}	NC	DQ17	DQ7
D	NC	DQ29	DQ19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	DQ16
E	NC	NC	DQ20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQ15	DQ6
F	NC	DQ30	DQ21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	DQ31	DQ22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ14
H	$\overline{\text{Doff}}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	DQ32	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ13	DQ4
K	NC	NC	DQ23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ12	DQ3
L	NC	DQ33	DQ24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	DQ34	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ11	DQ1
N	NC	DQ35	DQ25	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	DQ10
P	NC	NC	DQ26	SA	SA	C	SA	SA	NC	DQ9	DQ0
R	TDO	TCK	SA	SA	SA	$\overline{\text{C}}$	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—13 x 15 mm^2 Body—1 mm Bump Pitch

Notes:

1. $\overline{\text{BW0}}$ controls writes to DQ0:DQ8; $\overline{\text{BW1}}$ controls writes to DQ9:DQ17; $\overline{\text{BW2}}$ controls writes to DQ18:DQ26; $\overline{\text{BW3}}$ controls writes to DQ27:DQ35.

4M x 18 SigmaDDR-II SRAM—Top View

	1	2	3	4	5	6	7	8	9	10	11
A	$\overline{CQ}$	SA	SA	R/$\overline{W}$	$\overline{BW1}$	$\overline{K}$	NF	$\overline{LD}$	SA	SA	CQ
B	NC	DQ9	NF	SA	NF	K	$\overline{BW0}$	SA	NC	NC	DQ8
C	NC	NC	NF	V_{SS}	SA	SA0	SA	V_{SS}	NC	DQ7	NF
D	NC	NF	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NF
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NF	DQ6
F	NC	DQ12	NF	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NF	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NF
H	$\overline{Doff}$	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NF	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NF
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NF	DQ3
L	NC	DQ15	NF	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NF	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NF
N	NC	NF	DQ16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NF
P	NC	NC	DQ17	SA	SA	C	SA	SA	NC	NF	DQ0
R	TDO	TCK	SA	SA	SA	$\overline{C}$	SA	SA	SA	TMS	TDI

11 x 15 Bump BGA—13 x 15 mm^2 Body—1 mm Bump Pitch

Notes:

1. $\overline{BW0}$ controls writes to DQ0:DQ8; $\overline{BW1}$ controls writes to DQ9:DQ17.

Pin Description Table

Symbol	Description	Type	Comments
SA	Synchronous Address Inputs	Input	—
R/$\overline{W}$	Synchronous Read/Write	Input	—
$\overline{BW0}$–$\overline{BW3}$	Synchronous Byte Writes	Input	Active Low
$\overline{LD}$	Synchronous Load Pin	Input	Active Low
K	Input Clock	Input	Active High
$\overline{K}$	Input Clock	Input	Active Low
C	Output Clock	Input	Active High
$\overline{C}$	Output Clock	Input	Active Low
TMS	Test Mode Select	Input	—
TDI	Test Data Input	Input	—
TCK	Test Clock Input	Input	—
TDO	Test Data Output	Output	—
V_{REF}	HSTL Input Reference Voltage	Input	—
ZQ	Output Impedance Matching Input	Input	—
DQ	Data I/O	Input/Output	Three State
$\overline{Doff}$	Disable DLL when low	Input	Active Low
CQ	Output Echo Clock	Output	—
$\overline{CQ}$	Output Echo Clock	Output	—
V_{DD}	Power Supply	Supply	1.8 V Nominal
V_{DDQ}	Isolated Output Buffer Supply	Supply	1.8 V or 1.5 V Nominal
V_{SS}	Power Supply: Ground	Supply	—
NC	No Connect	—	—
NF	No Function	—	—

Notes:

1. NC = Not Connected to die or any other pin
2. NF = No Function. There is an electrical connection to this input pin, but the signal has no function in the device. It can be left unconnected, or tied to V_{SS} or V_{DDQ}.
3. C, $\overline{C}$, K, or $\overline{K}$ cannot be set to V_{REF} voltage.

Background

Common I/O SRAMs, from a system architecture point of view, are attractive in read dominated or block transfer applications. Therefore, the SigmaDDR-II ECCRAM interface and truth table are optimized for burst reads and writes. Common I/O SRAMs are unpopular in applications where alternating reads and writes are needed because bus turnaround delays can cut high speed Common I/O SRAM data bandwidth in half.

Burst Operations

Read and write operations are "burst" operations. In every case where a read or write command is accepted by the ECCRAM, it will respond by issuing or accepting two beats of data, executing a data transfer on subsequent rising edges of K and $\overline{\text{K}}$, as illustrated in the timing diagrams. This means that it is possible to load new addresses every K clock cycle. Addresses can be loaded less often, if intervening deselect cycles are inserted.

Deselect Cycles

Chip Deselect commands are pipelined to the same degree as read commands. This means that if a deselect command is applied to the ECCRAM on the next cycle after a read command captured by the ECCRAM, the device will complete the two beat read data transfer and then execute the deselect command, returning the output drivers to high-Z. A high on the $\overline{\text{LD}}$ pin prevents the RAM from loading read or write command inputs and puts the RAM into deselect mode as soon as it completes all outstanding burst transfer operations.

SigmaDDR-II ECCRAM Read Cycles

The SRAM executes pipelined reads. The status of the Address, $\overline{\text{LD}}$ and R/$\overline{\text{W}}$ pins are evaluated on the rising edge of K. The read command ($\overline{\text{LD}}$ low and R/$\overline{\text{W}}$ high) is clocked into the SRAM by a rising edge of K. After the next rising edge of K, the SRAM produces data out in response to the next rising edge of $\overline{\text{C}}$ (or the next rising edge of $\overline{\text{K}}$, if C and $\overline{\text{C}}$ are tied high). The second beat of data is transferred on the next rising edge of C, for a total of two transfers per address load.

SigmaDDR-II ECCRAM Write Cycles

The status of the Address, $\overline{\text{LD}}$ and R/$\overline{\text{W}}$ pins are evaluated on the rising edge of K. The ECCRAM executes "late write" data transfers. Data in is due at the device inputs on the rising edge of K following the rising edge of K clock used to clock in the write command ($\overline{\text{LD}}$ and R/$\overline{\text{W}}$ low) and the write address. To complete the remaining beat of the burst of two write transfer, the ECCRAM captures data in on the next rising edge of $\overline{\text{K}}$, for a total of two transfers per address load.

Power-Up Sequence for SigmaDDR-II ECCRAMs

SigmaDDR-II ECCRAMs must be powered-up in a specific sequence in order to avoid undefined operations.

1. After power supplies power-up and clocks (K, $\overline{K}$) are stablized, 163,840 cycles are required to set Output Driver Impedance.
2. Thereafter, an additional 65,536 clock cycles are required to lock the DLL after it has been enabled.
3. Begin Read and Write operations.

For more information, read **AN1021 SigmaQuad and SigmaDDR Power-Up.**

On-Chip Error Correction

SigmaDDR-II ECCRAMs implement a single-bit error detection and correction algorithm (specifically, a Hamming Code) on each DDR data word (comprising two 9-bit data bytes) transmitted on each 9-bit data bus (i.e., transmitted on D/Q[8:0], D/Q[17:9], D/Q[26:18], or D/Q[35:27]). To accomplish this, 5 ECC parity bits (invisible to the user) are utilized per every 18 data bits (visible to the user).

The ECC algorithm neither corrects nor detects multi-bit errors. However, GSI ECCRAMs are architected in such a way that a single SER event very rarely causes a multi-bit error across any given "transmitted data unit", where a "transmitted data unit" represents the data transmitted as the result of a single read or write operation to a particular address. The extreme rarity of multi-bit errors results in the SER mentioned previously (i.e., <0.002 FITs/Mb measured at sea level.)

Not only does the on-chip ECC significantly improve SER performance, but it also frees up the entire memory array for data storage. Very often SRAM applications allocate 1/9th of the memory array (i.e., one "error bit" per eight "data bits", in any 9-bit "data byte") for error detection (either simple parity error detection, or system-level ECC error detection and correction). Such error-bit allocation is unnecessary with ECCRAMs the entire memory array can be utilized for data storage, effectively providing 12.5% greater storage capacity compared to SRAMs of the same density not equipped with on-chip ECC.

Output Register Control

SigmaDDR-II ECCRAMs offer two mechanisms for controlling the output data registers. Typically, control is handled by the Output Register Clock inputs, C and $\overline{C}$. The Output Register Clock inputs can be used to make small phase adjustments in the firing of the output registers by allowing the user to delay driving data out as much as a few nanoseconds beyond the next rising edges of the K and $\overline{K}$ clocks. If the C and $\overline{C}$ clock inputs are tied high, the RAM reverts to K and $\overline{K}$ control of the outputs, allowing the RAM to function as a conventional pipelined read ECCRAM.

Special Functions

Byte Write Control

Byte Write Enable pins are sampled at the same time that Data In is sampled. A High on the Byte Write Enable pin associated with a particular byte (e.g., $\overline{\text{BW}}$0 controls D0–D8 inputs) will inhibit the storage of that particular byte, leaving whatever data may be stored at the current address at that byte location undisturbed. Any or all of the Byte Write Enable pins may be driven High or Low during the data in sample times in a write sequence.

Each write enable command and write address loaded into the RAM provides the base address for a 2-beat data transfer. The x18 version of the RAM, for example, may write 36 bits in association with each address loaded. Any 9-bit byte may be masked in any write sequence.

Note: If "Half Write" operations (i.e., write operations in which a $\overline{\text{BW}}$n pin is asserted for only half of a DDR write data transfer on the associated 9-bit data bus, causing only 9 bits of the 18-bit DDR data word to be written) are initiated, the on-chip ECC will be disabled for as long as the SRAM remains powered up thereafter. This must be done because ECC is implemented across entire 18-bit data words, rather than across individual 9-bit data bytes.

Byte Write Truth Table

The truth table below applies to write operations to Address "m", where Address "m" is the 18-bit memory location comprising the 2 beats of DDR write data associated with each $\overline{\text{BW}}$*n* pin in a given clock cycle.

$\overline{\text{BW}}$*n*		Input Data Byte *n*		Operation	Result
↑ K (Beat 1)	↑$\overline{\text{K}}$ (Beat 2)	↑K (Beat 1)	↑$\overline{\text{K}}$ (Beat 2)		
0	0	D0	D1	Full Write	D0 and D1 written to Address m
0	1	D0	X	Half Write	Only D0 written to Address m
1	0	X	D1	Half Write	Only D1 written to Address m
1	1	X	X	Abort	Address m unchanged

Notes:

1. $\overline{\text{BW0}}$ is associated with Input Data Byte D[8:0].
2. $\overline{\text{BW1}}$ is associated with Input Data Byte D[17:9].
3. $\overline{\text{BW2}}$ is associated with Input Data Byte D[26:18] (in x36 only).
4. BW3 is associated with Input Data Byte D[35:27] (in x36 only).
5. ECC is disabled if a "Half Write" operation is initiated.

FLXDrive-II Output Driver Impedance Control

HSTL I/O SigmaDDR-II ECCRAMs are supplied with programmable impedance output drivers. The ZQ pin must be connected to V_{SS} via an external resistor, RQ, to allow the ECCRAM to monitor and adjust its output driver impedance. The value of RQ must be 5X the value of the desired RAM output impedance. The allowable range of RQ to guarantee impedance matching continuously is between 175Ω and 275Ω. Periodic readjustment of the output driver impedance is necessary as the impedance is affected by drifts in supply voltage and temperature. The ECCRAM's output impedance circuitry compensates for drifts in supply voltage and temperature. A clock cycle counter periodically triggers an impedance evaluation, resets and counts again. Each impedance evaluation may move the output driver impedance level one step at a time towards the optimum level. The output driver is implemented with discrete binary weighted impedance steps.

Common I/O SigmaDDR-II ECCRAM Truth Table

K_n	$\overline{LD}$	$R/\overline{W}$	DQ		Operation
			A + 0	A + 1	
↑	1	X	Hi-Z	Hi-Z	Deselect
↑	0	0	D@K_{n+1}	D@$\overline{K}_{n+1}$	Write
↑	0	1	Q@$\overline{K}_{n+1}$ or $\overline{C}_{n+1}$	Q@K_{n+2} or C_{n+2}	Read

Note:
Q is controlled by K clocks if C clocks are not used.

Byte Write Clock Truth Table

$\overline{BW}$	$\overline{BW}$	Current Operation	D	D
K ↑ (t_{n+1})	$\overline{K}$ ↑ ($t_{n+1½}$)	K ↑ (t_n)	K ↑ (t_{n+1})	$\overline{K}$ ↑ ($t_{n+1½}$)
T	T	Write Dx stored if $\overline{BWn}$ = 0 in both data transfers	D1	D2
T	F	Write Dx stored if $\overline{BWn}$ = 0 in 1st data transfer only	D1	X
F	T	Write Dx stored if $\overline{BWn}$ = 0 in 2nd data transfer only	X	D2
F	F	Write Abort No Dx stored in either data transfer	X	X

Notes:
1. "1" = input "high"; "0" = input "low"; "X" = input "don't care"; "T" = input "true"; "F" = input "false".
2. If one or more $\overline{BWn}$ = 0, then $\overline{BW}$ = "T", else $\overline{BW}$ = "F".

x36 Byte Write Enable ($\overline{\text{BWn}}$) Truth Table

$\overline{\text{BW0}}$	$\overline{\text{BW1}}$	$\overline{\text{BW2}}$	$\overline{\text{BW3}}$	D0–D8	D9–D17	D18–D26	D27–D35
1	1	1	1	Don’t Care	Don’t Care	Don’t Care	Don’t Care
0	1	1	1	Data In	Don’t Care	Don’t Care	Don’t Care
1	0	1	1	Don’t Care	Data In	Don’t Care	Don’t Care
0	0	1	1	Data In	Data In	Don’t Care	Don’t Care
1	1	0	1	Don’t Care	Don’t Care	Data In	Don’t Care
0	1	0	1	Data In	Don’t Care	Data In	Don’t Care
1	0	0	1	Don’t Care	Data In	Data In	Don’t Care
0	0	0	1	Data In	Data In	Data In	Don’t Care
1	1	1	0	Don’t Care	Don’t Care	Don’t Care	Data In
0	1	1	0	Data In	Don’t Care	Don’t Care	Data In
1	0	1	0	Don’t Care	Data In	Don’t Care	Data In
0	0	1	0	Data In	Data In	Don’t Care	Data In
1	1	0	0	Don’t Care	Don’t Care	Data In	Data In
0	1	0	0	Data In	Don’t Care	Data In	Data In
1	0	0	0	Don’t Care	Data In	Data In	Data In
0	0	0	0	Data In	Data In	Data In	Data In

x18 Byte Write Enable ($\overline{\text{BWn}}$) Truth Table

$\overline{\text{BW0}}$	$\overline{\text{BW1}}$	D0–D8	D9–D17
1	1	Don’t Care	Don’t Care
0	1	Data In	Don’t Care
1	0	Don’t Care	Data In
0	0	Data In	Data In

Absolute Maximum Ratings

(All voltages reference to V_{SS})

Symbol	Description	Value	Unit
V_{DD}	Voltage on V_{DD} Pins	–0.5 to 2.4	V
V_{DDQ}	Voltage in V_{DDQ} Pins	–0.5 to V_{DD}	V
V_{REF}	Voltage in V_{REF} Pins	–0.5 to V_{DDQ}	V
$V_{I/O}$	Voltage on I/O Pins	–0.5 to V_{DDQ} +0.5 (≤ 2.4 V max.)	V
V_{IN}	Voltage on Other Input Pins	–0.5 to V_{DDQ} +0.5 (≤ 2.4 V max.)	V
I_{IN}	Input Current on Any Pin	+/–100	mA dc
I_{OUT}	Output Current on Any I/O Pin	+/–100	mA dc
T_J	Maximum Junction Temperature	125	^oC
T_{STG}	Storage Temperature	–55 to 125	^oC

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

Power Supplies

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	V_{DD}	1.7	1.8	1.9	V
I/O Supply Voltage	V_{DDQ}	1.4	—	V_{DD}	V
Reference Voltage	V_{REF}	V_{DDQ}/2 – 0.05	—	V_{DDQ}/2 + 0.05	V

Note:
The power supplies need to be powered up simultaneously or in the following sequence: V_{DD}, V_{DDQ}, V_{REF}, followed by signal inputs. The power down sequence must be the reverse. V_{DDQ} must not exceed V_{DD}. For more information, read AN1021 SigmaQuad and SigmaDDR Power-Up.

Operating Temperature

Parameter	Symbol	Min.	Typ.	Max.	Unit
Junction Temperature (Commercial Range Versions)	T_J	0	25	85	°C
Junction Temperature (Industrial Range Versions)*	T_J	–40	25	100	°C

Note:
* The part numbers of Industrial Temperature Range versions end with the character “I”. Unless otherwise noted, all performance specifications quoted are evaluated for worst case in the temperature range marked on the device.

Thermal Impedance

Package	Test PCB Substrate	θ JA (C°/W) Airflow = 0 m/s	θ JA (C°/W) Airflow = 1 m/s	θ JA (C°/W) Airflow = 2 m/s	θ JB (C°/W)	θ JC (C°/W)
165 BGA	4-layer	15.25	12.38	11.41	4.79	1.31

Notes:
1. Thermal Impedance data is based on a number of of samples from mulitple lots and should be viewed as a typical number.
2. Please refer to JEDEC standard JESD51-6.
3. The characteristics of the test fixture PCB influence reported thermal characteristics of the device. Be advised that a good thermal path to the PCB can result in cooling or heating of the RAM depending on PCB temperature.

HSTL I/O DC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
DC Input Logic High	V_{IH} (dc)	V_{REF} + 0.1	V_{DDQ} + 0.3 V	V	1
DC Input Logic Low	V_{IL} (dc)	–0.3 V	V_{REF} – 0.1	V	1

Notes:
1. Compatible with both 1.8 V and 1.5 V I/O drivers.
2. These are DC test criteria. DC design criteria is V_{REF} ± 50 mV. The AC V_{IH}/V_{IL} levels are defined separately for measuring timing parameters.
3. V_{IL} (Min) DC = –0.3 V, V_{IL}(Min) AC = –1.5 V (pulse width $\leq$ 3 ns).
4. V_{IH} (Max) DC = V_{DDQ} + 0.3 V, V_{IH}(Max) AC = V_{DDQ} + 0.85 V (pulse width $\leq$ 3 ns).

HSTL I/O AC Input Characteristics

Parameter	Symbol	Min	Max	Units	Notes
AC Input Logic High	V_{IH} (ac)	V_{REF} + 0.2	—	V	2,3
AC Input Logic Low	V_{IL} (ac)	—	V_{REF} – 0.2	V	2,3
V_{REF} Peak-to-Peak AC Voltage	V_{REF} (ac)	—	5% V_{REF} (DC)	V	1

Notes:
1. The peak-to-peak AC component superimposed on V_{REF} may not exceed 5% of the DC component of V_{REF}.
2. To guarantee AC characteristics, V_{IH},V_{IL}, Trise, and Tfall of inputs and clocks must be within 10% of each other.
3. For devices supplied with HSTL I/O input buffers. Compatible with both 1.8 V and 1.5 V I/O drivers.

Capacitance

(T_A = 25°C, f = 1 MHz, V_{DD} = 1.8 V)

Parameter	Symbol	Test conditions	Typ.	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0 V	4	5	pF
Output Capacitance	C_{OUT}	V_{OUT} = 0 V	4.5	5.5	pF

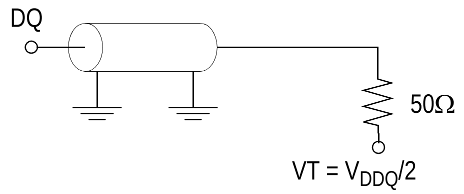
Note:
This parameter is sample tested.

AC Test Conditions

Parameter	Conditions
Input high level	1.25 V
Input low level	0 .25 V
Max. input slew rate	2 V/ns
Input reference level	0.75
Output reference level	$V_{DDQ}/2$

Note:
Test conditions as specified with output loading as shown unless otherwise noted.

AC Test Load Diagram



RQ = 250 Ω (HSTL I/O)
V_{REF} = 0.75 V

Input and Output Leakage Characteristics

Parameter	Symbol	Test Conditions	Min.	Max
Input Leakage Current (except mode pins)	I_{IL}	V_{IN} = 0 to V_{DD}	–2 uA	2 uA
$\overline{\text{Doff}}$	$I_{IL\ \overline{DOFF}}$	V_{IN} = 0 to V_{DD}	–2 uA	100 uA
Output Leakage Current	I_{OL}	Output Disable, V_{OUT} = 0 to V_{DDQ}	–2 uA	2 uA

*Assuming stable conditions, the RAM can achieve optimum impedance within 1024 cycles.

Programmable Impedance HSTL Output Driver DC Electrical Characteristics

Parameter	Symbol	Min.	Max.	Units	Notes
Output High Voltage	V_{OH1}	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$	V	1
Output Low Voltage	V_{OL1}	$V_{DDQ}/2 - 0.12$	$V_{DDQ}/2 + 0.12$	V	2
Output High Voltage	V_{OH2}	$V_{DDQ} - 0.2$	V_{DDQ}	V	3, 4
Output Low Voltage	V_{OL2}	Vss	0.2	V	3, 5
Output Driver Impedance	R_{OUT}	(RQ/5) * 0.88	(RQ/5) * 1.12	Ω	6, 7

Notes:
1. $I_{OH} = (V_{DDQ}/2) / (RQ/5)$ +/– 15% @ $V_{OH} = V_{DDQ}/2$ (for: $175\Omega \leq RQ \leq 275\Omega$).
2. $I_{OL} = (V_{DDQ}/2) / (RQ/5)$ +/– 15% @ $V_{OL} = V_{DDQ}/2$ (for: $175\Omega \leq RQ \leq 275\Omega$).
3. $0\Omega \leq RQ \leq \infty\Omega$
4. $I_{OH} = -1.0$ mA
5. $I_{OL} = 1.0$ mA
6. Parameter applies when $175\Omega \leq RQ \leq 275\Omega$
7. Tested at $V_{OUT} = V_{DDQ} * 0.2$ and $V_{DDQ} * 0.8$

Operating Currents

Parameter	Symbol	Test Conditions	-400		-333		-300		-250		-200		Notes
			0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	0 to 70°C	–40 to 85°C	
Operating Current (x36): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0 mA Cycle Time ≥ t_{KHKH} Min	1430 mA	1450 mA	1260 mA	1280 mA	1180 mA	1200 mA	1040 mA	1060 mA	900 mA	920 mA	1, 2
Operating Current (x18): DDR	I_{DD}	V_{DD} = Max, I_{OUT} = 0 mA Cycle Time ≥ t_{KHKH} Min	1070 mA	1090 mA	950 mA	970 mA	890 mA	910 mA	800 mA	820 mA	700 mA	720 mA	1, 2

Notes:

1. Minimum cycle, I_{OUT} = 0 mA
2. Operating current is calculated with 50% read cycles and 50% write cycles.

AC Electrical Characteristics

Parameter	Symbol	-400		-333		-300		-250		-200		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Clock													
K, $\overline{K}$ Clock Cycle Time C, $\overline{C}$ Clock Cycle Time	t_{KHKH} t_{CHCH}	2.5	8.4	3.0	8.4	3.3	8.4	4.0	8.4	5.0	8.4	ns	
tKC Variable	t_{KCVar}	—	0.2	—	0.2	—	0.2	—	0.2	—	0.2	ns	6
K, $\overline{K}$ Clock High Pulse Width C, $\overline{C}$ Clock High Pulse Width	t_{KHKL} t_{CHCL}	1.0	—	1.2	—	1.32	—	1.6	—	2.0	—	ns	
K, $\overline{K}$ Clock Low Pulse Width C, $\overline{C}$ Clock Low Pulse Width	t_{KLKH} t_{CLCH}	1.0	—	1.2	—	1.32	—	1.6	—	2.0	—	ns	
K to $\overline{K}$ High C to $\overline{C}$ High	$t_{KH\overline{K}H}$ $t_{CH\overline{C}H}$	1.0	—	1.35	—	1.49	—	1.8	—	2.2	—	ns	
$\overline{K}$ to K High $\overline{C}$ to C High	$t_{\overline{K}HKH}$ $t_{\overline{C}HCH}$	1.0	—	1.35	—	1.49	—	1.8	—	2.2	—	ns	
K, $\overline{K}$ Clock High to C, $\overline{C}$ Clock High	t_{KHCH}	0	1.1	0	1.1	0	1.1	0	1.1	0	1.1	ns	
DLL Lock Time	t_{KCLock}	65,536	—	65,536	—	65,536	—	65,536	—	65,536	—	cycle	7
K Static to DLL reset	$t_{KCReset}$	30	—	30	—	30	—	30	—	30	—	ns	
Output Times													
K, $\overline{K}$ Clock High to Data Output Valid C, $\overline{C}$ Clock High to Data Output Valid	t_{KHQV} t_{CHQV}	—	0.45	—	0.45	—	0.45	—	0.45	—	0.45	ns	4
K, $\overline{K}$ Clock High to Data Output Hold C, $\overline{C}$ Clock High to Data Output Hold	t_{KHQX} t_{CHQX}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	–0.45	—	ns	4
K, $\overline{K}$ Clock High to Echo Clock Valid C, $\overline{C}$ Clock High to Echo Clock Valid	t_{KHCQV} t_{CHCQV}	—	0.45	—	0.45	—	0.45	—	0.45	—	0.45	ns	
K, $\overline{K}$ Clock High to Echo Clock Hold C, $\overline{C}$ Clock High to Echo Clock Hold	t_{KHCQX} t_{CHCQX}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	–0.45	—	ns	
CQ, $\overline{CQ}$ High Output Valid	t_{CQHQV}	—	0.25	—	0.25	—	0.27	—	0.30	—	0.35	ns	8
CQ, $\overline{CQ}$ High Output Hold	t_{CQHQX}	–0.25	—	–0.25	—	–0.27	—	–0.30	—	–0.35	—	ns	8
CQ Phase Distortion	$t_{CQH\overline{CQ}H}$ $t_{\overline{CQ}HCQH}$	0.9	—	1.10	—	1.24	—	1.55	—	1.95	—	ns	
K Clock High to Data Output High-Z C Clock High to Data Output High-Z	t_{KHQZ} t_{CHQZ}	—	0.45	—	0.45	—	0.45	—	0.45	—	0.45	ns	4
K Clock High to Data Output Low-Z C Clock High to Data Output Low-Z	t_{KHQX1} t_{CHQX1}	–0.45	—	–0.45	—	–0.45	—	–0.45	—	–0.45	—	ns	4
Setup Times													
Address Input Setup Time	t_{AVKH}	0.4	—	0.4	—	0.4	—	0.5	—	0.6	—	ns	1
Control Input Setup Time (R/$\overline{W}$, $\overline{LD}$)	t_{IVKH}	0.4	—	0.4	—	0.4	—	0.5	—	0.6	—	ns	2
Control Input Setup Time ($\overline{BWX}$)	t_{IVKH}	0.28	—	0.28	—	0.3	—	0.35	—	0.4	—	ns	3
Data Input Setup Time	t_{DVKH}	0.28	—	0.28	—	0.3	—	0.35	—	0.4	—	ns	

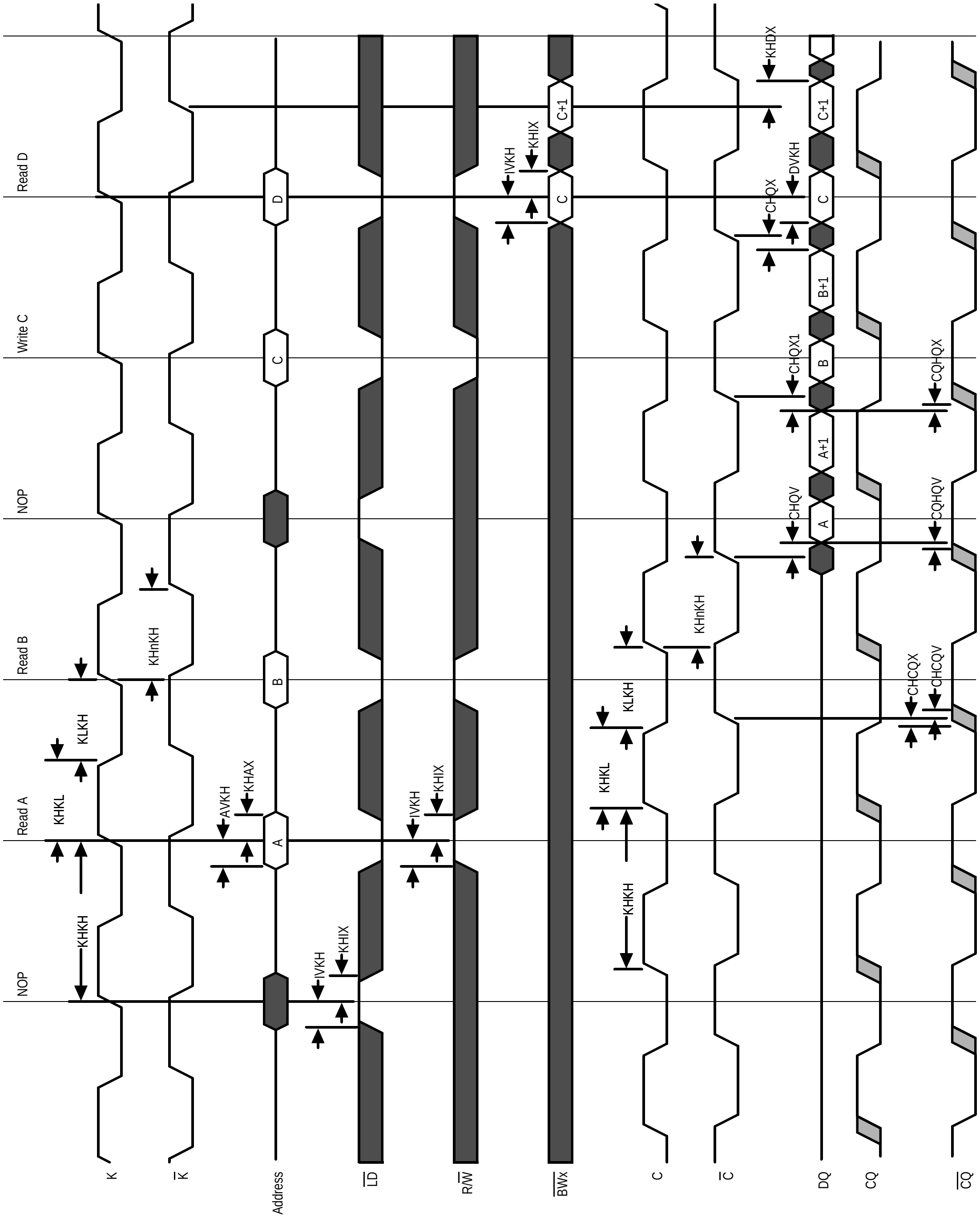
AC Electrical Characteristics

Parameter	Symbol	-400		-333		-300		-250		-200		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max		
Hold Times													
Address Input Hold Time	t_{KHAX}	0.4	—	0.4	—	0.4	—	0.5	—	0.6	—	ns	1
Control Input Hold Time (R/$\overline{W}$, $\overline{LD}$)	t_{KHIX}	0.4	—	0.4	—	0.4	—	0.5	—	0.6	—	ns	2
Control Input Setup Time ($\overline{BWX}$)	t_{IVKH}	0.28	—	0.28	—	0.3	—	0.35	—	0.4	—	ns	3
Data Input Hold Time	t_{KHDX}	0.28	—	0.28	—	0.3	—	0.35	—	0.4	—	ns	

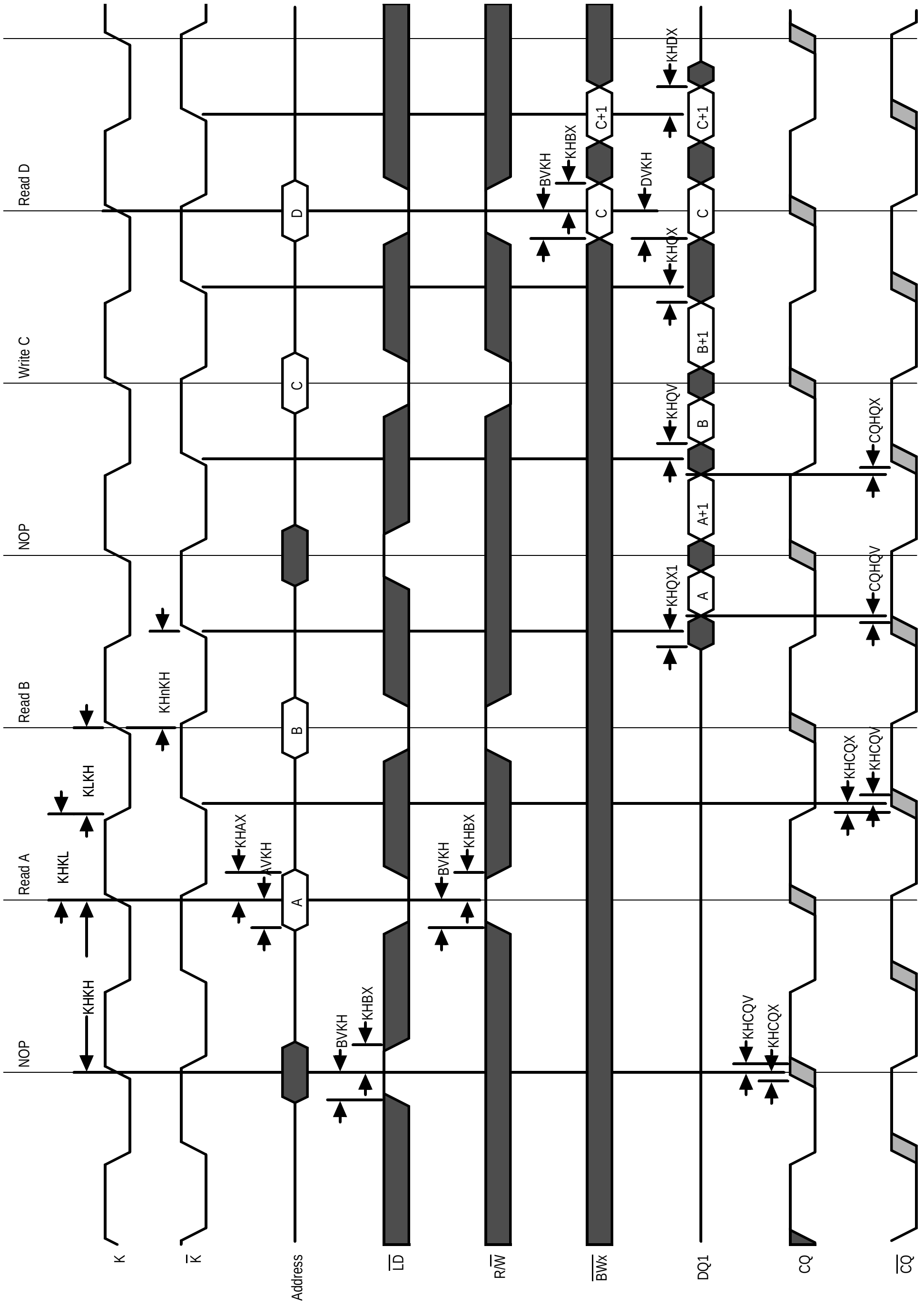
Notes:

1. All Address inputs must meet the specified setup and hold times for all latching clock edges.
2. Control signals are $\overline{LD}$, R/$\overline{W}$.
3. Control signals are $\overline{BW0}$, $\overline{BW1}$, and ($\overline{BW2}$, $\overline{BW3}$ for x36).
4. If C, $\overline{C}$ are tied high, K, $\overline{K}$ become the references for C, $\overline{C}$ timing parameters
5. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.
6. V_{DD} slew rate must be less than 0.1 V DC per 50 ns for DLL lock retention. DLL lock time begins once V_{DD} and input clock are stable.

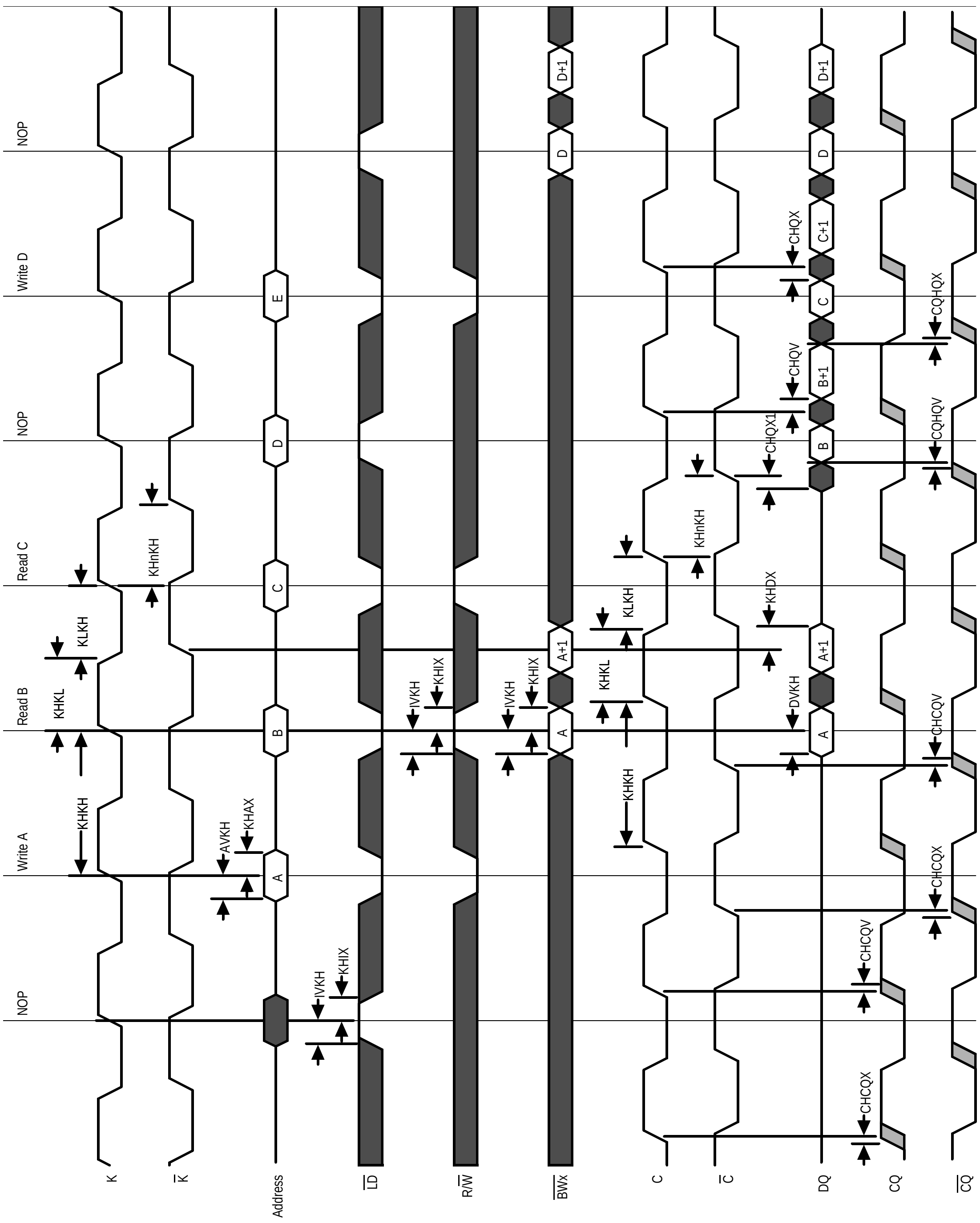
C and $\overline{C}$ Controlled Read First Timing Diagram



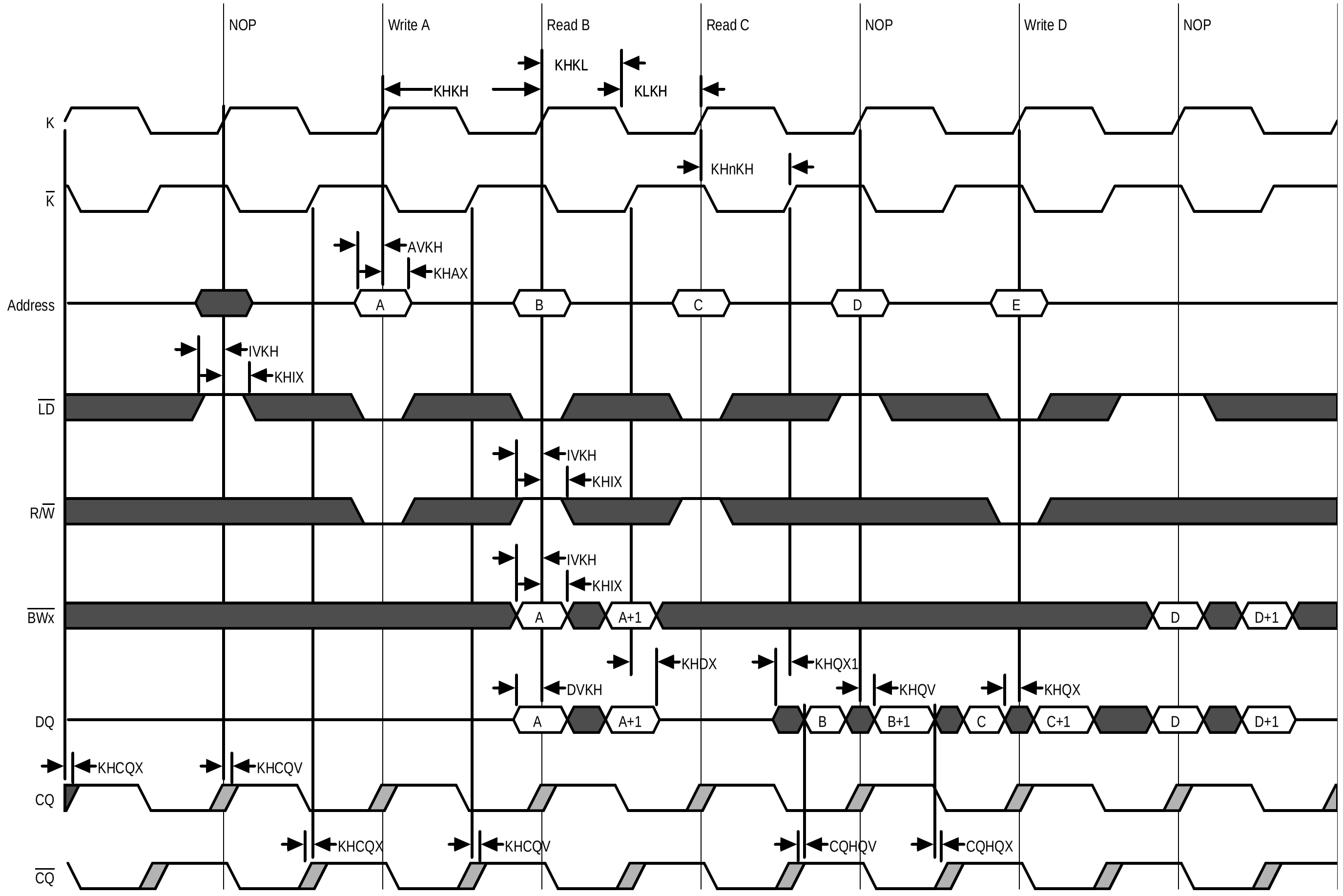
K and $\overline{K}$ Controlled Read First Timing Diagram



C and $\overline{C}$ Controlled Write First Timing Diagram



K and $\overline{K}$ Controlled Write First Timing Diagram



JTAG Port Operation

Overview

The JTAG Port on this RAM operates in a manner that is compliant with IEEE Standard 1149.1-1990, a serial boundary scan interface standard (commonly referred to as JTAG). The JTAG Port input interface levels scale with V_{DD}. The JTAG output drivers are powered by V_{DD}.

Disabling the JTAG Port

It is possible to use this device without utilizing the JTAG port. The port is reset at power-up and will remain inactive unless clocked. TCK, TDI, and TMS are designed with internal pull-up circuits.To assure normal operation of the RAM with the JTAG Port unused, TCK, TDI, and TMS may be left floating or tied to either V_{DD} or V_{SS}. TDO should be left unconnected.

JTAG Pin Descriptions

Pin	Pin Name	I/O	Description
TCK	Test Clock	In	Clocks all TAP events. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.
TMS	Test Mode Select	In	The TMS input is sampled on the rising edge of TCK. This is the command input for the TAP controller state machine. An undriven TMS input will produce the same result as a logic one input level.
TDI	Test Data In	In	The TDI input is sampled on the rising edge of TCK. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP Controller state machine and the instruction that is currently loaded in the TAP Instruction Register (refer to the TAP Controller State Diagram). An undriven TDI pin will produce the same result as a logic one input level.
TDO	Test Data Out	Out	Output that is active depending on the state of the TAP state machine. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.

Note:
This device does not have a TRST (TAP Reset) pin. TRST is optional in IEEE 1149.1. The Test-Logic-Reset state is entered while TMS is held high for five rising edges of TCK. The TAP Controller is also reset automaticly at power-up.

JTAG Port Registers

Overview

The various JTAG registers, refered to as Test Access Port or TAP Registers, are selected (one at a time) via the sequences of 1s and 0s applied to TMS as TCK is strobed. Each of the TAP Registers is a serial shift register that captures serial input data on the rising edge of TCK and pushes serial data out on the next falling edge of TCK. When a register is selected, it is placed between the TDI and TDO pins.

Instruction Register

The Instruction Register holds the instructions that are executed by the TAP controller when it is moved into the Run, Test/Idle, or the various data register states. Instructions are 3 bits long. The Instruction Register can be loaded when it is placed between the TDI and TDO pins. The Instruction Register is automatically preloaded with the IDCODE instruction at power-up or whenever the controller is placed in Test-Logic-Reset state.

Bypass Register

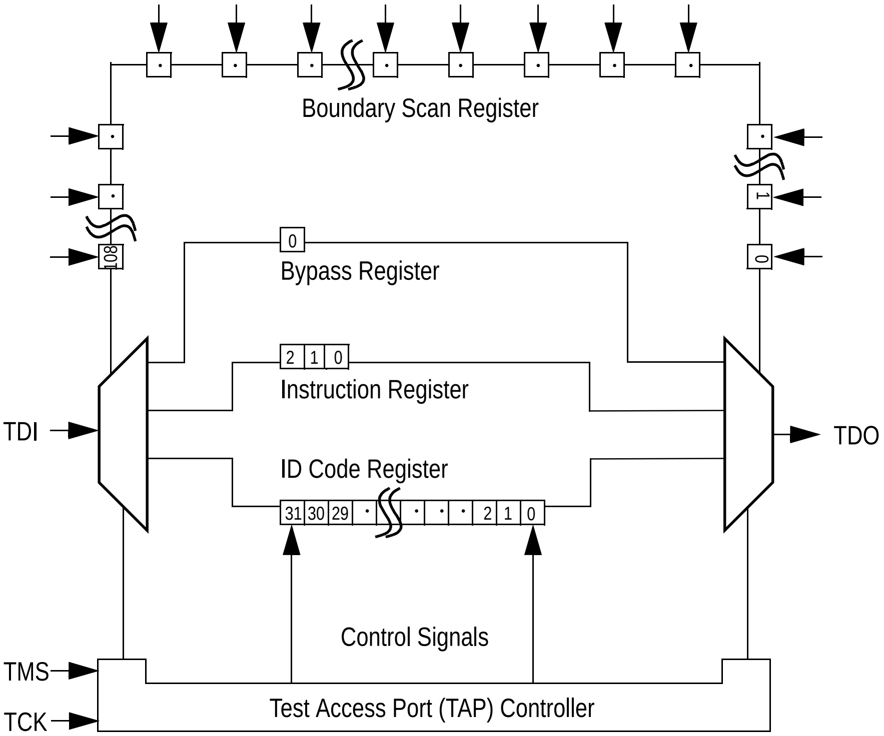
The Bypass Register is a single bit register that can be placed between TDI and TDO. It allows serial test data to be passed through the RAM's JTAG Port to another device in the scan chain with as little delay as possible.

Boundary Scan Register

The Boundary Scan Register is a collection of flip flops that can be preset by the logic level found on the RAM's input or I/O pins. The flip flops are then daisy chained together so the levels found can be shifted serially out of the JTAG Port's TDO pin. The Boundary Scan Register also includes a number of place holder flip flops (always set to a logic 1). The relationship between the device pins and the bits in the Boundary Scan Register is described in the Scan Order Table following. The Boundary Scan

Register, under the control of the TAP Controller, is loaded with the contents of the RAMs I/O ring when the controller is in Capture-DR state and then is placed between the TDI and TDO pins when the controller is moved to Shift-DR state. SAMPLE-Z, SAMPLE/PRELOAD and EXTEST instructions can be used to activate the Boundary Scan Register.

JTAG TAP Block Diagram



Identification (ID) Register

The ID Register is a 32-bit register that is loaded with a device and vendor specific 32-bit code when the controller is put in Capture-DR state with the IDCODE command loaded in the Instruction Register. The code is loaded from a 32-bit on-chip ROM. It describes various attributes of the RAM as indicated below. The register is then placed between the TDI and TDO pins when the controller is moved into Shift-DR state. Bit 0 in the register is the LSB and the first to reach TDO when shifting begins.

ID Register Contents

	Not Used																				GSI Technology JEDEC Vendor ID Code											Presence Register
Bit #	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	1	1	0	1	1	0	0	1	1

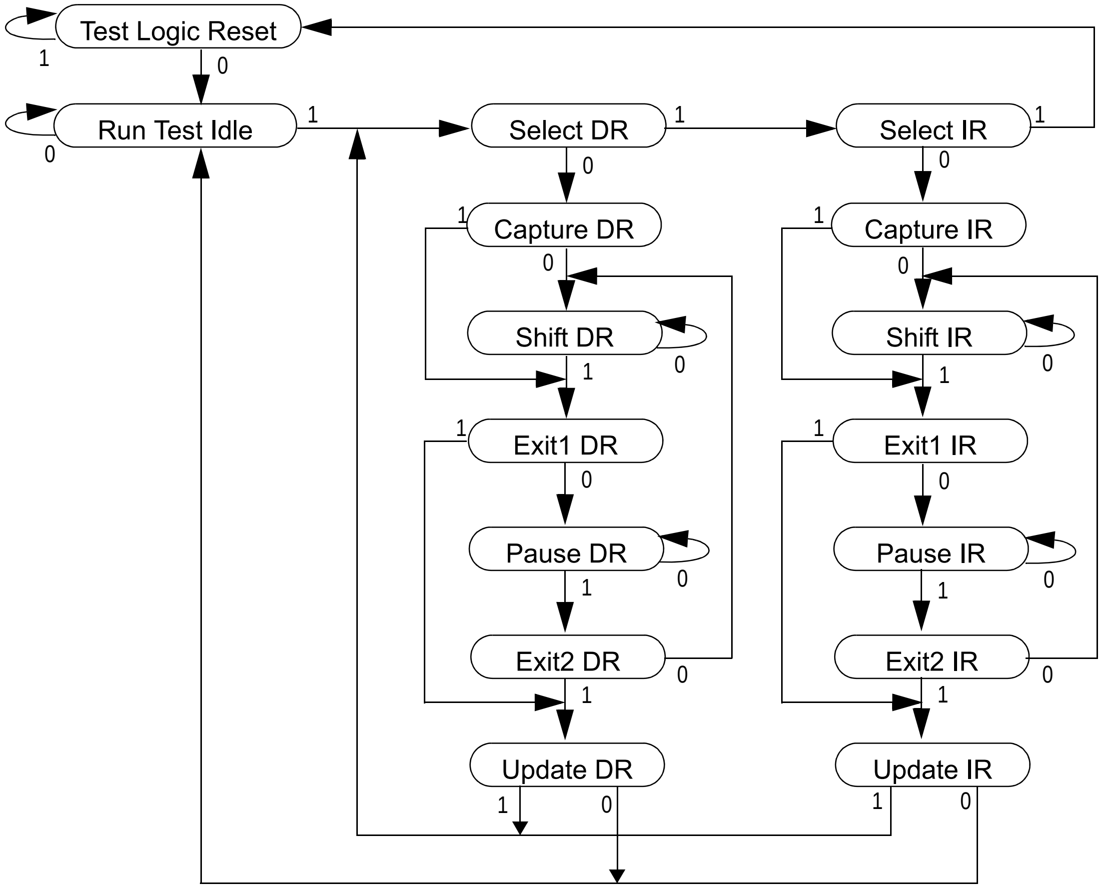
Tap Controller Instruction Set

Overview

There are two classes of instructions defined in the Standard 1149.1-1990; the standard (Public) instructions, and device specific (Private) instructions. Some Public instructions are mandatory for 1149.1 compliance. Optional Public instructions must be implemented in prescribed ways. The TAP on this device may be used to monitor all input and I/O pads, and can be used to load address, data or control signals into the RAM or to preload the I/O buffers.

When the TAP controller is placed in Capture-IR state the two least significant bits of the instruction register are loaded with 01. When the controller is moved to the Shift-IR state the Instruction Register is placed between TDI and TDO. In this state the desired instruction is serially loaded through the TDI input (while the previous contents are shifted out at TDO). For all instructions, the TAP executes newly loaded instructions only when the controller is moved to Update-IR state. The TAP instruction set for this device is listed in the following table.

JTAG Tap Controller State Diagram



Instruction Descriptions

BYPASS

When the BYPASS instruction is loaded in the Instruction Register the Bypass Register is placed between TDI and TDO. This occurs when the TAP controller is moved to the Shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.

SAMPLE/PRELOAD

SAMPLE/PRELOAD is a Standard 1149.1 mandatory public instruction. When the SAMPLE / PRELOAD instruction is loaded in the Instruction Register, moving the TAP controller into the Capture-DR state loads the data in the RAMs input and I/O buffers into the Boundary Scan Register. Boundary Scan Register locations are not associated with an input or I/O pin, and are loaded with the default state identified in the Boundary Scan Chain table at the end of this section of the datasheet. Because the RAM clock is independent from the TAP Clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e. in a metastable state). Although allowing the TAP to sample metastable inputs will not harm the device, repeatable results cannot be expected. RAM input signals must be stabilized for long enough to meet the TAPs input data capture set-up plus hold time (tTS plus tTH). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the Boundary Scan Register. Moving the controller to Shift-DR state then places the boundary scan register between the TDI and TDO pins.

EXTEST

EXTEST is an IEEE 1149.1 mandatory public instruction. It is to be executed whenever the instruction register is loaded with all logic 0s. The EXTEST command does not block or override the RAM’s input pins; therefore, the RAM’s internal state is still determined by its input pins.

Typically, the Boundary Scan Register is loaded with the desired pattern of data with the SAMPLE/PRELOAD command. Then the EXTEST command is used to output the Boundary Scan Register’s contents, in parallel, on the RAM’s data output drivers on the falling edge of TCK when the controller is in the Update-IR state.

Alternately, the Boundary Scan Register may be loaded in parallel using the EXTEST command. When the EXTEST instruction is selected, the sate of all the RAM’s input and I/O pins, as well as the default values at Scan Register locations not associated with a pin, are transferred in parallel into the Boundary Scan Register on the rising edge of TCK in the Capture-DR state, the RAM’s output pins drive out the value of the Boundary Scan Register location with which each output pin is associated.

IDCODE

The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in Capture-DR mode and places the ID register between the TDI and TDO pins in Shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.

SAMPLE-Z

If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (high-Z) and the Boundary Scan Register is connected between TDI and TDO when the TAP controller is moved to the Shift-DR state.

JTAG TAP Instruction Set Summary

Instruction	Code	Description	Notes
EXTEST	000	Places the Boundary Scan Register between TDI and TDO.	1
IDCODE	001	Preloads ID Register and places it between TDI and TDO.	1, 2
SAMPLE-Z	010	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO. Forces all RAM output drivers to High-Z except CQ.	1
GSI	011	GSI private instruction.	1
SAMPLE/PRELOAD	100	Captures I/O ring contents. Places the Boundary Scan Register between TDI and TDO.	1
GSI	101	GSI private instruction.	1
GSI	110	GSI private instruction.	1
BYPASS	111	Places Bypass Register between TDI and TDO.	1

Notes:
1. Instruction codes expressed in binary, MSB on left, LSB on right.
2. Default instruction automatically loaded at power-up and in test-logic-reset state.

JTAG Port Recommended Operating Conditions and DC Characteristics

Parameter	Symbol	Min.	Max.	Unit	Notes
Test Port Input Low Voltage	V_{ILJ}	–0.3	0.3 * V_{DD}	V	1
Test Port Input High Voltage	V_{IHJ}	0.7 * V_{DD}	V_{DD} +0.3	V	1
TMS, TCK and TDI Input Leakage Current	I_{INHJ}	–300	1	uA	2
TMS, TCK and TDI Input Leakage Current	I_{INLJ}	–1	100	uA	3
TDO Output Leakage Current	I_{OLJ}	–1	1	uA	4
Test Port Output High Voltage	V_{OHJ}	V_{DD} –0.2	—	V	5, 6
Test Port Output Low Voltage	V_{OLJ}	—	0.2	V	5, 7
Test Port Output CMOS High	V_{OHJC}	V_{DD} –0 .1	—	V	5, 8
Test Port Output CMOS Low	V_{OLJC}	—	0.1	V	5, 9

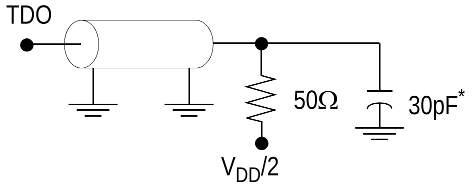
Notes:
1. Input Under/overshoot voltage must be –1 V < Vi < V_{DDn} +1 V not to exceed 2.4 V maximum, with a pulse width not to exceed 20% tTKC.
2. $V_{ILJ} \le V_{IN} \le V_{DDn}$
3. $0\ V \le V_{IN} \le V_{ILJn}$
4. Output Disable, V_{OUT} = 0 to V_{DDn}
5. The TDO output driver is served by the V_{DD} supply.
6. I_{OHJ} = –2 mA
7. I_{OLJ} = + 2 mA
8. I_{OHJC} = –100 uA
9. I_{OLJC} = +100 uA

JTAG Port AC Test Conditions

Parameter	Conditions
Input high level	V_{DD} – 0.2 V
Input low level	0.2 V
Input slew rate	1 V/ns
Input reference level	$V_{DD}/2$
Output reference level	$V_{DD}/2$

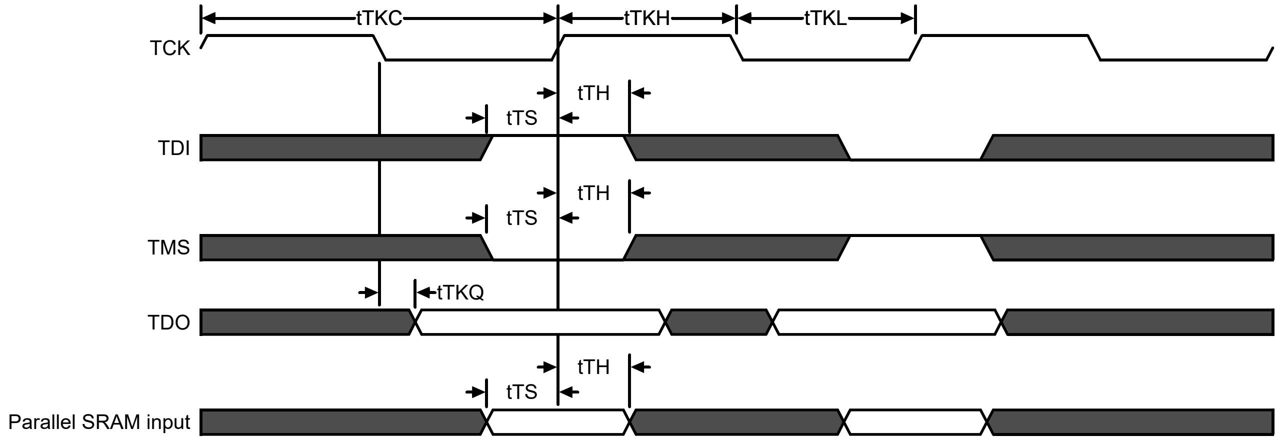
Notes:
1. Include scope and jig capacitance.
2. Test conditions as shown unless otherwise noted.

JTAG Port AC Test Load



* Distributed Test Jig Capacitance

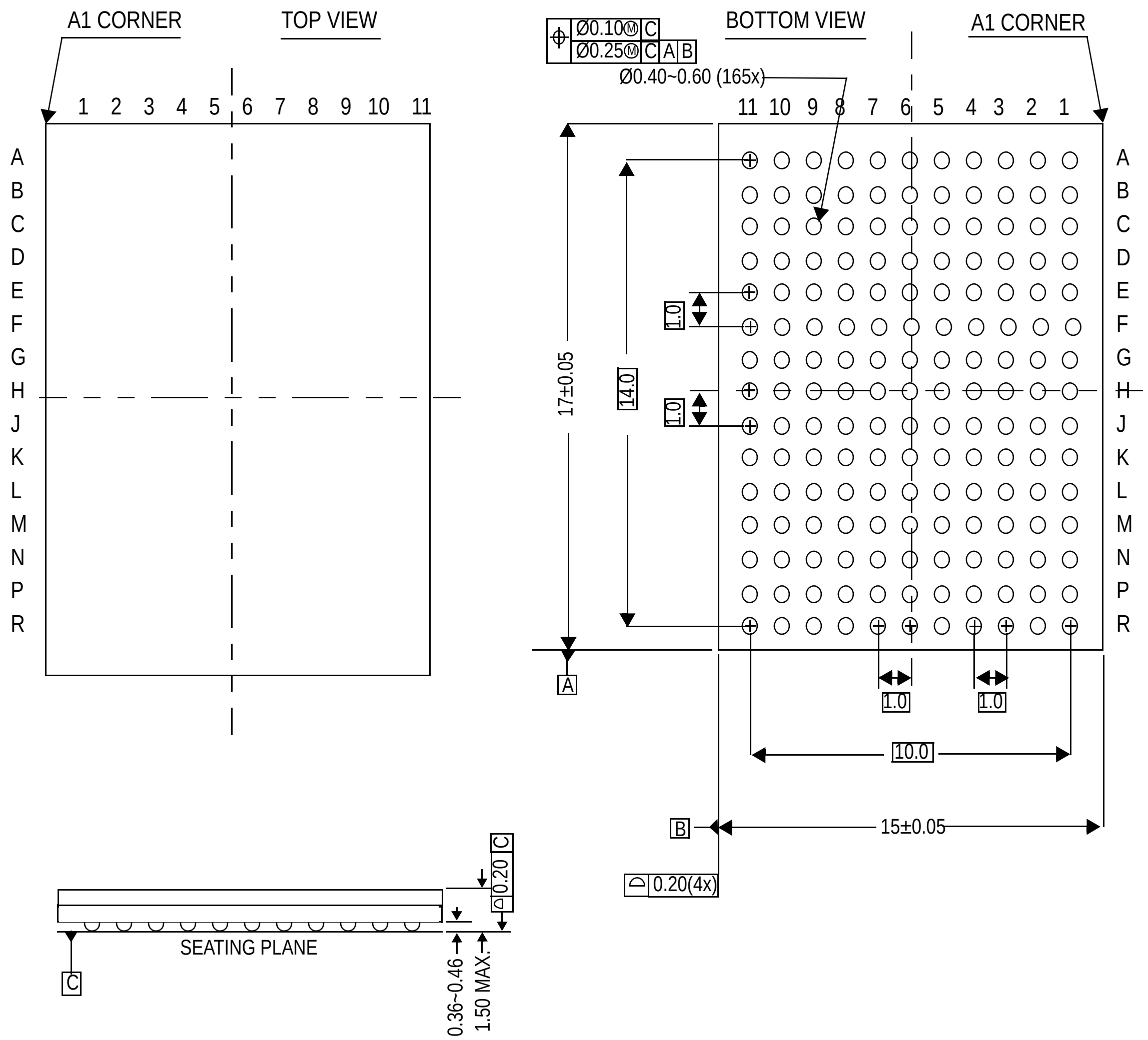
JTAG Port Timing Diagram



JTAG Port AC Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
TCK Cycle Time	tTKC	50	—	ns
TCK Low to TDO Valid	tTKQ	—	20	ns
TCK High Pulse Width	tTKH	20	—	ns
TCK Low Pulse Width	tTKL	20	—	ns
TDI & TMS Set Up Time	tTS	10	—	ns
TDI & TMS Hold Time	tTH	10	—	ns

Package Dimensions—165-Bump FPBGA (Package E)



Ordering Information—GSI SigmaDDR-II ECCRAM

Org	Part Number[1]	Type	Package	Speed (MHz)	T_J[2]
4M x 18	GS8672T18BE-400	SigmaDDR-II ECCRAM	165-bump BGA	400	C
4M x 18	GS8672T18BE-333	SigmaDDR-II ECCRAM	165-bump BGA	333	C
4M x 18	GS8672T18BE-300	SigmaDDR-II ECCRAM	165-bump BGA	300	C
4M x 18	GS8672T18BE-250	SigmaDDR-II ECCRAM	165-bump BGA	250	C
4M x 18	GS8672T18BE-200	SigmaDDR-II ECCRAM	165-bump BGA	200	C
4M x 18	GS8672T18BE-400I	SigmaDDR-II ECCRAM	165-bump BGA	400	I
4M x 18	GS8672T18BE-333I	SigmaDDR-II ECCRAM	165-bump BGA	333	I
4M x 18	GS8672T18BE-300I	SigmaDDR-II ECCRAM	165-bump BGA	300	I
4M x 18	GS8672T18BE-250I	SigmaDDR-II ECCRAM	165-bump BGA	250	I
4M x 18	GS8672T18BE-200I	SigmaDDR-II ECCRAM	165-bump BGA	200	I
2M x 36	GS8672T36BE-400	SigmaDDR-II ECCRAM	165-bump BGA	400	C
2M x 36	GS8672T36BE-333	SigmaDDR-II ECCRAM	165-bump BGA	333	C
2M x 36	GS8672T36BE-300	SigmaDDR-II ECCRAM	165-bump BGA	300	C
2M x 36	GS8672T36BE-250	SigmaDDR-II ECCRAM	165-bump BGA	250	C
2M x 36	GS8672T36BE-200	SigmaDDR-II ECCRAM	165-bump BGA	200	C
2M x 36	GS8672T36BE-400I	SigmaDDR-II ECCRAM	165-bump BGA	400	I
2M x 36	GS8672T36BE-333I	SigmaDDR-II ECCRAM	165-bump BGA	333	I
2M x 36	GS8672T36BE-300I	SigmaDDR-II ECCRAM	165-bump BGA	300	I
2M x 36	GS8672T36BE-250I	SigmaDDR-II ECCRAM	165-bump BGA	250	I
2M x 36	GS8672T36BE-200I	SigmaDDR-II ECCRAM	165-bump BGA	200	I
4M x 18	GS8672T18BGE-400	SigmaDDR-II ECCRAM	RoHS-compliant 165-bump BGA	400	C
4M x 18	GS8672T18BGE-333	SigmaDDR-II ECCRAM	RoHS-compliant 165-bump BGA	333	C
4M x 18	GS8672T18BGE-300	SigmaDDR-II ECCRAM	RoHS-compliant 165-bump BGA	300	C
4M x 18	GS8672T18BGE-250	SigmaDDR-II ECCRAM	RoHS-compliant 165-bump BGA	250	C
4M x 18	GS8672T18BGE-200	SigmaDDR-II ECCRAM	RoHS-compliant 165-bump BGA	200	C
4M x 18	GS8672T18BGE-400I	SigmaDDR-II ECCRAM	RoHS-compliant 165-bump BGA	400	I
4M x 18	GS8672T18BGE-333I	SigmaDDR-II ECCRAM	RoHS-compliant 165-bump BGA	333	I
4M x 18	GS8672T18BGE-300I	SigmaDDR-II ECCRAM	RoHS-compliant 165-bump BGA	300	I
4M x 18	GS8672T18BGE-250I	SigmaDDR-II ECCRAM	RoHS-compliant 165-bump BGA	250	I
4M x 18	GS8672T18BGE-200I	SigmaDDR-II ECCRAM	RoHS-compliant 165-bump BGA	200	I
2M x 36	GS8672T36BGE-400	SigmaDDR-II ECCRAM	RoHS-compliant 165-bump BGA	400	C
2M x 36	GS8672T36BGE-333	SigmaDDR-II ECCRAM	RoHS-compliant 165-bump BGA	333	C

Notes:

1. For Tape and Reel add the character “T” to the end of the part number. Example: GS8672T36BE-300T.
2. C = Commercial Temperature Range. I = Industrial Temperature Range.