260 Pin BGA
Commercial Temp
Industrial Temp

72Mb SigmaDDR-IIIe™ Burst of 2 ECCRAM™

Up to 725 MHz
1.35V V_{DD}
1.2V or 1.35V or 1.5V V_{DDQ}

Features

- For use with GSI SRAM Port IP
- 2Mb x 36 and 4Mb x 18 organizations available
- 725 MHz maximum operating frequency
- 725 MT/s peak transaction rate (in millions per second)
- 52 Gb/s peak data bandwidth (in x36 devices)
- Common I/O DDR Data Bus
- Non-multiplexed SDR Address Bus
- One operation - Read or Write - per clock cycle
- Burst of 2 Read and Write operations
- 3 cycle Read Latency
- On-chip ECC with virtually zero SER
- 1.35V core voltage
- 1.2V or 1.35V or 1.5V I/O interface (HSTL or SSTL)
- Configurable ODT (on-die termination)
- ZQ pin for programmable driver impedance
- ZT pin for programmable ODT impedance
- IEEE 1149.1 JTAG-compliant Boundary Scan
- 260 pin, 14 mm x 22 mm, 1 mm ball pitch BGA package
  - –K: 5/6 RoHS-compliant package
  - –GK: 6/6 RoHS-compliant package

SigmaDDR-IIIe™ Family Overview

SigmaDDR-IIIe ECCRAMs are the Common I/O half of the SigmaQuad-IIIe/SigmaDDR-IIIe family of high performance ECCRAMs. Although very similar to GSI's second generation of networking SRAMs (the SigmaQuad-II/SigmaDDR-II family), these third generation devices offer several new features that help enable significantly higher performance.

Clocking and Addressing Schemes

The GS8673ET18/36BK SigmaDDR-IIIe ECCRAMs are synchronous devices. They employ three pairs of positive and negative input clocks; one pair of master clocks, CK and $\overline{CK}$, and two pairs of write data clocks, KD[1:0] and $\overline{KD}$[1:0]. All six input clocks are single-ended; that is, each is received by a dedicated input buffer.

CK and $\overline{CK}$ are used to latch address and control inputs, and to control all output timing. KD[1:0] and $\overline{KD}$[1:0] are used solely to latch data inputs.

Each internal read and write operation in a SigmaDDR-IIIe B2 ECCRAM is two times wider than the device I/O bus. An input data bus de-multiplexer is used to accumulate incoming data before it is simultaneously written to the memory array. An output data multiplexer is used to capture the data produced from a single memory array read and then route it to the appropriate output drivers as needed. Therefore, the address field of a SigmaDDR-IIIe B2 ECCRAM is always one address pin less than the advertised index depth (e.g. the 4M x 18 has 2M addressable index).

On-Chip ECC

GSI's ECCRAMs implement an ECC algorithm that detects and corrects all single-bit memory errors, including those induced by SER events such as cosmic rays, alpha particles, etc. The resulting Soft Error Rate of these devices is anticipated to be <0.002 FITs/Mb — a 5-order-of-magnitude improvement over comparable SRAMs with no on-chip ECC, which typically have an SER of 200 FITs/Mb or more.

All quoted SER values are at sea level in New York City.

Parameter Synopsis

Speed Grade	Max Operating Frequency	Read Latency	V_{DD}
-725S	725 MHz	3 cycles	1.3V to 1.4V
-625S	625 MHz	3 cycles	1.3V to 1.4V
-550S	550 MHz	3 cycles	1.3V to 1.4V

4M x 18 (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	V_{DD}	V_{DDQ}	V_{DD}	V_{DDQ}	MCL	MCH (CFG)	MCL	ZQ	PZT1	V_{DDQ}	V_{DD}	V_{DDQ}	V_{DD}
B	V_{SS}	NU_{IO}	V_{SS}	NU_I	MVQ	MCL	NC (RSVD)	MCL (SIOM)	PZT0	NU_I	V_{SS}	DQ0	V_{SS}
C	DQ17	V_{DDQ}	NU_I	V_{DDQ}	V_{SS}	SA	V_{DD}	SA	V_{SS}	V_{DDQ}	NU_I	V_{DDQ}	NU_{IO}
D	V_{SS}	NU_{IO}	V_{SS}	NU_I	SA	V_{DDQ}	NC (288 Mb)	V_{DDQ}	NC (144 Mb)	NU_I	V_{SS}	DQ1	V_{SS}
E	DQ16	V_{DDQ}	NU_I	V_{DD}	V_{SS}	SA	V_{SS}	SA	V_{SS}	V_{DD}	NU_I	V_{DDQ}	NU_{IO}
F	V_{SS}	NU_{IO}	V_{SS}	NU_I	SA	V_{DD}	V_{DDQ}	V_{DD}	SA	NU_I	V_{SS}	DQ2	V_{SS}
G	DQ15	NU_{IO}	NU_I	NU_I	V_{SS}	SA	MZT1	SA	V_{SS}	NU_I	NU_I	DQ3	NU_{IO}
H	DQ14	V_{DDQ}	NU_I	V_{DDQ}	SA	V_{DDQ}	R/$\overline{W}$	V_{DDQ}	SA	V_{DDQ}	NU_I	V_{DDQ}	NU_{IO}
J	V_{SS}	NU_{IO}	V_{SS}	NU_I	V_{SS}	SA	V_{SS}	SA	V_{SS}	NU_I	V_{SS}	DQ4	V_{SS}
K	CQ1	V_{DDQ}	V_{REF}	V_{DD}	KD1	V_{DD}	CK	V_{DD}	KD0	V_{DD}	V_{REF}	V_{DDQ}	CQ0
L	$\overline{CQ}$1	V_{SS}	QVLD1	V_{SS}	$\overline{KD}$1	V_{DDQ}	$\overline{CK}$	V_{DDQ}	$\overline{KD}$0	V_{SS}	QVLD0	V_{SS}	$\overline{CQ}$0
M	V_{SS}	DQ13	V_{SS}	NU_I	V_{SS}	SA	V_{SS}	SA	V_{SS}	NU_I	V_{SS}	NU_{IO}	V_{SS}
N	NU_{IO}	V_{DDQ}	NU_I	V_{DDQ}	MCL	V_{DDQ}	$\overline{LD}$	V_{DDQ}	MCH	V_{DDQ}	NU_I	V_{DDQ}	DQ5
P	NU_{IO}	DQ12	NU_I	NU_I	V_{SS}	SA	MZT0	SA	V_{SS}	NU_I	NU_I	NU_{IO}	DQ6
R	V_{SS}	DQ11	V_{SS}	NU_I	MCH	V_{DD}	V_{DDQ}	V_{DD}	RST	NU_I	V_{SS}	NU_{IO}	V_{SS}
T	NU_{IO}	V_{DDQ}	NU_I	V_{DD}	V_{SS}	SA	V_{SS}	SA	V_{SS}	V_{DD}	NU_I	V_{DDQ}	DQ7
U	V_{SS}	DQ10	V_{SS}	NU_I	NU_I	V_{DDQ}	MCL	V_{DDQ}	NU_I	NU_I	V_{SS}	NU_{IO}	V_{SS}
V	NU_{IO}	V_{DDQ}	NU_I	V_{DDQ}	V_{SS}	SA (x18)	V_{DD}	SA (B2)	V_{SS}	V_{DDQ}	NU_I	V_{DDQ}	DQ8
W	V_{SS}	DQ9	V_{SS}	NU_I	TCK	MCH	NC (RSVD)	MCL	TMS	NU_I	V_{SS}	NU_{IO}	V_{SS}
Y	V_{DD}	V_{DDQ}	V_{DD}	V_{DDQ}	TDO	ZT	MCH	MCL	TDI	V_{DDQ}	V_{DD}	V_{DDQ}	V_{DD}

Notes:

1. Pins 5A, 5N, 6B, 7A, 7U, 8W, and 8Y must be tied Low in this device.
2. Pins 5R, 6W, 7Y, and 9N must be tied High in this device.
3. Pins 5U and 9U are unused in this device. They must be left unconnected or driven Low.
4. Pin 6A is defined as mode pin CFG in the pinout standard. It must be tied High in this device to select x18 configuration.
5. Pin 8B is defined as mode pin SIOM in the pinout standard. It must be tied Low in this device to select Common I/O configuration.
6. Pin 6V is defined as address pin SA for x18 devices. It is used in this device.
7. Pin 8V is defined as address pin SA for B2 devices. It is used in this device.
8. Pin 9D is reserved as address pin SA for 144Mb devices. It is a true no-connect in this device.
9. Pin 7D is reserved as address pin SA for 288Mb devices. It is a true no-connect in this device.

2M x 36 (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13
A	V_{DD}	V_{DDQ}	V_{DD}	V_{DDQ}	MCL	MCL (CFG)	MCL	ZQ	PZT1	V_{DDQ}	V_{DD}	V_{DDQ}	V_{DD}
B	V_{SS}	DQ35	V_{SS}	NU_I	MVQ	MCL	NC (RSVD))	MCL (SIOM)	PZT0	NU_I	V_{SS}	DQ0	V_{SS}
C	DQ26	V_{DDQ}	NU_I	V_{DDQ}	V_{SS}	SA	V_{DD}	SA	V_{SS}	V_{DDQ}	NU_I	V_{DDQ}	DQ9
D	V_{SS}	DQ34	V_{SS}	NU_I	SA	V_{DDQ}	NC (288 Mb)	V_{DDQ}	NC (144 Mb)	NU_I	V_{SS}	DQ1	V_{SS}
E	DQ25	V_{DDQ}	NU_I	V_{DD}	V_{SS}	SA	V_{SS}	SA	V_{SS}	V_{DD}	NU_I	V_{DDQ}	DQ10
F	V_{SS}	DQ33	V_{SS}	NU_I	SA	V_{DD}	V_{DDQ}	V_{DD}	SA	NU_I	V_{SS}	DQ2	V_{SS}
G	DQ24	DQ32	NU_I	NU_I	V_{SS}	SA	MZT1	SA	V_{SS}	NU_I	NU_I	DQ3	DQ11
H	DQ23	V_{DDQ}	NU_I	V_{DDQ}	SA	V_{DDQ}	R/$\overline{W}$	V_{DDQ}	SA	V_{DDQ}	NU_I	V_{DDQ}	DQ12
J	V_{SS}	DQ31	V_{SS}	NU_I	V_{SS}	SA	V_{SS}	SA	V_{SS}	NU_I	V_{SS}	DQ4	V_{SS}
K	CQ1	V_{DDQ}	V_{REF}	V_{DD}	KD1	V_{DD}	CK	V_{DD}	KD0	V_{DD}	V_{REF}	V_{DDQ}	CQ0
L	$\overline{CQ}$1	V_{SS}	QVLD1	V_{SS}	$\overline{KD}$1	V_{DDQ}	$\overline{CK}$	V_{DDQ}	$\overline{KD}$0	V_{SS}	QVLD0	V_{SS}	$\overline{CQ}$0
M	V_{SS}	DQ22	V_{SS}	NU_I	V_{SS}	SA	V_{SS}	SA	V_{SS}	NU_I	V_{SS}	DQ13	V_{SS}
N	DQ30	V_{DDQ}	NU_I	V_{DDQ}	MCL	V_{DDQ}	$\overline{LD}$	V_{DDQ}	MCH	V_{DDQ}	NU_I	V_{DDQ}	DQ5
P	DQ29	DQ21	NU_I	NU_I	V_{SS}	SA	MZT0	SA	V_{SS}	NU_I	NU_I	DQ14	DQ6
R	V_{SS}	DQ20	V_{SS}	NU_I	MCH	V_{DD}	V_{DDQ}	V_{DD}	RST	NU_I	V_{SS}	DQ15	V_{SS}
T	DQ28	V_{DDQ}	NU_I	V_{DD}	V_{SS}	SA	V_{SS}	SA	V_{SS}	V_{DD}	NU_I	V_{DDQ}	DQ7
U	V_{SS}	DQ19	V_{SS}	NU_I	NU_I	V_{DDQ}	MCL	V_{DDQ}	NU_I	NU_I	V_{SS}	DQ16	V_{SS}
V	DQ27	V_{DDQ}	NU_I	V_{DDQ}	V_{SS}	NU_I (x18)	V_{DD}	SA (B2)	V_{SS}	V_{DDQ}	NU_I	V_{DDQ}	DQ8
W	V_{SS}	DQ18	V_{SS}	NU_I	TCK	MCH	NC (RSVD)	MCL	TMS	NU_I	V_{SS}	DQ17	V_{SS}
Y	V_{DD}	V_{DDQ}	V_{DD}	V_{DDQ}	TDO	ZT	MCH	MCL	TDI	V_{DDQ}	V_{DD}	V_{DDQ}	V_{DD}

Notes:

1. Pins 5A, 5N, 6B, 7A, 7U, 8W, and 8Y must be tied Low in this device.
2. Pins 5R, 6W, 7Y, and 9N must be tied High in this device.
3. Pins 5U and 9U are unused in this device. They must be left unconnected or driven Low.
4. Pin 6A is defined as mode pin CFG in the pinout standard. It must be tied Low in this device to select x36 configuration.
5. Pin 8B is defined as mode pin SIOM in the pinout standard. It must be tied Low in this device to select Common I/O configuration.
6. Pin 6V is defined as address pin SA for x18 devices. It is unused in this device, and must be left unconnected or driven Low.
7. Pin 8V is defined as address pin SA for B2 devices. It is used in this device.
8. Pin 9D is reserved as address pin SA for 144Mb devices. It is a true no-connect in this device.
9. Pin 7D is reserved as address pin SA for 288Mb devices. It is a true no-connect in this device.

Pin Description

Symbol	Description	Type
SA	**Address** — Read or Write Address is registered on ↑CK.	Input
DQ[35:0]	**Write/Read Data** — Registered on ↑KD and ↑$\overline{KD}$ during Write operations; aligned with ↑CQ and ↑$\overline{CQ}$ during Read operations. DQ[17:0] - x18 and x36. DQ[35:18] - x36 only.	I/O
QVLD[1:0]	**Read Data Valid**—Driven high one half cycle before valid read data.	Output
CK, $\overline{CK}$	**Primary Input Clocks** — Dual single-ended. Used for latching address and control inputs, for internal timing control, and for output timing control.	Input
KD[1:0], $\overline{KD}$[1:0]	**Write Data Input Clocks** — Dual single-ended. Used for latching write data inputs. KD0, $\overline{KD}$0: latch DQ[17:0] in x36, DQ[8:0] in x18. KD1, $\overline{KD}$1: latch DQ[35:18] in x36, DQ[17:9] in x18.	Input
CQ[1:0], $\overline{CQ}$[1:0]	**Echo Clocks** — Free-running output (echo) clocks, tightly aligned with read data outputs. Facilitate source-synchronous operation. CQ0, $\overline{CQ}$0: align with DQ[17:0] in x36, DQ[8:0] in x18. CQ1, $\overline{CQ}$1: align with DQ[35:18] in x36, DQ[17:9] in x18.	Output
$\overline{LD}$	**Load Enable** — Registered on↑CK. $\overline{LD}$ = 0: Loads a new address and initiates a Read or Write operation. $\overline{LD}$ = 1: Initiates a NOP operation.	Input
R/$\overline{W}$	**Read / Write Enable** — Registered on ↑CK. R/$\overline{W}$ = 0: initiates a Write operation when $\overline{LD}$ = 0. R/$\overline{W}$ = 1: initiates a Read operation when $\overline{LD}$ = 0.	Input
RST	**Reset** — Holds the device inactive and resets the device to its initial power-on state when asserted High. Weakly pulled Low internally.	Input
ZQ	**Driver Impedance Control Resistor Input** — Must be connected to V_{SS} through an external resistor RQ to program driver impedance.	Input
ZT	**ODT Impedance Control Resistor Input** — Must be connected to V_{SS} through an external resistor RT to program ODT impedance.	Input
MZT[1:0]	**ODT Mode Select** — Set the ODT state globally for all input groups. Must be tied High or Low. MZT[1:0] = 00: disables ODT on all input groups, regardless of PZT[1:0]. MZT[1:0] = 01: enables strong ODT on select input groups, as specified by PZT[1:0]. MZT[1:0] = 10: enables weak ODT on select input groups, as specified by PZT[1:0]. MZT[1:0] = 11: reserved.	Input
PZT[1:0]	**ODT Configuration Select** — Set the ODT state for various combinations of input groups when MZT[1:0] = 01 or 10. Must be tied High or Low. PZT[1:0] = 00: enables ODT on write data only. PZT[1:0] = 01: enables ODT on write data and input clocks. PZT[1:0] = 10: enables ODT on write data, address, and control. PZT[1:0] = 11: enables ODT on write data, input clocks, address, and control.	Input

Pin Description (Continued)

Symbol	Description	Type
MVQ	**I/O Voltage Select** — Indicates what voltage is supplied to the V_{DDQ} pins. Must be tied High or Low. MVQ = 0: Configure for 1.2V or 1.35V nominal V_{DDQ}. MVQ = 1: Configure for 1.5V nominal V_{DDQ}.	Input
V_{DD}	**Core Power Supply** — 1.35V nominal core supply voltage.	—
V_{DDQ}	**I/O Power Supply** — 1.2V or 1.35V or 1.5V nominal I/O supply voltage. Configurable via MVQ pin.	—
V_{REF}	**Input Reference Voltage** — Input buffer reference voltage.	—
V_{SS}	**Ground**	—
TCK	**JTAG Clock**	Input
TMS	**JTAG Mode Select** — Weakly pulled High internally.	Input
TDI	**JTAG Data Input** — Weakly pulled High internally.	Input
TDO	**JTAG Data Output**	Output
MCH	**Must Connect High** — May be tied to V_{DDQ} directly or via a 1kΩ resistor.	Input
MCL	**Must Connect Low** — May be tied to V_{SS} directly or via a 1kΩ resistor.	Input
NC	**No Connect** — There is no internal chip connection to these pins. They may be left unconnected, or tied High or Low.	—
NU_I	**Not Used Input** — There is an internal chip connection to these input pins, but they are unused by the device. They are pulled Low internally. They may be left unconnected or tied/driven Low. They should not be tied/driven High.	Input
NU_{IO}	**Not Used Input/Output** — There is an internal chip connection to these I/O pins, but they are unused by the device. The drivers are tri-stated internally. They are pulled Low internally. They may be left unconnected or tied/driven Low. They should not be tied/driven High.	I/O

Power-Up and Reset Requirements

For reliability purposes, power supplies must power up simultaneously, or in the following sequence:
V_{SS}, V_{DD}, V_{DDQ}, V_{REF} and inputs.
Power supplies must power down simultaneously, or in the reverse sequence.

After power supplies power up, the following start-up sequence must be followed.

Step 1 (Recommended, but not required): Assert RST High for at least 1ms.
While RST is asserted high:
• Read and Write operations are ignored.

Note: If possible, RST should be asserted High before input clocks (begin toggling, and remain asserted High until input clocks are stable and toggling within specification, in order to prevent unstable, out-of-spec input clocks from causing trouble in the SRAM.

Step 2: Begin toggling input clocks.
After input clocks begin toggling, but not necessarily within specification:
• CQ, $\overline{CQ}$ begin toggling, but not necessarily within specification.

Step 3: Wait until input clocks are stable and toggling within specification.

Step 4: De-assert RST Low (if asserted High).

Step 5: Wait at least 160K (163,840) cycles for driver and ODT impedances to calibrate.
After the impedances have calibrated:
• CQ, $\overline{CQ}$ begin toggling within specification.

Step 6: Begin initiating Read and Write operations.

Reset Usage

Although not generally recommended, RST may be asserted High at any time after completion of the initial power-up sequence described above, to reset the SRAM control logic to its initial power-on state. However, whenever RST is subsequently de-asserted Low (as in Step 4 in the power up sequence), at least 160K NOP cycles must be initiated (as in Step 5 in the power-up sequence) before Read and Write operations are initiated.

Note: Memory array content may be perturbed/corrupted when RST is asserted High.

Error Correction (ECC)

These devices implement a single-bit error detection and correction algorithm (specifically, a Hamming Code) on each DDR data word (comprising two 9-bit data bytes) transmitted on each 9-bit data bus (i.e., transmitted on DQ[8:0], DQ[17:9], DQ[26:18], and DQ[35:27]). To accomplish this, 5 ECC parity bits (invisible to the user) are utilized per every 18 data bits (visible to the user).

The ECC algorithm neither corrects nor detects multi-bit errors. However, ECCRAMs are architected in such a way that a single SER event very rarely causes a multi-bit error across any given "transmitted data unit", where a "transmitted data unit" represents the data transmitted as the result of a single read or write operation to a particular address. The extreme rarity of multi-bit errors results in the SER mentioned previously (i.e., <0.002 FITs/Mb (measured at sea level)).

Not only does the on-chip ECC significantly improve SER performance, but it also frees up the entire memory array for data storage. Frequently, SRAM applications allocate 1/9th of the memory array (i.e., one "error bit" per eight "data bits") for error detection (either simple parity error detection, or system-level ECC error detection and correction). Such error-bit allocation is unnecessary with ECCRAMs; the entire memory array can be utilized for data storage, effectively providing 12.5% greater storage capacity compared to SRAMs of the same density not equipped with on-chip ECC.

Input Timing

These devices utilize three pairs of positive and negative input clocks, CK & $\overline{CK}$ and KD[1:0] & $\overline{KD}$[1:0], to latch the various synchronous inputs. Specifically:

↑CK latches all address (SA) inputs.

↑CK latches all control ($\overline{LD}$, R/$\overline{W}$) inputs.

↑KD[1:0] and ↑$\overline{KD}$[1:0] latch particular write data (DQ) inputs, as follows:

- ↑KD0 and ↑$\overline{KD}$0 latch DQ[17:0] in x36, and DQ[8:0] in x18.
- ↑KD1 and ↑$\overline{KD}$1 latch DQ[35:18] in x36, and DQ[17:9] in x18.

Output Timing

These devices provide two pairs of positive and negative output clocks (aka "echo clocks"), CQ[1:0] & $\overline{CQ}$[1:0], whose timing is tightly aligned with read data in order to enable reliable source-synchronous data transmission.

Output timing is generated by ↑CK and ↑$\overline{CK}$, as follows:

- ↑CK generates ↑CQ[1:0], ↓$\overline{CQ}$[1:0], Q1 active, and Q2 inactive.
- . ↑$\overline{CK}$ generates ↑$\overline{CQ}$[1:0], ↓CQ[1:0], Q1 inactive, Q2 active, and QVLD active/inactive.

Note: Q1 and Q2 indicate the first and second pieces of read data transferred in any given clock cycle during Read operations.

↑CQ[1:0] and ↑$\overline{CQ}$[1:0] align with particular read data (DQ) and read data valid (QVLD) outputs, as follows:

- ↑CQ0 and ↑$\overline{CQ0}$ align with DQ[17:0], QVLD0 in x36, and with DQ[8:0], QVLD0 in x18.
- ↑CQ1 and ↑$\overline{CQ1}$ align with DQ[35:18], QLVD1 in x36, and with DQ[17:9], QVLD1 in x18.

Driver Impedance Control

Programmable Driver Impedance is implemented on the following output signals:

• CQ, $\overline{CQ}$, DQ, QVLD.

Driver impedance is programmed by connecting an external resistor RQ between the ZQ pin and V_{SS}.

Driver impedance is set to the programmed value within 160K cycles after input clocks are operating within specification and RST is de-asserted Low. It is updated periodically thereafter to compensate for temperature and voltage fluctuations in the system.

Output Signal	Pull-Down Impedance (R_{OUTL})	Pull-Up Impedance (R_{OUTH})
CQ, $\overline{CQ}$, DQ, QVLD	RQ*0.2 ± 15%	RQ*0.2 ± 15%

Notes:

1. R_{OUTL} and R_{OUTH} apply when 175Ω ≤ RQ ≤ 225Ω..
2. The mismatch between R_{OUTL} and R_{OUTH} is less than 10%, guaranteed by design.

ODT Impedance Control

Programmable ODT Impedance is implemented on the following input signals:

• CK, $\overline{CK}$, KD, $\overline{KD}$, SA, $\overline{LD}$, R/$\overline{W}$, DQ.

ODT impedance is programmed by connecting an external resistor RT between the ZT pin and V_{SS}.

ODT impedance is set to the programmed value within 160K cycles after input clocks are operating within specification and RST is de-asserted Low. It is updated periodically thereafter to compensate for temperature and voltage fluctuations in the system

Input Signal	PZT[1:0]	MZT[1:0]	Pull-Down Impedance (R_{INL})	Pull-Up Impedance (R_{INH})
CK, $\overline{CK}$, KD, $\overline{KD}$	X0	XX	disabled	disabled
	X1	01	RT ± 15%	RT ± 15%
		10	RT*2 ± 20%	RT*2 ± 20%
SA, $\overline{LD}$, R/$\overline{W}$	0X	XX	disabled	disabled
	1X	01	RT ± 15%	RT ± 15%
		10	RT*2 ± 20%	RT*2 ± 20%
DQ	XX	01	RT ± 15%	RT ± 15%
		10	RT*2 ± 20%	RT*2 ± 20%

Notes:

1. When MZT[1:0] = 00, ODT is disabled on all inputs. MZT[1:0] = 11 is reserved for future use.
2. R_{INL} and R_{INH} apply when 105Ω ≤ RT ≤ 135Ω.
3. The mismatch between R_{INL} and R_{INH} is less than 10%, guaranteed by design.
4. All ODT is disabled during JTAG EXTEST and SAMPLE-Z instructions.

Note: When ODT impedance is enabled on a particular input, that input should always be driven High or Low; it should never be tri-stated (i.e., in a High- Z state). If the input is tri-stated, the ODT will pull the signal to V_{DDQ} / 2 (i.e., to the switch point of the diff-amp receiver), which could cause the receiver to enter a meta-stable state and consume more power than it normally would. This could result in the device's operating currents being higher.

Truth Table

SA	LD	R/$\overline{W}$	Current Operation	DQ (D)		DQ (Q)	
↑CK (t_n)	↑CK (t_n)	↑CK (t_n)	(t_n)	↑KD (t_{n+1})	↑$\overline{KD}$ ($t_{n+1½}$)	↑CQ (t_{n+3})	↑$\overline{CQ}$ ($t_{n+3½}$)
V	1	X	NOP	X	X	Hi-Z / *	
V	0	0	Write	D1	D2	Hi-Z / *	
V	0	1	Read	X	X	Q1	Q2

Notes:
1. 1 = High; 0 = Low; V = Valid (High or Low); X = Don't Care.
2. D1 and D2 indicate the first and second pieces of write data transferred during Write operations.
3. Q1 and Q2 indicate the first and second pieces of read data transferred during Read operations.
4. When DQ ODT is disabled (MZT[1:0] = 00), DQ pins are tri-stated for one cycle in response to NOP and Write commands, 3 cycles after the command is sampled.
5. When DQ ODT is enabled (MZT[1:0] = 01 or 10), DQ drivers are disabled for one cycle in response to NOP and Write commands, 3 cycles after the command is sampled. The state of the DQ pins during that time (denoted by * in the table above) is determined by the state of the DQ ODT, as depicted in the Extended DQ Truth Table below.

Extended DQ Truth Table

LD	R/$\overline{W}$	Current Operation	DQ State	
↑CK (t_n)	↑CK (t_n)	(t_n)	↑CK (t_{n+2})	↑CK (t_{n+3})
1	0	NOPw	ODT Enabled	—
0	0	Write	ODT Enabled	—
1	1	NOPr	ODT Disabled, Drive Low	—
0	1	Read	ODT Disabled, Drive Low	Drive Read Data

Notes:
1. DQ ODT is enabled 2 cycles after R/$\overline{W}$ is sampled Low, and disabled 2 cycles after R/$\overline{W}$ is sampled High.
2. When DQ ODT is enabled, DQ output drivers are disabled.
   When DQ ODT is disabled, DQ output drivers are enabled, and drive Low when not driving read data.
3. When a Read operation is initiated in cycle "n", R/$\overline{W}$ must be High at ↑CK of cycle "n+1" (i.e. a Read operation must always be followed by a Read or NOPr operation). In that case, the DQ state in cycle "n+3" is "Drive Read Data", as indicated above.

DQ State Transition Timing Specifications

Parameter	Symbol	Min	Max	Units
CK Clock High to DQ State Transition	tKHDQT	1.0	2.5	ns

NOPr and NOPw Requirements

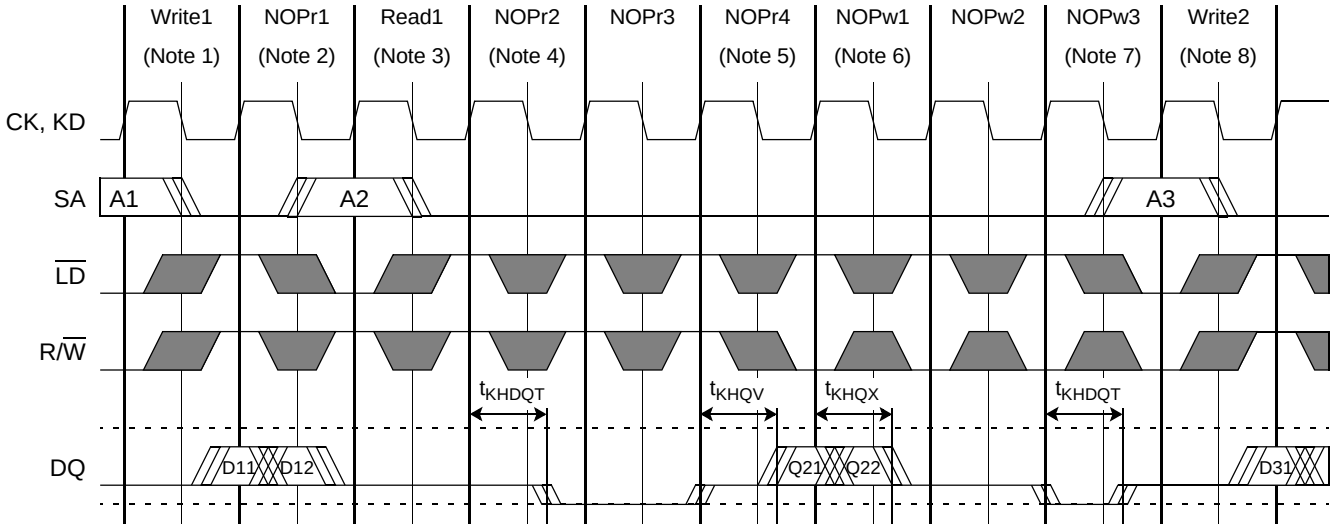
The number of NOPw and NOPr needed during Write -> Read transitions, and the number of NOPr and NOPw needed during Read -> Write transitions, are as follows:

Write -> Read Transition				Read -> Write Transition			
NOPw (after Write)		NOPr (before Read)		NOPr (after Read)		NOPw (before Write)	
min	typ	min	typ	min	typ	min	typ
0	0	0	1~2	2	3~4	2	3~4

Notes:

1. Min NOPw after Write (0) ensures that the SRAM disables DQ ODT 1.5 cycles after it latches the last piece of write data. Typ NOPw is the same as Min NOPw because it is sufficient to ensure that the controller stops driving the last piece of write data before SRAM DQ ODT disable reaches it (as the result of a subsequent NOPr or Read), regardless of SRAM tKQ, prop delay between SRAM and controller, and operating frequency.
2. Min NOPr before Read (0) ensures that the SRAM drives Low 1 cycle before it begins driving the first piece of read data. Typ NOPr is greater than Min NOPr in order to ensure that the controller enables DQ ODT after SRAM Low drive reaches it (and before the SRAM drives the first piece of read data), regardless of SRAM tKQ, prop delay between SRAM and controller, and operating frequency.
3. Min NOPr after Read (2) ensures that the SRAM drives Low for 1 cycle after it stops driving the last piece of read data and before it enables DQ ODT (as the result of a subsequent NOPw). Typ NOPr is greater than Min NOPr in order to ensure that the controller disables DQ ODT after SRAM Low drive reaches is (and before the SRAM enables DQ ODT), accounting for SRAM tKQ, prop delay between SRAM and controller, and operating frequency.
4. Min NOPw before Write (3) ensures that the SRAM enables DQ ODT 1 cycle before it latches the first piece of write data. Typ NOPw is greater than Min NOPw in order to ensure that the controller begins driving the first piece of write data after SRAM DQ ODT enable reaches it, accounting for SRAM tKQ, prop delay between SRAM and controller, and operating frequency.

DQ ODT Control Timing Diagram



Note: In the diagram above, the controller is disabling its DQ ODT except from the beginning of NOPr4 to the beginning of NOPw3. And while it is disabling its DQ ODT, the controller is driving DQ Low when it isn't driving write data. Whereas, the SRAM is enabling its DQ ODT except from the beginning of NOPr2 to the beginning of NOPw3. And while it is disabling its DQ ODT, the SRAM is driving DQ Low when it isn't driving read data.

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Rating	Units
Core Supply Voltage	V_{DD}	-0.3 to +1.6	V
I/O Supply Voltage when MVQ = 0	V_{DDQ}	-0.3 to V_{DD}	V
I/O Supply Voltage when MVQ = 1	V_{DDQ}	-0.3 to V_{DD} + 0.3	V
Input Voltage when MVQ = 0	V_{IN}	-0.3 to V_{DDQ} + 0.3 (1.7 max)	V
Input Voltage when MVQ = 1	V_{IN}	-0.3 to V_{DDQ} + 0.3 (2.0 max)	V
Maximum Junction Temperature	T_J	125	°C
Storage Temperature	T_{STG}	-55 to 125	°C

Note:
Permanent damage to the device may occur if the Absolute Maximum Ratings are exceeded. Operation should be restricted to Recommended Operating Conditions. Exposure to conditions exceeding the Recommended Operating Conditions, for an extended period of time, may affect reliability of this component.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Core Supply Voltage	V_{DD}	1.3	1.35	1.4	V
I/O Supply Voltage - 1.2V nominal when MVQ = 0	V_{DDQ}	1.15	1.2	1.25	V
I/O Supply Voltage - 1.35V nominal when MVQ = 0	V_{DDQ}	1.3	1.35	V_{DD}	V
I/O Supply Voltage - 1.5V nominal when MVQ = 1	V_{DDQ}	1.4	1.5	1.6	V
Commercial Junction Temperature	T_{JC}	0	—	85	°C
Industrial Junction Temperature	T_{JI}	-40	—	100	°C

Note:
For reliability purposes, power supplies must power up simultaneously, or in the following sequence:
V_{SS}, V_{DD}, V_{DDQ}, V_{REF}, and Inputs.
Power supplies must power down simultaneously, or in the reverse sequence.

Thermal Impedance

Package	θ JA (C°/W) Airflow = 0 m/s	θ JA (C°/W) Airflow = 1 m/s	θ JA (C°/W) Airflow = 2 m/s	θ JB (C°/W)	θ JC (C°/W)
FBGA	15.5	13.1	12.1	4.4	0.2

I/O Capacitance

Parameter	Symbol	Min	Max	Units	Notes
Input Capacitance	C_{IN}	—	5.0	pF	1, 3
Output Capacitance	C_{OUT}	—	5.5	pF	2, 3

Notes:
1. $V_{IN} = V_{DDQ}/2$.
2. $V_{OUT} = V_{DDQ}/2$.
3. $T_A = 25°C$, f = 1 MHz.

Input Electrical Characteristics when MVQ = 0

Parameter	Symbol	Min	Max	Units	Notes
DC Input Reference Voltage	V_{REFdc}	0.48 * V_{DDQ}	0.52 * V_{DDQ}	V	—
DC Input High Voltage	V_{IH1dc}	V_{REF} + 0.08	V_{DDQ} + 0.15	V	4
DC Input Low Voltage	V_{IL1dc}	–0.15	V_{REF} – 0.08	V	4
DC Input High Voltage	V_{IH2dc}	0.75 * V_{DDQ}	V_{DDQ} + 0.15	V	5
DC Input Low Voltage	V_{IL2dc}	–0.15	0.25 * V_{DDQ}	V	5
AC Input Reference Voltage	V_{REFac}	0.47 * V_{DDQ}	0.53 * V_{DDQ}	V	1
AC Input High Voltage	V_{IH1ac}	V_{REF} + 0.15	V_{DDQ} + 0.25	V	2, 3, 4
AC Input Low Voltage	V_{IL1ac}	–0.25	V_{REF} – 0.15	V	2, 3, 4
AC Input High Voltage	V_{IH2ac}	V_{DDQ} – 0.2	V_{DDQ} + 0.25	V	2, 5
AC Input Low Voltage	V_{IL2ac}	– 0.25	0.2	V	2, 5

Notes:
1. V_{REFac} is equal to V_{REFdc} plus noise.
2. V_{IH} max and V_{IL} min apply for pulse widths less than one-quarter of the cycle time.
3. Input rise and fall times must be a minimum of 1 V/ns, and within 10% of each other.
4. Applies to: CK, $\overline{CK}$, KD, $\overline{KD}$, SA, $\overline{LD}$, R/$\overline{W}$, DQ.
5. Applies to: RST, MVQ, MZT, PZT.

Input Electrical Characteristics when MVQ = 1

Parameter	Symbol	Min	Max	Units	Notes
DC Input Reference Voltage	V_{REFdc}	0.47 * V_{DDQ}	0.53 * V_{DDQ}	V	—
DC Input High Voltage	V_{IH1dc}	V_{REF} + 0.1	V_{DDQ} + 0.15	V	4
DC Input Low Voltage	V_{IL1dc}	–0.15	V_{REF} – 0.1	V	4
DC Input High Voltage	V_{IH2dc}	0.75 * V_{DDQ}	V_{DDQ} + 0.15	V	5
DC Input Low Voltage	V_{IL2dc}	–0.15	0.25 * V_{DDQ}	V	5
AC Input Reference Voltage	V_{REFac}	0.46 * V_{DDQ}	0.54 * V_{DDQ}	V	1
AC Input High Voltage	V_{IH1ac}	V_{REF} + 0.2	V_{DDQ} + 0.25	V	2, 3, 4
AC Input Low Voltage	V_{IL1ac}	–0.25	V_{REF} – 0.2	V	2, 3, 4
AC Input High Voltage	V_{IH2ac}	V_{DDQ} – 0.2	V_{DDQ} + 0.25	V	2, 5
AC Input Low Voltage	V_{IL2ac}	–0.25	0.2	V	2, 5

Notes:
1. V_{REFac} is equal to V_{REFdc} plus noise.
2. V_{IH} max and V_{IL} min apply for pulse widths less than one-quarter of the cycle time.
3. Input rise and fall times must be a minimum of 1V/ns, and within 10% of each other.
4. Applies to: CK, $\overline{CK}$, KD, $\overline{KD}$, SA, $\overline{LD}$, R/$\overline{W}$, DQ.
5. Applies to: RST, MVQ, MZT, PZT.

Output Electrical Characteristics

Parameter	Symbol	Min	Max	Units	Notes
DC Output High Voltage	V_{OHdc}	—	V_{DDQ} + 0.15	V	1
DC Output Low Voltage	V_{OLdc}	-0.15	—	V	1
AC Output High Voltage	V_{OHac}	—	V_{DDQ} + 0.25	V	1
AC Output Low Voltage	V_{OLac}	-0.25	—	V	1

Notes:
1. Applies to: CQ, $\overline{CQ}$, DQ, QVLD.

Leakage Currents

Parameter	Symbol	Min	Max	Units	Notes
Input Leakage Current	I_{LI1}	-2	2	uA	1, 2
	I_{LI2}	-20	2	uA	1, 3
	I_{LI3}	-2	20	uA	1, 4
Output Leakage Current	I_{LO}	-2	2	uA	5, 6

Notes:
1. $V_{IN} = V_{SS}$ to V_{DDQ}.
2. Applies to: CK, $\overline{CK}$, KD, $\overline{KD}$, SA, $\overline{LD}$, R/$\overline{W}$, DQ when ODT is disabled.
   Applies to: MVQ, MZT, PZT, TCK.
3. Applies to: TMS, TDI (weakly pulled up).
4. Applies to: RST (weakly pulled down).
5. $V_{OUT} = V_{SS}$ to V_{DDQ}.
6. Applies to: CQ, $\overline{CQ}$, DQ, QVLD, TDO.

Operating Currents

Parameter	Symbol	Operating Frequency	@ 1.3V V_{DD}	@ 1.35V V_{DD}	@ 1.4V V_{DD}	Units
x18 Operating Current	I_{DD}	725 MHz	1640	1730	1830	mA
		625 MHz	1470	1550	1650	mA
		550 MHz	1330	1410	1490	mA
x36 Operating Current	I_{DD}	725 MHz	2250	2370	2490	mA
		625 MHz	2000	2110	2230	mA
		550 MHz	1820	1930	2030	mA

Notes:
1. I_{OUT} = 0 mA; $V_{IN} = V_{IH}$ or V_{IL}.
2. Applies at 50% Reads + 50% Writes.

AC Test Conditions for 1.2V nominal V_{DDQ} (MVQ = 0)

Parameter	Symbol	Conditions	Units
Core Supply Voltage	V_{DD}	1.3 to 1.4	V
I/O Supply Voltage	V_{DDQ}	1.15 to 1.25	V
Input Reference Voltage	V_{REF}	0.6	V
Input High Level	V_{IH}	0.9	V
Input Low Level	V_{IL}	0.3	V
Input Rise and Fall Time	—	2.0	V/ns
Input and Output Reference Level	—	0.6	V

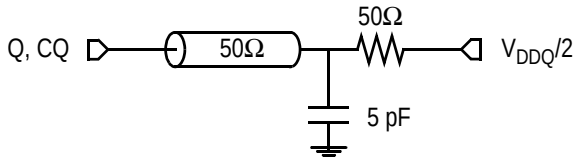
Note:
Output Load Conditions RQ = 200Ω. Refer to figure below.

AC Test Conditions for 1.5V nominal V_{DDQ} (MVQ = 1)

Parameter	Symbol	Conditions	Units
Core Supply Voltage	V_{DD}	1.3 to 1.4	V
I/O Supply Voltage	V_{DDQ}	1.4 to 1.6	V
Input Reference Voltage	V_{REF}	0.75	V
Input High Level	V_{IH}	1.25	V
Input Low Level	V_{IL}	0.25	V
Input Rise and Fall Time	—	2.0	V/ns
Input and Output Reference Level	—	0.75	V

Note:
Output Load Conditions RQ = 200Ω. Refer to figure below.

AC Test Output Load



AC Timing Specifications

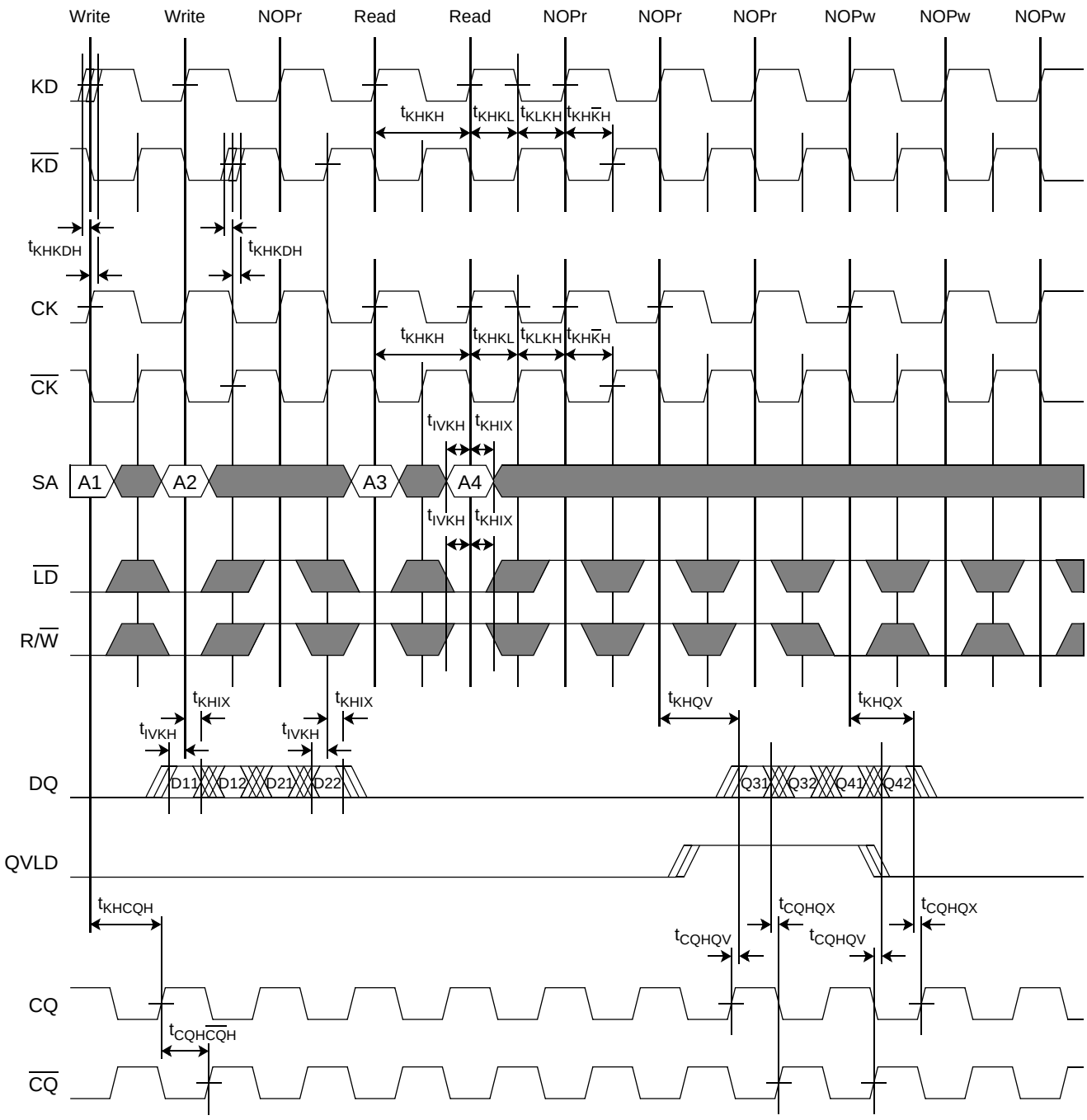
Parameter	Symbol	Min	Max	Units	Notes
Input Clock Timing (Met by the IP)					
Clk Cycle Time (-725)	t_{KHKH}	1.38	—	ns	1
Clk Cycle Time (-625)		1.6			
Clk Cycle Time (-550)		1.8			
Clk High Pulse Width	t_{KHKL}	0.45	—	cycles	1
Clk Low Pulse Width	t_{KLKH}	0.45	—	cycles	1
Clk High to $\overline{\text{Clk}}$ High	$t_{KH\overline{K}H}$	0.45	0.55	cycles	2
Clk High to Write Data Clk High	t_{KHKDH}	-200	200	ps	3
Input Timing (Met by the IP)					
Input Valid to Clk High	t_{IVKH}	not specified	—	ps	4
Clk High to Input Hold	t_{KHIX}	not specified	—	ps	4
Input Pulse Width	t_{IPW}	200	—	ps	5
Output Timing (Accounted for by the IP)					
Clk High to Data Output Valid / Hold	$t_{KHQV/X}$	1.0	2.5	ns	6
Clk High to Echo Clock High	t_{KHCQH}	1.0	2.5	ns	7
Echo Clk High to $\overline{\text{Echo Clk}}$ High	$t_{CQH\overline{CQ}H}$	$t_{KH\overline{K}H}$ (min) - 50	$t_{KH\overline{K}H}$ (max) + 50	ps	8, 11
$\overline{\text{Echo Clk}}$ High to Echo Clk High	$t_{\overline{CQ}HCQH}$	$t_{\overline{K}HKH}$ (min) - 50	$t_{\overline{K}HKH}$ (max) + 50	ps	9, 11
Echo Clk High to Data Output Valid / Hold	$t_{CQHQV/X}$	-150	150	ps	10, 11

Notes:

All parameters are measured from the mid-point of the object signal to the mid-point of the reference signal.

1. Parameters apply to CK, $\overline{\text{CK}}$, KD, $\overline{\text{KD}}$.
2. Parameters specify ↑CK → ↑$\overline{\text{CK}}$ and ↑KD → ↑$\overline{\text{KD}}$ requirements.
3. Parameters specify ↑CK → ↑KD and ↑$\overline{\text{CK}}$ → ↑$\overline{\text{KD}}$ requirements.
4. Parameters apply to SA, and are referenced to ↑CK.
   Parameters apply to $\overline{\text{LD}}$, R/$\overline{\text{W}}$, and are referenced to ↑CK.
   Parameters apply to DQ, and are referenced to ↑KD & ↑$\overline{\text{KD}}$.
   The unspecified setup and hold time requirements for these inputs are met by the IP (via per-pin calibration for the DDR inputs).
5. Parameter applies to SA, $\overline{\text{LD}}$, R/$\overline{\text{W}}$, DQ.
6. Parameters apply to DQ and are referenced to ↑CK & ↑$\overline{\text{CK}}$.
7. Parameters specify ↑CK → ↑CQ and ↑$\overline{\text{CK}}$ → ↑$\overline{\text{CQ}}$ timing.
8. Parameter specifies ↑CQ → ↑$\overline{\text{CQ}}$ timing. $t_{KH\overline{K}H}$ (min) and $t_{KH\overline{K}H}$ (max) are the minimum and maximum input delays from ↑CK to ↑$\overline{\text{CK}}$.
9. Parameter specifies ↑$\overline{\text{CQ}}$ → ↑CQ timing. $t_{\overline{K}HKH}$ (min) and $t_{\overline{K}HKH}$ (max) are the minimum and maximum input delays from ↑$\overline{\text{CK}}$ to ↑CK.
10. Parameters apply to DQ, QVLD and are referenced to ↑CQ & ↑$\overline{\text{CQ}}$.
11. Parameters are not tested. They are guaranteed by design, and verified through extensive corner-lot characterization.

Read and Write Timing Diagram



JTAG Test Mode Description

These devices provide a JTAG Test Access Port (TAP) and Boundary Scan interface using a limited set of IEEE std. 1149.1 functions. This test mode is intended to provide a mechanism for testing the interconnect between master (processor, controller, etc.), ECCRAM, other components, and the printed circuit board. In conformance with a subset of IEEE std. 1149.1, these devices contain a TAP Controller and multiple TAP Registers. The TAP Registers consist of one Instruction Register and multiple Data Registers.

The TAP consists of the following four signals:

Pin	Pin Name	I/O	Description
TCK	Test Clock	I	Induces (clocks) TAP Controller state transitions.
TMS	Test Mode Select	I	Inputs commands to the TAP Controller. Sampled on the rising edge of TCK.
TDI	Test Data In	I	Inputs data serially to the TAP Registers. Sampled on the rising edge of TCK.
TDO	Test Data Out	O	Outputs data serially from the TAP Registers. Driven from the falling edge of TCK.

Concurrent TAP and Normal ECCRAM Operation

According to IEEE std. 1149.1, most public TAP Instructions do not disrupt normal device operation. In these devices, the only exceptions are EXTEST and SAMPLE-Z. See the Tap Registers section for more information.

Disabling the TAP

When JTAG is not used, TCK should be tied Low to prevent clocking the ECCRAM. TMS and TDI should either be tied High through a pull-up resistor or left unconnected. TDO should be left unconnected.

JTAG DC Operating Conditions

Parameter	Symbol	Min	Max	Units	Notes
JTAG Input High Voltage	V_{TIH}	$0.75 * V_{DDQ}$	$V_{DDQ} + 0.15$	V	1
JTAG Input Low Voltage	V_{TIL}	–0.15	$0.25 * V_{DDQ}$	V	1
JTAG Output High Voltage	V_{TOH}	$V_{DDQ} – 0.2$	—	V	2, 3
JTAG Output Low Voltage	V_{TOL}	—	0.2	V	2, 4

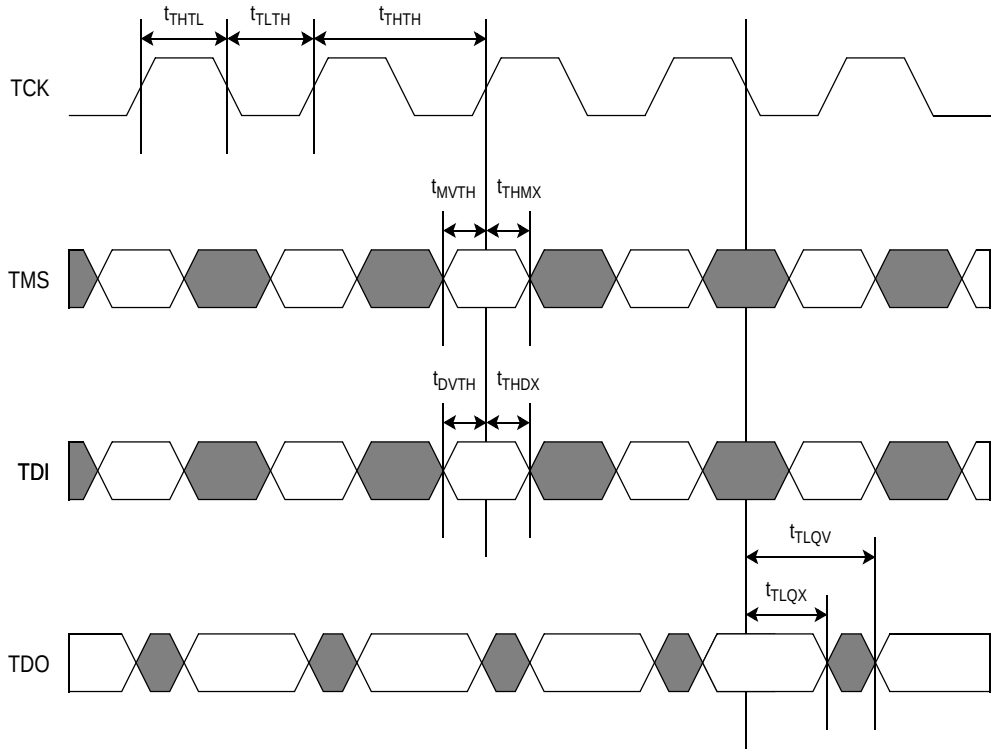
Notes:

1. Parameters apply to TCK, TMS, and TDI during JTAG Testing.
2. Parameters apply to TDO during JTAG testing.
3. I_{TOH} = –2.0 mA.
4. I_{TOL} = 2.0 mA.

JTAG AC Timing Specifications

Parameter	Symbol	Min	Max	Units
TCK Cycle Time	t_{THTH}	50	—	ns
TCK High Pulse Width	t_{THTL}	20	—	ns
TCK Low Pulse Width	t_{TLTH}	20	—	ns
TMS Setup Time	t_{MVTH}	10	—	ns
TMS Hold Time	t_{THMX}	10	—	ns
TDI Setup Time	t_{DVTH}	10	—	ns
TDI Hold Time	t_{THDX}	10	—	ns
Capture Setup Time (Address, Control, Data, Clock)	t_{CS}	10	—	ns
Capture Hold Time (Address, Control, Data, Clock)	t_{CH}	10	—	ns
TCK Low to TDO Valid	t_{TLQV}	—	10	ns
TCK Low to TDO Hold	t_{TLQX}	0	—	ns

JTAG Timing Diagram



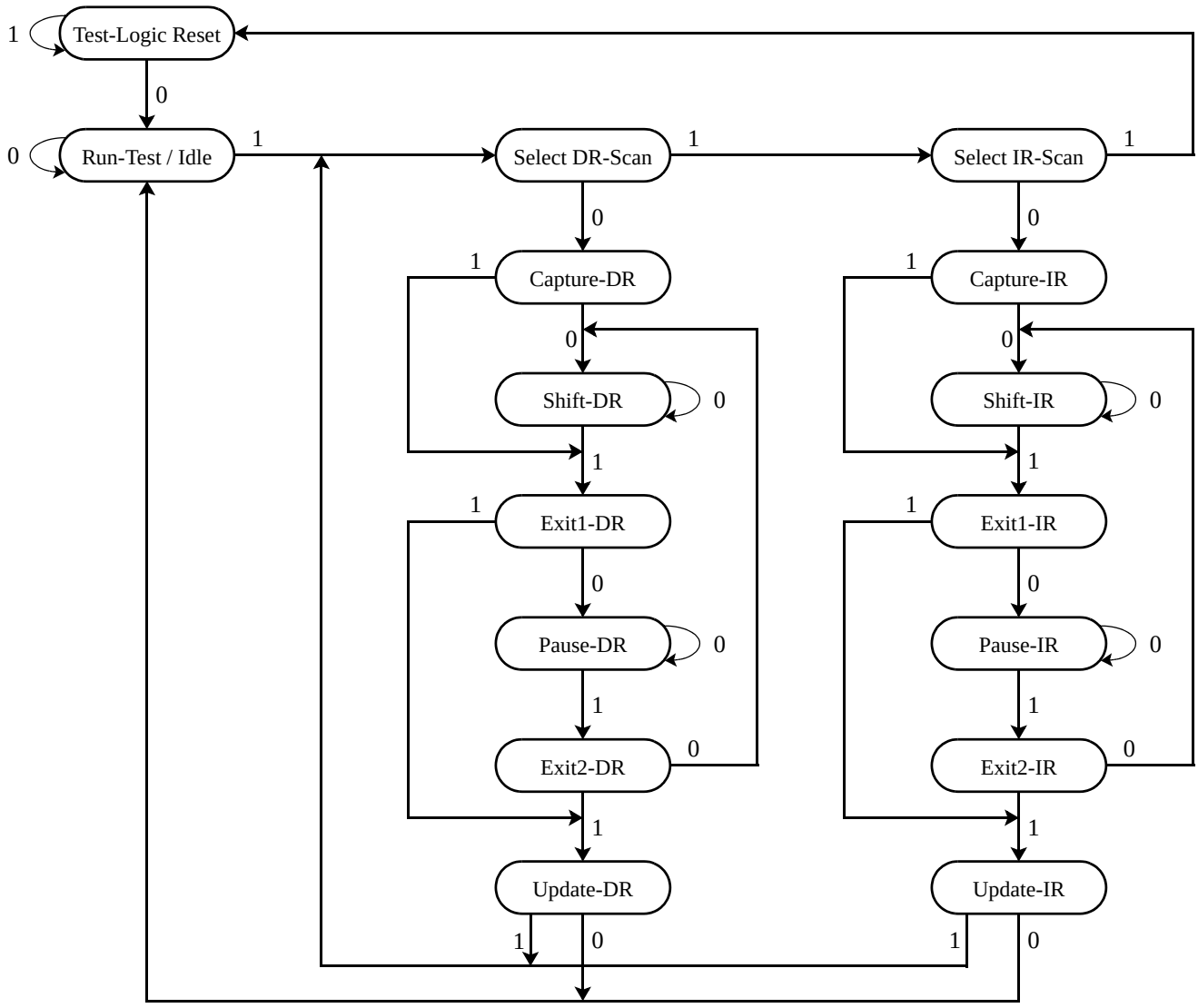
TAP Controller

The TAP Controller is a 16-state state machine that controls access to the various TAP Registers and executes the operations associated with each TAP Instruction. State transitions are controlled by TMS and occur on the rising edge of TCK.
The TAP Controller enters the Test-Logic Reset state in one of two ways:

1. At power up.
2. When a logic 1 is applied to TMS for at least 5 consecutive rising edges of TCK.

The TDI input receiver is sampled only when the TAP Controller is in either the Shift-IR state or the Shift-DR state.
The TDO output driver is enabled only when the TAP Controller is in either the Shift-IR state or the Shift-DR state.

TAP Controller State Diagram



TAP Registers

TAP Registers are serial shift registers that capture serial input data (from TDI) on the rising edge of TCK, and drive serial output data (to TDO) on the subsequent falling edge of TCK. They are divided into two groups: Instruction Registers (IR), which are manipulated via the IR states in the TAP Controller, and Data Registers (DR), which are manipulated via the DR states in the TAP Controller.

Instruction Register (IR - 3 bits)

The Instruction Register stores the various TAP Instructions supported by ECCRAM. It is loaded with the IDCODE instruction (logic 001) at power-up, and when the TAP Controller is in the Test-Logic Reset and Capture-IR states. It is inserted between TDI and TDO when the TAP Controller is in the Shift-IR state, at which time it can be loaded with a new instruction. However, newly loaded instructions are not executed until the TAP Controller has reached the Update-IR state.

The Instruction Register is 3 bits wide, and is encoded as follows:

Code (2:0)	Instruction	Description
000	EXTEST	Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state. Also transfers the contents of the Boundary Scan Register associated with all output signals (DQ, QVLD, CQ, $\overline{CQ}$) directly to their corresponding output pins. However, newly loaded Boundary Scan Register contents do not appear at the output pins until the TAP Controller has reached the Update-DR state. Also disables all ODT. See the Boundary Scan Register description for more information.
001	IDCODE	Loads a predefined device- and manufacturer-specific identification code into the ID Register when the TAP Controller is in the Capture-DR state, and inserts the ID Register between TDI and TDO when the TAP Controller is in the Shift-DR state. See the ID Register description for more information.
010	SAMPLE-Z	Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state. Also disables all ODT. Also forces DQ output drivers to a High-Z state. See the Boundary Scan Register description for more information.
011	PRIVATE	Reserved for manufacturer use only.
100	SAMPLE	Loads the logic states of all signals composing the ECCRAM I/O ring into the Boundary Scan Register when the TAP Controller is in the Capture-DR state, and inserts the Boundary Scan Register between TDI and TDO when the TAP Controller is in the Shift-DR state. See the Boundary Scan Register description for more information.
101	PRIVATE	Reserved for manufacturer use only.
110	PRIVATE	Reserved for manufacturer use only.
111	BYPASS	Loads a logic 0 into the Bypass Register when the TAP Controller is in the Capture-DR state, and inserts the Bypass Register between TDI and TDO when the TAP Controller is in the Shift-DR state. See the Bypass Register description for more information.

Bypass Register (DR - 1 bit)

The Bypass Register is one bit wide, and provides the minimum length serial path between TDI and TDO. It is loaded with a logic 0 when the BYPASS instruction has been loaded in the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the BYPASS instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

ID Register (DR - 32 bits)

The ID Register is loaded with a predetermined device- and manufacturer-specific identification code when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the IDCODE instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

The ID Register is 32 bits wide, and is encoded as follows:

See BSDL Model (31:12)	**GSI ID** (11:1)	**Start Bit (0)**
XXXX XXXX XXXX XXXX XXXX	0001 1011 001	1

Bit 0 is the LSB of the ID Register, and Bit 31 is the MSB. When the ID Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

Boundary Scan Register (DR - 127 bits)

The Boundary Scan Register is equal in length to the number of active signal connections to the ECCRAM (excluding the TAP pins) plus a number of place holder locations reserved for functional and/or density upgrades. It is loaded with the logic states of all signals composing the ECCRAM's I/O ring when the EXTEST, SAMPLE, or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the Capture-DR state. It is inserted between TDI and TDO when the EXTEST, SAMPLE, or SAMPLE-Z instruction has been loaded into the Instruction Register and the TAP Controller is in the Shift-DR state.

Additionally, the contents of the Boundary Scan Register associated with the ECCRAM outputs (DQ, QVLD, CQ, $\overline{CQ}$) are driven directly to the corresponding ECCRAM output pins when the EXTEST instruction is selected. However, after the EXTEST instruction has been selected, any new data loaded into Boundary Scan Register when the TAP Controller is in the Shift-DR state does not appear at the output pins until the TAP Controller has reached the Update-DR state.

The value captured in the boundary scan register for NU pins is determined by the external pin state while the NC pins are 0 regardless of the external pin state. The value captured in the internal cells is 1.

Output Driver State During EXTEST

EXTEST allows the Internal Cell (Bit 127) in the Boundary Scan Register to control the state of DQ drivers. That is, when Bit 127 = 1, DQ drivers are enabled (i.e., driving High or Low), and when Bit 127 = 0, DQ drivers are disabled (i.e., forced to High-Z state). See the Boundary Scan Register section for more information.

ODT State During EXTEST and SAMPLE-Z

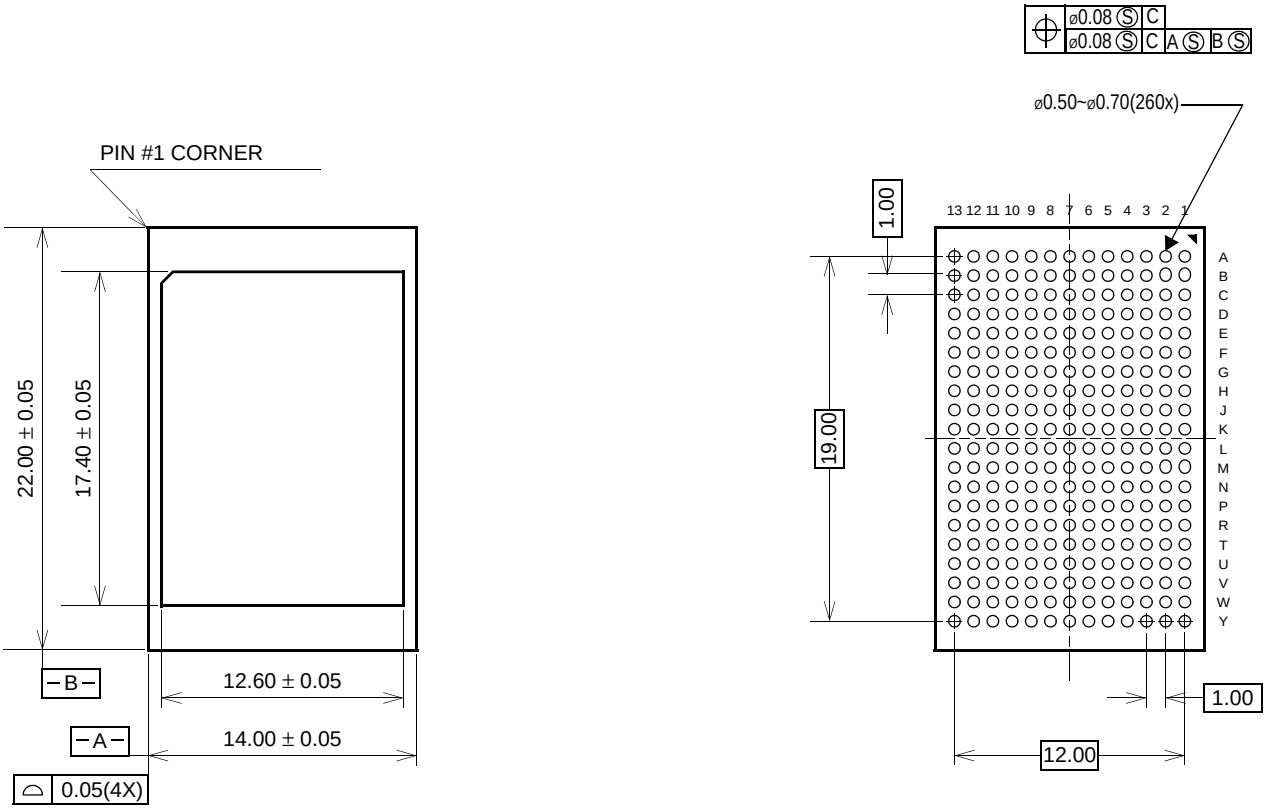
ODT on all inputs is disabled during EXTEST and SAMPLE-Z.

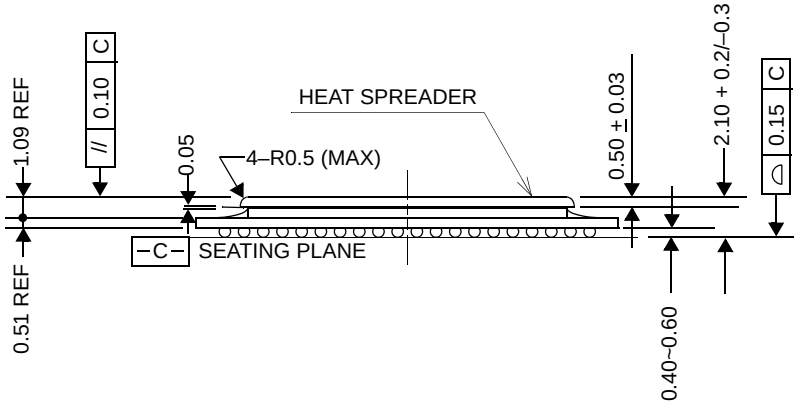
Boundary Scan Register Bit Order Assignment

The table below depicts the order in which the bits are arranged in the Boundary Scan Register. Bit 1 is the LSB and Bit 127 is the MSB. When the Boundary Scan Register is selected, TDI serially shifts data into the MSB, and the LSB serially shifts data out through TDO.

Bit	Pad	Bit	Pad	Bit	Pad	Bit	Pad	Bit	Pad
1	7L	27	10F	53	10U	79	3V	105	3G
2	7K	28	12F	54	13V	80	1V	106	2F
3	9L	29	11G	55	11V	81	4U	107	4F
4	9K	30	13G	56	12W	82	2U	108	1E
5	8J	31	10G	57	10W	83	3T	109	3E
6	7H	32	12G	58	8V	84	1T	110	2D
7	9H	33	11H	59	9U	85	4R	111	4D
8	7G	34	13H	60	8T	86	2R	112	1C
9	8G	35	10J	61	9R	87	3P	113	3C
10	9F	36	12J	62	8P	88	1P	114	2B
11	8E	37	13K	63	9N	89	4P	115	4B
12	7D	38	13L	64	8M	90	2P	116	6A
13	9D	39	11L	65	6M	91	3N	117	6B
14	8C	40	12M	66	7N	92	1N	118	6C
15	8B	41	10M	67	5N	93	4M	119	5D
16	9B	42	13N	68	7P	94	2M	120	6E
17	7A	43	11N	69	6P	95	3L	121	5F
18	9A	44	12P	70	5R	96	1L	122	6G
19	10B	45	10P	71	6T	97	1K	123	5H
20	12B	46	13P	72	7U	98	2J	124	6J
21	11C	47	11P	73	5U	99	4J	125	5K
22	13C	48	12R	74	6V	100	1H	126	5L
23	10D	49	10R	75	6W	101	3H	127	Internal
24	12D	50	13T	76	7Y	102	2G		
25	11E	51	11T	77	4W	103	4G		
26	13E	52	12U	78	2W	104	1G		

260-Pin BGA Package Drawing (Package K)





Ball Pitch:	1.00	Substrate Thickness:	0.51
Ball Diameter:	0.60	Mold Thickness:	—

Ordering Information — GSI SigmaDDR-IIIe ECCRAMs

Org	Part Number	Type	Package	Speed (MHz)	T_A
4M x 18	GS8673ET18BK-725S	SigmaDDR-IIIe B2	260 Pin BGA	725	C
4M x 18	GS8673ET18BK-625S	SigmaDDR-IIIe B2	260 Pin BGA	625	C
4M x 18	GS8673ET18BK-550S	SigmaDDR-IIIe B2	260 Pin BGA	550	C
4M x 18	GS8673ET18BK-725IS	SigmaDDR-IIIe B2	260 Pin BGA	725	I
4M x 18	GS8673ET18BK-625IS	SigmaDDR-IIIe B2	260 Pin BGA	625	I
4M x 18	GS8673ET18BK-550IS	SigmaDDR-IIIe B2	260 Pin BGA	550	I
2M x 36	GS8673ET36BK-725S	SigmaDDR-IIIe B2	260 Pin BGA	725	C
2M x 36	GS8673ET36BK-625S	SigmaDDR-IIIe B2	260 Pin BGA	625	C
2M x 36	GS8673ET36BK-550S	SigmaDDR-IIIe B2	260 Pin BGA	550	C
2M x 36	GS8673ET36BK-725IS	SigmaDDR-IIIe B2	260 Pin BGA	725	I
2M x 36	GS8673ET36BK-625IS	SigmaDDR-IIIe B2	260 Pin BGA	625	I
2M x 36	GS8673ET36BK-550IS	SigmaDDR-IIIe B2	260 Pin BGA	550	I
4M x 18	GS8673ET18BGK-725S	SigmaDDR-IIIe B2	RoHS-compliant 260 Pin BGA	725	C
4M x 18	GS8673ET18BGK-625S	SigmaDDR-IIIe B2	RoHS-compliant 260 Pin BGA	625	C
4M x 18	GS8673ET18BGK-550S	SigmaDDR-IIIe B2	RoHS-compliant 260 Pin BGA	550	C
4M x 18	GS8673ET18BGK-725IS	SigmaDDR-IIIe B2	RoHS-compliant 260 Pin BGA	725	I
4M x 18	GS8673ET18BGK-625IS	SigmaDDR-IIIe B2	RoHS-compliant 260 Pin BGA	625	I
4M x 18	GS8673ET18BGK-550IS	SigmaDDR-IIIe B2	RoHS-compliant 260 Pin BGA	550	I
2M x 36	GS8673ET36BGK-725S	SigmaDDR-IIIe B2	RoHS-compliant 260 Pin BGA	725	C
2M x 36	GS8673ET36BGK-625S	SigmaDDR-IIIe B2	RoHS-compliant 260 Pin BGA	625	C
2M x 36	GS8673ET36BGK-550S	SigmaDDR-IIIe B2	RoHS-compliant 260 Pin BGA	550	C
2M x 36	GS8673ET36BGK-725IS	SigmaDDR-IIIe B2	RoHS-compliant 260 Pin BGA	725	I
2M x 36	GS8673ET36BGK-625IS	SigmaDDR-IIIe B2	RoHS-compliant 260 Pin BGA	625	I
2M x 36	GS8673ET36BGK-550IS	SigmaDDR-IIIe B2	RoHS-compliant 260 Pin BGA	550	I

Note: C = Commercial Temperature Range. I = Industrial Temperature Range.

