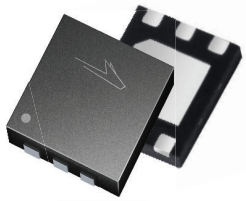
GTRA360502M

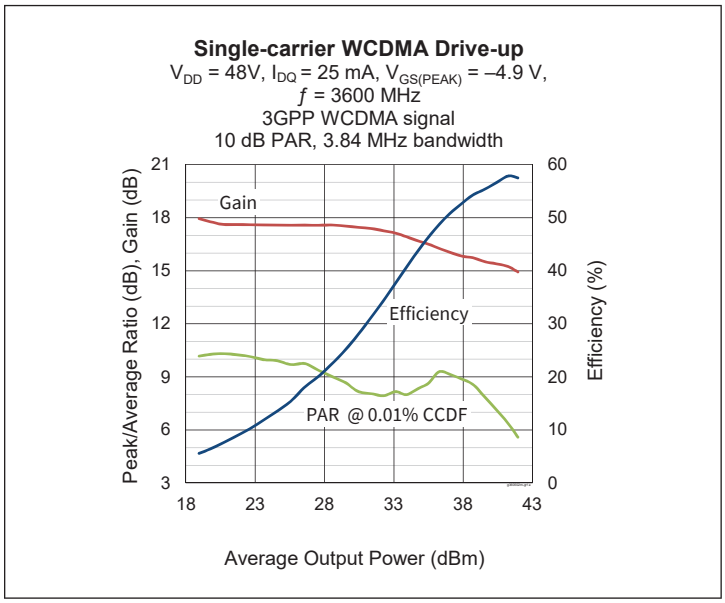
Thermally-Enhanced High Power RF GaN on SiC HEMT
50 W, 48 V, 3400 – 3800 MHz

Description

The GTRA360502M houses two GaN-on-SiC power transistor for use in asymmetric Doherty power amplifiers. The device has been designed for use in communications infrastructure applications from 3,400 MHz to 3,800 MHz. It operates from a supply voltage of up to 50 volts and delivers a maximum, average output power of 8 watts.



GTRA360502M
Package PG-DFN-6.5x7-1



Features

- GaN on SiC HEMT technology
- Asymmetrical Doherty design
  - Main: P_{3dB} = 20 W Typ
  - Peak: P_{3dB} = 36 W Typ
- Typical pulsed CW performance, 3600 MHz, 48 V, 10 µs bandwidth, 10% duty cycle (Doherty configuration)
  - Output power at P_{3dB} = 50 W
  - Drain efficiency = 62% @ 50 W
- Human Body Model Class 1A (per ANSI/ESDA/JEDEC JS-001)
- Pb-free and RoHS compliant
- Low thermal resistance

RF Characteristics

Typical RF Characteristics (tested in Wolfspeed application circuit)
V_{DD} = 48 V, I_{DQ} = 25 mA, $V_{GS(PEAK)}$ = –4.9 V, channel bandwidth = 3.84 MHz, 10 dB peak/average @ 0.01% CCDF

Freq MHz	Pout W	Gain dB	Eff %	PAR dB	ALT1 dBc	–ALT1 dBc	ALT2 dBc	–ALT2 dBc
3400	39.0	14.9	54.1	8.8	–23.3	–23.1	–34.4	–34.2
3500	39.0	15.6	55.2	8.7	–24.5	–24.6	–36.2	–36.2
3600	39.0	15.6	53.9	8.3	–26.1	–26.2	–37.0	–37.0
3700	39.0	15.2	55.3	7.9	–29.4	–29.1	–39.1	–38.7
3800	39.0	14.5	50.9	6.9	–32.0	–31.8	–41.0	–40.6

All published data at T_{CASE} = 25°C unless otherwise indicated

ESD: Electrostatic discharge sensitive device—observe handling precautions!

RoHS COMPLIANT

4600 Silicon Drive | Durham, NC 27703 | www.wolfspeed.com

DC Characteristics

Characteristic		Conditions	Symbol	Min	Typ	Max	Unit
Drain-source Breakdown Voltage	(main)	V_{GS} = –8 V, I_D = 0.36 mA	$V_{(BR)DSS}$	150	—	—	V
	(peak)	V_{GS} = –8 V, I_D = 0.60 mA	$V_{(BR)DSS}$	150	—	—	V
Drain-source Leakage Current	(main)	V_{DS} = 10 V, V_{GS} = –8 V	I_{DSS}	—	—	0.36	mA
	(peak)	V_{DS} = 10 V, V_{GS} = –8 V	I_{DSS}	—	—	0.80	mA
Gate Threshold Voltage	(main)	V_{DS} = 10 V, I_D = 2.6 mA	$V_{GS(th)}$	–3.8	–3.0	–2.3	V
	(peak)	V_{DS} = 10 V, I_D = 4.3 mA	$V_{GS(th)}$	–3.8	–3.0	–2.3	V

Recommended Operating Conditions

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Operating Voltage		V_{DD}	0	—	50	V
Gate Quiescent Voltage	V_{DS} = 48 V, I_D = 25 mA	$V_{GS(Q)}$	–4	–3.0	–2.1	V

Absolute Maximum Ratings

Parameter		Symbol	Value	Unit
Drain-source Voltage		V_{DSS}	125	V
Gate-source Voltage		V_{GS}	–10 to +2	V
Operating Voltage		V_{DD}	55	V
Gate Current	(main)	I_G	2.6	mA
	(peak)	I_G	4.30	mA
Drain Current	(main)	I_D	0.97	A
	(peak)	I_D	1.60	A
Junction Temperature		T_J	225	°C
Storage Temperature Range		T_{STG}	–65 to +150	°C

Operation above the maximum values listed here may cause permanent damage. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the component. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. For reliable continuous operation, the device should be operated within the operating voltage range (V_{DD}) specified above.

Thermal Characteristics

Parameter		Symbol	Value	Unit
Thermal Resistance	(main) T_{CASE} = 70°C, 5 W DC	$R_{\theta JC}$	7.3	°C/W
	(peak) T_{CASE} = 70°C, 20 W DC	$R_{\theta JC}$	6.5	°C/W

Moisture Sensitivity Level

Level	Test Signal	Package Temperature	Unit
3	IPC/JEDEC J-STD-020	260	°C

RF Characteristics

Single-carrier WCDMA Specifications (tested in Wolfspeed Doherty production test fixture)
V_{DD} = 48 V, I_{DQ} = 22 to 28 mA, P_{OUT} = 7.9 W avg, $V_{GS(PEAK)}$ = –4.5 V, f = 3600 MHz, channel bandwidth = 3.84 MHz, peak/average = 10 dB @ 0.01% CCDF

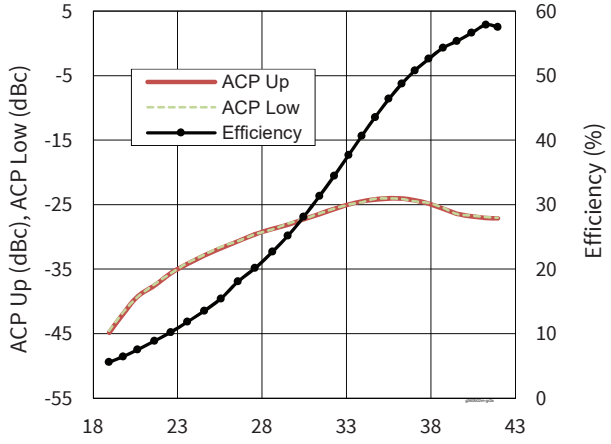
Characteristic	Symbol	Min	Typ	Max	Unit
Gain	G_{ps}	12	13	—	dB
Drain Efficiency	η_D	42	46	—	%
Adjacent Channel Power Ratio	ACPR	—	–22	–19	dBc
Output PAR @ 0.01% CCDF	OPAR	6.5	7.5	—	dB

Ordering Information

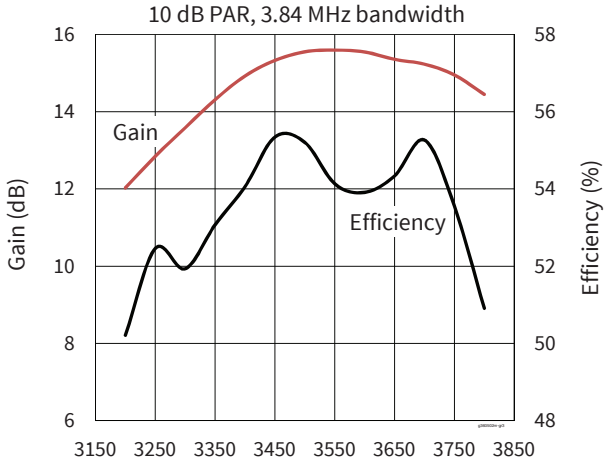
Type and Version	Order Code	Package Description	Shipping
GTRA360502M V1 R3K	GTRA360502M-V1-R3K	PG-DFN-6.5x7-1	Tape & Reel, 3,000 pcs

Typical Performance (data taken in Wolfspeed application circuit)

Single-carrier WCDMA Drive-up
V_{DD} = 48 V, I_{DQ} = 25 mA, $V_{GS(PEAK)}$ = –4.9V,
f = 3600 MHz
3GPP WCDM signal, 10 dB PAR, 3.84 MHz bandwidth



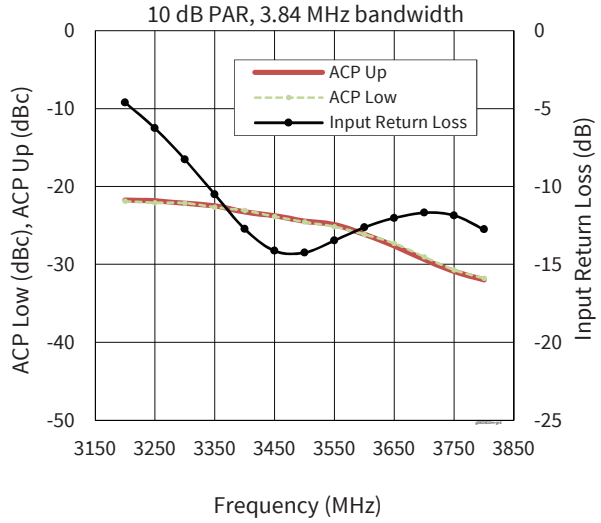
Single-carrier WCDMA, Broadband
V_{DD} = 48 V, I_{DQ} = 25 mA,
$V_{GS(PEAK)}$ = –4.9 V, P_{OUT} = 39 dBm,
3GPP WCDMA signal,
10 dB PAR, 3.84 MHz bandwidth



Typical Performance (cont.)

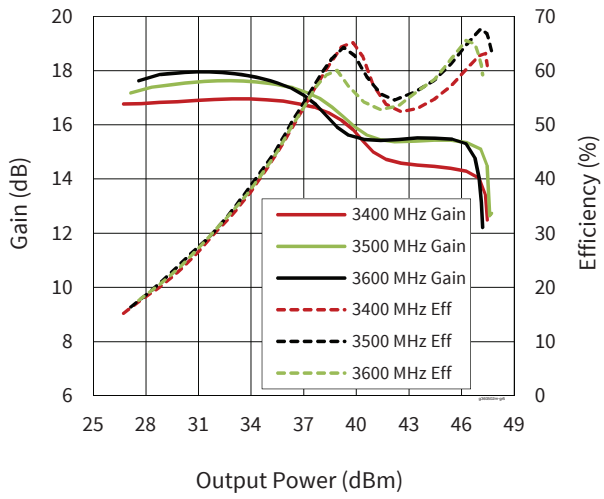
Single-carrier WCDMA, Broadband

V_{DD} = 48 V, I_{DQ} = 25 mA,
$V_{GS(PEAK)}$ = –4.9 V, P_{OUT} = 39 dBm,
3GPP WCDMA signal,
10 dB PAR, 3.84 MHz bandwidth



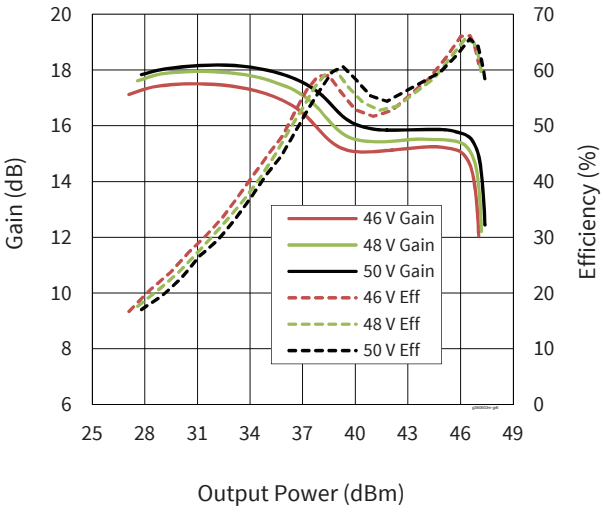
Pulsed CW Performance

V_{DD} = 48 V, I_{DQ} = 25 mA, $V_{GS(PEAK)}$ = –4.9 V
20 µs pulse width, 10% duty cycle



Pulsed CW Performance at various V_{DD}

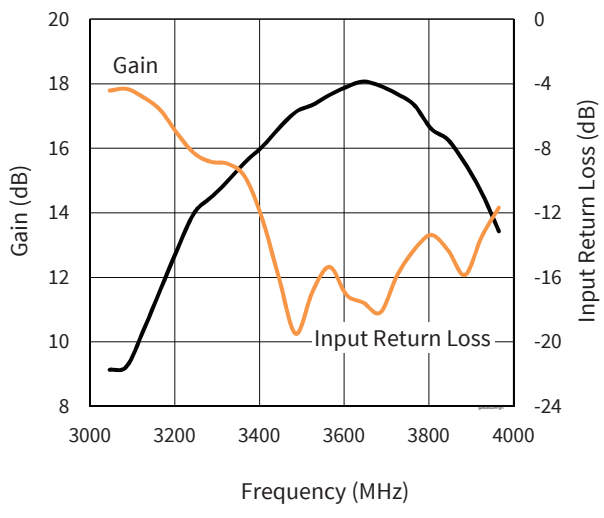
I_{DQ} = 25 mA, $V_{GS(PEAK)}$ = –4.9 V, 20 µs pulse width,
10% duty cycle, f = 3600 MHz



CW Performance, Small Signal

Gain and Input Return Loss

V_{DD} = 48 V, I_{DQ}= 25 mA, $V_{GS(PEAK)}$ = –4.9 V



Load Pull

Main Side Load Pull Performance – Pulsed CW signal: 10 µs, 10% duty cycle, 48 V, I_{DQ} = 25 mA, class AB

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Z_L [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Z_L [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]
3400	12.4 – j29.6	24.8 + j17.8	15.2	43.8	24	62.0	13.6 + j31.3	18	42.2	17	67
3600	22.3 – j22.7	20.8 + j11.8	15.9	43.6	23	60.0	13.2 + j27.6	20	41.8	15	65

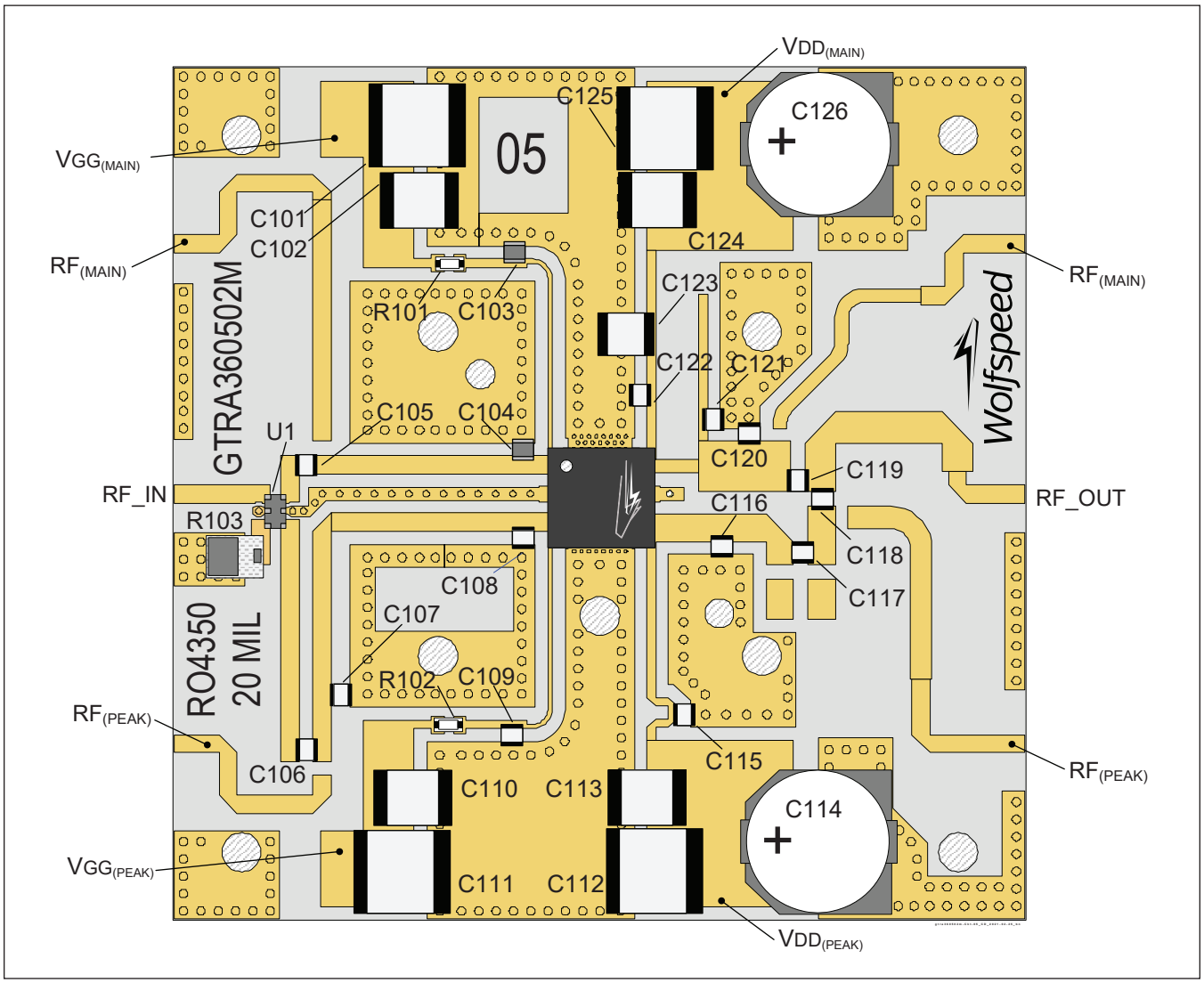
Peak Side Load Pull Performance – Pulsed CW signal: 10 µs, 10% duty cycle, 48 V, I_{DQ} = 43 mA, class AB

		P_{3dB}									
		Max Output Power					Max Drain Efficiency				
Freq [MHz]	Zs [Ω]	Z_L [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]	Z_L [Ω]	Gain [dB]	P_{3dB} [dBm]	P_{3dB} [W]	ηD [%]
3400	19.2 – j19.5	13.6 + j11.9	15.7	46.3	43	60.0	9.2 + j20	17.5	44.9	31	66
3600	10.3 – j2.9	11 + j11	15.5	45.7	37	57.0	8.5 + j16.6	16.8	44.7	30	62

See next page for application circuit

Application Circuit, 3400 – 3600 MHz

DUT	GTRA360502M V1
Test Fixture Part No.	LTA/GTRA360502M-E10
PCB	Rogers 4350, 0.508 mm [0.020”] thick, 2 oz. copper, ε_r = 3.66



Application circuit assembly diagram (not to scale)

Application Circuit (cont.)

Components Table

Component	Description	Manufacturer	P/N
C101, C111, C112, C125	Capacitor, 10 µF, 100 V	TDK Corporation	C5750X7S2A106M230KB
C102, C110, C113, C124	Capacitor, 1 µF 100 V	TDK Corporation	C4532X7R2A105M230KA
C103, C105, C106, C109, C115, C117,C118, C119, C122	Capacitor, 10 pF	ATC	ATC800A100JT250T
C104	Capacitor, 0.3 pF	ATC	ATC800A0R3CT250T
C107	Capacitor, 0.1 pF	ATC	ATC800A0R1CT250T
C108	Capacitor, 0.7 pF	ATC	ATC800A0R7CT250T
C114, C126	100 µF	Panasonic Electronic Components	EEE-FK1J101P
C116	Capacitor, 1.2 pF	ATC	ATC800A1R2CT250T
C120	Capacitor, 1.0 pF	ATC	ATC800A1R0CT250T
C121	Capacitor, 15 pF	ATC	ATC800A150JT250T
C123	10 µF, 100 V	Murata Electronics	GRM32EC72A106KE05L
R101, R102	Resistor, 5.1 ohms	Panasonic Electronic Components	ERJ-8GEYJ5R1V
R103	Resistor, 50 ohms	Anaren	C8A50Z4A
U1	90-degree Hybrid Coupler, 3.3 – 3.7 GHz	Anaren	C3337J5003AH

Bias Sequencing

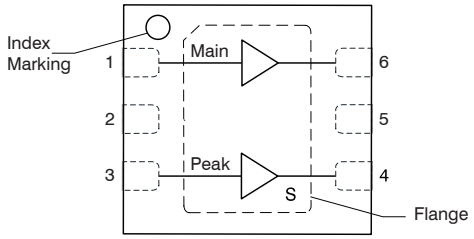
Bias ON

1. Ensure RF is turned off
2. Apply pinch-off voltage of –5 V to the gate
3. Apply nominal drain voltage
4. Bias gate to desired quiescent drain current
5. Apply RF

Bias OFF

1. Turn RF off
2. Appliy pinch-off voltage to the gate
3. Turn off drain voltage
4. Turn off gate voltage

Pinout Diagram (Package PG-DFN-6.5x7-1, top view)



Pin	Description
1	RF_{IN} (main)
2	N/C*
3	RF_{IN} (peak)
4	RF_{OUT} (peak)
5	N/C*
6	RF_{OUT} (main)
S	Ground (package, flange)

** It is recommended that all pins labelled "N/C" be connected to ground*

Package Outline Specifications

Package PG-DFN-6.5x7-1

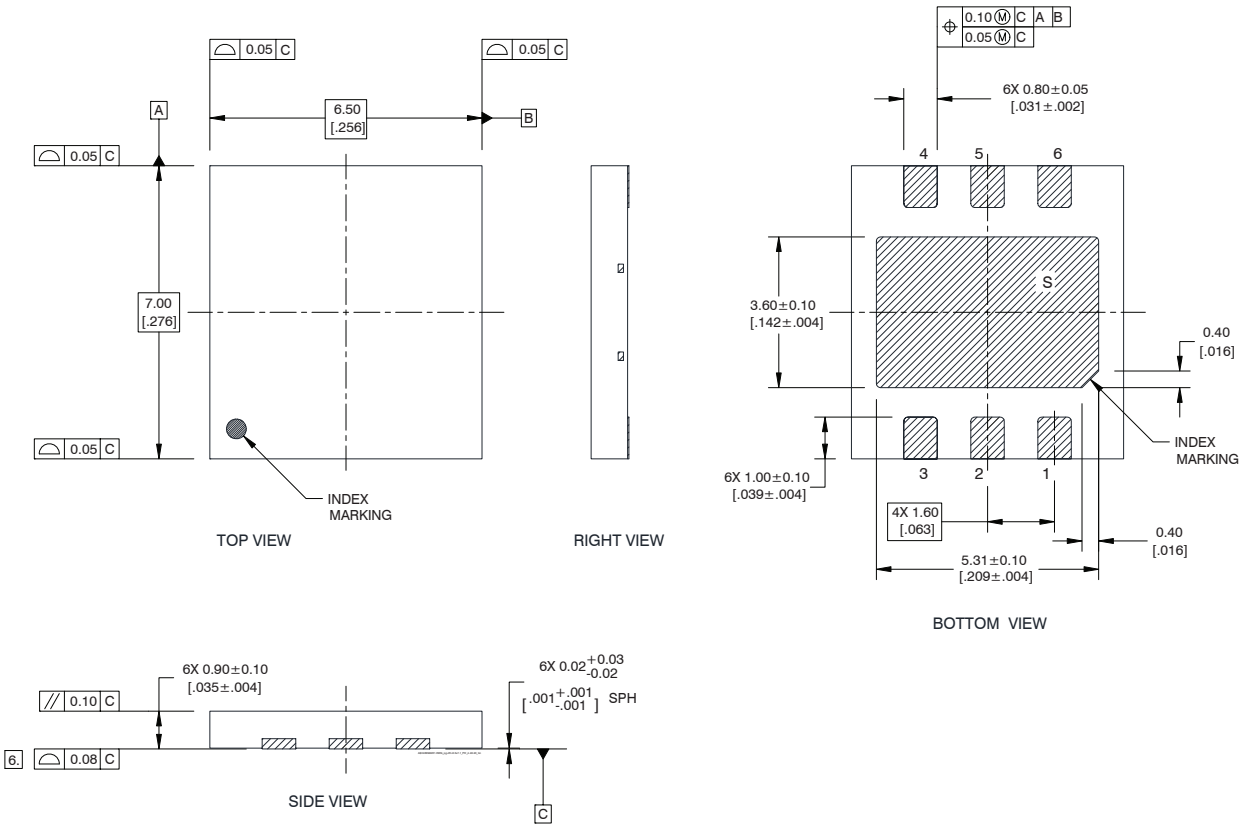


Diagram Notes—unless otherwise specified

1. Interpret dimensions and tolerances per ASME Y14.5M-1994
2. Package dimensions: 6.50 mm X 7.00 mm X 0.90 mm
3. Primary dimensions are mm; alternate dimensions are inches
4. Pinout Diagram on previous page
5. Tin plating thickness: 7 to 15 micron [275.6 to 590.6 microinch]
6. Coplanarity applies to all terminals and flange