GOWIN
PROGRAMMING FOR FUTURE

GW1N series of FPGA Products

Data Sheet

DS100-1.8E, 07/08/2019

Disclaimer

Revision History

Date	Version	Description
06/08/2018	1.19E	Initial version published.
07/31/2018	1.2E	● PLL Structure diagram updated; ● User Flash timing parameters added; ● The desxription of systemIO status for blank chips added.
09/12/2018	1.3E	The UG256 package added.
12/10/2018	1.4E	● GW1N-2B/GW1N-4B added; ● The BANK0 and BANK2 of GW1N-6 and GW1N-9 support I3C OpenDrain/PushPull conversion; ● Change the step delay of IODELAY from 25ps to 30 ps.
01/09/2019	1.5E	Oscillator frequency updated.
02/14/2019	1.6E	● Power supply for UV devices updated; ● Recommended Operating Conditions for UV devices updated; ● Part naming figures updated.
06/04/2019	1.7E	● Operating temperature changed to Junction temperature; ● GW1N-1S added; ● Power supply restrictions of BANK0/1/3 in GW1N-6/9 added; ● Description of User Flash in GW1N-2/2B/4/4B/6/9 added； ● GW1N-6/9 EQ144 added.
07/08/2019	1.8E	● GW1N-6/9 MG196, UG169, and EQ176 added; ● GW1N-1S CS30 added.

Contents

List of Figures

List of Tables

1 About This Guide

1.1 Purpose

This data sheet describes the features, product resources and structure, AC/DC characteristics, timing specifications of the configuration interface, and the ordering information of the GW1N series of FPGA products. It is designed to help you to understand the GW1N series of FPGA products quickly and select and use devices appropriately.

1.2 Supported Products

The information in this guide applies to the following products:

GW1N series of FPGA products: GW1N-1, GW1N-1S, GW1N-2, GW1N-2B, GW1N-4, GW1N-4B, GW1N-6, and GW1N-9.

1.3 Related Documents

The latest user guides are available on GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. GW1N series of FPGA Products Data Sheet
2. Gowin FPGA Products Programming and Configuration User Guide
3. GW1N series of FPGA Products Package and Pinout
4. GW1N-1 Pinout
5. GW1N-1S Pinout
6. GW1N-2&2B&4&4B Pinout
7. GW1N-6&9 Pinout

1.4 Abbreviations and Terminology

The abbreviations and terminologies used in this manual are set out in Table 1-1 below.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminology	Name
FPGA	Field Programmable Gate Array
CFU	Configurable Function Unit
CLS	Configurable Logic Slice
CRU	Configurable Routing Unit
LUT4	4-input Look-up Tables
LUT5	5-input Look-up Tables
LUT6	6-input Look-up Tables
LUT7	7-input Look-up Tables
LUT8	8-input Look-up Tables
REG	Register
ALU	Arithmetic Logic Unit
IOB	Input/Output Block
S-SRAM	Shadow SRAM
B-SRAM	Block SRAM
SP	Single Port
SDP	Semi Dual Port
DP	Dual Port
DSP	Digital Signal Processing
DQCE	Dynamic Quadrant Clock Enable
DCS	Dynamic Clock Selector
PLL	Phase-locked Loop
DLL	Delay-locked Loop
CS30	WLCSP30
CM64	WLCSP64
CS72	WLCSP72
QN32	QFN32
QN48	QFN48
LQ100	LQFP100

Abbreviations and Terminology	Name
LQ144	LQFP144
EQ144	ELQFP144
LQ176	LQFP176
EQ176	ELQFP176
MG160	MBGA160
MG196	MBGA196
PG204	PBGA204
PG256	PBGA256
PG256M	PBGA256M
UG332	UBGA332
UG169	UBGA169
TDM	Time Division Multiplexing

1.5 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

+Tel: +86 755 8262 0391

2General Description

The GW1N series of FPGA products are the first generation products in the LittleBee® family. They offer abundant logic resources, multiple I/O standards, embedded BSRAM, DSP, PLL/DLL, and built-in Flash. They are non-volatile FPGA products with low power, instant-start, low-cost, high-security, small size, various packages, and flexible usage.

GOWINSEMI provides a new generation of FPGA hardware development environment through market-oriented independent research and development that supports the GW1N series of FPGA products and applies to FPGA synthesizing, layout, place and routing, data bitstream generation and download, etc.

2.1 Features

- User Flash (GW1N-1,GW1N-1S)
  - 100,000 write cycles
  - Greater than10 years data retention at +85 ℃
  - Selectable 8/16/32 bits data-in and data-out
  - Page size: 256 bytes
  - 3 μA standby current
  - Page write time: 8.2 ms
- User Flash (GW1N-2/2B/4/4B/6/9)
  - Up to 608Kbits
  - 10,000 write cycles
- Lower power consumption
  - 55 nm embedded flash technology
  - LV: supports 1.2 V core voltage
  - UV: supports same power supply for V_{CC}/ V_{CCO}/ V_{CCx}

    Note!

    GW1N-1 and GW1N-1S devices do not support UV Version.The other devices support both LV and UV versions.
  - Clock dynamically turns on and off
- Multiple I/O Standards

  - LVCMOS33/25/18/15/12; LVTTL33, SSTL33/25/18 I, SSTL33/25/18 II, SSTL15; HSTL18 I, HSTL18 II, HSTL15 I; PCI, LVDS25, RSDS, LVDS25E, BLVDSE

    MLVDSE, LVPECLE, RSDSE
  - Input hysteresis option
  - Supports 4mA,8mA,16mA,24mA,etc. drive options
  - Slew rate option
  - Output drive strength option
  - Individual bus keeper, weak pull-up, weak pull-down, and open drain option
  - Hot socket
  - I/Os in the top layer of GW1N-1S and GW1N-6/9 devices support MIPI input
  - I/Os in the bottom layer of GW1N-6/9 devices support MIPI output
  - I/Os in the Top layer and Bottom layer of GW1N-6/9 devices support I3C OpenDrain/PushPull conversion
- High performance DSP
  - High performance digital signal processing ability
  - Supports 9 x 9,18 x 18,36 x 36 bits multiplier and 54 bits accumulator;
  - Multipliers cascading
  - Registers pipeline and bypass
  - Adaptive filtering through signal feedback
  - Supports barrel shifter
- Abundant slices
  - Four input LUT (LUT4)
  - Double-edge flip-flops
  - Supports shift register and distributed register
- Block SRAM with multiple modes
  - Supports dual port, single port, and semi-dual port
  - Supports bytes write enable
- Flexible PLLs+DLLs
  - Frequency adjustment (multiply and division) and phase adjustment
  - Supports global clock
- Built-in flash programming
  - Instant-on
  - Supports security bit operation
  - Supports AUTO BOOT and DUAL BOOT
- Configuration
  - JTAG configuration

- The GW1N-2B and GW1N-4B devices support JTAG transparent transmission
- Offers up to six GowinCONFIG configuration modes: AUTOBOOT, SSPI, MSPI, CPU, SERIAL, DUAL BOOT

2.2 Product Resources

Table 2-1 Product Resources

Device	GW1N-1	GW1N-2/ GW1N-2B	GW1N-4/ GW1N-4B	GW1N-6	GW1N-9	GW1N-1S
LUT4	1,152	2,304	4,608	6,912	8,640	1,152
Flip-Flop (FF)	864	1,728	3,456	5,184	6,480	864
Shadow SRAM S-SRAM(bits)	0	0	0	13,824	17,280	0
Block SRAM B-SRAM(bits)	72 K	180 K	180 K	468 K	468 K	72K
B-SRAM quantity B-SRAM	4	10	10	26	26	4
User Flash (bits)	96 K	256 K	256 K	608 K	608 K	96K
18 x 18 Multiplier	0	16	16	20	20	0
PLLs+DLLs	1+0	2+2	2+2	2+4	2+4	1+0
Total number of I/O banks	4	4	4	4	4	3
Max. user I/O[1]	119	207	207	273	273	25
Core Voltage (LV)	1.2 V	1.2 V	1.2 V	1.2 V	1.2 V	1.2V
Core Voltage (UV)	–	1.8V/2.5V/3.3V				–

Note!

The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The Max. I/O noted in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O.

2.3 Package Information

Table2-2 Package Information and Max. I/O

Package	Pitch (mm)	Size (mm)	GW1N-1S	GW1N-1	GW1N-2/ GW1N-2B	GW1N-4/ GW1N-4B	GW1N-6	GW1N-9
CS30	0.4	2.3 x 2.4	23	24	-	-	-	-
QN32	0.5	5 x 5	-	26	24（3）	24（3）	-	-
FN32	0.4	4 x 4	25	-	-	-	-	-
QN48	0.4	6 x 6	-	41	40（9）	40（9）	40（12）	40（12）
CM64	0.5	4.1 x 4.1	-				55（16）	55（16）
CS72	0.4	3.6 x 3.3	-	-	57（19）	57（19）	-	-
QN88	0.4	10 x 10	-	-	70（11）	70（11）	70（19）	70（19）
LQ100	0.5	16 x 16	-	79	79（13）	79（13）	79（20）	79（20）
LQ144	0.5	22 x 22	-	116	119（22）	119（22）	120（28）	120（28）
EQ144	0.5	22 x 22	-	-	-	-	120（28）	120（28）
MG160	0.5	8 x 8	-	-	131（25）	131（25）	131（38）	131（38）
UG169	0.8	11 x 11	-	-	-	-	129（38）	129（38）
LQ176	0.4	22 x 22	-	-	-	-	147（37）	147（37）
EQ176	0.4	22 x 22	-	-	-	-	147（37）	147（37）
MG196	0.5	8 x 8	-	-	-	-	113（35）	113（35）
PG256	1.0	17 x 17	-	-	207（32）	207（32）	207（36）	207（36）
PG256M	1.0	17 x 17	-	-	207（32）	207（32）	-	-
UG256	0.8	14 x 14	-	-	-	-	207（36）	207（36）
UG332	0.8	17 x 17	-	-	-	-	273（43）	273（43）

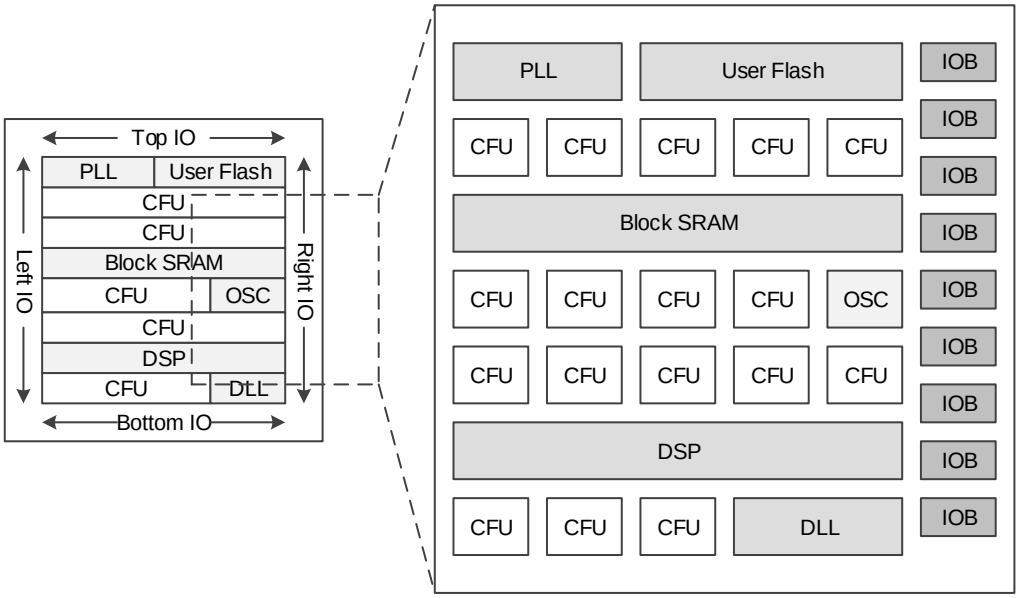
Note!

- The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The Max. I/O noted in this table refers to when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O. See *GW1N series of FPGA Products Package and Pinout* for further details.
- [1] The package types in this data sheet are written with abbreviations. See 5.1Part Name.
- " ⟷ " denotes that the various device pins are compatible when the package types are the same.
- The GW1N-2/GW1N-2B and GW1N-4/GW1N-4B pins are fully compatible. GW1N-6 and GW1N-9 pins are fully compatible.

3 Architecture

3.1 Architecture Overview

Figure 3-1 Architecture Overview of GW1N series of FPGA Products



As shown above, the core of GW1N series of FPGA products is CFU. GW1N series of FPGA products also provide B-SRAMs, PLLs, DLLs, User Flash, and on-chip oscillator, and supports Instant-on. See Table 2-1 for more detailed information.

Note!

GW1N series of FPGA products include the devices of GW1N-1, GW1N-1S, GW1N-2, GW1N-2B, GW1N-4, GW1N-4B, and GW1N-6/9. In these devices, CFU, B-SRAM, GCLK, and on chip crystals are the same, but the other resources, such as DSP, Flash, I/Os, PLL/DLL, high-speed clock, etc, are slightly different.

Configurable Function Unit (CFU) is the base cell for the array of GW1N series FPGA Products. Devices with different capacities have different numbers of rows and columns. CFU can be configured as LUT4 mode, ALU mode, and memory mode. Memory mode is supported in GW1N-6 and GW1N -9. For more detailed information, see 3.2

Configurable Function Unit.

The I/O resources in the GW1N series of FPGA products are arranged around the periphery of the devices in groups referred to as banks[1]. Up to four Banks are supported, including Bank0, Bank1, Bank2, and Bank3. The I/O resources support multiple level standards, and support basic mode, SRD mode, and generic DDR mode. For more detailed information, see 3.3 IOB.

Note!

[1]GW1N-1S includes three Banks, which are Bank0, Bank1, and Bank2 respectively. For further detailed information, please refer to the I/O BANK distribution view in 3.3.1I/O Buffer.

The B-SRAM is embedded as a row in the GW1N series of FPGA products. In the FPGA array, each B-SRAM occupies three columns of CFU. Each B-SRAM has 18,432 bits (18 Kbits) and supports multiple configuration modes and operation modes. For more detailed information, see 3.4 Block SRAM (B-SRAM).

The User Flash is embedded in the GW1N series of FPGA products, without loss of data, even if powered off. For more detailed information, see 3.5 User Flash (GW1N-1 and GW1N-1S) and 3.6 User Flash (GW1N-2/2B/4/4B/6/9).

GW1N-2/GW1N-2B, GW1N-4/GW1N-4B, GW1N-6, and GW1N-9 support DSP. DSP blocks are embedded as row in the FPGA array. Each DSP occupies nine CFU columns. Each DSP block contains two Macros, and each Macro contains two pre-adders, two multipliers with 18 by 18 inputs, and a three input ALU54. For more detailed information, see 3.7 DSP.

Note!

GW1N-1 and GW1N-1S do not support DSP currently.

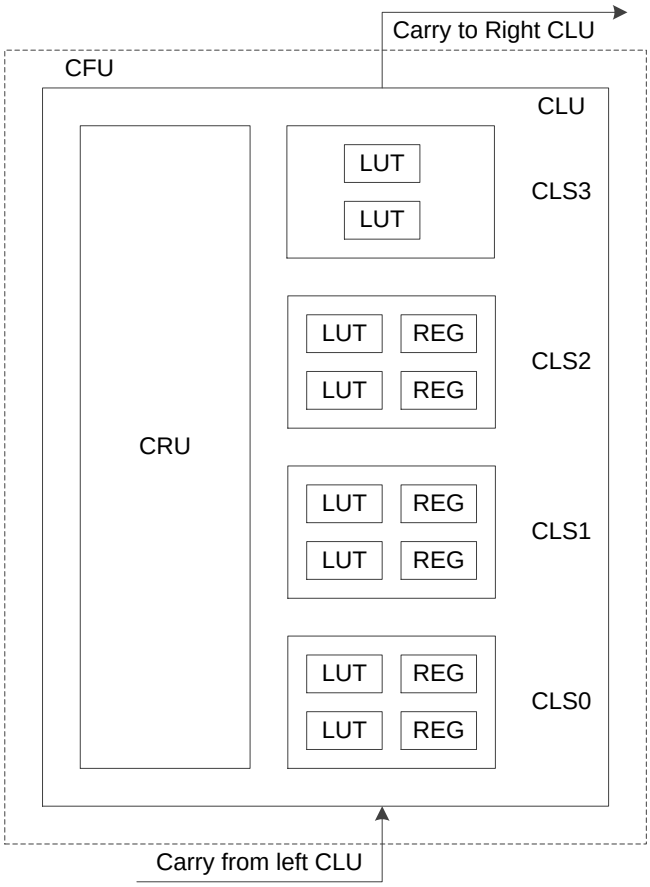
GW1N-1 and GW1N-1S provide one PLL. GW1N-2/GW1N-2B, GW1N-4/GW1N-4B, GW1N-6, and GW1N-9 provide PLLs and DLLs. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted using the configuration of parameters. There is an internal programmable on-chip oscillator in each GW1N series of FPGA product. The on-chip oscillator supports the clock frequencies ranging from 2.5 MHz to 125 MHz, providing the clock resource for the MSPI mode. It also provides a clock resource for user designs with the clock precision reaching ±5%. For more detailed information, see 3.8 Clock, 3.12 On Chip Oscillator.

FPGA provides abundant CRUs, connecting all the resources in the FPGA. For example, routing resources distributed in CFU and IOB connect resources in CFU and IOB. Routing resources can automatically be generated by Gowin software. In addition, the GW1N series of FPGA Products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), and programming options, etc. For more detailed information, see3.8 Clock, 3.9 Long Wire (LW), 3.10 Global Set/Reset (GSR).

3.2 Configurable Function Unit

The configurable function unit (CFU) is the base cell for the array of the GW1N series of FPGA Products. Each CFU consists of a configurable logic unit (CLU) and its routing resource configurable routing unit (CRU). In each CLU, there are four configurable logic slices (CLS). Each CLS contains look-up tables (LUT) and registers, as shown in Figure 3-2 below.

Figure 3-2 CFU View



3.2.1 CLU

The CLU supports three operation modes: basic logic mode, ALU mode, and memory mode.

- Basic Logic Mode

Each LUT can be configured as one four input LUT. A higher input number of LUT can be formed by combining LUT4 together.

  - Each CLS can form one five input LUT5.
  - Two CLSs can form one six input LUT6.
  - Four CLSs can form one seven input LUT7.
  - Eight CLSs (two CLUs) can form one eight input LUT8.

- ALU Mode

When combined with carry chain logic, the LUT can be configured as

the ALU mode to implement the following functions.

- Adder and subtractor
- Up/down counter
- Comparator, including greater-than, less-than, and not-equal-to
- MULT

- Memory mode

GW1N-6 and GW1N-9 support memory mode. In this mode, a 16 x 4 S-SRAM or ROM can be constructed by using CLSs.

This S-SRAM can be initialized during the device configuration stage. The initialization data can be generated in the bit stream file from Gowin Yunyuan software.

Register

Each configurable logic slice (CLS0~CLS2) has two registers (REG), as shown in Figure 3-3 below.

Figure 3-3 Register in CLS

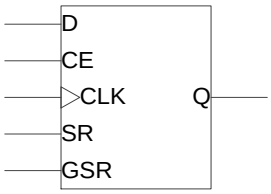


Table3-1 Register Description in CLS

Signal	I/O	Description
D	I	Data input [1]
CE	I	CLK enable, can be high or low effective [2]
CLK	I	Clock, can be rising edge or falling edge trigging [2]
SR	I	Set/Reset, can be configured as [2]: ● Synchronized reset ● Synchronized set ● Asynchronous reset ● Asynchronous set ● Non
GSR[3,4]	I	Global Set/Reset, can be configured as[4]: ● Asynchronous reset ● Asynchronous set ● Non
Q	O	Register

Note!

- [1] The source of the signal D can be the output of a LUT, or the input of the CRU; as such, the register can be used alone when LUTs are in use.

- [2] CE/CLK/SR in CFU is independent.
- [3] In the GW1N series of FPGA products,GSR has its own dedicated network.
- [4] When both SR and GSR are effective, GSR has higher priority.

3.2.2 CRU

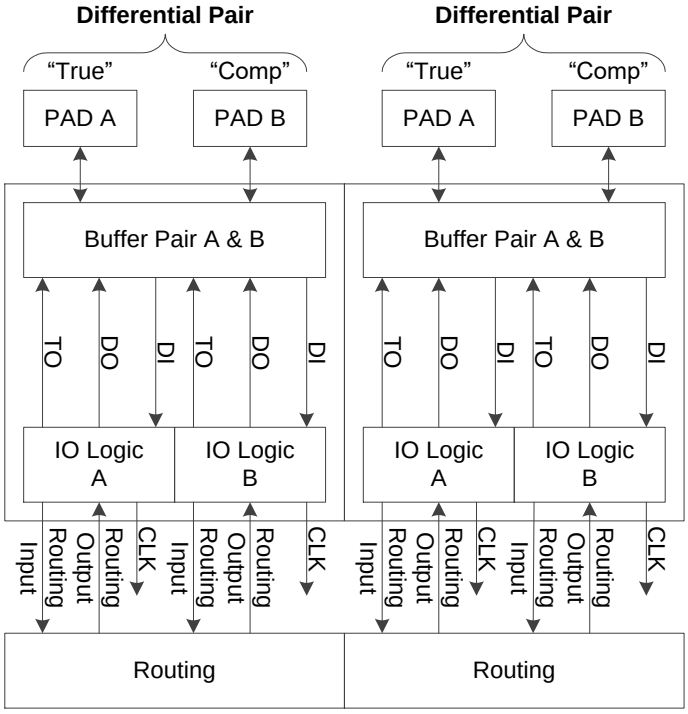
The main functions of the CRU are as follows:

- Input selection: Select input signals for the CFU.
- Configurable routing: Connect the input and output of the CFUs, including inside the CFU, CFU to CFU, and CFU to other functional blocks in FPGA.

3.3 IOB

The IOB in the GW1N series of FPGA products includes I/O buffer, I/O logic, and its routing unit. As shown in Figure 3-4, each IOB connects to two pins (Marked A and B). They can be used as a differential pair or as two single-end input/output.

Figure 3-4 IOB Structure View



IOB Features:

- V_{CCO} supplied with each bank
- LVCMOS, PCI, LVTTL, LVDS, SSTL, and HSTL (true LVDS not supported in GW1N-1 and GW1N-1S)
- Input hysteresis option
- Output drive strength option
- Slew rate option
- Individual bus keeper, weak pull-up, weak pull-down, and open drain option

- Hot socket
- IO logic supports basic mode, SRD mode, and generic DDR mode
- I/Os in the top layer of GW1N-1S and GW1N-6/9 devices support MIPI input
- I/Os in the bottom layer of GW1N-6/9 devices support MIPI output
- I/Os in the Top layer and Bottom layer of GW1N-6/9 devices support I3C OpenDrain/PushPull conversion

3.3.1 I/O Buffer

There are four IO Banks in the GW1N series of FPGA products, as shown in Figure 3-5. Each Bank supports single power supply and has independent I/O power supply V_{CCO}. GW1N-1S includes three IO Banks, as shown in Figure 3-6. Each Bank supports single power supply and has independent I/O power supply V_{CCO}.To support SSTL, HSTL, etc., each bank also provides one independent voltage source (V_{REF}) as referenced voltage. The user can choose from the internal reference voltage of the bank (0.5 x V_{CCO}) or the external reference voltage using any IO from the bank.

Figure 3-5 I/O Bank Distribution View of GW1N-1/2/4/2B/4B

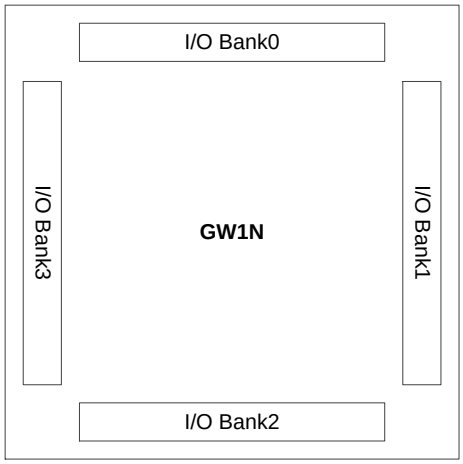


Figure 3-6 I/O Bank Distribution View of GW1N-6/9

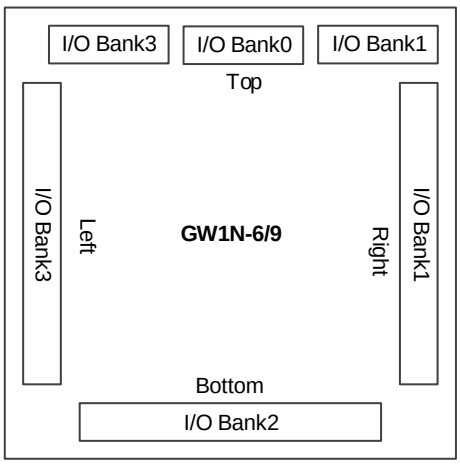
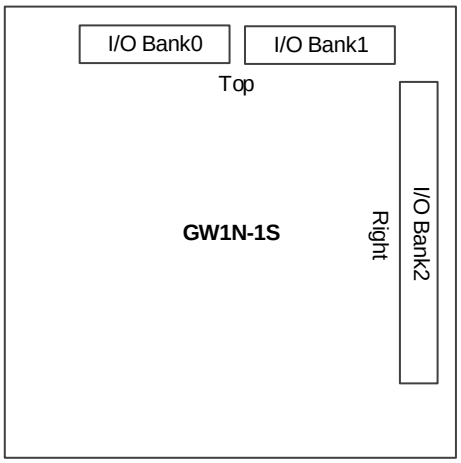


Figure 3-7 I/O Bank Distribution View of GW1N-1S



The GW1N series of FPGA products support LV and UV.

LV devices support 1.2 V V_{CC} to meet users' low power needs.

V_{CCO} can be set as 1.2 V, 1.5 V, 1.8 V, 2.5 V, or 3.3 V according to requirements[1].

V_{CCX} supports 2.5 V or 3.3 V power supply.

UV devices support 1.8V, 2.5 V, and 3.3 V, and linear voltage regulator is integrated to facilitate single power supply.

For the devices of GW1N-1S, GW1N-6, and GW1N-9, I/Os of the top layer support MIPI input. For the devices of GW1N-6 and GW1N-9, I/Os of the bottom layer support MIPI output. I/Os of the top and bottom layer in GW1N-6/9 support MIPI I3C OpenDrain/PushPull conversion.

Note!

- By default, the systemIO is weak pull-up for blank chips;
- For the recommended operating conditions of different devices, please refer to 4.1Operating Conditions;
- When the I/O in Top layer of GW1N-6/9 is used as MIPI input, the V_{CCOx} of the used I/O needs to be supplied with 1.2V power supply, where x can be 0, 1, and 3.
- When the I/O in Bottom layer of GW1N-6/9 is used as MIPI output, VCCO2 needs to be supplied with 1.2V power supply.
- The I/O power supply restrictions of BANK0, BANK1, BANK3 in GW1N-6/9 are as follows:
  - When V_{CCO0} is greater than or equal to 1.8V 时，V_{CCO1} and V_{CCO3} support 1.2V, 1.5V, 1.8V, 2.5V, and 3.3V.
  - When V_{CCO0} is 1.5V 时，V_{CCO1} and V_{CCO3} support 1.2V, 1.5V, 1.8V, and 2.5V.

For the V_{CCO} requirements of different I/O standards, see Table 3-2.

Table 3-2 Output I/O Standards and Configuration Options

I/O output standard	Single/Differ	Bank V_{CCO} (V)	Driver Strength (mA)
LVTTL33	Single end	3.3	4,8,12,16,24
LVCMOS33	Single end	3.3	4,8,12,16,24

I/O output standard	Single/Differ	Bank V_{CCO} (V)	Driver Strength (mA)
LVCMOS25	Single end	2.5	4,8,12,16
LVCMOS18	Single end	1.8	4,8,12
LVCMOS15	Single end	1.5	4,8
LVCMOS12	Single end	1.2	4,8
SSTL25_I	Single end	2.5	8
SSTL25_II	Single end	2.5	8
SSTL33_I	Single end	3.3	8
SSTL33_II	Single end	3.3	8
SSTL18_I	Single end	1.8	8
SSTL18_II	Single end	1.8	8
SSTL15	Single end	1.5	8
HSTL18_I	Single end	1.8	8
HSTL18_II	Single end	1.8	8
HSTL15_I	Single end	1.5	8
PCI33	Single end	3.3	N/A
LVPECL33E	Differential	3.3	16
MVLDS25E	Differential	2.5	16
BLVDS25E	Differential	2.5	16
RSDS25E	Differential	2.5	8
LVDS25E	Differential	2.5	8
LVDS25	Differential	2.5/3.3	3.5/2.5/2/1.25
RSDS	Differential	2.5/3.3	2
MINILVDS	Differential	2.5/3.3	2
PPLVDS	Differential	2.5/3.3	3.5
SSTL15D	Differential	1.5	8
SSTL25D_I	Differential	2.5	8
SSTL25D_II	Differential	2.5	8
SSTL33D_I	Differential	3.3	8
SSTL33D_II	Differential	3.3	8
SSTL18D_I	Differential	1.8	8
SSTL18D_II	Differential	1.8	8
HSTL18D_I	Differential	1.8	8

I/O output standard	Single/Differ	Bank V_{CCO} (V)	Driver Strength (mA)
HSTL18D_II	Differential	1.8	8
HSTL15D_I	Differential	1.5	8

Table 3-3 Input Standards and Configuration Options

I/O Input Standard	Single/Differ	Bank V_{CCO} (V)	Hysteresis	Need V_{REF}
LVTTL33	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS33	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS25	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS18	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS15	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS12	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
SSTL15	Single end	1.5/1.8/2.5/3.3	No	Yes
SSTL25_I	Single end	2.5/3.3	No	Yes
SSTL25_II	Single end	2.5/3.3	No	Yes
SSTL33_I	Single end	3.3	No	Yes
SSTL33_II	Single end	3.3	No	Yes
SSTL18_I	Single end	1.8/2.5/3.3	No	Yes
SSTL18_II	Single end	1.8/2.5/3.3	No	Yes
HSTL18_I	Single end	1.8/2.5/3.3	No	Yes
HSTL18_II	Single end	1.8/2.5/3.3	No	Yes
HSTL15_I	Single end	1.5/1.8/2.5/3.3	No	Yes
PCI33	Single end	3.3	Yes	No
LVDS	Differential	2.5/3.3	No	No
RSDS	Differential	2.5/3.3	No	No
MINILVDS	Differential	2.5/3.3	No	No
PPLVDS	Differential	2.5/3.3	No	No
LVDS25E	Differential	2.5/3.3	No	No
MLVDS25E	Differential	2.5/3.3	No	No
BLVDS25E	Differential	2.5/3.3	No	No
RSDS25E	Differential	2.5/3.3	No	No
LVPECL33	Differential	3.3	No	No
SSTL15D	Differential	1.5/1.8/2.5/3.3	No	No

I/O Input Standard	Single/Differ	Bank V_{CCO} (V)	Hysteresis	Need V_{REF}
SSTL25D_I	Differential	2.5/3.3	No	No
SSTL25D_II	Differential	2.5/3.3	No	No
SSTL33D_I	Differential	3.3	No	No
SSTL33D_II	Differential	3.3	No	No
SSTL18D_I	Differential	1.8/2.5/3.3	No	No
SSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL18D_I	Differential	1.8/2.5/3.3	No	No
HSTL18D_II	Differential	1.8/2.5/3.3	No	No
HSTL15D_I	Differential	1.5/1.8/2.5/3.3	No	No

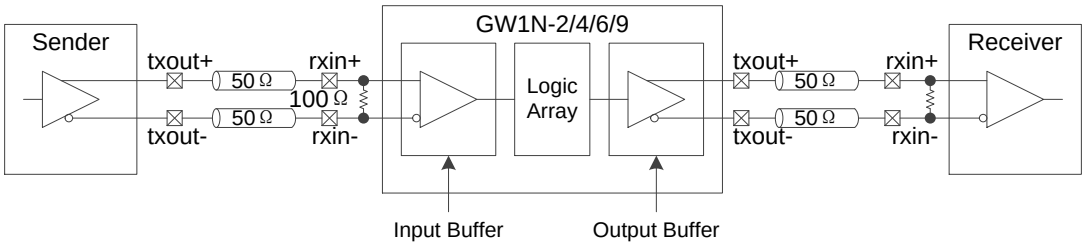
3.3.2 True LVDS Design

BANK1/2/3 in the GW1N-2/2B/4/4B/6/9 devices support true LVDS output, but BANK1/2/3 do not support internal 100Ω input differential matched resistance. Bank0 supports internal 100Ω input differential matched resistance. BANK0/1/2/3 support LVDS25E, MLVDS25E, BLVDS25E,etc. For more detailed information about different levels, please refer to *Gowin systemIO User Guide*.

For more detailed information about true LVDS, please refer to *GW1N series of FPGA products Pinout*.

True LVDS input I/O needs external 100Ω terminal resistance for matching. SeeFigure 3-8for the true LVDS design.

Figure 3-8 True LVDS Design



For more detailed information about LVDS25E, MLVDS25E, and BLVDS25E on IO terminal matched resistance, please refer to *Gowin SystemIO User Guide*.

3.3.3 I/O Logic

Figure 3-9 shows the I/O logic output of the GW1N series of FPGA products.

Figure 3-9 I/O Logic Output

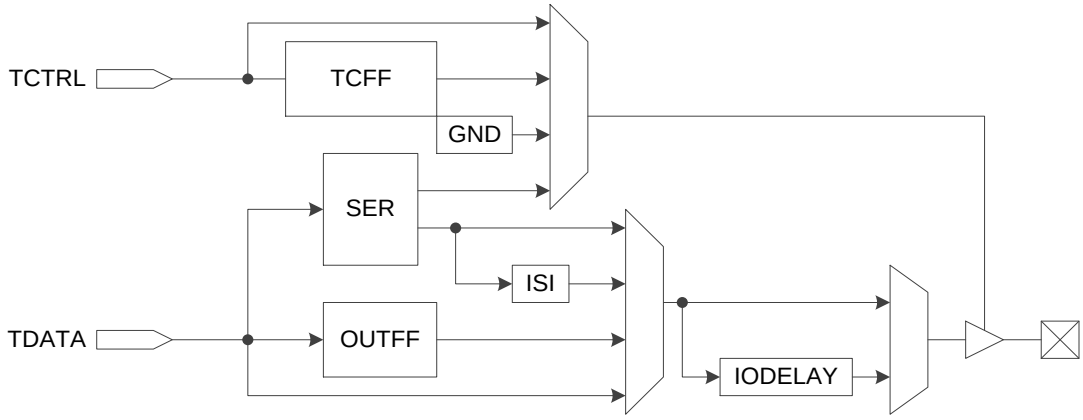
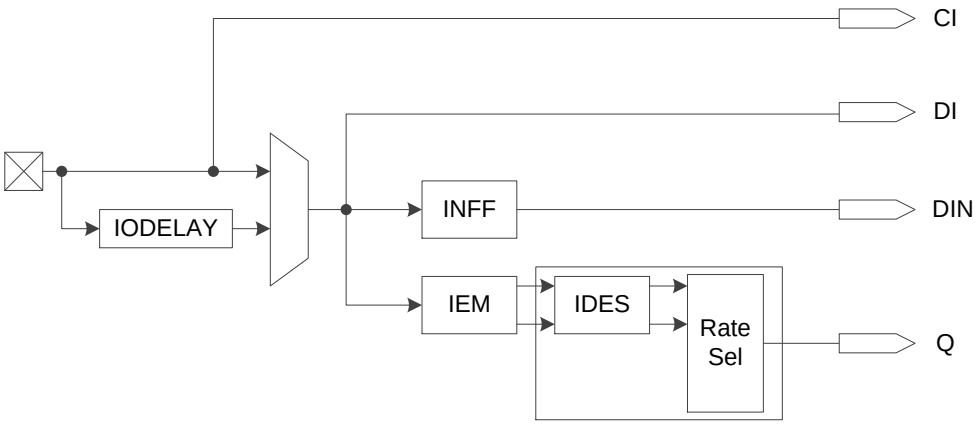


Figure 3-10 shows the I/O logic input of the GW1N series of FPGA products.

Figure 3-10 I/O Logic Input

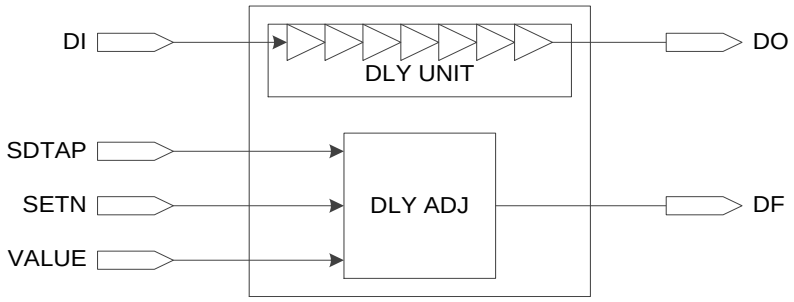


A description of the I/O logic modules of the GW1N series FPGA products is presented below.

IODELAY

See Figure 3-11 for an overview of the IODELAY. Each I/O of the GW1N series of FPGA products has an IODELAY cell. The longest delay it can provide is about 128 steps x 30ps = 3840ps.

Figure 3-11 IODELAY



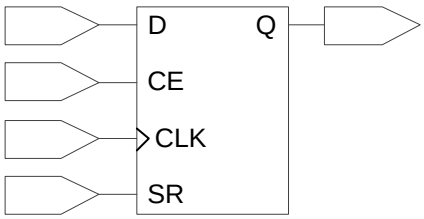
There are two ways to control the delay cell:

- Static control:
- Dynamic control: Usually used to sample delay window together with IEM. The IODELAY cannot be used for both input and output at the same time

I/O Register

See Figure 3-12 for I/O register in the GW1N series of FPGA products. Each I/O provides one input register, INFF, one output register, OUTFF, and a tristate Register, TCFF.

Figure 3-12 Register Structure in I/O Logic



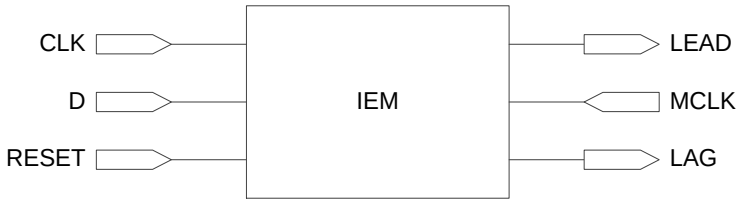
Note!

- CE can be either active low (0: enable)or active high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The register can be programmed as register or latch.

IEM

IEM is for sampling clock edge and is used in the generic DDR mode. See Figure 3-13 for the IEM structure.

Figure 3-13 IEM Structure



De-serializer DES

The GW1N series of FPGA products provide a simple Serializer SER for each output I/O to support advanced I/O protocols.

Serializer SER

The GW1N series of FPGA products provide a simple Serializer SER for each output I/O to support advanced I/O protocols.

3.3.4 I/O Logic Modes

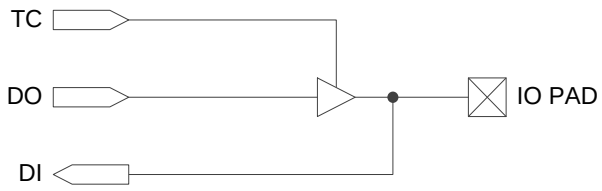
The I/O Logic in the GW1N series of FPGA products supports several operations. In each operation, the I/O (or I/O differential pair) can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

GW1N-1S, GW1N-6, and GW1N-9 pins support IO logic. The GW1N-1 pins IOL6 (A,B,C….J) and IOR6 (A,B,C….J) do not support IO logic. The other pins support IO logic. The GW1N-2/GW1N-2B and GW1N-4/GW1N-4B pins IOL10(A,B,C….J) and IOR10(A,B,C….J) do not support IO logic. The other pins support IO logic.

Basic Mode

In basic mode, the I/O Logic is as shown in Figure 3-14, and the TC, DO, and DI signals can connect to the internal cores directly through CRU.

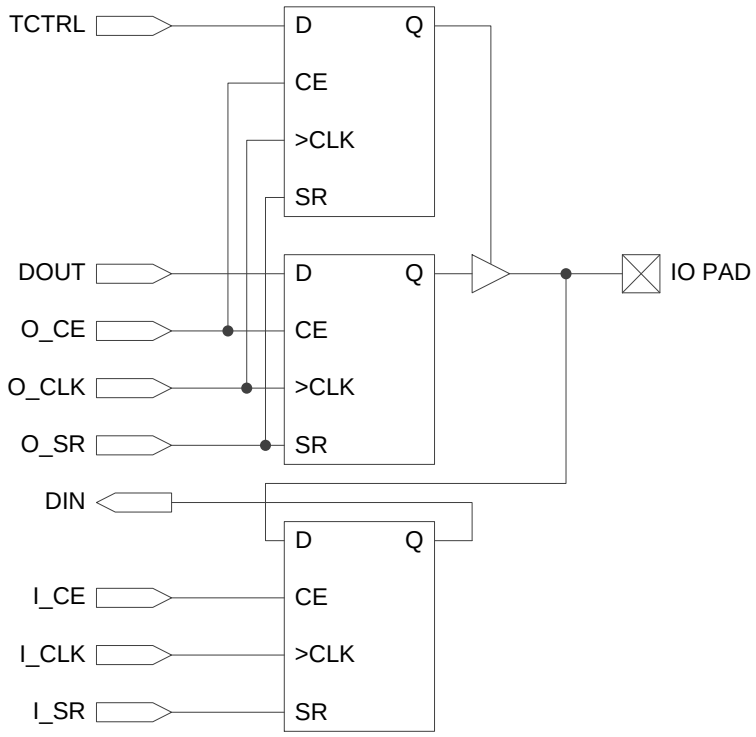
Figure 3-14 I/O Logic in Basic Mode



SDR Mode

In comparison with the basic mode, SDR utilizes the IO register, as shown in Figure 3-15. This can effectively improve IO timing.

Figure 3-15 I/O Logic in SDR Mode



Note!

- CLK enable O_CE and I_CE can be configured as active high or active low;
- O_CLK and I_CLK can be either rising edge trigger or falling edge trigger;
- Local set/reset signal O_SR and I_SR can be either synchronized reset, synchronized set, asynchronous reset, asynchronous set, or no-function;
- I/O in SDR mode can be configured as basic register or latch.

Generic DDR Mode

Higher speed IO protocols can be supported in generic DDR mode.

GW1N-1S, GW1N-6, and GW1N-9 devices support IDES16 mode and OSER16 mode. The other devices do not support.

Figure 3-16 shows the generic DDR input, with a speed ratio of the internal logic to PAD 1:2.

Figure 3-16 I/O Logic in DDR Input Mode

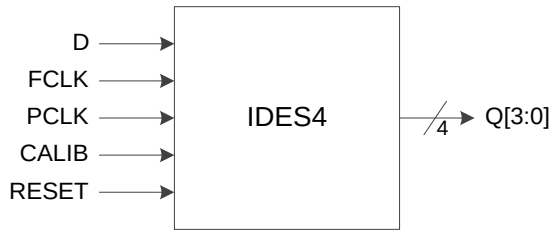
Figure 3-17 shows generic DDR output, with a speed ratio of PAD to FPGA internal logic 2:1.

Figure 3-17 I/O Logic in DDR Output Mode

IDES4

In IDES4 mode, the speed ratio of the PAD to FPGA internal logic is 1:4.

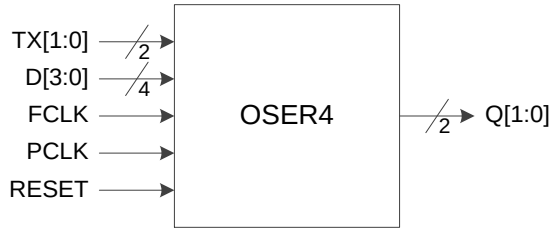
Figure 3-18 I/O Logic in IDES10 Mode



OSER4 Mode

In OSER4 mode, the speed ratio of the PAD to FPGA internal logic is 4:1.

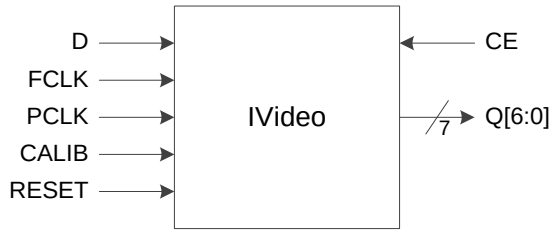
Figure 3-19 I/O Logic in OSER4 Mode



IVideo Mode

In IVideo mode, the speed ratio of the PAD to FPGA internal logic is 1:7.

Figure 3-20 I/O Logic in IVideo Mode



Note!

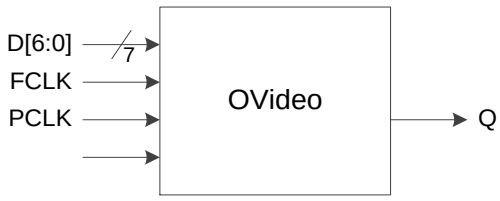
IVideo and IDES8/10 will occupy the neighboring I/O logic. If the I/O logic of a single port is occupied, the pin can only be programmed in SDR or BASIC mode.

OVideo Mode

In OVideo mode, the speed ratio of the PAD to FPGA internal logic is

7:1.

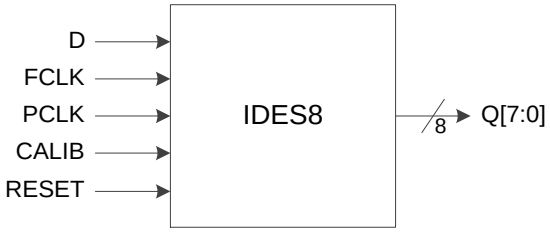
Figure 3-21 I/O Logic in OVideo Mode



IDES8 Mode

In IDES8 mode, the speed ratio of the PAD to FPGA internal logic is 1:8.

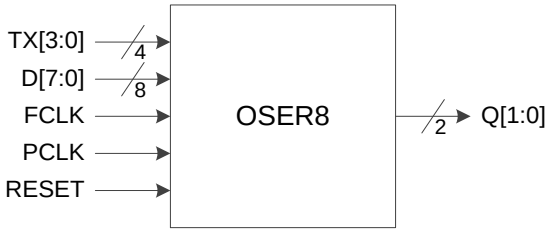
Figure 3-22 I/O Logic in IDES8 Mode



OSER8 Mode

In OSER8 mode, the speed ratio of the PAD to FPGA internal logic is 8:1.

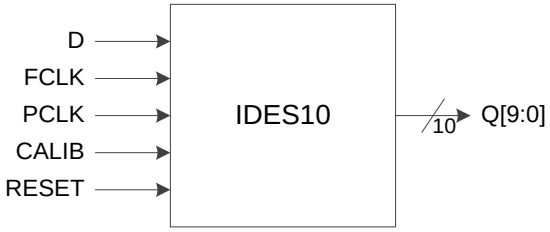
Figure 3-23 I/O Logic in OSER8 Mode



IDES10 Mode

In IDES10 mode, the speed ratio of the PAD to FPGA internal logic is 1:10.

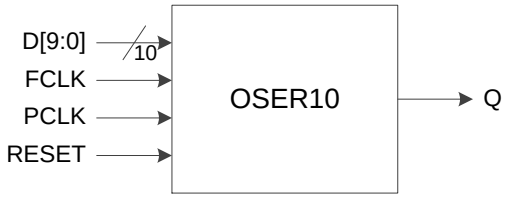
Figure 3-24 I/O Logic in IDES10 Mode



OSER10 Mode

In OSER10 mode, the speed ratio of the PAD to FPGA internal logic is 10:1.

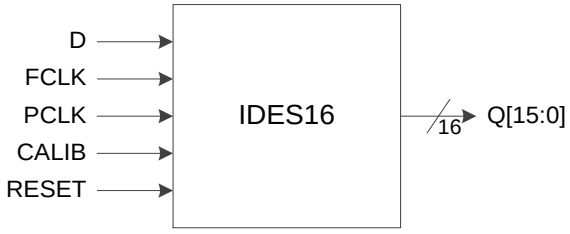
Figure 3-25 I/O Logic in OSER10 Mode



IDES16 Mode

Only GW1N-1S, GW1N-6, and GW1N-9 devices support this mode. In IDES16 mode, the speed ratio of the PAD to FPGA internal logic is 1:16.

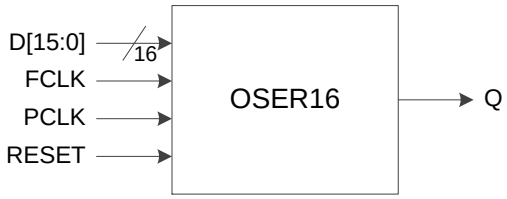
Figure 3-26 I/O Logic in IDES16 Mode



OSER16 Mode

Only GW1N-1S, GW1N-6, and GW1N-9 devices support this mode. In OSER16 mode, the speed ratio of the PAD to FPGA internal logic is 16:1.

Figure 3-27 I/O Logic in OSER16 Mode



3.4 Block SRAM (B-SRAM)

3.4.1 Introduction

The GW1N series of FPGA products provide abundant B-SRAMs. The Block SRAM (B-SRAM) is embedded as a row in the FPGA array and is different from S-SRAM (Shadow SRAM). Each B-SRAM occupies three columns of CFU in the FPGA array. Each B-SRAM has 18,432 bits (18Kbits). There are five operation modes: Single Port, Dual Port, Semi Dual Port, ROM, and FIFO. The signals and functional descriptions of B-SRAM are listed in Table 3-4.

An abundance of B-SRAM resources provide a guarantee for the user's high-performance design. B-SRAM features include the following:

- Max.18,432 bits per B-SRAM
- B-SRAM itself can run at 190 MHz at max
- Single Port
- Dual Port
- Semi Dual Port
- Parity bits
- ROM
- Data width from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Enable Byte operation for double byte or above
- Asynchronous reset, Synchronous reset
- Normal Read and Write Mode
- Read-before-write Mode
- Write-through Mode

Table 3-4 B-SRAM Signals

Port Name	I/O	Description
DIA	I	Port A data input
DIB	I	Port B data input
ADA	I	Port A address
ADB	I	Port B address
CEA	I	Clock enable, Port A
CEB	I	Clock enable, Port B
RESETA	I	Register reset, Port A
RESETB	I	Register reset, Port B
WREA	I	Read/write enable, Port A

Port Name	I/O	Description
WREB	I	Read/write enable, Port B
BLKSEL	I	Block select
CLKA	I	Read/write cycle clock for Port A input registers
CLKB	I	Read/write cycle clock for Port B input registers
OCEA	I	Clock enable for Port A output registers
OCEB	I	Clock enable for Port B output registers
DOA	O	Port A data output
DOB	O	Port B data output

3.4.2 Configuration Mode

The B-SRAM mode in the GW1N series of FPGA products supports different data bus widths. See Table 3-5.

Table 3-5 Memory Size Configuration

Single Port Mode	Dual Port Mode	Semi-Dual Port Mode	Read Only
16 K x 1	16 K x 1	16 K x 1	16K x 1
8K x 2	8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32	512 x 32
2K x 9	2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36	512 x 36

3.4.3 Mixed Data Bus Width Configuration

The B-SRAM in the GW1N series of FPGA products supports mixed data bus width operation. In the dual port and semi-dual port modes, the data bus width for read and write can be different. For the configuration options that are available, please see Table 3-6 and Table 3-7 below.

Table 3-6 Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	*	*	*	*	*		
8K x 2	*	*	*	*	*		
4K x 4	*	*	*	*	*		
2K x 8	*	*	*	*	*		
1K x 16	*	*	*	*	*		
2K x 9						*	*
1K x 18						*	*

Note!

"*"denotes the modes supported.

Table 3-7Semi Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512 x 32	2K x 9	1K x 18	512 x 36
16K x 1	*	*	*	*	*	*			
8K x 2	*	*	*	*	*	*			
4K x 4	*	*	*	*	*	*			
2K x 8	*	*	*	*	*	*			
1K x 16	*	*	*	*	*	*			
512 x 32	*	*	*	*	*	*			
2K x 9							*	*	*
1K x 18							*	*	*

Note!

"*"denotes the modes supported.

3.4.4 Byte-enable

The B-SRAM in the GW1N series of FPGA products supports byte-enable. For data longer than a byte, the additional bits can be blocked, and only the selected portion can be written into. The blocked bits will be retained for future operation. Read/write enable ports (WREA, WREB), and byte-enable parameter options can be used to control the B-SRAM write

operation.

3.4.5 Parity Bit

There are parity bits in B-SRAM. The 9th bit in each byte can be used as a parity bit or for data storage. However, the parity operation is not yet supported.

3.4.6 Synchronous Operation

- All the input registers of B-SRAM support synchronous write;
- The output registers can be used as pipeline register to improve design performance;
- The output registers are bypass-able.

3.4.7 Power up Conditions

B-SRAM initialization is supported when powering up. During the power-up process, B-SRAM is in standby mode, and all the data outputs are “0”. This also applies in ROM mode.

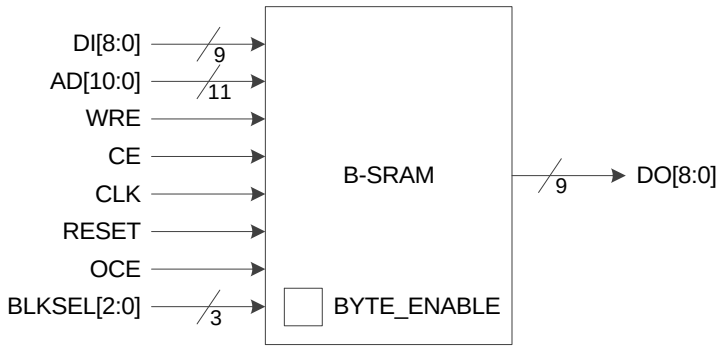
3.4.8 Operation Modes

The input registers of B-SRAM can be used for synchronous write. The output registers can be used as pipeline register to improve design performance. In the dual port mode, the two ports of B-SRAM can be operated totally independently. Port A and Port B have their own clock and are write-enabled; as such, both ports can be written to and read independently from each other.

Single Port Mode

In the single port mode, as shown below, B-SRAM can write to or read from one port at one clock edge. During the write operation, the data can show up at the output of B-SRAM. Normal write mode (Normal-write Mode) and write-through mode can be supported. When the output register is bypassed, the new data will show at the same write clock rising edge. For the single port 2 K x 9bit block memory, see Figure 3-28 below.

Figure 3-28 Single Port Block Memory



The table below shows all the configuration options that are available in the single port mode:

Table 3-8 Single Port Block Memory Configuration

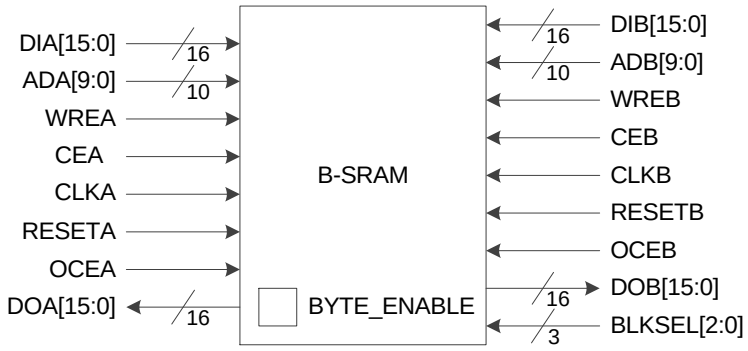
Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Data Depth
SP	B-SRAM_16K_S1	16 K	16 K x 1	16,384	1
	B-SRAM_8K_S2	16K	8K x 2	8,192	2
	B-SRAM_4K_S4	16K	4K x 4	4,096	4
	B-SRAM_2K_S8	16K	2K x 8	2,048	8
	B-SRAM_1K_S16	16K	1K x 16	1,024	16
	B-SRAM_512_S32	16K	512 x 32	512	32
SPX9	B-SRAM_2K_S9	18K	2K x 9	2,048	9
	B-SRAM_1K_S18	18K	1K x 18	1,024	18
	B-SRAM_512_S36	18K	512 x 36	512	36

Dual Port Mode

B-SRAM support Dual Port mode, as shown in Figure 3-29. The applicable operations are as follows:

- Two independent read
- Two independent write
- An independent read and an independent write at different clock frequencies

Figure 3-29 Dual Port Block Memory



All the configuration options for the dual port mode are as shown in Table 3-9 .

Table 3-9 Semi Dual Port Memory Configuration

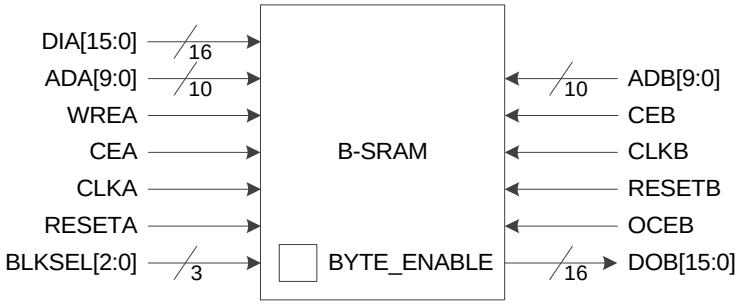
Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Data Depth
DP	B-SRAM_16K_D1	16K	16K x 1	16384	1
	B-SRAM_8K_D2	16K	8K x 2	8192	2

Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Data Depth
	B-SRAM_4K_D4	16K	4K x 4	4096	4
	B-SRAM_2K_D8	16K	2K x 8	2048	8
	B-SRAM_1K_D16	16K	1K x 16	1024	16
DPX9	B-SRAM_2K_D9	18K	2K x 9	2048	9
	B-SRAM_1K_D18	18K	1K x 18	1024	18

Semi-Dual Port Mode

The figure below shows the semi Dual Port 1K x 16bit mode. It supports read and write at the same time on different ports. It is not possible to write and read to the same port at the same time. The system only supports write on Port A , read on Port B.

Figure 3-30 Semi Dual Port Block Memory 1



All the configuration options for the dual port mode are as shown in Table 3-10.

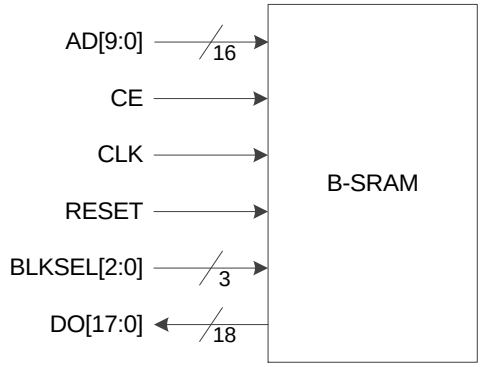
Table 3-10Semi Dual Port Memory Configuration

Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Data Depth
SDP	B-SRAM_16K_SD1	16K	16K x 1	16,384	1
	B-SRAM_8K_SD2	16K	8K x 2	8,192	2
	B-SRAM_4K_SD4	16K	4K x 4	4,096	4
	B-SRAM_2K_SD8	16K	2K x 8	2,048	8
	B-SRAM_1K_SD16	16K	1K x 16	1,024	16
	B-SRAM_512_SD32	16K	512 x 32	512	32
SDPX9	B-SRAM_2K_SD9	18K	2K x 9	2,048	9
	B-SRAM_1K_SD18	18K	1K x 18	1,024	18
	B-SRAM_512_SD36	18K	512 x 36	512	36

Read Only

B-SRAM can be configured as ROM, as shown in Figure 3-31. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization completes during the device power-on process.

Figure 3-31 ROM Block Memory



Each B-SRAM can be configured as one 16 Kbits ROM. Table 3-11 lists all the configuration options for the ROM mode.

Table 3-11 Block ROM Configuration

Primitive	Configuration	RAM (Bit)	Port Mode	Memory Depth	Data Depth
ROM	B-SRAM_16K_O1	16K	16K x 1	16,384	1
	B-SRAM_8K_O2	16K	8K x 2	8,192	2
	B-SRAM_4K_O4	16K	4K x 4	4,096	4
	B-SRAM_2K_O8	16K	2K x 8	2,048	8
	B-SRAM_1K_O16	16K	1K x 16	1,024	16
	B-SRAM_512_O32	16K	512 x 32	512	32
ROMX9	B-SRAM_2K_O9	18K	2K x 9	2,048	9
	B-SRAM_1K_O18	18K	1K x 18	1,024	18
	B-SRAM_512_O36	18K	512 x 36	512	36

Note!

In the ROM mode, the RESET signal can only reset the input and output registers. It cannot clear the ROM content.

3.4.9 B-SRAM Operation Modes

B-SRAM supports five different operations, including two read operations (Bypass Mode and Pipeline Read Mode) and three write operations (Normal Write Mode, Write-through Mode, and Read-before-write Mode).

Read Mode

Read data from the B-SRAM via output registers or without using the registers.

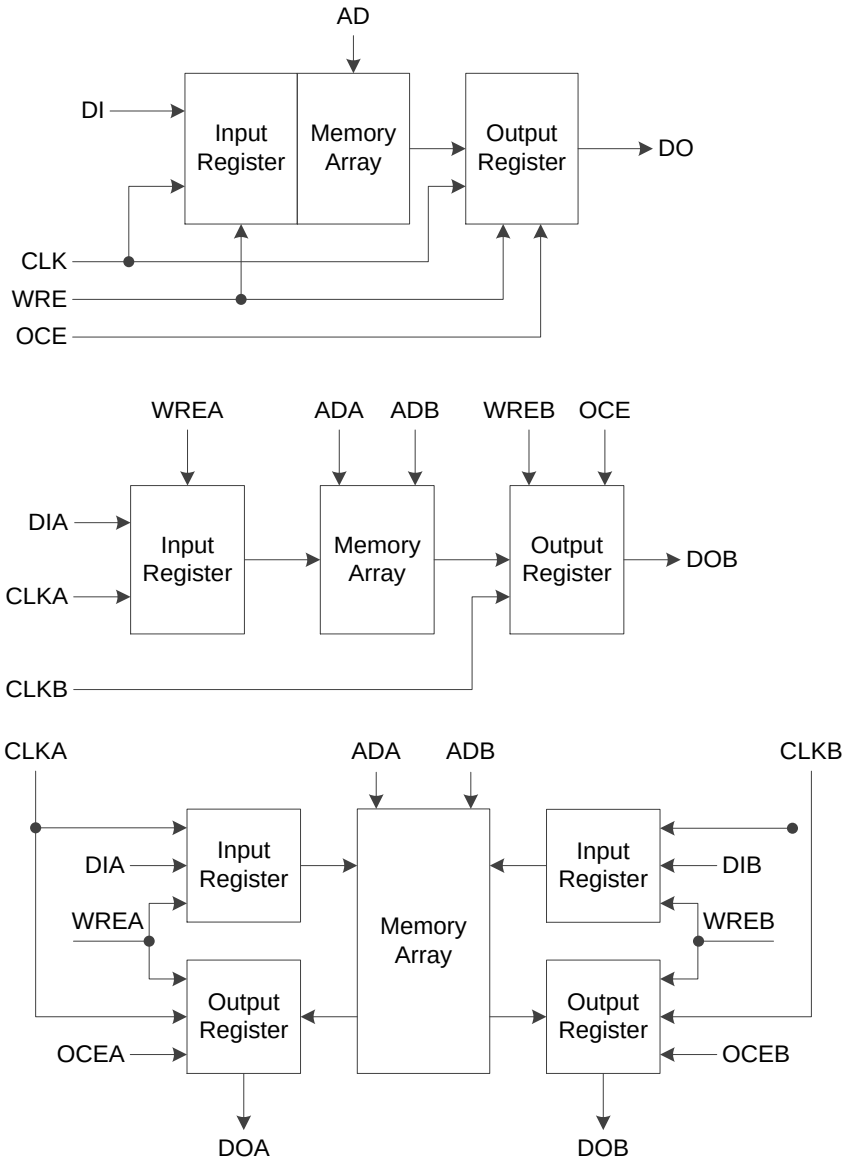
Pipeline Mode

While writing in the B-SRAM, the output register and pipeline register are also being written. The data bus can be up to 36 bits in this mode.

Bypass Mode

The output register is not used. The data is kept in the output of memory array.

Figure 3-32 Pipeline Mode in Single Port, Dual Port and Semi Dual Port



Write Mode

NORMAL WRITE MODE

In this mode, when the user writes data to one port, and the output data of this port does not change. The data written in will not appear at the read port.

WRITE-THROUGH MODE

In this mode, when the user writes data to one port, and the data written in will also appear at the output of this port.

READ-BEFORE-WRITE MODE

In this mode, when the user writes data to one port, and the data written in will be stored in the memory according to the address. The original data in this address will appear at the output of this port.

3.4.10 Clock Operations

Table 3-12 lists the clock operations in different B-SRAM modes:

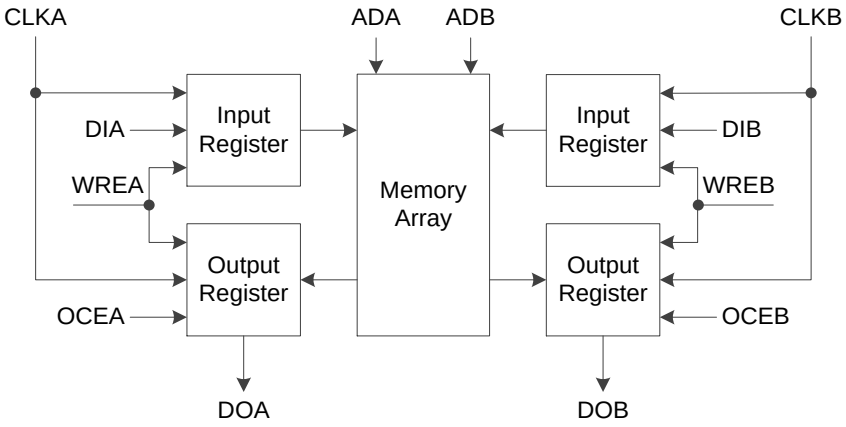
Table 3-12 Clock Operations in Different B-SRAM Modes

Clock Operations	Dual Port Mode	Semi-Dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes

Independent Clock Mode

Figure 3-33 shows the independent clocks in the dual port mode with each port with one clock. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

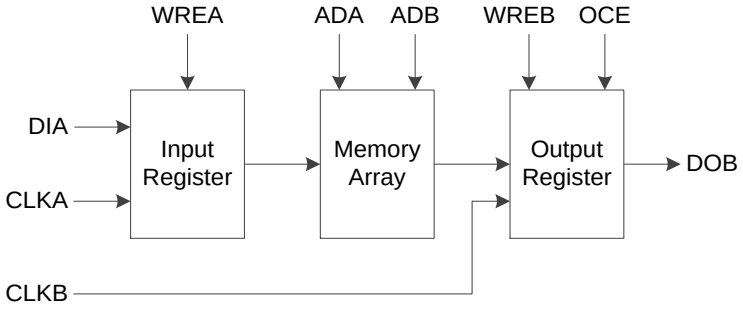
Figure 3-33 Independent Clock Mode



Read/Write Clock Operation

Figure 3-34 shows the read/write clock operations in the semi-dual port mode with one clock at each port. The write clock (CLKA) controls Port A data inputs, write address and read/write enable signals. The read clock (CLKB) controls Port B data output, read address, and read enable signals.

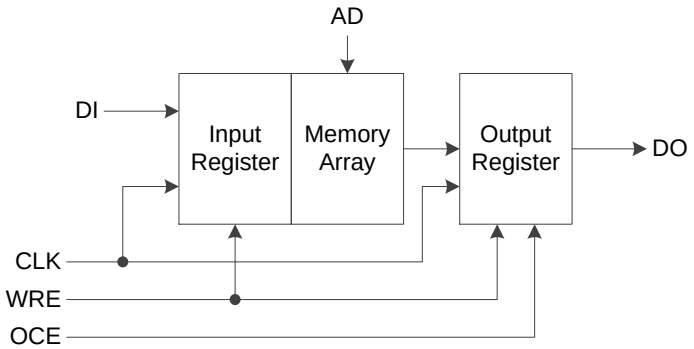
Figure 3-34 Read/Write Clock Mode



Single Port Clock Mode

Figure 3-35shows the clock operation in single port mode.

Figure 3-35 Single Port Clock Mode



3.5 User Flash (GW1N-1 and GW1N-1S)

3.5.1 Introduction

GW1N-1 and GW1N-1S devices support User Flash with 12 Kbytes (48 page x 256 Bytes). The features are as following:

- 100,000 write cycles
- Greater than10 years Data Retention at +85 ℃
- Selectable 8/16/32 bits data-in and data-out
- Page size: 256 Bytes
- 3 μA standby current
- Page Write Time: 8.2 ms

3.5.2 Port Signal

See Figure 3-36 for GW1N-1 and GW1N-1S user flash:

Figure 3-36 GW1N-1/GW1N-1S User Flash Ports

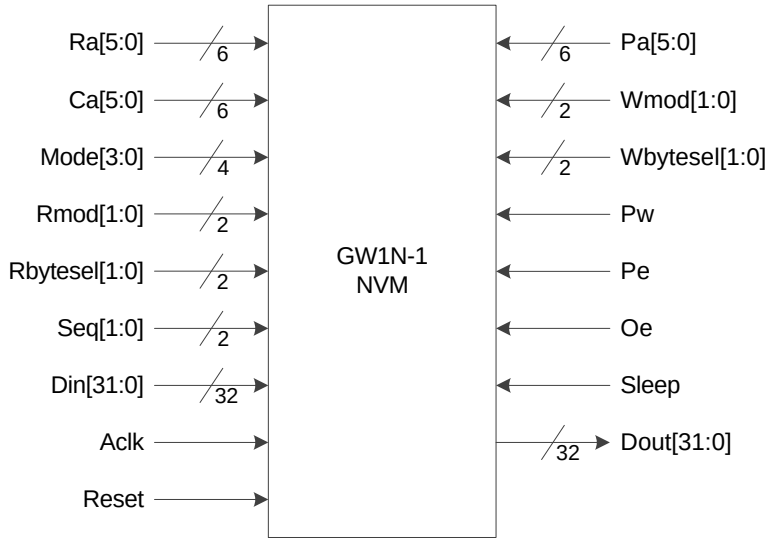


Table 3-13 Flash Module Signal Description

Pin name1	I/O	Description
Ra[5:0]	I	X address bus, used to select one row within memory block.
Ca[5:0]	I	Y address bus, used to select one column within memory block.
Pa[5:0][2]	I	I
Mode[3:0]	I	Select operation mode.
Seq[1:0]	I	Control operation sequence.
Aclk	I	Synchronize clock for read-write operations.
Rmod[1:0]	I	Read data bit width selection.
Wmod[1:0]	I	Write data bit width selection.
Rbytesel[1:0]	I	Read data byte selection.
Wbytesel[1:0]	I	Write data bit width selection.
Pw	I	Write Page latch clock.
Reset[3]	I	Reset signal, active-high.
Pe	I	Charge pump enabled.
Oe	I	Data output enable.
Sleep[4]	I	Sleep mode, active-high.
Din[31:0]	I	Data input bus.
Dout[31:0]	O	Data output bus.

Note!

- [1] Port names of Control, address,and data signals.
- [2] Pa signal has the same function as Ca signal, except that Pa signal is used for programming operation of page latch data, and Ca signal is used for other operations related to column selection in Flash.
- [3] The high-level effective time of reset signal is not less than 20ns. Wait for 6μs after that the reset signal changes to low-level, and then move on.

- [4] Save power through flash memory resources entering into sleep mode. Wait for 6μs after that the sleep signal changes to low-level, and then move on.

3.5.3 Data Output Bit Selection

Change data I/O bit width by Rmod/Wmod and Rbytesel/ Wbytesel. The correspondence between data bit width and control signal is shown in Table 3-14 and Table 3-15.

Table 3-14 Data Output Bit Selection

Rmod[1:0]	Rbytesel		Dout			
	[1]	[0]	[31:24]	[23:16]	[15:8]	[7:0]
0.0	√	√	×	×	×	√
0.1	√	×	×	×	√	√
1X	×	×	√	√	√	√

Table 3-15s Data Input Bit Selection

Wmod[1:0]	Wbytesel		Din			
	[1]	[0]	[31:24]	[23:16]	[15:8]	[7:0]
0.0	√	√	×	×	×	√
0.1	√	×	×	×	√	√
1X	×	×	√	√	√	√

Note!

"√" means valid input; "×"means invalid input.

3.5.4 Operation Mode

User can set Mode [3: 0] to select different operation modes, as shown in Table 3-16.

Table 3-16 Operation Modes Selection

Mode[3:0]	Description
0000	Normal read operation and page latch write operation
0001	Set pre-program and clear after any program cycle automatically
0100	Clear page latches
1000	Erase Page (or row)
1100	Program Page (or row)

3.5.5 Read Operation

When the Mode input is set as "0000", the user flash enters into read operation mode at the rising edge of Aclk. Seq [1: 0] should be "00" for read operation mode. When the data access time (<= 38ns) is met, the data would be available on the output pin Dout.\

3.5.6 Write Operation

The write operation of user flash memory module includes five steps:

1. Clear page latches
2. Write data into the page latches;
3. Preprogram the selected memory location to pseudo "1";
4. Erase the selected memory location;
5. Program page latch contents into memory location.

After being erased, the data would be "0"; and after being programmed, the data would be "1". An erased location "0" can be programmed to "1", but a programmed location"1" can not be programmed to "0", so erasing is always needed for a new write operation.

Write page latch es

Page latch can be regarded as one page of SRAM that will be wrote into Flash memory. The operation writing into page latches is controlled by Pw signal, independent of Aclk. Pa (Page Addresses) are used for addressing page latches.

Clear page latches should be done before writing. Write Page latches one by one, set Mode value as "0000", and Seq [1: 0] as "00". Write page latch and data read operation are completely independent.

Clear page latches

Unlike write page latches, clear page latches is controlled by Aclk. When the Mode input is set as "0100", the user flash enters into clear page latch mode at rising edge of Aclk.In the mode, Seq [1: 0] should be "00" and page latch data will be cleared in one Aclk cycle.

Erase and Programming

Erase and Programming operation has to go through Seq sequence 1> 2> 3> 0, which are long operations requiring milliseconds. It is forbidden to program the same page twice after an erasure operation.

Before erasing and programming, program all the selected memory locations to pseudo "1". To execute pre-program operation, set PEP (pre-program) first (Mode "0001"), and then program (Mode "1100") the selected locations with high-voltage duration in time of hundreds of microseconds.

3.6 User Flash (GW1N-2/2B/4/4B/6/9)

3.6.1 Introduction

GW1N-2/2B/4/4B/6/9 offers User Flash. The capacity of the user Flash in GW1N-2/2B/4/4B is 256Kbits. The capacity of the user flash in GW1N-6/9 is 608Kbits. The user Flash memory is composed of row memory and column memory. One row memory is composed of 64 column memories. The capacity of one column memory is 32 bits, and the capacity

of one row memory is 64*32=2048 bits. Page erase is supported, and one page capacity is 2048 bytes, i.e., one page includes 8 rows. The features are shown below:

- 10,000 write cycles
- Greater than10 years Data Retention at +85 ℃
- Data Width: 32
- GW1N-2/2B/4/4B capacity: 128 rows x 64 columns x 32 = 256kbits
- GW1N-6/9 capacity: 304 rows x 64 columns x 32 = 608kbits
- Page Erase Capability: 2,048 bytes per page
- Fast Page Erasure/Word Programming Operation
- Clock frequency: 40 MHz
- Word Programming Time:≤16 μs
- Page Erasure Time:≤120 ms
- Electric current
  - Read current/duration:2.19 mA/25 ns (V_{CC}) & 0.5 mA/25 ns (V_{CCX}) (MAX)
  - Program / Erase operation: 12/12 mA(MAX)

3.6.2 Port Signal

SeeFigure 3-37 for GW1N-2/4/2B/4B/6/9 user flash:

Figure 3-37 GW1N-2/4/2B/4B/6/9 Flash Port Signal

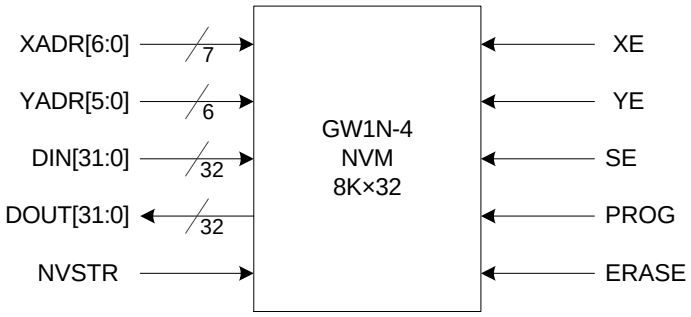


Table 3-17 Flash Module Signal Description

Pin name1	I/O	Description
XADR[5:0][2]	I	X address bus, used to access row address. XADR[n:3] is used to select one page; XADR[2:0] is used to select one row on one page. One page is composed of eight rows, and one row is composed of 64 columns. GW1N-2/2B/4/4B: 128 rows in all, n=6 GW1N-6/9: 304 rows in all, n=8
YADR[5:0][2]	I	Y address bus, used to select one column within a row of memory block. One row consists of 64 columns.
DIN[31:0]	I	Data input bus.
DOUT[31:0]	O	Data output bus.

Pin name1	I/O	Description
XE[2]	I	X address enable signal, if XE is 0, all of row addresses are not enabled.
YE[2]	I	Y address enable signal, if YE is 0, all of column addresses are not enabled.
SE[2]	I	Detect amplifier enable signal, active high.
ERASE	I	Erase port, active-high.
PROG	I	Programming port, active-high.
NVSTR	I	Flash data storage port, active-high.

Note!

- [1] Port names of Control, address,and data signals.
- [2] The read operation is valid only if XE = YE = V_{CC} and SE meets the pulse timing requirements (T_{pws}, T_{nws}). The address of read data is determined by XADR [5: 0] and YADR [5: 0].

3.6.3 Operation Mode

Table 3-18 Truth Table in User Mode

Mode	XE	YE	SE	PROG	ERASE	NVSTR
Read Mode	H	H	H	L	L	L
Programming Mode	H	H	L	H	L	H
Page Erasure Mode	H	L	L	L	H	H

Note!

"H" and "L" means high level and low level of VCC.

3.7 DSP

3.7.1 Introduction

GW1N-2/4/2B/4B/6/9 devices offer abundant DSP modules. Gowin DSP solutions can meet user demands for high performance digital signal processing design, such as FIR, FFT, etc. DSP blocks have the advantages of stable timing performance, high-usage, and low-power.

DSP offers the following functions:

- Multiplier with three widths: 9-bit, 18-bit, 36-bit
- 54-bit ALU
- Multipliers cascading to support wider data
- Barrel shifter
- Adaptive filtering through signal feedback
- Computing with options to round to a positive number or a prime number

- Supports pipeline mode and bypass mode.

Macro

DSP blocks are embedded as rows in the FPGA array. Each DSP occupies nine CFU columns. Each DSP block contains two Macro, and each Macro contains two pre-adders, two 18 x 18 bit multipliers, and one three-input ALU.

Figure 3-38 shows the structure of one Macro.

Figure 3-38 DSP Macro

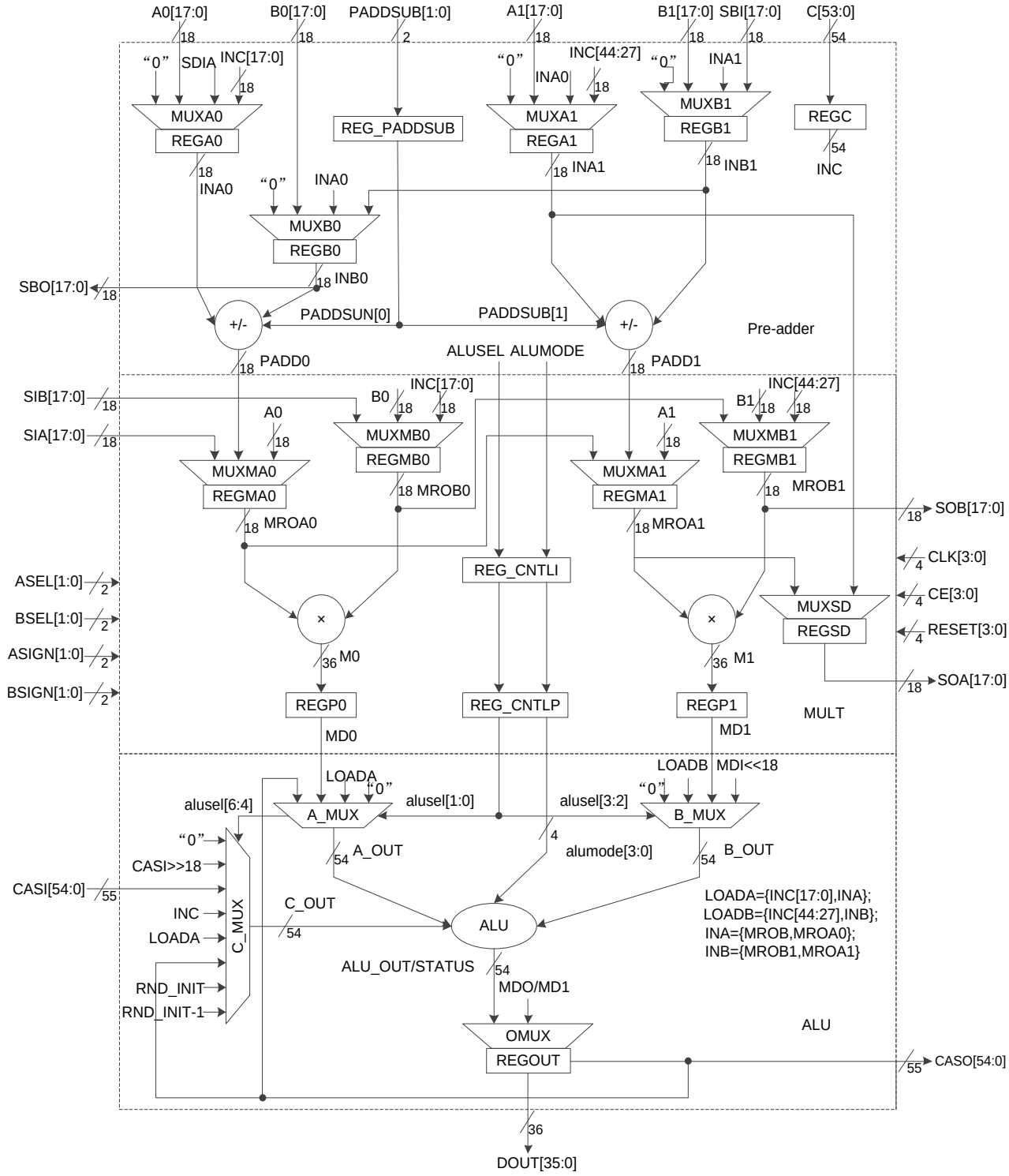


Table 3-19 shows DSP ports description. Table 3-20 shows internal registers.

Table 3-19 DSP Ports Description

Port Name	I/O	Description
A0[17:0]	I	18-bit data input A0
B0[17:0]	I	18-bit data input B0

Port Name	I/O	Description
A1[17:0]	I	18-bit data input A1
B1[17:0]	I	18-bit data input B1
C[53:0]	I	54-bit data input C
SIA[17:0]	I	Shift data input A, used for CASCADE connection. The input signal SIA is directly connected to the output signal SOA of previously adjacent DSP and the delay from SIA to SOA inside a DSP is one clock cycle.
SIB[17:0]	I	Shift data input B, used for CASCADE connection. The input signal SIB is directly connected to the output signal SOB of previously adjacent DSP and the delay from SIB to SOB inside a DSP is one clock cycle.
SBI[17:0]	I	Pre‐adder logic shift input, backward direction.
CASI[54:0]	I	ALU input from previous DSP block, used for cascade connection.
PADDSI0[1:0]	I	Source select for Multiplier or pre-adder input A
BSEL[1:0]	I	Source select for Multiplier input B
ASIGN[1:0]	I	Sign bit for input A
BSIGN[1:0]	I	Sign bit for input B
PADDSUB[1:0]	I	Operation control signals of pre-adder, used for pre-adder logic add/subtract selection
CLK[3:0]	I	Clock input
CE[3:0]	I	Clock Enable
RESET[3:0]	I	Reset input, synchronous or asynchronous
SOA[17:0]	O	Shift data output A
SOB[17:0]	O	Shift data output B
SBO[17:0]	O	Pre‐adder logic shift output, backward direction.
DOUT[35:0]	O	DSP output data
CASO[54:0]	O	ALU output to next DSP block for cascade connection, the highest bit is sign extended.

Table 3-20 Internal Registers Description

Register	Description and Associated Attributes
A0 register	Registers for A0 input
A1 register	Registers for A1 input
B0 register	Registers for B0 input
B1 register	Registers for B1 input
C register	Registers for C input
P1_A0 register	Registers for A0 input of left multiplier
P1_A1 register	Registers for A1 input of right multiplier
P1_B0 register	Registers for B0 input of left multiplier
P1_B1 register	Registers for B1 input of right multiplier
P2_0 register	Registers for pipeline of left multiplier
P2_1 register	Registers for pipeline of right multiplier
OUT register	Registers for DOUT output
OPMODE register	Registers for operation mode control
SOA register	Registers for shift output at port SOA

PADD

Each DSP macro features two units of pre-adders to implement pre-add, pre-subtraction, and shifting.

PADD locates at the first stage with two inputs.,

- Parallel 18-bit input B or SBI;
- Parallel 18-bit input A or SIA.

Note!

Each input end supports pipeline mode and bypass mode.

GOWINSEMI PADD can be used as function block independently, which supports 9-bit and 18-bit width.

MULT

Multipliers locate after the pre-adder. Multipliers can be configured as 9 x 9, 18 x 18, 36 x 18 or 36 x 36. Registered mode and bypass mode are supported both in input and output ports. The configuration modes that a macro supports include:

- One 18 x 36 multiplier
- Two 18 x 18 multipliers
- Four 9 x 9 multipliers

Note!

Two adjacent DSP macros can form a 36 x 36 multiplier.

ALU

Each Macro has one 54 bits ALU54, which can further enhance MULT's functions. The registered and bypass mode are supported both in input and output ports. The functions are as following:

- Multiplier output data / 0, addition/subtraction operations for data A and data B;
- Multiplier output data / 0, addition/subtraction operations for data B and bit C;
- Addition/subtraction operations for data A, data B, and bit C;

3.7.2 DSP Operations

- Multiplier
- Accumulator
- MULTADDALU

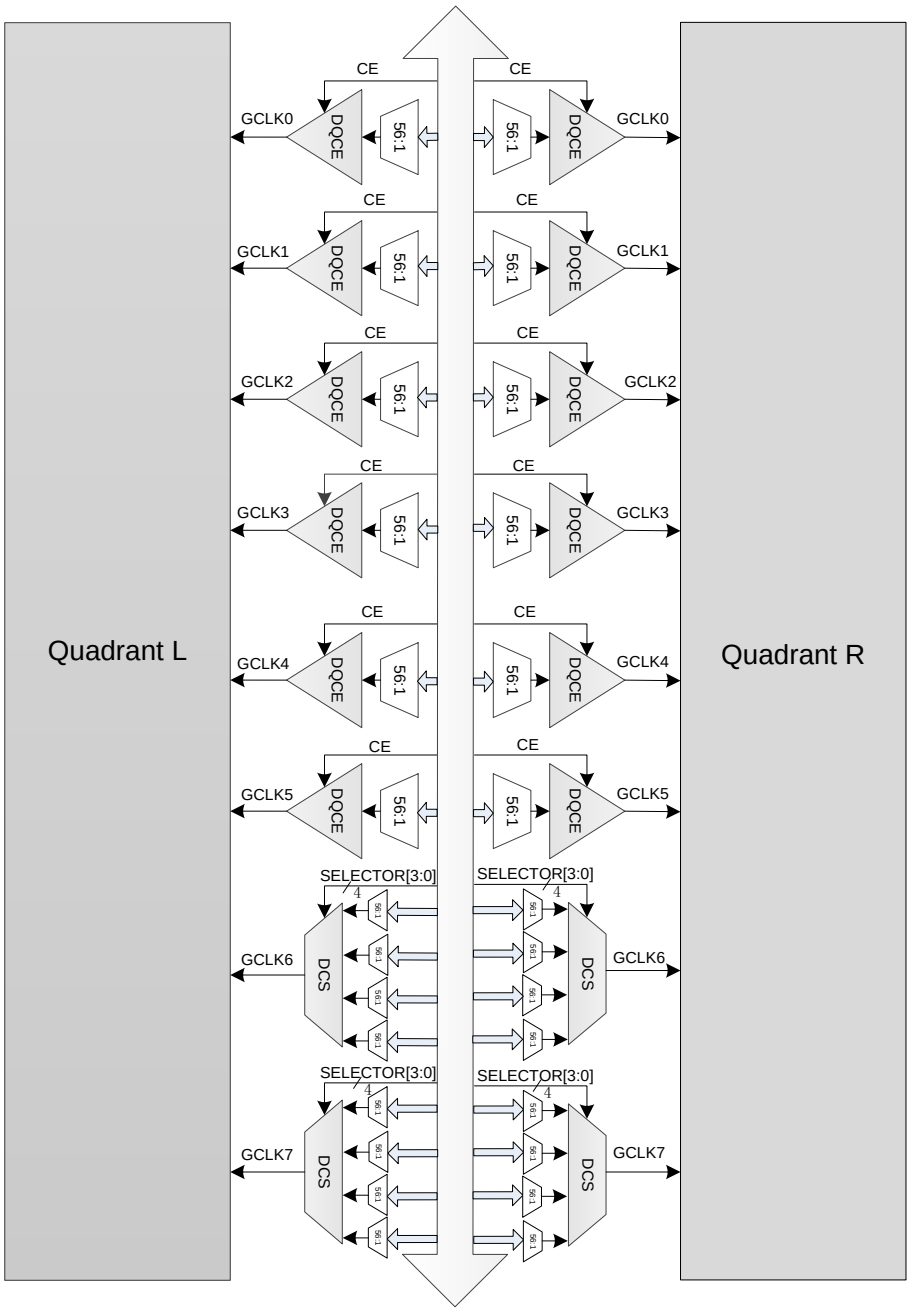
3.8 Clock

The clock resources and wiring are critical for high-performance applications in FPGA. The GW1N series of FPGA products provide the global clock network (GCLK) which connects to all the registers directly. Besides the global clock network, the GW1N series of FPGA products provide high-speed clock HCLK, PLLs, DLLs, etc.

3.8.1 Global Clock

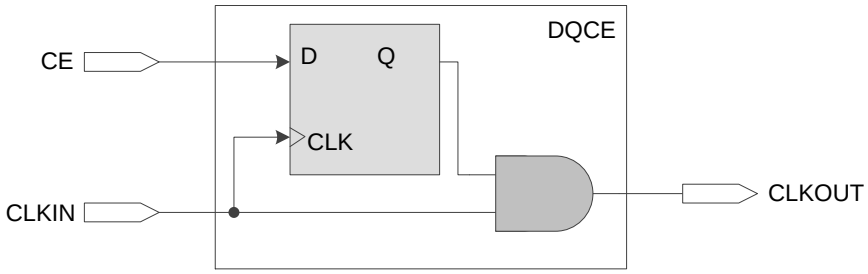
The GCLK is distributed in GW1N-1 as two quadrants, L and R. Each quadrant provides eight GCLKs. The optional clock resources of GCLK can be pins or CRU. Users can employ dedicated pins as clock resources to achieve better timing.

Figure 3-39 GCLK Quadrant Distribution



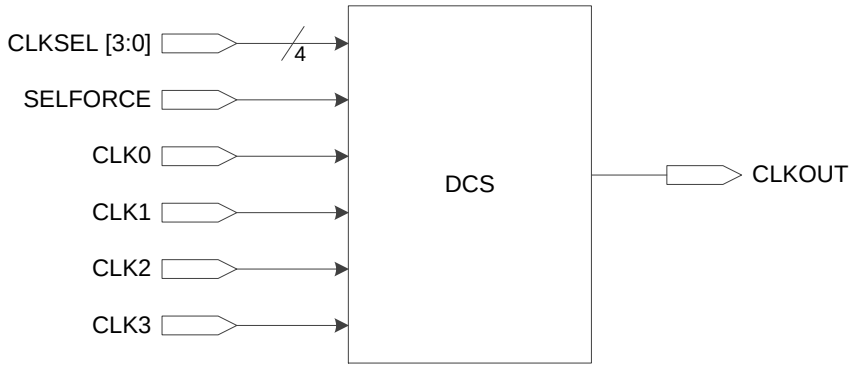
GCLK0~GCLK5 can be turned on or off by Dynamic Quadrant Clock Enable (DQCE). When GCLK0~GCLK5 in the quadrant is off, all the logic driven by it will not toggle; therefore, lower power can be achieved.

Figure 3-40 DQCE Concept



GCLK6~GCLK7 of each quadrant is controlled by the DCS, as shown in Figure 3-41. Select dynamically between CLK0~CLK3 by CRU, and output a glitch-free clock.

Figure 3-41 DCS Concept

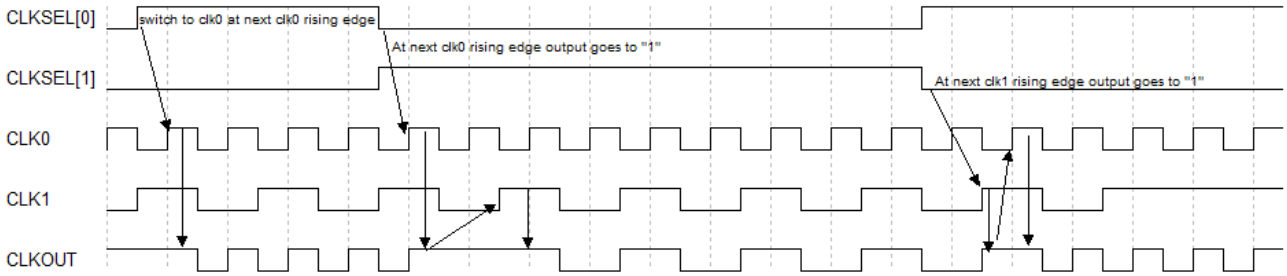


DCS can be configured in the following modes:

1. DCS Rising Edge

Stay as 1 after current selected clock rising edge, and the new select clock will be effective after its first rising edge, as shown in Figure 3-42.

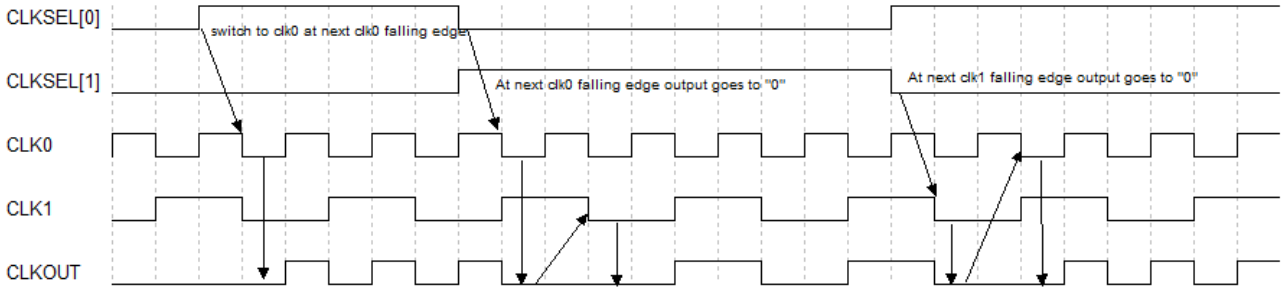
Figure 3-42 DCS Rising Edge



2. DCS Falling Edge

Stay as 0 after current selected clock falling edge, and the new select clock will be effective after its first falling edge, as shown in Figure 3-43.

Figure 3-43 DCS Falling Edge



3. Clock Buffer Mode

In this mode, DCS acts as a clock buffer.

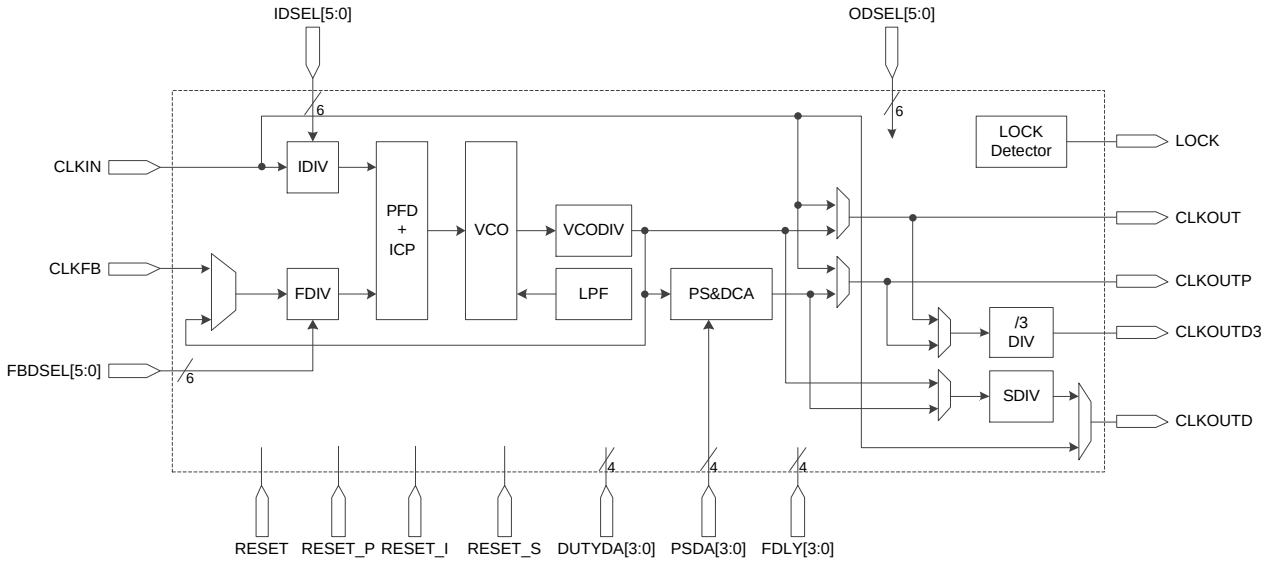
3.8.2 PLL

Phase-locked Loop (PLL) is one kind of a feedback control circuit. The frequency and phase of the internal oscillator signal is controlled by the external input reference clock.

GW1N PLL blocks in the GW1N series of FPGA products provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted by parameters configuration.

See Figure 3-44 for the PLL structure.

Figure 3-44 PLL Structure



The PLL reference clock source can come from an external PLL pin or from internal routing GCLK, HCLK, or general data signal. PLL feedback signal can come from the external PLL feedback input or from internal routing GCLK, HCLK, or general data signal.

PLL features of GW1N-1/2/4/6/9/2B/4B devices are as follows:

- Input frequency:3 MHz~450 MHz
- VCO vibration frequency: 400 MHz~900 MHz
- CLKOUT output frequency: 3.125 MHz~450 MHz

PLL features of GW1N-1S devices are as follows:

- Input frequency:3 MHz~450 MHz
- VCO vibration frequency: 400 MHz~1.2GHz
- CLKOUT output frequency: 3.125 MHz~600 MHz

PLL can adjust the frequency of the input clock CLKIN (multiply and division). The formulas for doing so are as follows:

1. $f_{CLKOUT} = (f_{CLKIN}*FDIV)/IDIV$
2. $f_{VCO} = f_{CLKOUT}*ODIV$
3. $f_{CLKOUTD} = f_{CLKOUT}/SDIV$
4. $f_{PFD} = f_{CLKIN}/IDIV = f_{CLKOUT}/FDIV$

Note!

- f_{CLKIN}: The frequency of the input clock CLKIN
- f_{CLKOUT}: The clock frequency of CLKOUT and CLKOUTP
- $f_{CLKOUTD}$: The clock frequency of CLKOUTD, and CLKOUTD is the clock CLKOUT after division
- f_{PFD}: PFD Phase Comparison Frequency

Adjust IDIV, FDIV, ODIV, and SDIV to achieve the required clock frequency.

See Table 3-21 for a definition of the PLL ports.

Table 3-21 PLL Ports Definition

Port Name	Signal	Description
CLKIN [5：0]	I	Reference clock input
CLKFB	I	Feedback clock input
RESET	I	PLL reset
RESET_P	I	PLL Power Down
RESET_I	I	IDIV reset
RESET_S	I	SDIV and DIV3 reset
INSEL[2：0]	I	Dynamic clock control selector: 0~5
IDSEL [5：0]	I	Dynamic IDIV control: 1~64
FBDSEL [5：0]	I	Dynamic FDIV control:1~64
PSDA [3：0]	I	Dynamic phase control (rising edge effective)
DUTYDA [3：0]	I	Dynamic duty cycle control (falling edge effective)
FDLY[3:0]	I	CLKOUTP dynamic delay control
CLKOUT	O	Clock output with no phase and duty cycle adjustment
CLKOUTP	O	Clock output with phase and duty cycle

Port Name	Signal	Description
		adjustment
CLKOUTD	O	Clock divider from CLKOUT and CLKOUTP (controlled by SDIV)
CLKOUTD3	O	clock divider from CLKOUT and CLKOUTP (controlled by DIV3 with the constant division value 3)
LOCK	O	PLL lock status: 1: locked, 0: unlocked

3.8.3 HCLK

HCLK is the high-speed clock in the GW1N series of FPGA products, which can support high-speed data transfer and is mainly suitable for source synchronous data transfer protocols. See Figure 3-45 and Figure 3-46, Figure 3-47, and Figure 3-48.

Note!

The features of the HCLK in GW1N_1, GW1N-2/4, and GW1N-2B/4B are the same; the features of the HCLK in GW1N-1S and GW1N-6/9 are slightly different.

Figure 3-45 GW1N-1 HCLK Distribution

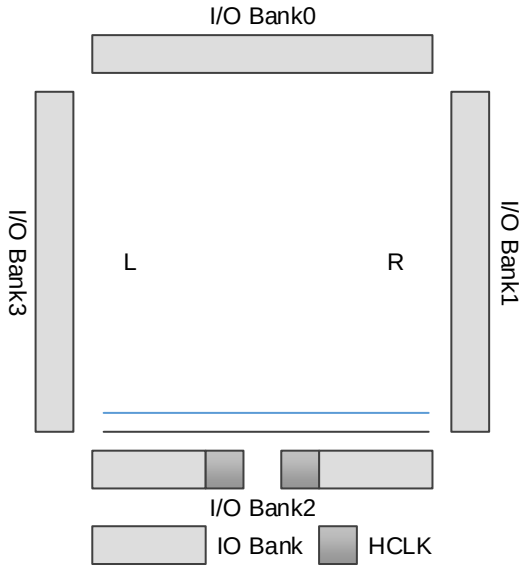


Figure 3-46 GW1N-2/2B/4 /4B HCLK Distribution

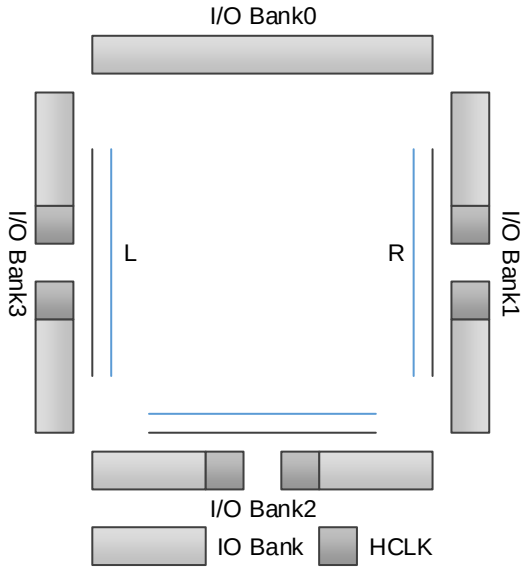


Figure 3-47 GW1N-6/9 HCLK Distribution

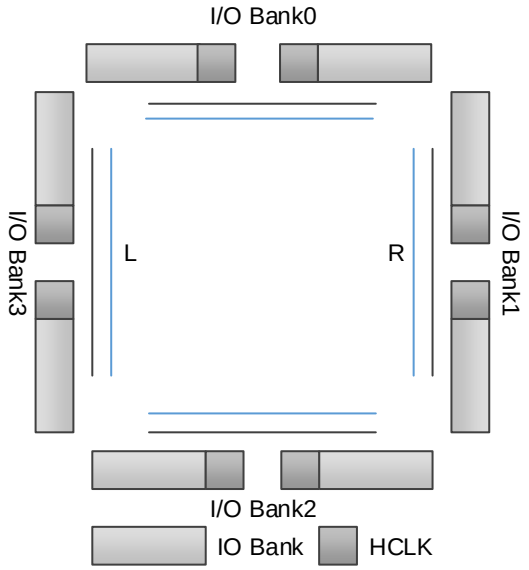
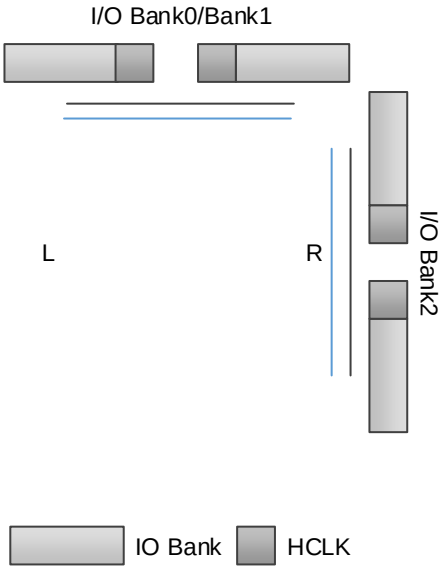


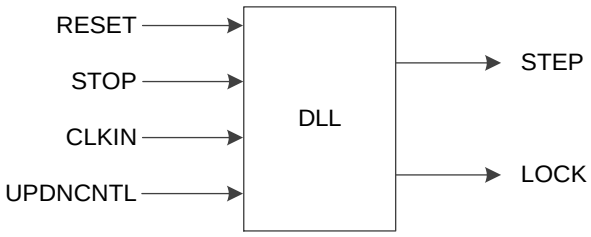
Figure 3-48 GW1N-1S HCLK Distribution



3.8.4 DLL

The GW1N series of FPGA products support DLL. For DLL function, see Figure 3-49.

Figure 3-49 GW1N DLL Function



The source of CLKIN can come from GCLK and the neighboring

HCLK.

The calculated STEP will be sent to the neighboring Banks. For example, the signal STEP of DLL can be sent to HCLK in Bank2. At the same time, the signal STEP can also be sent to user logic through CRU.

3.9 Long Wire (LW)

As a supplement to CRU, the GW1N series of FPGA products provide another routing resource- Long Wire, which can be used as clock, clock enable, set/reset,or other high fan out signals.

3.10 Global Set/Reset (GSR)

A global set/rest (GSR) network is built in the GW1N series of FPGA product. There is a direct connection to core logic. It can be used as asynchronous/synchronous set or asynchronous/synchronous reset. The registers in CFU and I/O can be individually configured to use GSR.

3.11 Programming Configuration

The GW1N series of FPGA products support SRAM and Flash. The Flash programming mode supports on-chip Flash and off-chip Flash. The GW1N series of FPGA products support DUAL BOOT, providing a selection for users to backup data to off chip Flash according to requirements.

Besides JTAG, the GW1N series of FPGA products also support GOWINSEMI own configuration mode: GowinCONFIG (AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU). All the devices support JTAG and AUTO BOOT. For more detailed information, please refer to *GW1N series FPGA Products Programming and Configuration User Guide*.

3.11.1 SRAM Configuration

When you adopt SRAM to configure the device, each time the device is powered on, it needs to download the bit stream file to configure.

3.11.2 Flash Configuration

The Flash configuration data is stored in the on-chip flash. Each time the device is powered on, the configuration data is transferred from the Flash to the SRAM, which controls the working of the device. This mode can complete configuration within a few ms, and is referred to as “Quick Start”.

B version of GW1N devices has the feature of transparent transmission. That is to say, the B version device can program the on-chip Flash or off-chip Flash via the JTAG interface without affecting the current working state. During programming, the B version device works according to the previous configuration. After programming, provide one low pulse for RECONFIG_N to complete the online upgrade. This feature applies to the applications with long online time and irregular upgrades.

The GW1N series of FPGA products also support off-chip Flash configuration and dual-boot. Please refer to *Gowin FPGA Products Programming and Configuration User Guide* for more detailed information.

3.12 On Chip Oscillator

There is an internal oscillator in each of the GW1N series of FPGA product. The on-chip oscillator supports the clock frequencies ranging from 2.5 MHz to 125MHz.It provides programmable user clock with clock precision ±5%. During the configuration process, it can provide a clock for MSPI mode. See Table 3-23 for GW1N-1/1S/6/9 output frequency; see Table 3-23 for GW1N-2/2B/4/4B output frequency.

Table 3-22 GW1N-2/2B/4/4B Oscillator Output Frequency Options

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.1MHz[1]	8	6.6MHz	16	13.1MHz
1	4.6MHz	9	7MHz	17	15MHz
2	4.8MHz	10	7.5MHz	18	17.5MHz
3	5MHz	11	8.1MHz	19	21MHz
4	5.3MHz	12	8.8MHz	20	26.3MHz
5	5.5MHz	13	9.5MHz	21	35MHz
6	5.8MHz	14	10.5MHz	22	52.5MHz
7	6.2MHz	15	11.7MHz	23	105MHz[2]

Table 3-23 GW1N-1/1S/6/9 Oscillator Output Frequency Options

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.5MHz[1]	8	7.8MHz	16	15.6MHz
1	5.4MHz	9	8.3MHz	17	17.9MHz
2	5.7MHz	10	8.9MHz	18	21MHz
3	6.0MHz	11	9.6MHz	19	25MHz
4	6.3MHz	12	10.4MHz	20	31.3MHz
5	6.6MHz	13	11.4MHz	21	41.7MHz
6	6.9MHz	14	12.5MHz	22	62.5MHz
7	7.4MHz	15	13.9MHz	23	125MHz[2]

Note!

- [1] Default frequency
- [2] 125MHz is not suitable for MSPI.

The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters.

The following formula is used to get GW1N-1/1S/6/9 output clock frequency:f_{out}=250MHz/Param.

The following formula is used to get GW1N-2/2B/4/4B output clock frequency:f_{out}=210MHz/Param

“Param” is the configuration parameter with a range of 2~128. It

supports even number only.

4 AC/DC Characteristic

Note!

Please ensure that you use GOWINSEMI devices within the recommended operating conditions and range. Data beyond the working conditions and range are for reference only. GOWINSEMI does not guarantee that all devices will operate normally beyond the operating conditions and range.

4.1 Operating Conditions

Table 4-1 Absolute Max. Ratings

Name	Description	Min.	Max.
V_{CC}	LV: Core Power	-0.5V	1.32V
	UV:Core Power	-0.5V	3.75V
V_{CCO}	I/O Bank Power	-0.5V	3.75V
V_{CCX}	Auxiliary voltage	-0.5V	3.75V
Storage Temperature	Storage Temperature	-65 ℃	+150 ℃
Junction Temperature	Junction Temperature	-40 ℃	+125 ℃

Table 4-2 Recommended Operating Conditions

Name	Description	Min.	Max.
V_{CC}	LV: Core Power	1.14V	1.26V
	UV:Core Power	1.71V	3.465V
V_{CCO}	I/O Bank Power	1.14V	3.465V
V_{CCX}	Auxiliary voltage	2.375V	3.465V
T_{JCOM}	Junction temperature commercial operation	0 ℃	+85 ℃
T_{JIND}	Junction temperature Industrial operation	-40 ℃	+100 ℃
T_{RAMP}	Power supply ramp rates for all power supplies	0.01mV/μs	10mV/μs

Note!

- For some packages, V_{CCO} and V_{CCX} may share one pin. In this case, V_{CCX} requirements must be met first.

- For the power supply info, please refer to GW1N-1 Pinout, GW1N-2&2B&4&4B Pinout, and GW1N-6&9 Pinout.

Table 4-3 Hot Socket Specifications

Name	Description	Condition	Max.
I_{HS}	Input or I/O leakage current	$V_{IN}=V_{IL}$ (MAX)	TBD

4.2 ESD

Table 4-4 GW1N ESD - HBM

Device	GW1N-1	GW1N-2/ GW1N-2B	GW1N-4/ GW1N-4B	GW1N-6	GW1N-9	GW1N-1S
LQ100	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V	-
LQ144	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V	-
EQ144	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V	-
LQ176	-	-	-	HBM>1,000V	HBM>1,000V	-
EQ176	-	-	-	HBM>1,000V	HBM>1,000V	-
MG160	-	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V	-
MG196	-	-	-	HBM>1,000V	HBM>1,000V	-
PG256	-	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V	-
PG256 M	-	HBM>1,000V	HBM>1,000V	-	-	-
UG169	-	-	-	HBM>1,000V	HBM>1,000V	-
UG256	-	-	-	HBM>1,000V	HBM>1,000V	-
UG332	-	-	-	HBM>1,000V	HBM>1,000V	-
QN32	HBM>1,000V	HBM>1,000V	HBM>1,000V	-	-	-
QN48	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V	-
CS30	HBM>1,000V	-	-	-	-	-
CS72	-	HBM>1,000V	HBM>1,000V	-	-	-
QN88	-	HBM>1,000V	HBM>1,000V	HBM>1,000V	HBM>1,000V	-
FN32	-	-	-	-	-	HBM>1,000V

Table 4-5 GW1N ESD - CDM

Device	GW1N-1	GW1N-2/ GW1N-2B	GW1N-4/ GW1N-4B	GW1N-6	GW1N-9	GW1N-1S
LQ100	CDM>500V	CDM>500V	CDM>500V	CDM>500V	CDM>500V	-
LQ144	CDM>500V	CDM>500V	CDM>500V	CDM>500V	CDM>500V	-
EQ144	CDM>500V	CDM>500V	CDM>500V	CDM>500V	CDM>500V	-
LQ176	-	-	-	CDM>500V	CDM>500V	-

Device	GW1N-1	GW1N-2/ GW1N-2B	GW1N-4/ GW1N-4B	GW1N-6	GW1N-9	GW1N-1S
EQ176	-	-	-	CDM>500V	CDM>500V	-
MG160	-	CDM>500V	CDM>500V	CDM>500V	CDM>500V	-
MG196	-	-	-	CDM>500V	CDM>500V	-
PG256	-	CDM>500V	CDM>500V	CDM>500V	CDM>500V	-
PG256M	-	CDM>500V	CDM>500V	-	-	-
UG169				CDM>500V	CDM>500V	
UG256	-	-	-	CDM>500V	CDM>500V	-
UG332	-	-	-	CDM>500V	CDM>500V	-
QN32	CDM>500V	-	-	-	-	-
QN48	CDM>500V	CDM>500V	CDM>500V	CDM>500V	CDM>500V	-
CS30	CDM>500V	-	-	-	-	-
CS72	-	CDM>500V	CDM>500V	-	-	-
QN88	-	CDM>500V	CDM>500V	CDM>500V	CDM>500V	-
FN32	-	-	-	-	-	CDM>500V

Table 4-6 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I_{IL},I_{IH}	Input or I/O leakage	$V_{CCO}<V_{IN}<V_{IH}$ (MAX)	-	-	210 μA
		$0V<V_{IN}<V_{CCO}$	-	-	10 μA
I_{PU}	I/O Active Pull-up Current	$0<V_{IN}<0.7V_{CCO}$	-30 μA	-	-150 μA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX)$<V_{IN}<V_{CCO}$	30 μA	-	150 μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN}=V_{IL}$ (MAX)	30 μA	-	-
I_{BHHO}	Bus Hold High Sustaining Current	$V_{IN}=0.7V_{CCO}$	-30 μA	-	-
I_{BHLO}	Bud HoldLow Overdrive Current	$0\leq V_{IN}\leq V_{CCO}$	-	-	150 μA
I_{BHHO}	BusHoldHigh Overdrive Current	$0\leq V_{IN}\leq V_{CCO}$	-	-	-150 μA
V_{BHT}	Bus hold trip points		V_{IL} (MAX)	-	V_{IH} (MIN)
C1	I/O Capacitance			5 pF	8 pF
V_{HYST}	Hysteresis for Schmitt Trigge	V_{CCO}=3.3V, Hysteresis= Large	-	482mV	-
		V_{CCO}=2.5V, Hysteresis= Large	-	302mV	-

Name	Description	Condition	Min.	Typ.	Max.
	inputs	V_{CCO}=1.8V, Hysteresis= Large	-	152mV	-
		V_{CCO}=1.5V, Hysteresis= Large	-	94mV	-
		V_{CCO}=3.3V, Hysteresis= Small	-	240mV	-
		V_{CCO}=2.5V, Hysteresis= Small	-	150mV	-
		V_{CCO}=1.8V, Hysteresis= Small	-	75mV	-
		V_{CCO}=1.5V, Hysteresis= Small	-	47mV	-

Table 4-7 Static Supply Current

Name	Description	LV/UV	Device	Min.	Typ.	Max.
I_{CC}	Core current V_{CCX}=3.3V, V_{CCX}=2.5V	LV	GW1N-1		1.8mA (test data)	
I_{CCX}	V_{CCX} current（V_{CCX}=3.3V)	LV	GW1N-1		1mA (test data)	
	V_{CCX} current（V_{CCX}=2.5V)	LV	GW1N-1		0.8mA (test data)	
I_{CCO}	I/O Bank current (V_{CCO}=2.5V)	LV	GW1N-1		NA	
I_{CC}	Core current（V_{CCX}=3.3V）	LV/UV	GW1N-4		2.8mA (test data)	
I_{CCX}	V_{CCX} current（V_{CCX}=3.3V)	LV/UV	GW1N-4		1.15mA (test data)	
I_{CCO}	I/O Bank current (V_{CCO}=2.5V)	LV/UV	GW1N-4		0.55mA (test data)	
I_{CC}	Core current（V_{CCX}=3.3V）	LV/UV	GW1N-9		3.5mA（test data）	
I_{CCX}	V_{CCX} current（V_{CCX}=3.3V）	LV/UV	GW1N-9		5mA（test data）	
I_{CCO}	I/O Bank power current (V_{CCO}=2.5V)	LV/UV	GW1N-9		2mA（test data）	
I_{CC}	Core current under load（V_{CCX}=3.3V）	LV	GW1N-1	1.6mA		1.9mA
I_{CCX}	Core current under load（VCCX=3.3V）	LV	GW1N-1	2.45mA		2.74mA
I_{CCO}	I/O Bank current under load(V_{CCO}=2.5V)	LV	GW1N-1		0.06mA	

4.3 DC Characteristic

Table 4-8 I/O Operating Conditions Recommended

Name	Output V_{CCO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.465	-	-	-
LVCMOS33	3.135	3.3	3.465	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.465	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.465	1.3	1.5	1.7
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.465	-	-	-
LVPECL33E	3.135	3.3	3.465	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.465	-	-	-
SSTL33D_II	3.135	3.3	3.465	-	-	-

Name	Output V_{CCO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

Table 4-9 IOB Single - Ended DC Electrical Characteristic

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}0.4V	4	-4
							8	-8
							12	-12
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}-0.4V	2	-2
							6	-6
					0.2V	V_{CCO}-0.2V	0.1	-0.1
PCI33	-0.3V	0.3 x V_{CCO}	0.5 x V_{CCO}	3.6V	0.1 x V_{CCO}	0.9 x V_{CCO}	1.5	-0.5
SSTL33_I	-0.3V	V_{REF}-0.2V	V_{REF}+0.2V	3.6V	0.7	V_{CCO}-1.1V	8	-8

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max				
SSTL25_I	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	0.54V	V_{CCO}-0.62V	8	-8
SSTL25_II	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	NA	NA	NA	NA
SSTL18_II	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	NA	NA	NA	NA
SSTL18_I	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
SSTL15	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA
HSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL15_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA

Table 4-10 IOB Differential Electrical Characteristics

LVDS25 (GW1N-1 and GW1N-1S do not support.)

Name	Description	Condition	Min.	Typ.	Max.	Unit
V_{INA},V_{INB}	Input Voltage (Input Voltage)		0	-	2.4	V
V_{CM}	Input Common Mode Voltage (Input Common Mode Voltage)	Half the Sum of the Two Inputs	0.05	-	2.35	V
V_{THD}	Differential Input Threshold	Difference Between the Two Inputs	±100	-	-	mV
I_{IN}	Input Current	Power On or Power Off	-	-	± 10	μA
V_{OH}	Output High Voltage for V_{OP} or V_{OM}	R_T = 100Ω	-	-	1.60	V
V_{OL}	Output Low Voltage for V_{OP} or V_{OM}	R_T = 100Ω	0.9	-	-	V
V_{OD}	Output Voltage Differential	(V_{OP} - V_{OM}), R_T = 100Ω	250	350	450	mV
ΔV_{OD}	Change in V_{OD} Between High and Low		-	-	50	mV
V_{OS}	Output Voltage Offset	(V_{OP} + V_{OM})/2, R_T = 100Ω	1.125	1.20	1.375	V
ΔV_{OS}	Change in V_{OS} Between High and Low		-	-	50	mV
I_S	Short-circuit current	V_{OD} = 0V output short-circuit	-	-	15	mA

4.4 Switching Characteristic

4.4.1 Internal Switching Characteristics

Table 4-11 CFU Block Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{LUT4_CFU}	LUT4 delay	-	0.674	ns
t_{LUT5_CFU}	LUT5 delay	-	1.388	ns
t_{LUT6_CFU}	LUT6 delay	-	2.01	ns
t_{LUT7_CFU}	LUT7 delay	-	2.632	ns
t_{LUT8_CFU}	LUT8 delay	-	3.254	ns
t_{SR_CFU}	Set/Reset to Register output	-	1.86	ns
t_{CO_CFU}	Clock to Register output	-	0.76	ns

Table 4-12 B-SRAM Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COAD_BSRAM}	Clock to output from read address/data	-	5.10	ns
t_{COOR_BSRAM}	Clock to output from output register	-	0.56	ns

Table 4-13 DSP Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COIR_DSP}	Clock to output from output register	-	4.80	ns
t_{COPR_DSP}	Clock to output from output register	-	2.40	ns
t_{COOR_DSP}	Clock to output from output register	-	0.84	ns

Table 4-14 GearboxInternal Timing Parameters

Name	Description	Typ.	Unit
FMAXIDDR	2:1 Gearbox maximum input frequency	410	MHz
$FMAX_{IDES4}$	4:1 Gearbox maximum input frequency	410	MHz
$FMAX_{IDES8}$	8:1 Gearbox maximum input frequency	410	MHz
$FMAX_{IVIDEO}$	7:1 Gearbox maximum input frequency	390	MHz

Name	Description	Typ.	Unit
$FMAX_{IDES10}$	10:1 Gearbox maximum input frequency	410	MHz
$FMAX_{ODDR}$	1:2 Gearbox maximum input frequency	355	MHz
$FMAX_{OSER4}$	1:4 Gearbox maximum input frequency	360	MHz
$FMAX_{OSER8}$	1:8 Gearbox maximum input frequency	355	MHz
$FMAX_{OVIDEO}$	1:7 Gearbox maximum input frequency	355	MHz
$FMAX_{OSER10}$	1:10 Gearbox maximum input frequency	355	MHz

4.4.2 External Switching Characteristics

Table 4-15 External Switching Characteristics

Name	Description	Device	-5		-6		Unit
			Min	Max	Min	Max	
Clocks	TBD	TBD	TBD	TBD	TBD	TBD	
Pin-LUT-Pin Delay	TBD	TBD	TBD	TBD	TBD	TBD	
General I/O Pin Parameters	TBD	TBD	TBD	TBD	TBD	TBD	

Table 4-16 On chip Oscillator Output Frequency

Name	Description		Min.	Typ.	Max.
f_{MAX}	On chip Oscillator Output Frequency (0 ~ +85℃)	GW1N-2/4	118.75MHz	125MHz	131.25MHz
		GW1N-1/1S/6/9	99.75MHz	105MHz	110.25MHz
	On chip Oscillator Output Frequency (-40 ~ +100℃)	GW1N-2/4	112.5MHz	125MHz	137.5MHz
		GW1N-1/1S/6/9	94.5MHz	105MHz	115.5MHz
t_{DT}	Clock Duty Cycle		43%	50%	57%
t_{OPJIT}	Clock Period Jitter		0.01 UIPP	0.012 UIPP	0.02 UIPP

Table4-17 PLL Parameters

Name	Description	Min.	Typ.	Max.
F_{in}	Input clock frequency	3MHz	-	450MHz/ 600MHz
F_{out}	Output clock frequency	Fvco/128	-	Fvco/2
F_{vco}	Voltage-controlled oscillator clock frequency	400MHz	-	900MHz/ 1.2GHz

Name	Description	Min.	Typ.	Max.
t_{DT}	Output Clock Duty Cycle	-	$0.0625T_{pll}$	
T_{PAS}	Phase adjustment step	-	$0.0625T_{pll}$	

4.5 User Flash Characteristics

4.5.1 DC Characteristics[1]

(T_J = -40~+100℃, V_{CC} = 0.95~1.05V, V_{CCX} = 1.7~3.45V, V_{SS} = 0V)

Table 4-18 GW1N-1/ GW1N-1S User Flash DC Characteristic

Name	Description	Spec.			Unit
		Min.	Nomal	Max.	
Ta	Environmental temperature	-40	25	85	℃
Tj	Junction Temperature	-40	25	100	℃
Ilkg	Leakage current	-	-	1	μA
Isb	Standbycurrent	-	-	3（Ta=25）	μA
		-	-	20（Ta=85）	
Icc0	Idle current	-	-	1.3	mA
Icc1	Read operationcurrent	-	-	2（Rmod=00）	mA
		-	-	2.5（Rmod=01）	mA
		-	-	3（Rmod=00）	mA
Icc2	Page write current	-	-	2	mA
Icc3	programming/erasing current	-	-	3	mA

Table 4-19 GW1N-2/2B/4/4B/6/9 User Flash DC Characteristic

Name	Param-eter	Max.		Unit	Wake-up Time	Condition
		V_{CC}[3]	V_{CCX}			
Read mode (w/I 25ns)[1]	I_{CC1}[2]	2.19	0.5	mA	NA	Min. Clcok period, duty cycle 100%, VIN = “1/0”
Write mode		0.1	12	mA	NA	
Erase mode		0.1	12	mA	NA	
Page Erasure Mode		0.1	12	mA	NA	
Read mode static current (25-50ns)	I_{CC2}	980	25	μA	NA	XE=YE=SE=“1”, between T=Tacc and T=50ns, I/O=0mA; later than T=50ns, read mode is turned off, and I/O current is

Name	Param-eter	Max.		Unit	Wake-up Time	Condition
		V_{CC}[3]	V_{CCX}			
						the current of standby mode.
Standby mode	I_{SB}	5.2	20	μA	0	V_{SS}, V_{CCX}, and V_{CC}

Note!

- [1] Means the average current, and the peak value is higher than the average one.
- [2] Calculated in different T_{new} clock periods.
  - $T_{new} < T_{acc}$ is not allowed
  - $T_{new} = T_{acc}$
  - $T_{acc} < T_{new}$ - 50ns: I_{CC1} (new) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + I_{CC2}
  - T_{new}>50ns: I_{CC1} (new) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + 50ns x I_{CC2}/T_{new} + I_{SB}
  - t > 50ns, $I_{CC2} = I_{SB}$
- [3] V_{CC} must be greater than 1.08V from the zero wake-up time.

4.5.2 Timing Parameters[1,5,6]

(T_J = -40~+100℃, V_{CC} = 0.95~1.05V, V_{CCX} = 1.7~3.45V, V_{SS} = 0V)

Table 4-20 GW1N-1/GW1N-1S User Flash Timing Parameters

Name	Description	Spec.			Unit
		Min.	Nomal	Max.	
Taa	Data acquisition time	-	-	38	ns
Tcy	Read cycle	43	-	-	ns
Tawl	Aclk high-level time	10	-	-	ns
Tawl	Aclk low-level time	10	-	-	ns
Tas	Setup time	3	-	-	ns
Tah	Hold-up time	3	-	-	ns
Toz	Oe down to high resistance	-	-	2	ns
Toe	Oe up to Dout	-	-	2	ns
Twcy	Write cycle	40	-	-	ns
Tpw	PwAclk high-level time	16	-	-	ns
Tpwl	Pw low-level time	16	-	-	ns
Tpas	Page address set up time	3	-	-	ns
Tpas	Page address hold-up time	3	-	-	ns
Tds	Data set up time	16	-	-	ns
Tdh	Data hold-up time	3	-	-	ns
Ts0	Seq0 cycle	6	-	-	μs
Ts1	Seq1 cycle	15	-	-	μs
Ts2p	Set up time from Aclk to Pe rising edge	5	-	10	μs

Name	Description	Spec.			Unit
		Min.	Nomal	Max.	
Ts3	Seq3 cycle	5	–	10	μs
Tps3	Set up time from Pe falling edge to Aclk	60	–	–	μs
Tpe	Mode=1000 erasure time	5.7	6	6.3	ms
	Mode=1100 programming time	1.9	2	2.1	ms
	Mode=11xx preprogramming time	190	200	210	us

Table 4-21 GW1N-2/2B/4/4B/6/9 User Flash Timing Parameters

User Modes	Parameter	Name	Min.	Max.	Unit
Access time[2]	WC1	T_{acc}[3]	-	25	ns
	TC		-	22	ns
	BC		-	21	ns
	LT		-	21	ns
	WC		-	25	ns
Program/Erase to data storage		T_{nvs}	5	-	μs
Data storage hold time		T_{nvh}	5	-	μs
Data storage hold time (Overall erase)		T_{nvh1}	100	-	μs
Time from data storage to program setup		T_{pgs}	10	-	μs
Program hold time		T_{pgh}	20	-	ns
Write time		T_{prog}	8	16	μs
Write ready time		T_{wpr}	>0	-	ns
Erase hold time		T_{whd}	>0	-	ns
Time from control signal to write/Erase setup		T_{cps}	-10	-	ns
Time from SE to read setup		T_{as}	0.1	-	ns
E pulse high level time		T_{pws}	5	-	ns
Adress/data setup time		T_{ads}	20	-	ns
Adress/data hold time		T_{adh}	20	-	ns
Data hold-up time		T_{dh}	0.5	-	ns
Read mode address hold time[3]	WC1	T_{ah}	25	-	ns
	TC		22	-	ns
	BC		21	-	ns
	LT		21	-	ns
	WC		25	-	ns

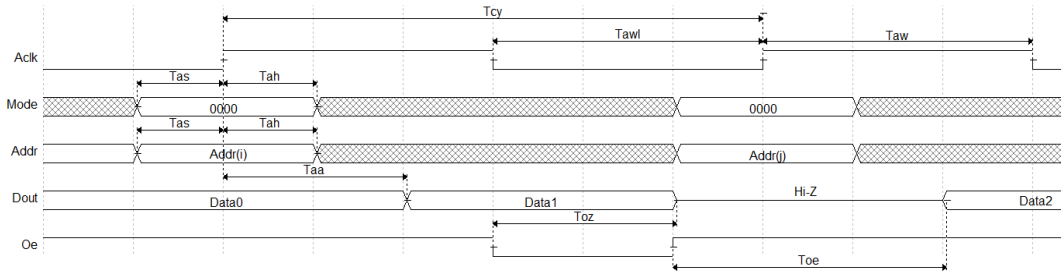
User Modes	Parameter	Name	Min.	Max.	Unit
SE pulse low level time		T_{nws}	2	-	ns
Recovery time		T_{rcv}	10	-	μs
Data storage time		T_{hv}[4]	-	6	ms
Erasure time		T_{erase}	100	120	ms
Overall erase time		T_{me}	100	120	ms
Wake-up time from power down to standby mode		T_{wk_pd}	7	-	μs
Standby hold time		T_{sbh}	100	-	ns
V_{CC} setup time		T_{ps}	0	-	ns
V_{CCX} hold time		T_{ph}	0	-	ns

Note!

- [1] The parameter values may change;
- [2] The values are simulation data only.
- [3]After XADR, YADR, XE, and YE are valid, T_{acc} start time is SE rising edge. DOUT is kept until the next valid read operation;
- [4]T_{hv} is the time between write and the next erasure.The same address can not be written twice before erasure, so does the same register. This limitation is for safety;
- [5]Both the rising edge time and falling edge time for all waveform is 1ns;
- [6] TX, YADR, XE, and YE hold time need to be T_{acc} at leaset, and T_{acc} start from SE rising edge.

4.5.3 Operation Timing Diagrams (GW1N-1/ GW1N-1S)

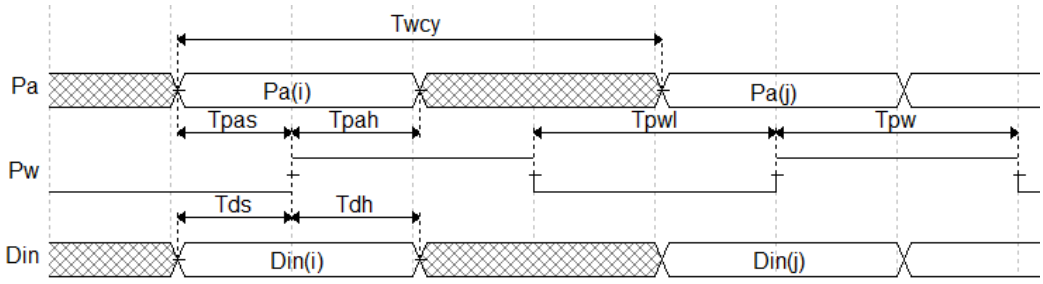
Figure 4-1 Read Mode



Note!

Read operation cycle Seq=0, Addr signal contains Ra, Ca, Rmod, and Rbytesel.

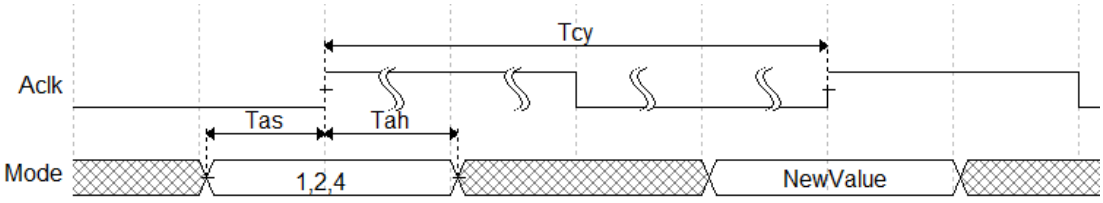
Figure 4-2 Write Page Latches Mode



Note!

Write Page Latches Cycle Seq=0, Mode=0000.

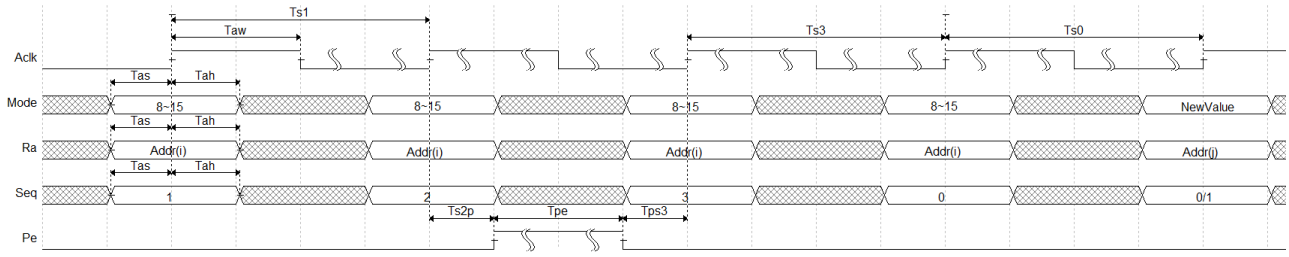
Figure 4-3 Clear Page Latches Mode



Note!

The timing parameters of Setting PEP, writing to all pages, and clearing page latches are all the same.The MODE values are different.

Figure 4-4 High Level Cycle



4.5.4 Operation Timing Diagrams (GW1N-2/2B/4/4B/6/9)

Figure 4-5 User Flash Read Operation

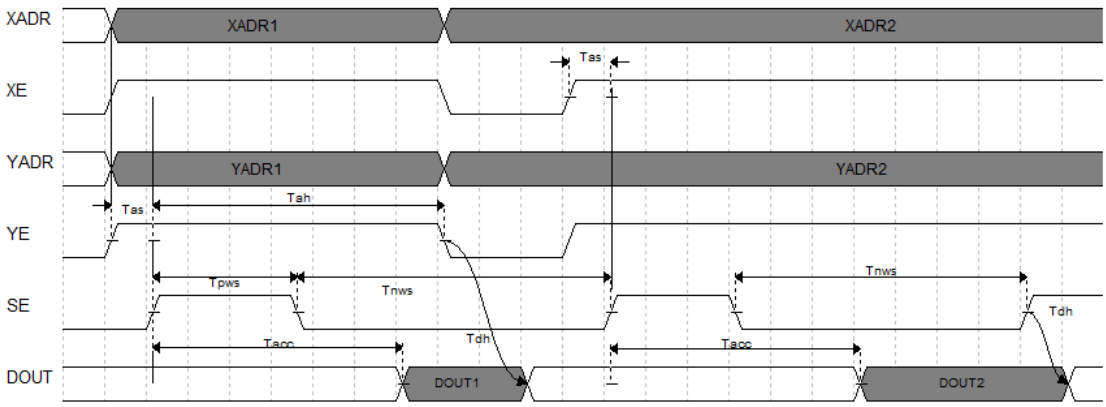


Figure 4-6 User Flash Program Operation

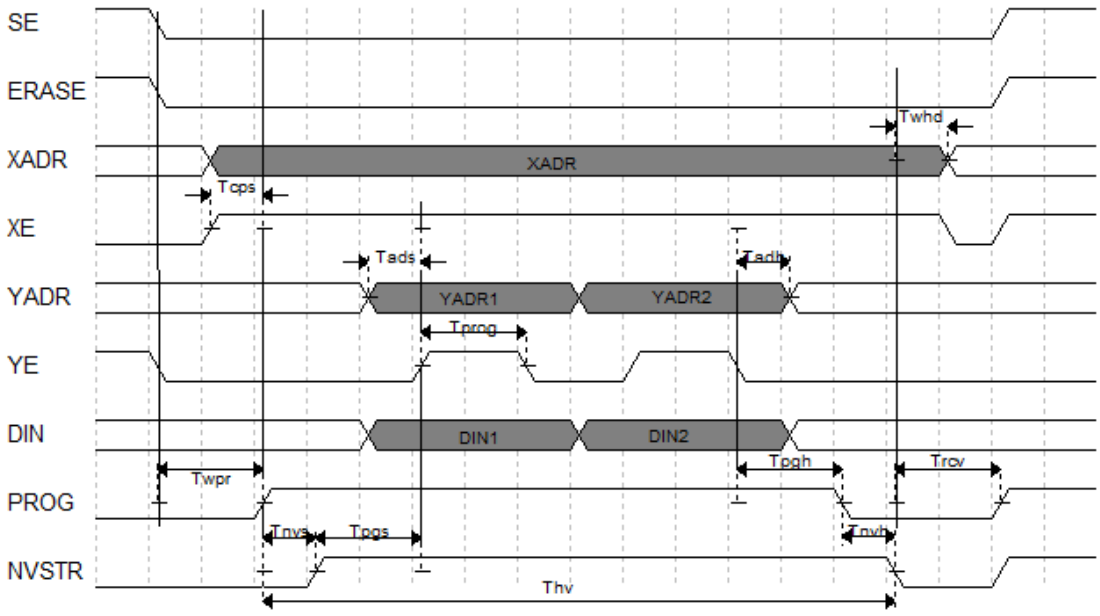
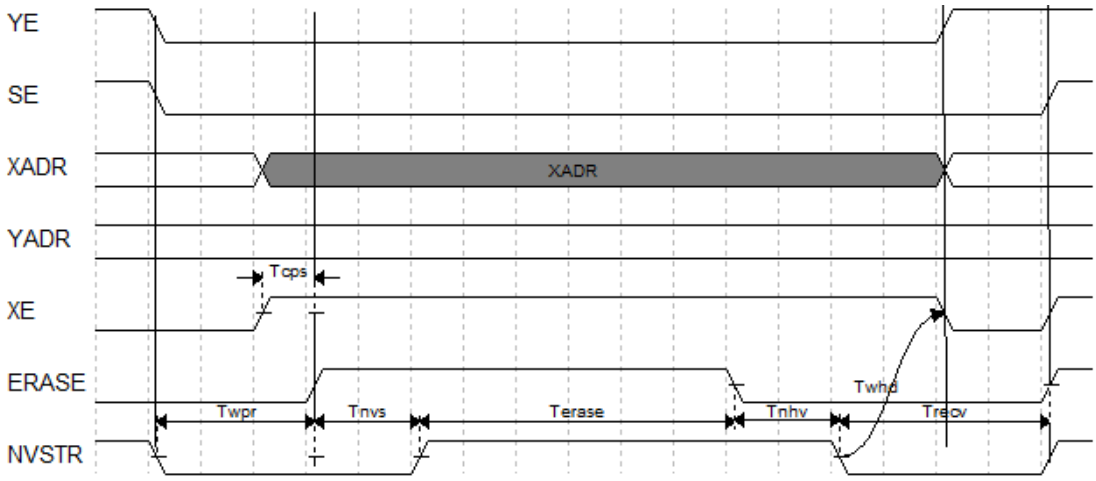


Figure 4-7 User Flash Erase Operation



4.6 Configuration Interface Timing Specification

The GW1N series of FPGA products GowinCONFIG support six configuration modes: AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU. For more detailed information, please refer to *Gowin FPGA Products Programming and Configuration* User Guide.

4.6.1 JTAG Port Timing Specifications

The JTAG mode of the GW1N series of FPGA products is in compliance with IEEE1532 and IEEE1149.1 boundary scan standards.

JTAG mode downloads the bitstream to SRAM, and the data is lost after power off.

See Figure 4-8 for JTAG timing.

Figure 4-8 JTAG Timing

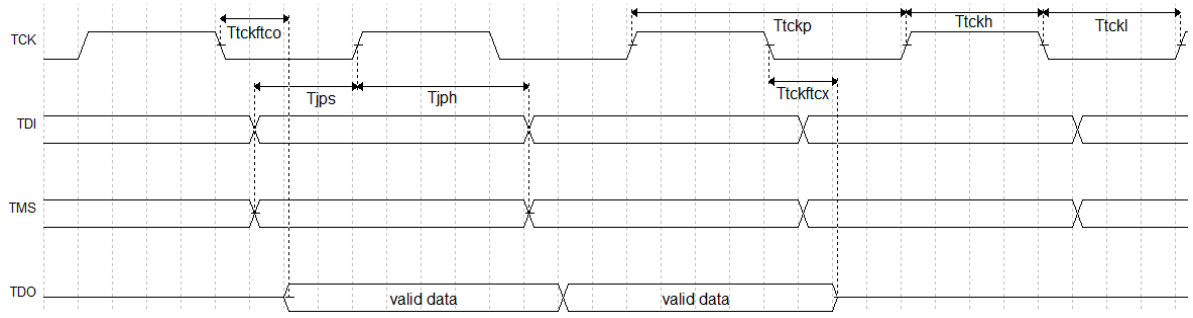


Table 4-22 JTAG Timing Parameters

Name	Description	Min.	Max.
$T_{tckftco}$	Time from TCK falling edge to output		10ns
$T_{tckftcx}$	Time from TCK falling edge to high impedance		10ns
T_{tckp}	TCK clock period	40ns	-
T_{tckh}	TCK clock high time	20ns	-
T_{tckl}	TCK clock low time	20ns	-
T_{jps}	JTAG PORT setup time	10ns	
T_{jph}	JTAG PORT hold time	8ns	

Other than the power requirements, the following conditions need to be met to use the MSPI configuration mode:

- MSPI port enable

Set RECONFIG_N as “NON-RECOVERY” for the first programming activity after power-up or the previous programming activity.

- Initiate new program

Power-up again or provide one low pulse for programming pin RECONFIG_N.

4.6.2 AUTO BOOT Port Timing Specifications

The AUTOBOOT mode offers an instant-on feature for the GW1N series of FPGA products. In this mode, FPGA reads data from the on-chip Flash directly for the program to load after the chip is powered on.

On-chip Flash is configured via the JTAG interface. After the configuration, RECONFIG_N is triggered by a low level pulse, or auto boot configuration starts after power recycle. Figure 4-9 shows the timing.

Figure 4-9 Power Recycle Timing

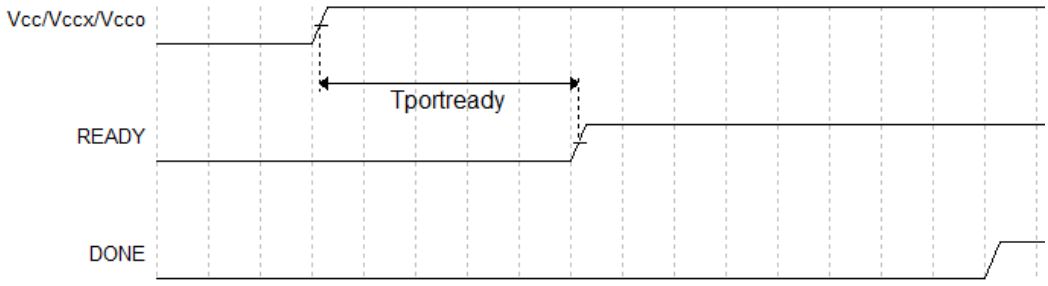


Figure 4-10 RECONFIG_N Trigger Timing

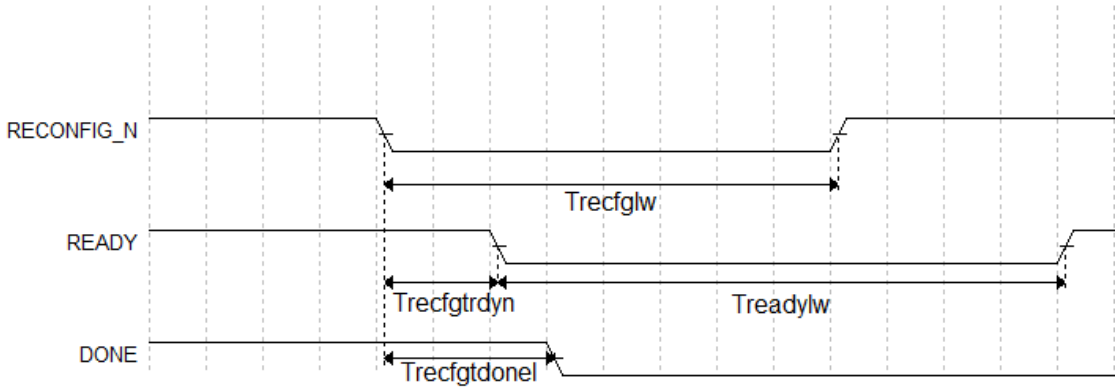


Table 4-23 shows the timing.

Table 4-23 Timing Parameters for Power-on and RECONFIG_N Trigger

Name	Description	Min.	Max.
$T_{portready}$[1]	Time from application of V_{CC}, V_{CCX} and V_{CCO} to the rising edge of READY	50μs	200μs
$T_{recfglw}$	RECONFIG_N low pulse width	25ns	
$T_{recfgtrdyn}$	Time from RECONFIG_N falling edge to READY low	-	70ns
$T_{readylw}$	READY low pulse width	TBD	
$T_{recfgtdonel}$	Time from RECONFIG_N falling edge to DONE low	-	80ns

Note!

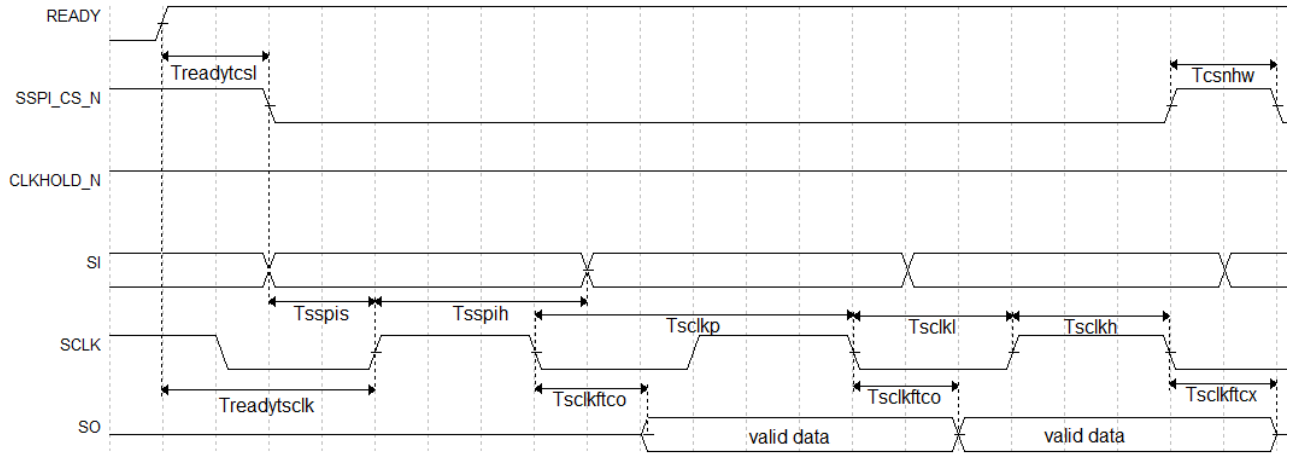
MODE0=0, the device power up waiting time is 200μs; MODE0=1, the device power up waiting time is 50μs.

4.6.3 SSPI Port Timing Specifications

In the slave SSPI mode, the GW1N series of FPGA products are configured by the hardware processer via SPI.

See Figure 4-11 for the SSPI timing diagram.

Figure 4-11 SSPI Timing Diagram



See Table 4-24 for the timing parameters.

Table 4-24 SSPI Timing parameters

Name	Description	Min.	Max.
T_{sclkp}	SCLK clock period	15ns	-
T_{sclkh}	SCLK clock high time	7.5ns	-
T_{sclkl}	SCLK clock low time	7.5ns	-
T_{sspis}	SSPI PORT setup time	2ns	-
T_{sspih}	SSPI PORT hold time	0ns	-
$T_{sclkftco}$	Time from SCLK falling edge to output	-	10ns
$T_{sclkftcx}$	Time from SCLK falling edge to high impedance	-	10ns
T_{csnhw}	CSN high time	25ns	-
$T_{readytcsl}$	Time from READY rising edge to CSN low		
$T_{readytsclk}$	Time from READY rising edge to first SCLK edge	TBD	-

Other than the power requirements, the following conditions need to be met to use the SSPI configuration mode:

- SSPI port enabled

Set RECONFIG_N as “NON-RECOVERY” for the first programming activity after power-up or the previous programming activity.

- Initiate new program

Power-up again or provide one low pulse for programming pin RECONFIG_N.

4.6.4 MSPI Port Timing Specifications

In master MSPI mode, the configuration data is retrieved automatically from the off chip SPI Flash. The default MCLK frequency of the GW1N-1, GW1N-1S, GW1N-6, and GW1N-9 is 2.5 MHz; the default MCLK

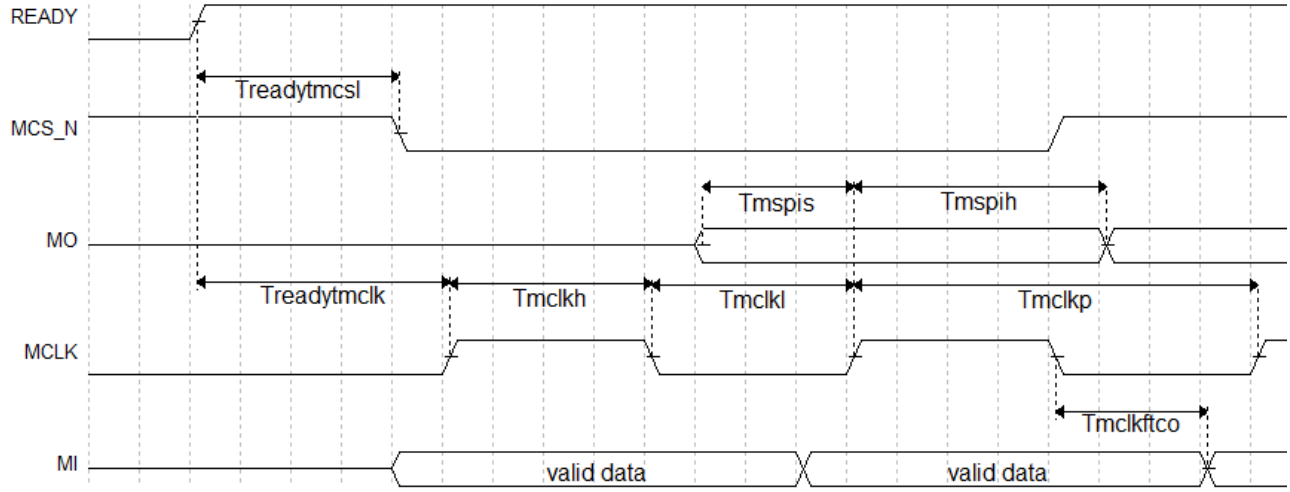
frequency of GW1N-2/2B, GW1N-4/4B is 2.1MHz. The MCLK accuracy is +/- 5%.

After MSPI writes the configuration data to the off-chip Flash, power recycle or RECONFIG_N will trigger device configuration. GW1N-1, GW1N-1S, GW1N-2/2B, and GW1N-4/4B only support one auto MSPI configuration; if fails, power recycle or RECONFIG_N will trigger device configuration.

GW1N-6 and GW1N-9 support multiple auto MSPI configurations; if this fails for the first time, FPGA automatically reads external Flash twice. Users can set the address, and the default address is 0.

See Figure 4-12 for the MSPI Timing Diagram.

Figure 4-12 MSPI Timing Diagram



See Table 4-25 for the MSPI timing diagram.

Table 4-25 MSPI Timing Parameters

Name	Description	Min.	Max.
T_{mclkp}	MCLK clock period	15ns	-
T_{mclkh}	MCLK clock high time	7.5ns	-
T_{mclkl}	MCLK clock low time	7.5ns	-
T_{mspis}	MSPI PORT setup time	5ns	-
T_{mspih}	MSPI PORT hold time	1ns	-
$T_{mclkftco}$	Time from MCLK falling edge to output	-	10ns
$T_{readytmcsl}$	Time from READY rising edge to MCS_N low	100ns	200ns
$T_{readytmclk}$	Time from READY rising edge to first MCLK edge	2.8μs	4.4μs

4.6.5 DUAL BOOT

In DUAL BOOT mode, the configuration data is retrieved automatically from the off-chip Flash or from the on-chip Flash.

GW1N-1, GW1N-1S, GW1N-6, and GW1N-9 products try to configure first from the on-chip Flash memory. If there is no data in the on-chip Flash or the configuration fails, the device attempts to configure from the off-chip Flash memory. If that fails too, the device cannot work. In addition, GW1N-6 and GW1N-9 devices also support to preferentially start from the external Flash. When the external Flash fails to configure, the device chooses to read the data stored on the built-in Flash for configuration. When the external Flash is empty, the device will not be configured.

GW1N-6 and GW1N-9 devices support multiple times configuration no matter starting from the off-chip Flash or from the on-chip Flash: the preferred store path can be started for three times; if those all fails, the other path will be employed for configuration. You can start internal Flash only from address 0, but for external Flash start, you can try three different start addresses.

See *DUAL BOOT Download Solution based on GW1N-4 Device* for the DUAL BOOT Config Mode implementation of GW1N-2/2B and GW1N-4/4B.

4.6.6 CPU

In CPU mode, the GW1N series of FPGA products are configured by hardware processor via DBUS interface. Other than the power requirements, the following conditions need to be met to use the CPU configuration mode:

- CPU port enable
  Set RECONFIG_N as “NON-RECOVERY” for the first programming after power up or the previous programming.
- Initiate new program
  Power recycle or provide one low pulse for programming pin RECONFIG_N.

4.6.7 SERIAL

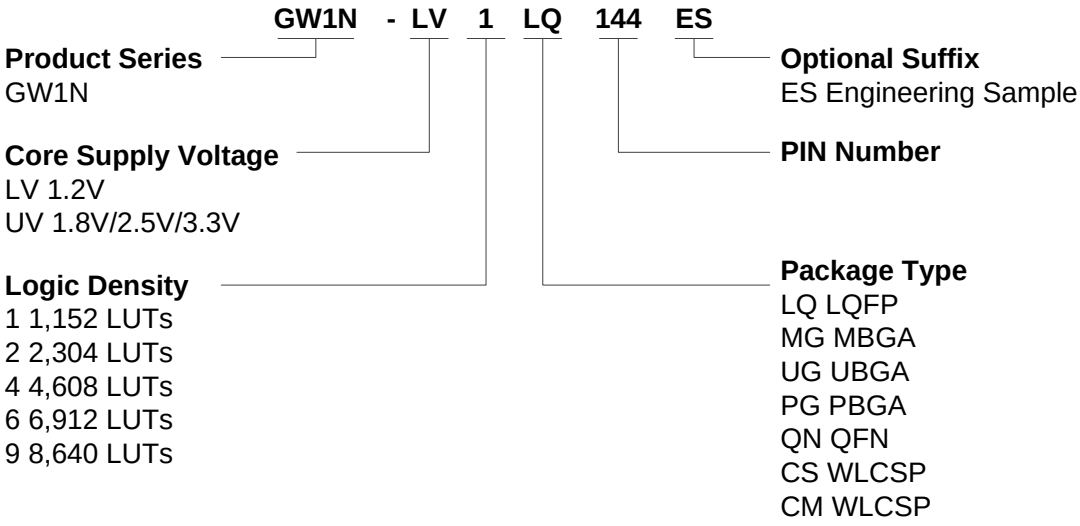
In SERIAL mode, the GW1N series of FPGA products are configured by hardware processor via serial interface. Other than the power requirements, the following conditions need to be met to use the SERIAL configuration mode:

- SERIAL port enable
  Set RECONFIG_N as “NON-RECOVERY” for the first programming activity after power-up or the previous programming activity.
- Initiate new program
  Power recycle or provide one low pulse for programming pin RECONFIG_N.

5 Ordering Information

5.1 Part Name

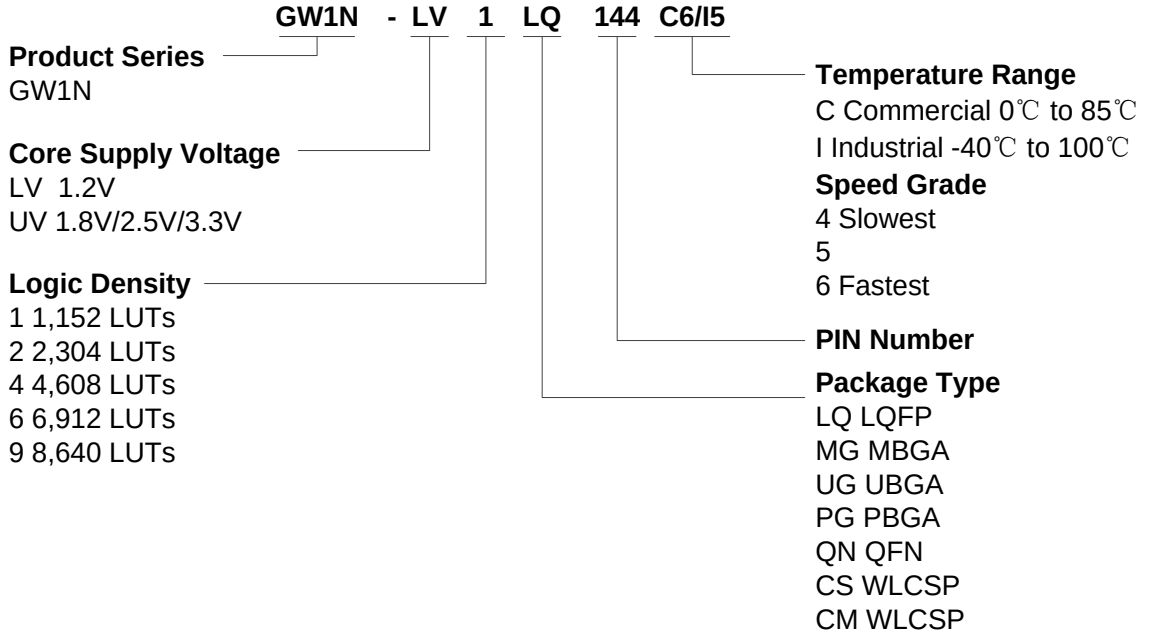
Figure 5-1 Part Naming–ES



Note!

- GW1N-1 and GW1N-1S parts support LV only;
- For the further detailed information about the device resources and packages, please refer to 2.2 Product Resources and 2.3 Package Information.

Figure 5-2 Part Naming–Production



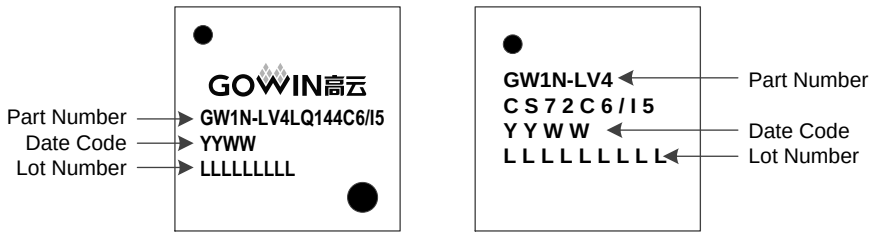
Note!

- GW1N-1 and GW1N-1S parts support LV only.
- Speed grade is used for both LV and UV.
- For the further detailed information about the device resources and packages, please refer to 2.2 Product Resources and 2.3 Package Information.

5.2 Package Mark

The device information is marked on the chip surface, as shown in Figure 5-3.

Figure 5-3 Package Mark



Note!

- The first two lines in the right figure above are the "Part Number"
- The third line in the right figure above is the "Date Code". The Data Code for B version devices ends with a "B".