GOWIN
PROGRAMMING FOR THE FUTURE

GW1NZ series of FPGA Products

Datasheet

DS841-1.6E,06/30/2020

Disclaimer

Revision History

Date	Version	Description
01/23/2019	1.0E	Initial version published.
02/12/2019	1.1E	Figures of part naming updated.
04/03/2019	1.2E	● I/O BANK view updated; ● The description of I3C bus and SPMI added; the precision of the on chip OSC added; ● Changerd “Operating Temperature” to “Junction Temperature”.
09/25/2019	1.3E	● The note of “GW1NZ-1 I/Os support differential output, rather than differential input” added; ● Power supply ramp rate modified.
11/06/2019	1.4E	Number of Max. I/O updated.
01/06/2020	1.5E	● The static current of ZV devices added; ● Low power description of user flash added.
06/30/2020	1.6E	GW1NZ-1 FN32F added.

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1 About This Guide

1.1 Purpose

This data sheet describes the features, product resources and structure, AC/DC characteristics, timing specifications of the configuration interface, and the ordering information of the GW1NZ series of FPGA product. It is designed to help you understand the GW1NZ series of FPGA products quickly and select and use devices appropriately.

1.2 Related Documents

The latest user guides are available on the GOWINSEMI Website. You can find the related documents at www.gowinsemi.com:

1. DS841, GW1NZ series of FPGA Products Data Sheet
2. UG290, Gowin FPGA Products Programming and Configuration User Guide
3. UG843, GW1NZ series of FPGA Products Package and Pinout
4. UG842, GW1NZ-1 Pinout

1.3 Abbreviations and Terminology

The abbreviations and terminology used in this manual are as shown in Table 1-1 below.

Table 1-1 Abbreviations and Terminologies

Abbreviations and Terminology	Full Name
FPGA	Field Programmable Gate Array
CFU	Configurable Functional Unit
CLS	Configurable Logic Slice
CRU	Configurable Routing Unit
LUT4	Four-input Look-up Table
LUT5	Five-input Look-up Tables
LUT6	Six-input Look-up Tables
LUT7	Seven-input Look-up Tables
LUT8	Eight-input Look-up Tables
REG	Register
ALU	Arithmetic Logic Unit
IOB	Input/output Bank
B-SRAM	Block SRAM
SP	Signal Port
SDP	Semi Dual Port
DP	Dual Port
DQCE	Dynamic Quadrant Clock Enable
DCS	Dynamic Clock Selector
PLL	Phase Locked Loop
SPMI	System Power Management Interface
GPIO	Gowin Programmable IO
CS30	WLCSP30
FN32	QFN32
LQ100	LQFP100
LQ144	LQFP144
MG160	MBGA160
PG204	PBGA204

1.4 Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

Website: www.gowinsemi.com

E-mail: support@gowinsemi.com

2 General Description

The GW1NZ series of FPGA products are the first generation products in the LittleBee® family. They offer ultra-low power consumption, instant on, low cost, non-volatile, high security, various packages, and flexible usage. They can be widely used in communication, industry control, consumer, video control, etc.

GOWINSEMI provides a new generation of FPGA hardware development environment through market-oriented independent research and development that supports the GW1NZ series of FPGA products and applies to FPGA synthesizing, layout, place and routing, data bitstream generation and download, etc.

2.1 Features

- Zero power consumption
  - 55nm embedded flash technology
  - LV: Supports 1.2V core voltage
  - ZV: Supports 0.9V core voltage. Please refer to Table 4-10 Static Supply Current (ZV Device) for the lowest power consumption.
  - Power Management Module
  - Clock dynamically turns on and off
  - User Falsh dynamically turns on and off
- Power Management Module
  - SPMI: System power management interface
  - VCC and VCCM are independent in the device
- User Flash
  - Dynamically turns on and off
  - 64K bits
  - Data Width: 32
  - 10,000 write cycles
  - Greater than ten years' data retention at +85 ℃
  - Supports page erasure: 2048 bytes per page
  - Duration: Max. 25ns
  - Electric current
    a). Read Operation: 2.19 mA/25 ns (V_{CC}) & 0.5 mA/25 ns (V_{CCX}) (MAX);
    b). Write operation/erase operation: 12/12 mA (MAX)

  - Quick page erasure/Write operation
  - Clock frequency: 40MHz
  - Write operation time: ≤16μs
  - Page erasure time: ≤120 ms
- Multiple I/O Standards
  - LVCMOS33/25/18/15/12;LVTTL33; PCI;
  - LVDS25E, BLVDSE, MLVDSE, LVPECLE, RSDSE
  - Input hysteresis option
  - Supports 4mA,8mA,16mA,24mA,etc. drive options
  - Slew Rate option
  - Output drive strength option
  - Individual Bus Keeper, Weak Pull-up, Weak Pull-down, and Open Drain option
  - Hot Socket
  - I3C hard core, supports SDR mode
  - Support differential output, rather than differential input
- Abundant Slices
  - Four input LUT (LUT4)
  - Double-edge flip-flops
  - Supports shifter register
  - Supports shadow SRAM
- Block SRAM with multiple modes
  - Supports Dual Port, Single Port, and Semi Dual Port
  - Supports bytes write enable
- Flexible PLLs
  - Frequency adjustment (multiply and division) and phase adjustment
  - Supports global clock
- Built-in Flash programming
  - Instant-on
  - Supports security bit operation
  - Supports AUTO BOOT and DUAL BOOT
- Configuration
  - JTAG configuration
  - Offers up to six GowinCONFIG configuration modes: AUTOBOOT, SSPI, MSPI, CPU, SERIAL, DUAL BOOT

2.2 Product Resources

Table 2-1 Product Resources

Device	GW1NZ-1
LUT4	1,152
Flip-Flop (FF)	864
Shadow SRAM S-SRAM (bits)	4K
Block SRAM B-SRAM (bits)	72K
PLLs	1
User Flash (bits)	64K
Max. I/O	48
V_{CC}	1.2V(LV); 0.9V(ZV)

2.3 Package Information

Table 2-2 Package Information and Max. User I/O

Package	Pitch (mm)	Size (mm)	GW1NZ-1
FN32	0.4	4 x 4	25
FN32F	0.4	4 x 4	25
CS16	0.4	1.8 x 1.8	11
QN48	0.4	6 x 6	40

Note!

- In this manual, abbreviations are employed to refer to the package types. See 5.1 Part Name.
- The JTAGSEL_N and JTAG pins cannot be used as I/O simultaneously. The data in this table is when the loaded four JTAG pins (TCK, TDI, TDO, and TMS) are used as I/O. When mode [2:0] = 001, JTAGSEL_N and the four JTAG pins (TCK, TDI, TDO, and TMS) can be used as GPIO simultaneously, and the Max. user I/O plus one.

3 Architecture

3.1 Architecture Overview

Figure 3-1 GW1NZ Architecture Overview

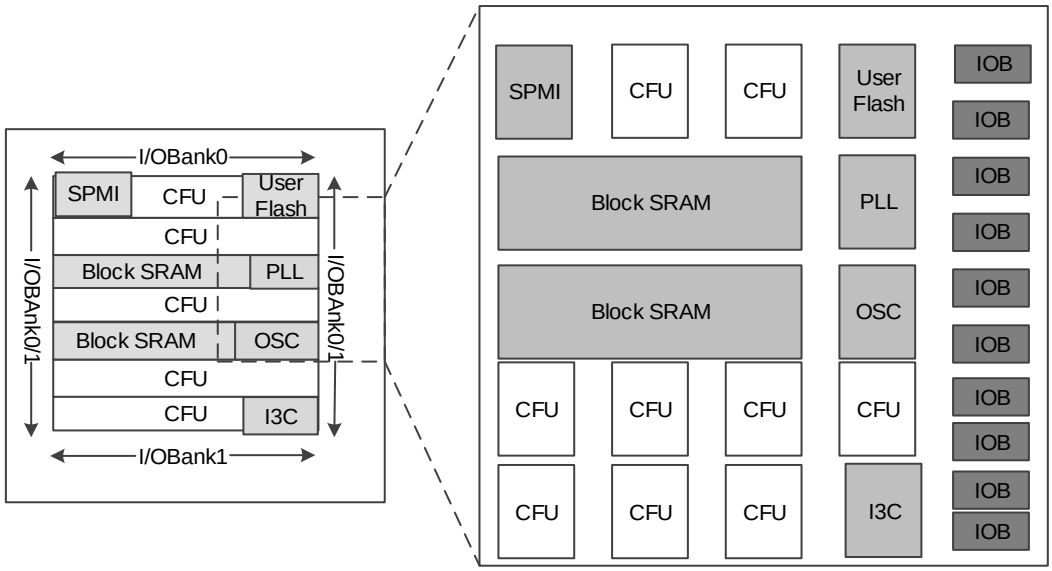


Figure 3-1 shows the GW1NZ devices architecture view.The core of the GW1NZ devices is the array of configurable logic unit (CFU) surrounded by IO blocks. GW1NZ also provides B-SRAM, DSP, PLL, user Flash, and on chip oscillator and supports Instant-on. SPMI and I3C are also embedded in the GW1NZ devices. See Table 2-1 for more detailed information on internal resources.

Configurable Function Unit (CFU) is the base cell for the array of the GW1NZ series of FPGA Products. These CFUs arrange in rows and columns. CFU can be configured as LUT4 mode, ALU mode, and memory mode. See 3.2Configurable Function Unit for further detailed information.

The I/O resources in the GW1NZ series of FPGA products are arranged around the periphery of the devices in groups referred to as banks, including Bank0 and Bank1. The I/O resources support multiple level standards, and support basic mode, SRD mode, and generic DDR mode. See 3.3IOB for further detailed information.

The B-SRAM is embedded as a row in the GW1NZ series of FPGA

products. In the FPGA array, each B-SRAM occupies three columns of CFU. Each B-SRAM has 18,432 bits (18 Kbits) and supports multiple configuration modes and operation modes. See 3.6Block SRAM (B-SRAM) for further detailed information.

The User Flash is embedded in the GW1NZ series of FPGA products, without loss of data even if power off. See Table 2-1 for further detailed information. See 3.7User Flash for further detailed information.

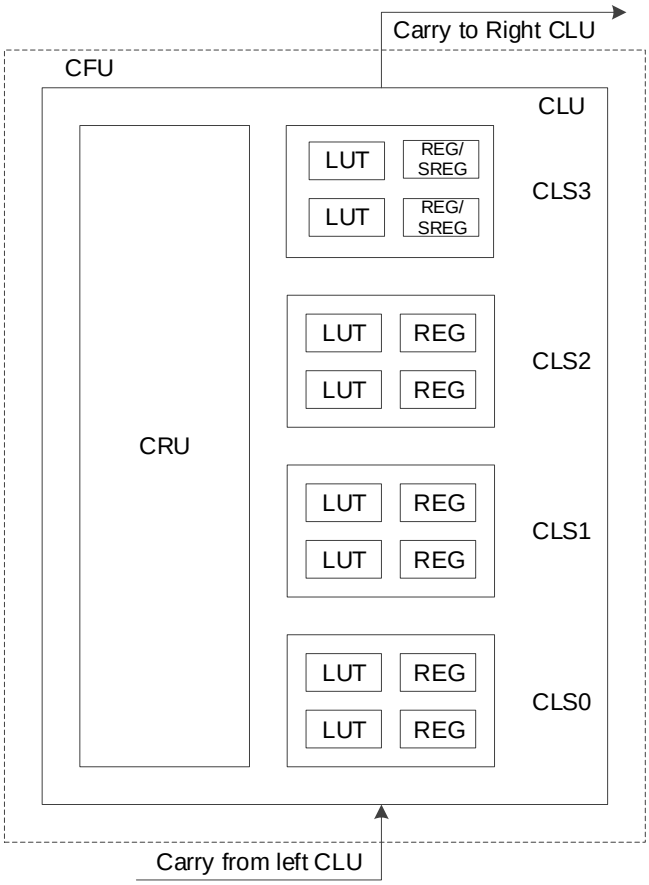
GW1NZ provides one PLL. PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted using the configuration of parameters. See 3.8Clock for further detailed information.

FPGA provides abundant CRUs, connecting all the resources in FPGA. For example, routing resources distributed in CFU and IOB connect resources in CFU and IOB. Routing resources can automatically be generated by Gowin software. In addition, the GW1NZ series of FPGA Products also provide abundant GCLKs, long wires (LW), global set/reset (GSR), and programming options, etc. See 3.9Long Wire (LW), 3.10Global Set/Reset (GSR), 3.11Programming Configuration for further detailed information.

3.2 Configurable Function Unit

The configurable function unit (CFU) is the base cell for the array of the GW1NZ series of FPGA Products. Each CFU consists of a configurable logic unit (CLU) and its routing resource configurable routing unit (CRU). In each CLU, there are four configurable logic slices (CLS). Each CLS contains look-up tables (LUT) and registers, as shown in Figure 3-2 below.

Figure 3-2 CFU View



Note!

SERG needs special patch supporting. Please contact Gowin technical support or local O ffice for this patch.

3.2.1 Look-up Table

The CLU supports three operation modes: Basic logic mode, ALU mode, and ROM mode.

- Basic Logic Mode

Each LUT can be configured as one four-input LUT. Higher input number of LUT can be formed by combining the LUT4 together.

  - Each CLS can form one five-input LUT5.
  - Two CLSs can form one six-input LUT6.
  - Four CLSs can form one seven-input LUT7.
  - Eight CLSs (two CLUs) can form one eight-input LUT8.

- ALU Mode

When combined with carry chain logic, the LUT can be configured as the ALU mode to implement the following functions.

  - Adder and subtractor
  - Up/down counter
  - Comparator,including greater-than, less-than, and not-equal-to
  - MULT

- Memory mode
  In this mode, a 16 x 4 S-SRAM or ROM can be constructed by using CLSs.
- This SRAM can be initialized during the device configuration stage. The initialization data can be generated in the bit stream file from Gowin Yunyuan software.

3.2.2 Register

Each configurable logic slice (CLS) has two registers (REG), as shown in Figure 3-3 below.

Figure 3-3 Register in CFU

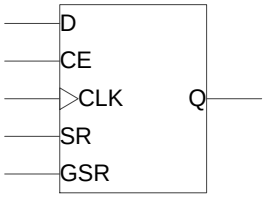


Table 3-1 Register Description in CFU

Signal	I/O	Description
D	I	Data input [1]
CE	I	CLK enable, can be high or low effective [2]
CLK	I	Clock, can be rising edge or falling edge trigging [2]
SR	I	Set/Reset, can be configured as [2]: ● Synchronized reset ● Synchronized set ● Asynchronous reset ● Asynchronous set ● Non
GSE[3,4]	I	Global Set/Reset, can be configured as[4]: ● Asynchronous reset ● Asynchronous set ● Non
Q	O	Register

Note!

- [1] The source of the signal D can be the output of a LUT, or the input of the CRU; as such, the register can be used alone when LUTs are in use.
- [2] CE/CLK/SR in CFU is independent.
- [3] In the GW1NZ series of FPGA products, GSR has its own dedicated network.
- [4] When both SR and GSR are effective, GSR has higher priority.

3.2.3 CRU

The main functions of the CRU are as follows:

- Input selection: Select input signals for the CFU.
- Configurable routing: Connect the input and output of the CFUs, including inside the CFU, CFU to CFU, and CFU to other functional blocks in FPGA.

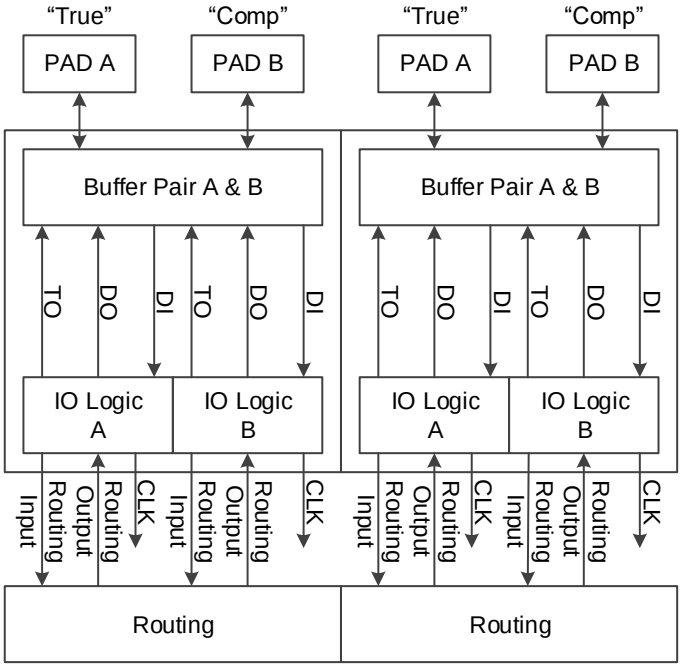
3.3 IOB

The IOB in the GW1NZ series of FPGA products includes IO buffer, IO logic, and its routing unit. As shown in Figure 3-4, each IOB connects to two Pins (Marked as A and B). As input, they can be used as a single-end signal; as output, they can be used as an output differential pair or as a single end input/output.

Note!

GW1NZ-1 I/Os support differential output, rather than differential input.

Figure 3-4 IOB Structure View



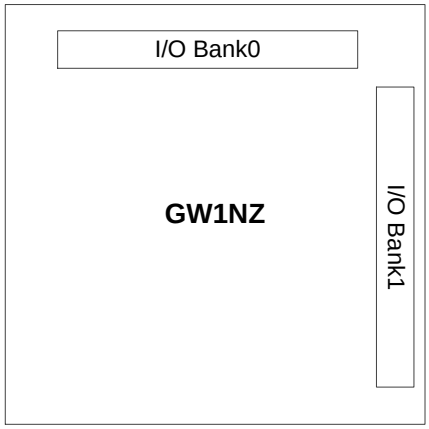
IOB Features:

- VCCO supplied with each bank
- Supports multiple levels: LVCMOS, PCI, LVTTL, etc.
- Input hysteresis option
- Output drive strength option
- Slew Rate option
- Individual Bus Keeper, Weak Pull-up, Weak Pull-down, and Open Drain option
- Hot Socket
- IO Logic supports basic mode, SRD mode, and generic DDR mode
- I3C hard core embedded, supports SDR mode
- Supports differential output, rather than differential input

3.3.1 I/O Buffer

GW1NZ series of FPGA products include Bank0 and Bank1, as shown in Figure 3-5. V_{CCO} can be 3.3V, 2.5V, 1.8V, 1.5V, or 1.2V.

Figure 3-5 I/O Bank Distribution of GW1NZ series of FPGA Products



GW1NZ series FPGA products contain both LV and UV. LV devices support 1.2V core voltage to meet users' low power needs. ZV devices support 0.9V core voltage. Zero-power consumption can be available for ZV devices. VCCO supplied with I/O Bank can be set as 1.2V, 1.5V, 1.8V, 2.5V, or 3.3V according to requirements. V_{CCX} supports 1.8V, 2.5 V, and 3.3 V power supply.

Note!

By default, the Gowin Programmable IO is tri-stated weak pull-up.

For the V_{CCO} requirements of different I/O standards, see Table 3-2.

Table 3-2 Output I/O Standards and Configuration Options

I/O output standard	Single/Differ	Bank V_{CCO} (V)	Driver Strength (mA)
LVTTL33	Single end	3.3	4,8,12,16,24
LVCMOS33	Single end	3.3	4,8,12,16,24
LVCMOS25	Single end	2.5	4,8,12,16
LVCMOS18	Single end	1.8	4,8,12
LVCMOS15	Single end	1.5	4,8
LVCMOS12	Single end	1.2	4,8
PCI33	Single end	3.3	N/A
LVPECL33E	Differential	3.3	16
MLVDS25E	Differential	2.5	16
BLVDS25E	Differential	2.5	16
RSDS25E	Differential	2.5	8
LVDS25E	Differential	2.5	8

Table 3-3 Output I/O Standards and Configuration Options

I/O Input Standard	Single/Differ	Bank V_{CCO} (V)	Hysteresis	Need V_{REF}
LVTTL33	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS33	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS25	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS18	Single end	1.5/1.8/2.5/3.3	Yes	No
LVCMOS15	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
LVCMOS12	Single end	1.2/1.5/1.8/2.5/3.3	Yes	No
PCI33	Single end	3.3	Yes	No

3.3.2 I/O Logic

Figure 3-6 shows the I/O logic output of the GW1NZ series of FPGA products.

Figure 3-6 I/O Logic Output

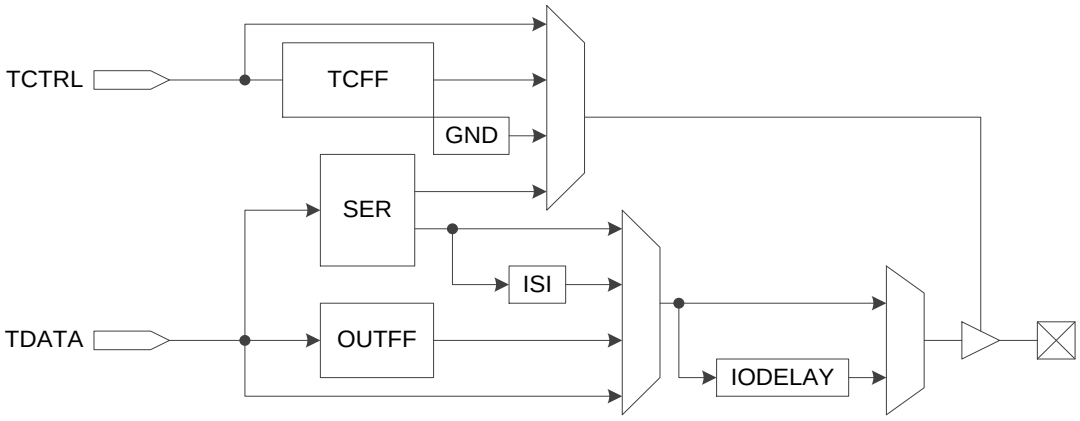
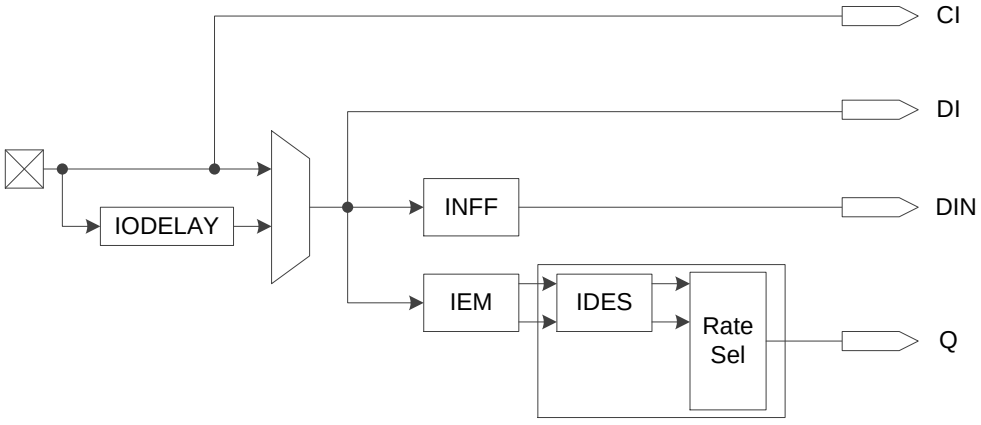


Figure 3-7 shows the I/O logic input of the GW1NZ series of FPGA products.

Figure 3-7 I/O Logic Input

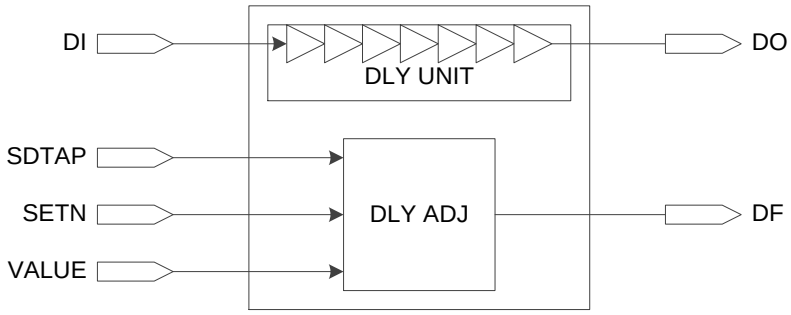


A description of the I/O logic modules of the GW1NZ series of FPGA products is presented below:

IODELAY

See Figure 3-8 for an overview of the IODELAY. Each I/O of the GW1NZ series of FPGA products has an IODELAY cell. A total of 128(0~127) step delay is provided, with one-step delay time of about 30ps.

Figure 3-8 IODELAY



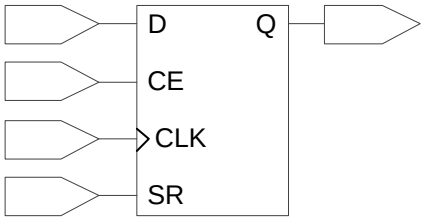
There are two ways to control the delay cell:

- Static control
- Dynamic control: usually used to sample delay window together with IEM. The IODELAY cannot be used for both input and output at the same time

I/O Register

See Figure Figure 3-9 for the I/O register in the GW1NZ series of FPGA products. Each I/O provides one input register, INFF, one output register, OUTFF, and a tristate Register, TCFF.

Figure 3-9 Register Structure in I/O Logic



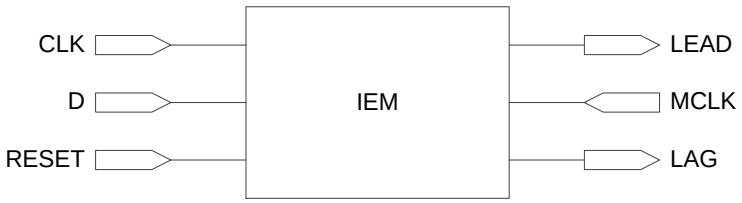
Note!

- CE can be either active ow (0: enable)or active high (1: enable).
- CLK can be either rising edge trigger or falling edge trigger.
- SR can be either synchronous/asynchronous SET or RESET or disable.
- The register can be programmed as register or latch.

IEM

IEM is for sampling clock edge and is used in the generic DDR mode, as shown in Figure 3-10.

Figure 3-10 IEM Structure



De-serializer DES and Clock Domain Transfer

The GW1NZ series of FPGA products provide a simple DES for each input I/O to support advanced I/O protocols.

Serializer SER

The GW1NZ series of FPGA products provide a simple Serializer SER for each output I/O to support advanced I/O protocols.

3.3.3 I/O Logic Modes

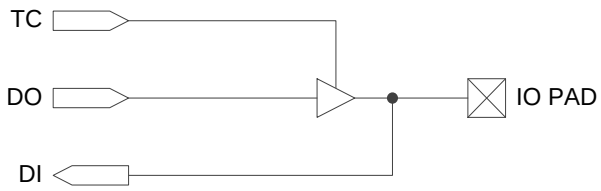
The I/O Logic in the GW1NZ series of FPGA products supports several modes. In each operation, the I/O can be configured as output, input, and INOUT or tristate output (output signal with tristate control).

The GW1NZ-1 pins IOR6 (A,B,C….J) do not support IO logic.

Basic Mode

In basic mode, the I/O Logic is as shown in Figure 3-11, and the TC, DO, and DI signals can connect to the internal cores directly through CRU.

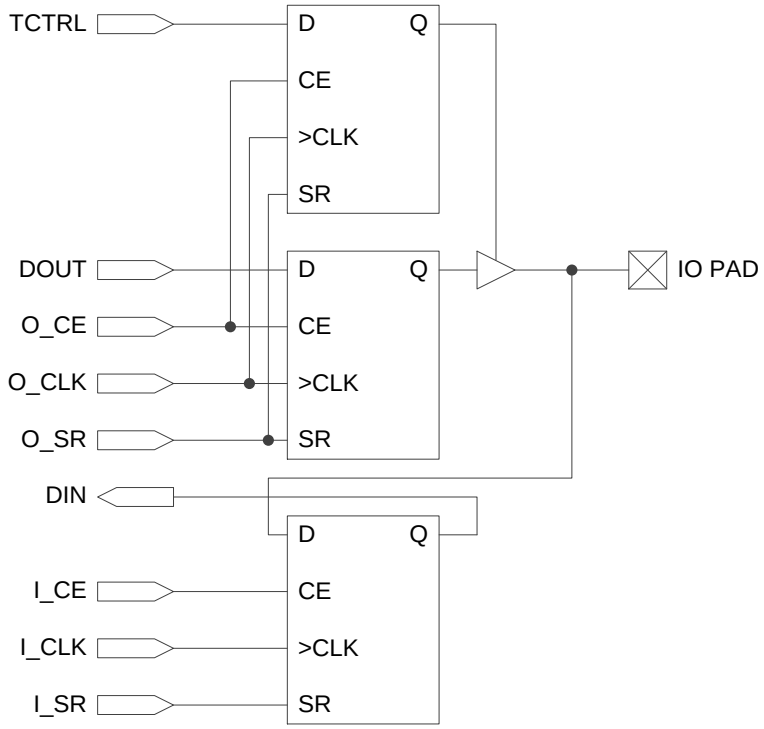
Figure 3-11 I/O Logic in Basic Mode



SDR Mode

In comparison with the basic mode, SDR utilizes the IO register, as shown in Figure 3-12. This can effectively improve IO timing.

Figure 3-12 I/O Logic in SDR Mode



Note!

- CLK enable O_CE and I_CE can be configured as active-high or active-low.
- O_CLK and I_CLK can be either rising edge trigger or falling edge trigger.
- Local set/reset signal O_SR and I_SR can be synchronized reset, synchronized set, asynchronous reset, asynchronous set, or no-function.
- I/O in SDR mode can be configured as basic register or latch.

Generic DDR Mode

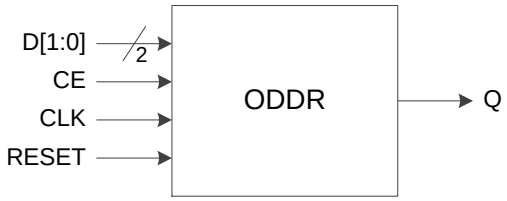
Higher speed I/O protocols can be supported in generic DDR mode.

Figure 3-13 shows generic DDR input, with the speed ratio of internal logic to PAD 1:2.

Figure 3-13 I/O Logic in DDR Input Mode

Figure 3-14 shows generic DDR output, with a speed ratio of PAD to FPGA internal logic 2:1.

Figure 3-14 I/O Logic in DDR Output Mode



IDES4

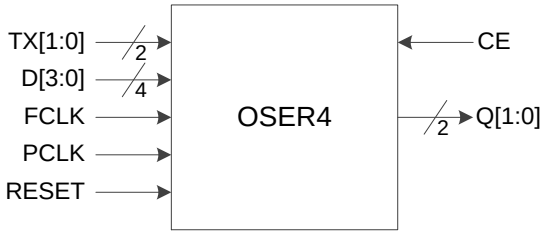
In IDES4 mode, higher I/O speed signals can be supported. The frequency of input signal (D) and the signal Q which is transferred to Pin has a ratio of 4:1.

Figure 3-15 I/O Logic in IDES10 Mode

OSER4 Mode

In OSER4 mode, higher speed signals can be supported. The frequency of input signal (D) and the signal Q which is transferred to Pin has a ratio of 4:1.

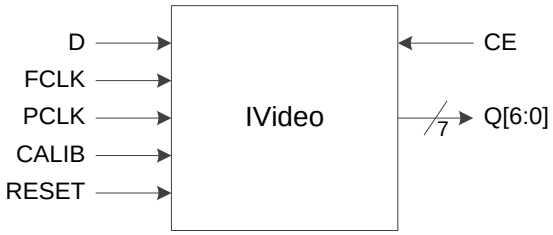
Figure 3-16 I/O Logic in OSER4 Mode



IVideo Mode

In IVideo mode, higher speed signals can be supported. The signal (D) frequency at the input of this block vs the signal Q which is transferred to core has a ratio of 7:1.

Figure 3-17 I/O Logic in IVideo Mode



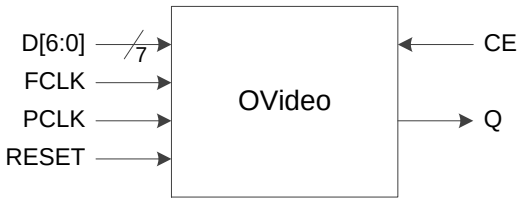
Note!

IVideo and IDES8/10 will occupy the neighboring I/O logic. If the I/O logic of a single port is occupied, the pin can only be programmed in SDR or BASIC mode.

OVideo Mode

In OVideo mode, higher speed signals can be supported. The signal (D) frequency at the input of this block vs the signal Q which is transferred to core has a ratio of 7:1.

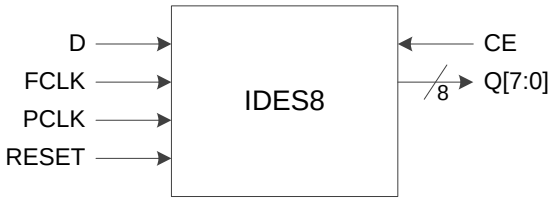
Figure 3-18 I/O Logic in OVideo Mode



IDES8 Mode

In IDES8 mode, higher I/O speed signals can be supported. The signal (D) frequency at the input of this block vs the signal Q which is transferred to Pin has a ratio of 1:8.

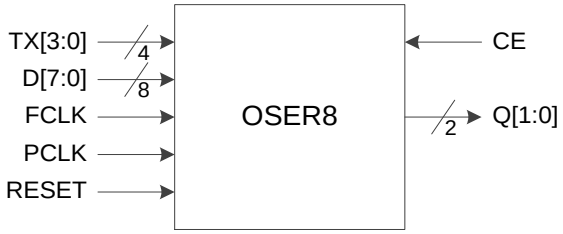
Figure 3-19 I/O Logic in IDES8 Mode



OSER8 Mode

In OSER8 mode, higher I/O speed signals can be supported. The signal (D) frequency at the input of this block vs the signal Q which is transferred to Pin has a ratio of 1:8.

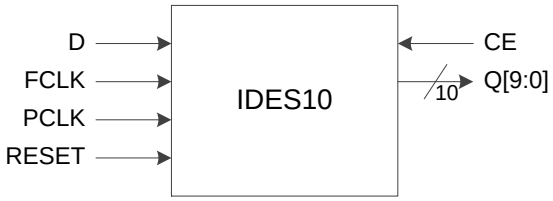
Figure 3-20 I/O Logic in OSER8 Mode



IDES10 Mode

In IDES10 mode, higher I/O speed signals can be supported. The signal (D) frequency at the input of this block vs the signal Q which is transferred to Pin has a ratio of 1:10.

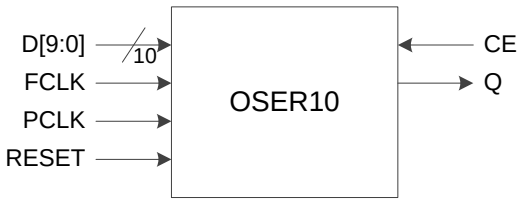
Figure 3-21 I/O Logic in IDES10 Mode



OSER10 Mode

In OSER10 mode, higher I/O speed signals can be supported. The signal (D) frequency at the input of this block vs the signal Q which is transferred to Pin has a ratio of 1:10.

Figure 3-22 I/O Logic in OSER10 Mode



3.4 I3C Bus

3.4.1 Overview

GW1NZ series of FPGA products includes a hard core of I3C bus controller, which supports SDR mode. The I3C controller is backwards compatible with I2C features low power, and is high speed and extensible. The I3C bus is compliant with MIPI I3C protocol, adopts register interfaces, and supports operation modes of I3C SDR Master and I3C SDR Slave.

I3C SDR Master

- Compliance with MIPI I3C protocol;
- Supports I3C address arbitration detection;
- Supports Single Data Rate (SDR) mode;
- The max. data transmission rate can up to 12.5Mbps;
- Start / Stop / Repeated Start / Acknowledge generation;
- Start / Stop / Repeated Start detection;
- Support dynamically allocating address via SETDASA or ENTDAA;
- Supports Receive/Send data;
- Supports In-band Interrupts;
- Supports Hot-Join;
- Supports dynamically allocating address when hot-join;
- Supports CCC's command;
- Supports dynamic adjusting SCL frequency;
- Compatible with I2C Slave;
- Adopts register interfaces.

I3C SDR Slave

- Compliance with MIPI I3C protocol;
- Start / Acknowledge generation;
- Start / Stop / Repeated Start detection;
- Support dynamically allocating address via SETDASA or ENTDAA;
- Receive/Send data;
- Send an IBI or hot-join request. If more than one slaves send the IBI or hot-join requests, the min. address obtains the arbitration;
- Static address of Slave configuration;
- Adopts register interfaces.

3.4.2 Port Signal

For the detailed information about I3C port signals, working principle, timing, and examples, please refer to *IPUG508-1.2_Gowin I3C SDR IP User Guide*.

Table 3-4 I3C Port Signals

Port Name	I/O	Description
AAC	Input	The setting to clear ACK response, single pulse signal
AAO	output	Output ACK signal
AAS	Input	Set ACK response, single pulse signal
ACC	Input	The setting to clear continuous operation mode, single pulse signal
ACKHS	Input	Set ACK high-level time
ACKLS	Input	Set ACK low-level time
ACO	output	Continuous operation mode output
ACS	Input	Set continuous operation mode, single pulse signal
ADDRS	Input	Set slave address
CE	Input	Clock enable signal
CLK	Input	Clock input
CMC	Input	Clear the current Master role, single pulse signal
CMO	output	Output the flag of current master role
CMS	Input	Set the current Master role, single pulse signal
DI[7:0]	Input	Data input
DO[7:0]	output	Data output
DOBUF[7:0]	output	Buffer data output
LGYC	Input	Clear the setting of I2C as the current communication object, single pulse signal
LGYO	output	Output of I2C as the current communication object
LGYS	Input	Set I2C as the current communication object, single pulse signal
PARITYERROR	output	Parity error signal
RECVDHS	Input	Set high-level time of receiving data
RECVDLS	Input	Set low-level time of receiving data
RESET	Input	Asynchronous reset, active high
SCLI	Input	I3C serial clock input
SCLO	output	I3C serial clock line
SCLOEN	output	I3C serial clock output enable
SCLPULLO	output	I3C serial clock pullup output
SCLPULLOEN	output	I3C serial clock pullup output enable
SDAI	Input	I3C serial data input
SDAO	output	I3C serial data output
SDAOEN	output	I3C serial data output enable
SDAPULLO	output	I3C serial data pullup output
SDAPULLOEN	output	I3C serial data pullup output enable

Port Name	I/O	Description
SENDAHS	Input	Set high-level time of sending address
SENDALS	Input	Set low-level time of sending address
SENDDHS	Input	Set high-level time of sending data
SENDDLS	Input	Set low-level time of sending data
SIC	Input	Signal of clearing interrupt flag
SIO	output	Signal of output signal interrupt
STRTC	Input	Setting of clearing the START command, single pulse signal
STRTO	output	Output START command
STRTS	Input	Set START command, single pulse signal
STATE	output	Output internal state
STRTHDS	Input	Set the holding time of the START command
STOPC	Input	Clear the STOP command setting, single pulse signal
STOPO	output	Output the STOP command
STOPS	Input	Set the STOP command, single pulse signal
STOPSUS	Input	Set the setting time of the STOP command
STOPHDS	Input	Set the holding time of the STOP command

3.5 SPMI

3.5.1 Overview

The GW1NZ series of FPGA products provides SPMI and the SPMI controller IP. As a Master, the GW1NZ device supports for the power management of the external Slave devices via the SPMI interface. As a Slave, it also supports for the FPGA power management.

The GW1NZ series of FPGA products supports two ways to control the main power:

- Using hardware I/O VCCEN: The main power is turned off when VCCEN is 0. The main power is on when VCCEN is 1;
- Sending the command of shut down by Master: Master sends reset / sleep / wakeup to recover FPGA main power. The main power can also be recovered at low pulse of SPMI_EN.

Note!

For the detailed information of operation modes, communication modes, commands, and timing, etc, please refer to *IPUG529, Gowin SPMI User Guide*.

3.5.2 Port Signal

Table 3-5 SPMI Port Signal

Name	I/O	Description
SPMI_EN	input	SPMI enable signal
SPMI_CLK	intput	System clock signal
SPMI_SCLK	inout	SPMI serial clock signal
SPMI_SDATA	inout	SPMI serial data signal

3.6 Block SRAM (B-SRAM)

3.6.1 Introduction

GW1NZ series FPGA products provide abundant SRAM. The Block SRAM (B-SRAM) is embedded as a row in the FPGA array and is different from S-SRAM (Shadow SRAM). Each B-SRAM occupies three columns of CFU in the FPGA array. Each B-SRAM has 18,432 bits (18Kbits). There are five operation modes: Single Port, Dual Port, Semi-dual Port, ROM, and FIFO. Table 3-6 lists the signals and functional descriptions of B-SRAM.

An abundance of B-SRAM resources provide a guarantee for the user's high-performance design. B-SRAM features:

- Max.18,432 bits per B-SRAM
- B-SRAM itself can run at 170MHz at max (typical, Read-before-write is 100MHz)
- Single Port
- Dual Port
- Semi-dual Port
- Parity bits
- ROM
- Data width from 1 to 36 bits
- Mixed clock mode
- Mixed data width mode
- Enable Byte operation for double byte or above
- Normal read and write mode
- Read-before-write mode
- Write-through Mode

Table 3-6 B-SRAM Signals

Port Name	I/O	Description
DIA	Input	Port A data input
DIB	Input	Port B data input
ADA	Input	Port A address
ADB	Input	Port B address
CEA	Input	Clock enable, Port A
CEB	Input	Clock enable, Port B
RESETA	Input	Register reset, Port A
RESETB	Input	Register reset, Port B
WREA	Input	Read/write enable, Port A
WREB	Input	Read/write enable, Port B
BLKSELA, BLKSELB	Input	Block select
CLKA	Input	Read/write cycle clock for Port A input registers
CLKB	Input	Read/write cycle clock for Port B input registers
OCEA	Input	Output enable for Port A registers
OCEB	Input	Output enable for Port B registers
DOA	Output	Port A data output
DOB	Output	Port B data output

3.6.2 Configuration Mode

The B-SRAM mode in the GW1NZ series of FPGA products supports different data bus widths. See Table 3-7.

Table 3-7 Memory Size Configuration

Single Port Mode	Dual Port Mode	Semi-Dual Port Mode
16K x 1	16K x 1	16K x 1
8K x 2	8K x 2	8K x 2
4K x 4	4K x 4	4K x 4
2K x 8	2K x 8	2K x 8
1K x 16	1K x 16	1K x 16
512 x 32	-	512 x 32
2K x 9	2K x 9	2K x 9
1K x 18	1K x 18	1K x 18
512 x 36	-	512 x 36

Single Port Mode

In the single port mode, B-SRAM can write to or read from one port at one clock edge. During the write operation, the data can show up at the output of B-SRAM. Normal-Write Mode and Write–through Mode can be supported. When the output register is bypassed, the new data will show at

the same write clock rising edge.

For further information about Single Port Block Memory ports and the related description, please refer to SUG283E, Gowin Primitives User Guide > 3 Memory.

Dual Port Mode

B-SRAM support dual port mode. The applicable operations are as follows:

- Two independent read
- Two independent write
- An independent read and an independent write at different clock frequencies

For further information about Dual Port Block Memory ports and the related description, please refer to SUG283E, Gowin Primitives User Guide > 3 Memory.

Semi-Dual Port Mode

Semi-Dual Port supports read and write at the same time on different ports, but it is not possible to write and read to the same port at the same time. The system only supports write on Port A, read on Port B.

For further information about Semi-Dual Port Block Memory ports and the related description, please refer to SUG283E, Gowin Primitives User Guide > 3 Memory.

Read Only

B-SRAM can be configured as ROM. The ROM can be initialized during the device configuration stage, and the ROM data needs to be provided in the initialization file. Initialization completes during the device power-on process.

Each B-SRAM can be configured as one 16 Kbits ROM. For further information about Read Only Port Block Memory ports and the related description, please refer to SUG283E, Gowin Primitives User Guide > 3 Memory.

3.6.3 Mixed Data Bus Width Configuration

B-SRAM in the GW1NZ series of FPGA products supports mixed data bus width operation. In the dual port and semi-dual port modes, the data bus width for read and write can be different. For the configuration options that are available, please see Table 3-8 and Table 3-9 below.

Table 3-8 Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port						
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	2K x 9	1K x 18
16K x 1	*	*	*	*	*		
8K x 2	*	*	*	*	*		
4K x 4	*	*	*	*	*		
2K x 8	*	*	*	*	*		
1K x 16	*	*	*	*	*		
2K x 9						*	*
1K x 18						*	*

Note!

"*"denotes the modes supported.

Table 3-9 Semi Dual Port Mixed Read/Write Data Width Configuration

Read Port	Write Port								
	16K x 1	8K x 2	4K x 4	2K x 8	1K x 16	512 x 32	2K x 9	1K x 18	512 x 36
16K x 1	*	*	*	*	*	*			
8K x 2	*	*	*	*	*	*			
4K x 4	*	*	*	*	*	*			
2K x 8	*	*	*	*	*	*			
1K x 16	*	*	*	*	*	*			
512 x 32	*	*	*	*	*	*			
2K x 9							*	*	*
1K x 18							*	*	*

Note!

"*"denotes the modes supported.

3.6.4 Byte-enable

The B-SRAM in the GW1NZ series of FPGA products supports byte-enable. For data longer than a byte, the additional bits can be blocked, and only the selected portion can be written into. The blocked bits will be retained for future operation. Read/write enable ports (WREA, WREB), and byte-enable parameter options can be used to control the B-SRAM write operation.

3.6.5 Parity Bit

There are parity bits in B-SRAM. The 9th bit in each byte can be used

as a parity bit or for data storage. However, the parity operation is not yet supported.

3.6.6 Synchronous Operation

- All the input registers of B-SRAM support synchronous write;
- The output registers can be used as pipeline register to improve design performance;
- The output registers are bypass-able.

3.6.7 Power up Conditions

B-SRAM initialization is supported when powering up. During the power-up process, B-SRAM is in standby mode, and all the data outputs are “0”. This also applies in ROM mode.

3.6.8 B-SRAM Operation Modes

B-SRAM supports five different operations, including two read operations (Bypass Mode and Pipeline Read Mode) and three write operations (Normal Write Mode, Write-through Mode, and Read-before-write Mode).

Read Mode

Read data from the B-SRAM via output registers or without using the registers.

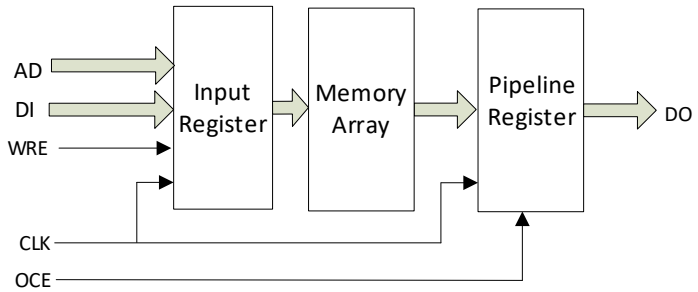
Pipeline Mode

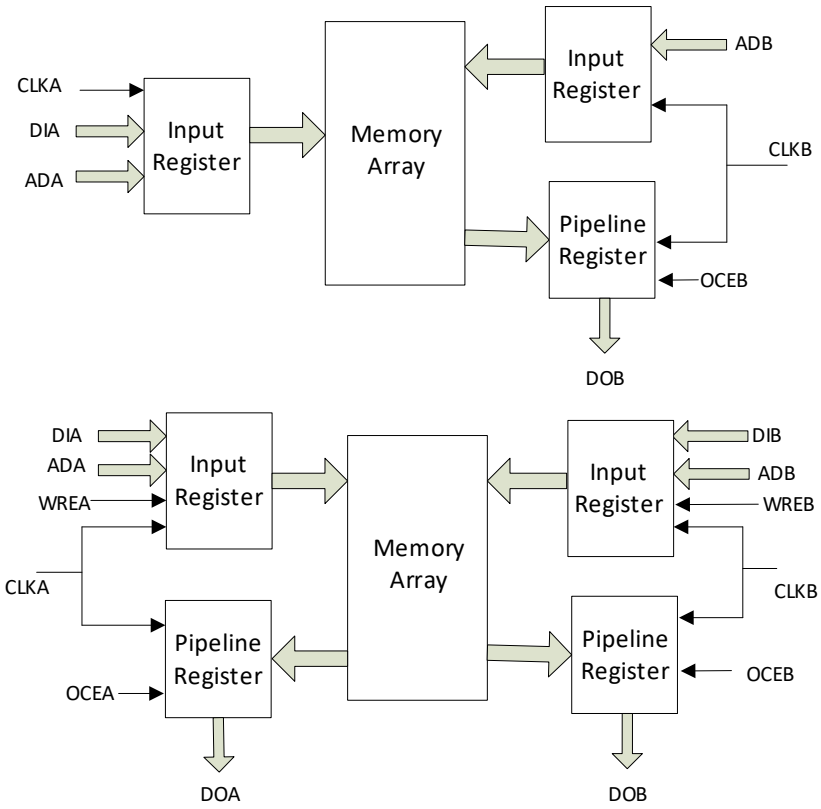
While writing in the B-SRAM, the output register and pipeline register are also being written. The data bus can be up to 36 bits in this mode.

Bypass Mode

The output register is not used. The data is kept in the output of memory array.

Figure 3-23 Pipeline Mode in Single Port, Dual Port and Semi Dual Port





Write Mode

NORMAL WRITE MODE

In this mode, when the user writes data to one port, and the output data of this port does not change. The data written in will not appear at the read port.

WRITE-THROUGH MODE

In this mode, when the user writes data to one port, and the data written in will also appear at the output of this port.

READ-BEFORE-WRITE MODE

In this mode, when the user writes data to one port, and the data written in will be stored in the memory according to the address. The original data in this address will appear at the output of this port.

3.6.9 Clock Operations

Table 3-10 lists the clock operations in different B-SRAM modes:

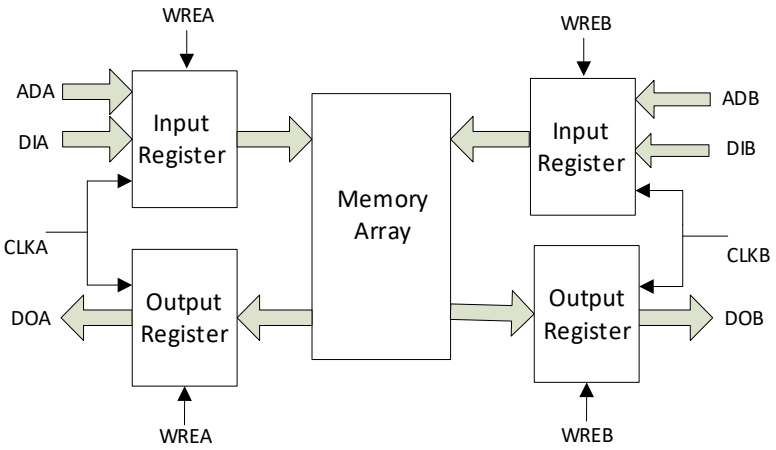
Table 3-10 Clock Operations in Different B-SRAM Modes

Clock Operations	Dual Port Mode	Semi-Dual Port Mode	Single Port Mode
Independent Clock Mode	Yes	No	No
Read/Write Clock Mode	Yes	Yes	No
Single Port Clock Mode	No	No	Yes

Independent Clock Mode

Figure 3-24 shows the independent clocks in dual port mode with each port with one clock. CLKA controls all the registers at Port A; CLKB controls all the registers at Port B.

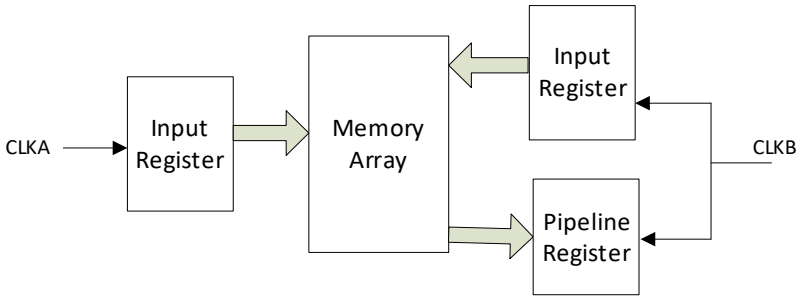
Figure 3-24 Independent Clock Mode



Read/Write Clock Operation

Figure 3-25 shows the read/write clock operations in the semi-dual port mode with one clock at each port. The write clock (CLKA) controls Port A data inputs, write address and write enable signals. The read clock (CLKB) controls Port B data output, read address, and read enable signals.

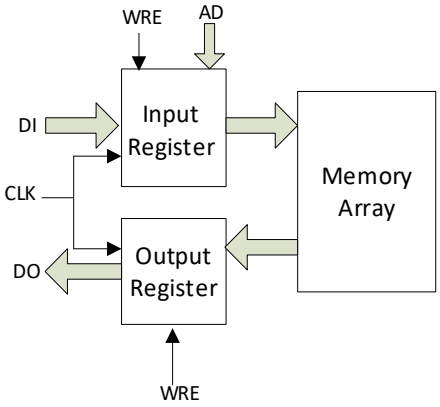
Figure 3-25 Read/Write Clock Mode



Single Port Clock Mode

Figure 3-26shows the clock operation in single port mode.

Figure 3-26 Single Port Clock Mode



3.7 User Flash

3.7.1 Introduction

GW1NZ-1 offers User Flash, the features are shown below:

- 10,000 write cycles
- Capacity: 64K bits
- Greater than ten years' data retention at +85 ℃
- Supports page erasure: 2,048 bytes per page
- Quick page erasure/Write operation
- Clock frequency: 40MHz
- Write operation time: ≤16μs
- Page erasure time: ≤120 ms
- Electric current
  - Read Operation: 2.19 mA/25 ns (V_{CC}) & 0.5 mA/25 ns (V_{CCX}) (MAX).
  - Write operation/erase operation: 12/12 mA(MAX)

3.7.2 Mode

The User Flash in GW1NZ series of FPGA products contains two modes: Normal mode and sleep mode.

- Normal mode: User flash is turned on by default. Users can perform erase/write/read operations after the device is power on. It cannot be turned off.
- Sleep mode: User flash is turned off by default to save power. Users can turn on/turn off the user flash mode using “Sleep” port. When the user flash is turned on, it’s the same as the normal mode user flash, and users can perform erase/write/read operations.

The GW1NZ LV/ZV devices with different speeds offer different user flash modes. For further detailed information, please refer to Table 3-11.

Table 3-11 User Flash Modes

Mode	Default Status	Turn on/Turn off	Device Version	Speed Grade
Normal mode	On	No	LV	C6/I5
				C5/I4
			ZV	C5/I4
Sleep mode	Off	Yes	ZV	I2
				I3

3.7.3 Port Signal

SeeFigure 3-27 for the User Flash signal diagram of GW1NZ-1.

Figure 3-27 GW1NZ-1 User Flash Ports

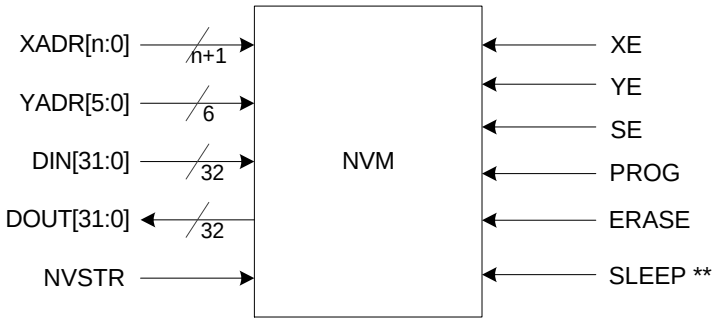


Table 3-12 Flash Module Signal Description

Pin name1	I/O	Description
XADR[5:0][2]	I	X address bus, used to select one row within a page of main memory block.
YADR[5:0][2]	I	Y address bus, used to select one column within a row of memory block.
DIN[31:0]	I	Data input bus.
DOUT[31:0]	O	Data output bus.
XE[2]	I	X address enable signal, if XE is 0, all of row addresses are not enabled.
YE[2]	I	Y address enable signal, if YE is 0, all of column addresses are not enabled.
SE[2]	I	Detect amplifier enable signal, active high.
ERASE	I	Erase port, active-high.
PROG	I	Programming port, active-high.
NVSTR	I	Flash data storage port, active-high.
SLEEP**	I[4]	Used to turn on/turn off user falsh. ● High level: On; ● Low level: Off.

Note!

- [1] Port names of Control, address, and data signals.
- [2] The read operation is valid only if XE = YE = V_{CC} and SE meets the pulse timing requirements (T_{pws}, T_{nws}). The address of read data is determined by XADR [5: 0] and YADR [5: 0].
- [3] The power pin and the ground pin connect in FPGA.

- [4] Only supported in user flash in sleep mode.

3.7.4 Operation Modes

Table 3-13 Truth Table in User Mode

Mode	XE	YE	SE	PROG	ERASE	NVSTR
Read mode	H	H	H	L	L	L
Programming mode	H	H	L	H	L	H
Page Erasure Mode	H	L	L	L	H	H

Note!

"H" and "L" means high level and low level of VCC.

3.8 Clock

3.8.1 Global Clock

The GCLK is distributed in GW1NZ-1 as two quadrants, L and R. Each quadrant provides eight GCLKs. Each GCLK has 12 optional clock sources. The optional clock resources of GCLK can be pins or CRU. Users can employ dedicated pins as clock resources to achieve better timing.

Figure 3-28 GW1NZ-1 Clock Resources

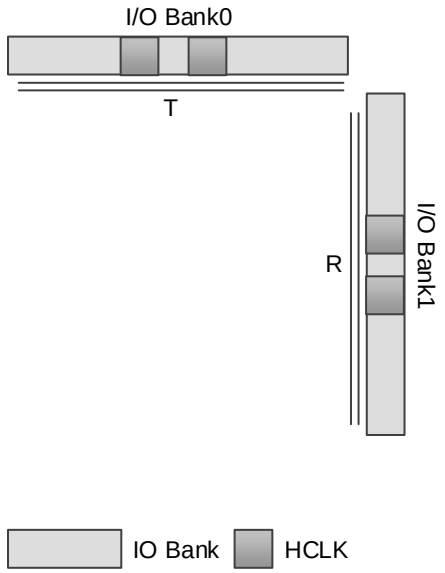
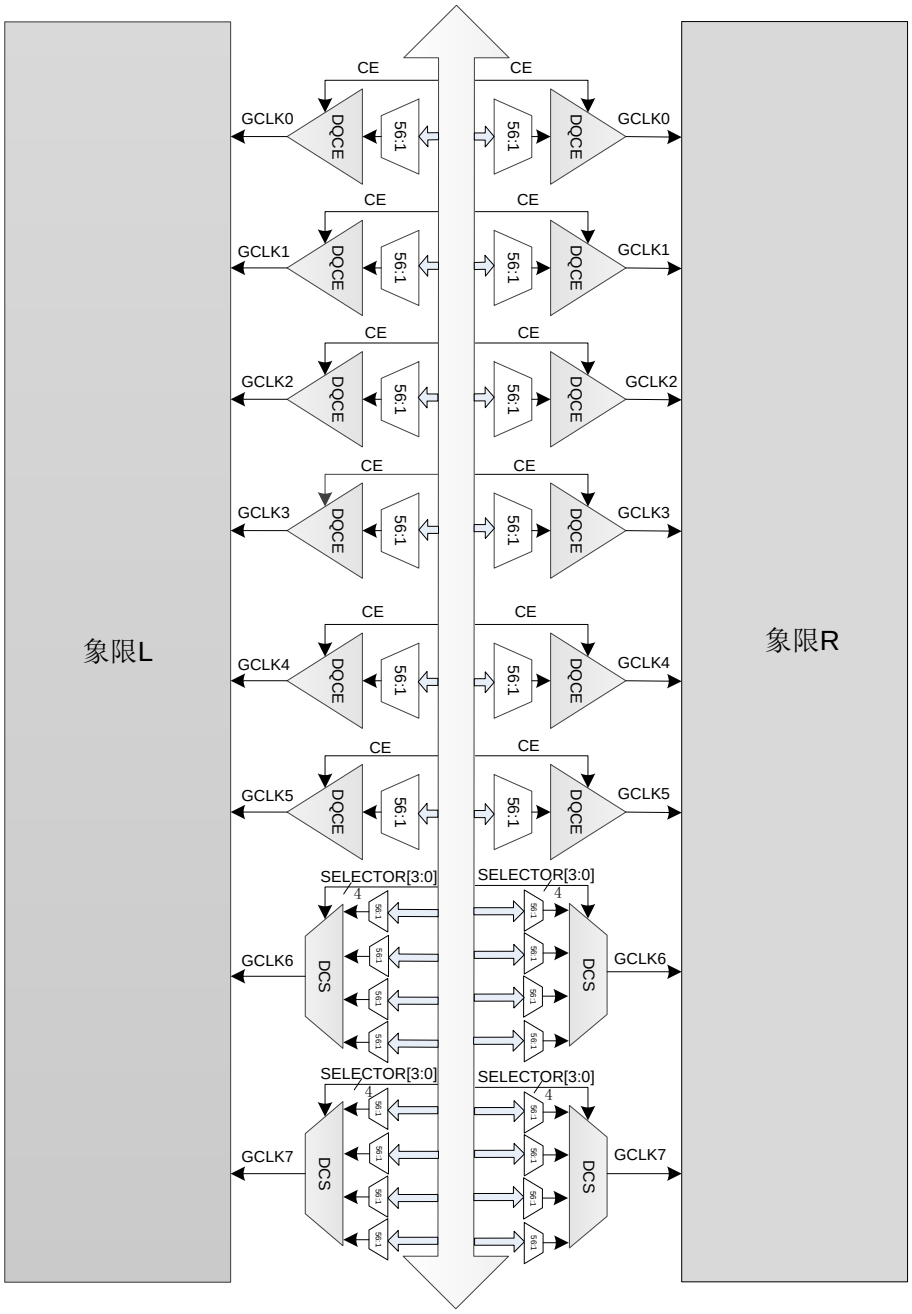
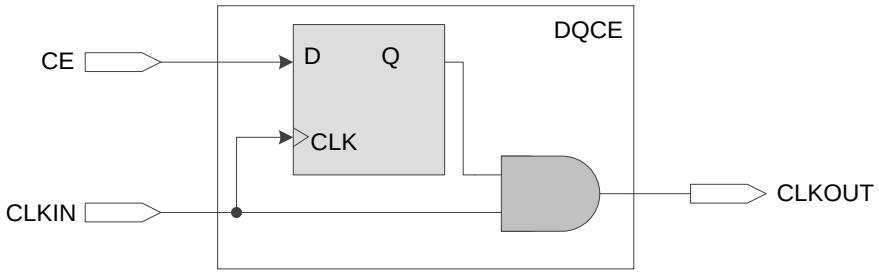


Figure 3-29 GCLK Quadrant Distribution



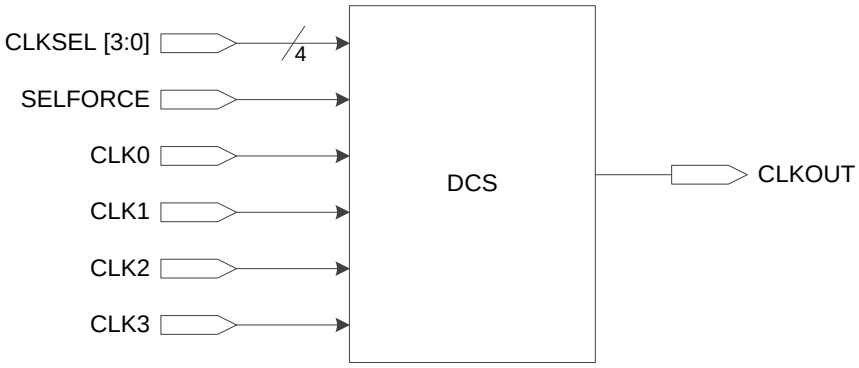
GCLK0~GCLK5 can be turned on or off by Dynamic Quadrant Clock Enable (DQCE). When GCLK0~GCLK5 in the quadrant is off, all the logic driven by it will not toggle; therefore, lower power can be achieved.

Figure 3-30 DQCE Concepts



GCLK6~GCLK7 of each quadrant is controlled by the DCS, as shown in Figure 3-31. Select dynamically between CLK0~CLK3 by CRU, and output a glitch-free clock.

Figure 3-31 DCS Concept

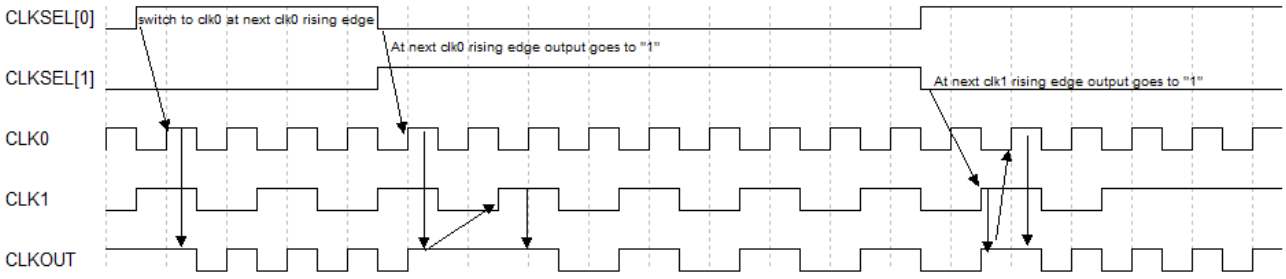


DCS can be configured in the following modes:

1. DCS Rising Edge

Stay as 1 after current selected clock rising edge, and the new select clock will be effective after its first rising edge, as shown in Figure 3-32.

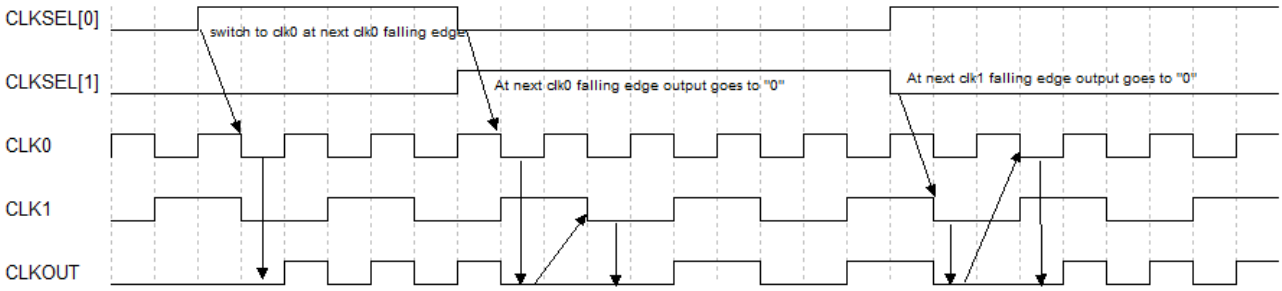
Figure 3-32 DCS Rising Edge



2. DCS Falling Edge

Stay as 0 after current selected clock falling edge, and the new select clock will be effective after its first falling edge, as shown in Figure 3-33.

Figure 3-33 DCS Falling Edge



3. Clock Buffer Mode

In this mode, the DCS acts as a clock buffer.

3.8.2 PLL

PLL (Phase-locked Loop) is one kind of a feedback control circuit. The frequency and phase of the internal oscillator signal is controlled by the external input reference clock.

PLL blocks provide the ability to synthesize clock frequencies. Frequency adjustment (multiply and division), phase adjustment, and duty cycle can be adjusted by configuring the parameters.

See Figure 3-34 for the PLL structure.

Figure 3-34 PLL Structure

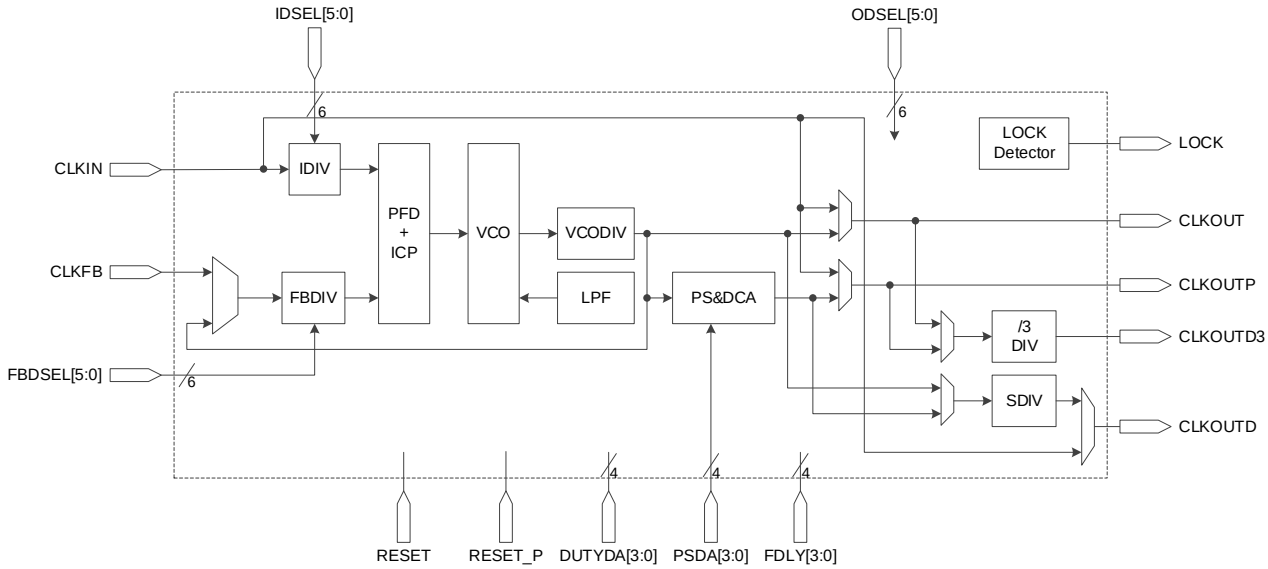


Table 3-14 PLL Ports Definition

Port Name	Signal	Description
CLKIN[5:0]	I	Reference clock input
CLKFB	I	Feedback clock input
RESET	I	PLL reset
RESET_P	I	PLL Power Down
IDSEL [5:0]	I	Dynamic IDIV control: 1~64
FBDSEL [5:0]	I	Dynamic FBDIV control:1~64
PSDA [3:0]	I	Dynamic phase control (rising edge effective)
DUTYDA [3:0]	I	Dynamic duty cycle control (falling edge effective)
FDLY[3:0]	I	CLKOUTP dynamic delay control
CLKOUT	Output	Clock output with no phase and duty cycle adjustment
CLKOUTP	Output	Clock output with phase and duty cycle adjustment
CLKOUTD	Output	Clock divider from CLKOUT and CLKOUTP (controlled by SDIV)
CLKOUTD3	Output	clock divider from CLKOUT and CLKOUTP (controlled by DIV3 with the constant division value 3)
LOCK	Output	PLL lock status: 1 locked, 0 unlocked

The PLL reference clock source can come from an external PLL pin or from internal routing GCLK, HCLK, or general data signal. PLL feedback

signal can come from the external PLL feedback input or from internal routing GCLK, HCLK, or general data signal.

For PLL features of GW1NZ series of FPGA products, please refer to 4.4.5 PLL Switching Characteristics.

PLL can adjust the frequency of the input clock CLKIN (multiply and division). The formulas for doing so are as follows:

1. $f_{CLKOUT} = (f_{CLKIN}*FBDIV)/IDIV$;
2. $f_{VCO} = f_{CLKOUT}*ODIV$;
3. $f_{CLKOUTD} = f_{CLKOUT}/SDIV$;
4. $f_{PFD} = f_{CLKIN}/IDIV = f_{CLKOUT}/FBDIV$.

Note!

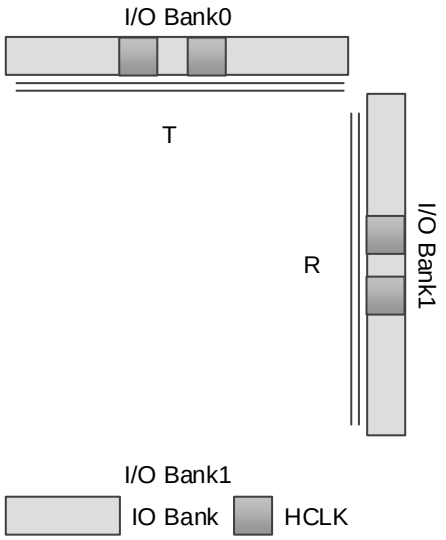
- f_{CLKIN}: The frequency of input clock CLKIN;
- f_{CLKOUT}: The clock frequency of CLKOUT and CLKOUTP
- $f_{CLKOUTD}$: The clock frequency of CLKOUTD, and CLKOUTD is the clock CLKOUT after division
- f_{PFD}: PFD Frequency, and the minimum value of f_{PFD} should be no less than 3MHz.

Adjust IDIV, FBDIV, ODIV, and SDIV to achieve the required clock frequency.

3.8.3 HCLK

HCLK is the high-speed clock in the GW1NZ series of FPGA products. It can support high-performance data transfer and is mainly suitable for source synchronous data transfer protocols. See Figure Figure 3-35. HCLK can be used for the whole I/O Bank.

Figure 3-35 GW1NZ-1 HCLK Distribution



3.9 Long Wire (LW)

As a supplement to the CRU, the GW1NZ series of FPGA products provides another routing resource, Long wire, which can be used as clock, clock enable, set/reset,or other high fan out signals.

3.10 Global Set/Reset (GSR)

A global set/reset (GSR) network is built in the GW1NZ series of FPGA product. There is a direct connection to core logic. It can be used as asynchronous/synchronous set. The registers in CFU and I/O can be individually configured to use GSR.

3.11 Programming Configuration

The GW1NZ series of FPGA products support SRAM and Flash. The Flash programming mode supports on-chip Flash and off-chip Flash. The GW1NZ series of FPGA products support DUAL BOOT, providing a selection for users to backup data to off chip Flash according to requirements.

Besides JTAG, the GW1NZ series of FPGA products also supports GOWINSEMI's own configuration mode: GowinCONFIG (AUTO BOOT, SSPI, MSPI, DUAL BOOT, SERIAL, and CPU). All the devices support JTAG and AUTO BOOT. For the detailed information, please refer to UG290, *Gowin FPGA Products Programming and Configureation User Guide*.

3.11.1 SRAM Configuration

When you adopt SRAM to configure the device, every time the device is powered on, the bit stream file needs to be downloaded to configure the device.

3.11.2 Flash Configuration

The Flash configuration data is stored in the on-chip flash. Each time the device is powered on, the configuration data is transferred from the Flash to the SRAM, which controls the working of the device. This mode can complete configuration within a few ms, and is referred to as “Quick Start”. The GW1NZ series of FPGA products also support off-chip Flash configuration and dual-boot. Please refer to UG290, *Gowin FPGA Products Programming and Configuration User Guide* for more detailed information.

3.12 On Chip Oscillator

There is an on chip oscillator in each of the GW1NZ series of FPGA product. The on chip oscillator provides a programmable user clock with precision of ±5%. During the configuration process, it can provide a clock for the MSPI mode. See Table 3-15 for the output frequency.

Table 3-15 Oscillator Output Frequency Options

Mode	Frequency	Mode	Frequency	Mode	Frequency
0	2.5MHz[1]	8	7.8MHz	16	15.6MHz
1	5.4MHz	9	8.3MHz	17	17.9MHz
2	5.7MHz	10	8.9MHz	18	21MHz
3	6.0MHz	11	9.6MHz	19	25MHz
4	6.3MHz	12	10.4MHz	20	31.3MHz
5	6.6MHz	13	11.4MHz	21	41.7MHz
6	6.9MHz	14	12.5MHz	22	62.5MHz
7	7.4MHz	15	13.9MHz	23	125MHz[2]

Note!

- [1] The default frequency is 2.5MHz.
- [2] 125 MHz is not suitable for MSPI.

The on-chip oscillator also provides a clock resource for user designs. Up to 64 clock frequencies can be obtained by setting the parameters. The following formula is employed to get the output clock frequency:

f_{out}=250MHz/Param.

“Param” is the configuration parameter with a range of 2~128. It supports even number only.

4 AC/DC Characteristic

4.1 Operating Conditions

4.1.1 Absolute Max. Ratings

Table 4-1 Absolute Max. Ratings

Name	Description	Min.	Max.
V_{CC}	Core voltage	-0.5V	1.32V
V_{CCO}	I/O Bank Power	-0.5V	3.75V
V_{CCX}	Auxiliary Power	-0.5V	3.75V
Storage Temperature	Storage Temperature	-65 ℃	+150 ℃
Junction Temperature	Junction Temperature	-40℃	+125℃

4.1.2 Recommended Operating Conditions

Table 4-2 Recommended Operating Conditions

Name	Description	Min.	Max.
V_{CC}	LV: Core Power	1.14V	1.26V
	ZV: Core Power	0.855V	0.945V
V_{CCO}	I/O Bank Power	1.14V	3.465V
V_{CCX}	Auxiliary voltage	1.71V	3.465V
T_{JCOM}	Junction temperature Commercial operation	0 ℃	+85 ℃
T_{JIND}	Junction temperature Industrial operation	-40℃	+100℃

4.1.3 Power Supply Ramp Rates

Table 4-3 Power Supply Ramp Rates

Name	Description	Min.	Typ.	Max.
T_{RAMP}	Power supply ramp rates for all power supplies	0.6mV/μs	-	6mV/μs

4.1.4 Hot Socket Specifications

Table 4-4 Hot Socket Specifications

Name	Description	Condition	I/O Type	Max.
I_{HS}	Input or I/O leakage current	$0<V_{IN}<V_{IH}$(MAX)	I/O	150uA
I_{HS}	Input or I/O leakage current	$0<V_{IN}<V_{IH}$(MAX)	TDI,TDO, TMS,TCK	120uA

4.1.5 POR Specification

Table 4-5 POR Specification

Name	Description	Min.	Max.
POR Voltage Value	Power on reset voltage of Vcc	TBD	TBD

4.2 ESD

Table 4-6 GW1NZ ESD - HBM

Device	CS16	FN32	FN32F
GW1NZ-1	TBD	HBM>1,000V	HBM>1,000V

Table 4-7 GW1NZ ESD - CDM

Device	CS16	FN32	FN32F
GW1NZ-1	TBD	CDM>500V	CDM>500V

4.3 DC Characteristic

4.3.1 DC Electrical Characteristics over Recommended Operating Conditions

Table 4-8 DC Electrical Characteristics over Recommended Operating Conditions

Name	Description	Condition	Min.	Typ.	Max.
I_{IL},I_{IH}	Input or I/O leakage	$V_{CCO}<V_{IN}<V_{IH}$ (MAX)	-	-	210 μA
		$0V<V_{IN}<V_{CCO}$	-	-	10μA
I_{PU}	I/O Active Pull-up Current (I/O Active Pull-up Current)	$0<V_{IN}<0.7V_{CCO}$	-30 μA	-	-150 μA
I_{PD}	I/O Active Pull-down Current	V_{IL} (MAX)$<V_{IN}<V_{CCO}$	30 μA	-	150 μA
I_{BHLS}	Bus Hold Low Sustaining Current	$V_{IN}=V_{IL}$ (MAX)	30 μA	-	-
I_{BHHO}	Bus Hold High Sustaining Current	$V_{IN}=0.7V_{CCO}$	-30 μA	-	-
I_{BHLO}	Bus HoldLow Overdrive Current	$0\le V_{IN}\le V_{CCO}$	-	-	150 μA
I_{BHHO}	Bus HoldHigh Overdrive Current	$0\le V_{IN}\le V_{CCO}$	-	-	-150 μA

Name	Description	Condition	Min.	Typ.	Max.
V_{BHT}	Bus hold trigger points		V_{IL} (MAX)	-	V_{IH} (MIN)
C1	I/O Capacitance (I/O Capacitance)			5 pF	8 pF
V_{HYST}	Hysteresis for Schmitt Trigge inputs (Hysteresis for Schmitt Trigger inputs)	V_{CCO}=3.3V, Hysteresis= Large	-	482mV	-
		V_{CCO}=2.5V, Hysteresis= Large	-	302mV	-
		V_{CCO}=1.8V, Hysteresis= Large	-	152mV	-
		V_{CCO}=1.5V, Hysteresis= Large	-	94mV	-
		V_{CCO}=3.3V, Hysteresis= Small	-	240mV	-
		V_{CCO}=2.5V, Hysteresis= Small	-	150mV	-
		V_{CCO}=1.8V, Hysteresis= Small	-	75mV	-
		V_{CCO}=1.5V, Hysteresis= Small	-	47mV	-

4.3.2 Static Current

Table 4-9 Static Supply Current (LV Device)

Name	Description	Device	Typ.
I_{CC}	Core current (Vcc=1.2V)	GW1NZ-1	3mA
I_{CCX}	V_{CCX} current (VCCX=3.3V)	GW1NZ-1	-
	V_{CCX} current (VCCX=2.5V)	GW1NZ-1	-
I_{CCO}	I/O Bank current (V_{CCO}=2.5V)	GW1NZ-1	-

Table 4-10 Static Supply Current (ZV Device)

Name	Description	Device	Typ.
I_{CC}	Core current (Vcc=0.9V)	GW1NZ-ZV1FN32C5/I4 GW1NZ-ZV1CS16C5/I4	50uA
		GW1NZ-ZV1FN32I3 GW1NZ-ZV1CS16I3	40uA
		GW1NZ-ZV1FN32I2 GW1NZ-ZV1CS16I2	30uA
I_{CCX}	V_{CCX} current (V_{CCX} floating)	GW1NZ-ZV1FN32C5/I4 GW1NZ-ZV1CS16C5/I4	0uA
		GW1NZ-ZV1FN32I3 GW1NZ-ZV1CS16I3	0uA
		GW1NZ-ZV1FN32I2 GW1NZ-ZV1CS16I2	0uA
	V_{CCX} current (VCCX=1.8V~3.3V)	GW1NZ-ZV1FN32C5/I4 GW1NZ-ZV1CS16C5/I4	1uA
		GW1NZ-ZV1FN32I3 GW1NZ-ZV1CS16I3	1uA
		GW1NZ-ZV1FN32I2 GW1NZ-ZV1CS16I2	1uA
I_{CCO}	I/O Bank current (V_{CCO}=3.3V)	GW1NZ-ZV1FN32C5/I4 GW1NZ-ZV1CS16C5/I4	0uA
		GW1NZ-ZV1FN32I3 GW1NZ-ZV1CS16I3	0uA
		GW1NZ-ZV1FN32I2 GW1NZ-ZV1CS16I2	0uA

Note!

- After device wake up, user can turn off external Vccx when they do not use user flash and chip still functional.
- The typical values in the table above are tested at room temperature.
- In zero power cirucumstance, if users use MODE pin, the PULL_MODE of this pin must be configured as KEEPER.

4.3.3 I/O Operating Conditions Recommended

Table 4-11 I/O Operating Conditions Recommended

Name	Output V_{CCO} (V)			Input V_{REF} (V)		
	Min.	Typ.	Max.	Min.	Typ.	Max.
LVTTL33	3.135	3.3	3.465	-	-	-
LVCMOS33	3.135	3.3	3.465	-	-	-
LVCMOS25	2.375	2.5	2.625	-	-	-
LVCMOS18	1.71	1.8	1.89	-	-	-
LVCMOS15	1.425	1.5	1.575	-	-	-
LVCMOS12	1.14	1.2	1.26	-	-	-
SSTL15	1.425	1.5	1.575	0.68	0.75	0.9
SSTL18_I	1.71	1.8	1.89	0.833	0.9	0.969
SSTL18_II	1.71	1.8	1.89	0.833	0.9	0.969
SSTL25_I	2.375	2.5	2.645	1.15	1.25	1.35
SSTL25_II	2.375	2.5	2.645	1.15	1.25	1.35
SSTL33_I	3.135	3.3	3.465	1.3	1.5	1.7
SSTL33_II	3.135	3.3	3.465	1.3	1.5	1
HSTL18_I	1.71	1.8	1.89	0.816	0.9	1.08
HSTL18_II	1.71	1.8	1.89	0.816	0.9	1.08
HSTL15	1.425	1.5	1.575	0.68	0.75	0.9
PCI33	3.135	3.3	3.465	-	-	-
LVPECL33E	3.135	3.3	3.465	-	-	-
MLVDS25E	2.375	2.5	2.625	-	-	-
BLVDS25E	2.375	2.5	2.625	-	-	-
RSDS25E	2.375	2.5	2.625	-	-	-
LVDS25E	2.375	2.5	2.625	-	-	-
SSTL15D	1.425	1.5	1.575	-	-	-
SSTL18D_I	1.71	1.8	1.89	-	-	-
SSTL18D_II	1.71	1.8	1.89	-	-	-
SSTL25D_I	2.375	2.5	2.625	-	-	-
SSTL25D_II	2.375	2.5	2.625	-	-	-
SSTL33D_I	3.135	3.3	3.465	-	-	-
SSTL33D_II	3.135	3.3	3.465	-	-	-
HSTL15D	1.425	1.575	1.89	-	-	-
HSTL18D_I	1.71	1.8	1.89	-	-	-
HSTL18D_II	1.71	1.8	1.89	-	-	-

4.3.4 Single - Ended IO DC Electrical Characteristic

Table 4-12 Single - Ended IO DC Electrical Characteristic

Name	V_{IL}		V_{IH}		V_{OL} (Max)	V_{OH} (Min)	I_{OL} (mA)	I_{OH} (mA)
	Min	Max	Min	Max				
LVCMOS33 LVTTL33	-0.3V	0.8V	2.0V	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
							24	-24
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS25	-0.3V	0.7V	1.7V	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
							12	-12
							16	-16
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS18	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}0.4V	4	-4
							8	-8
							12	-12
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS15	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}-0.4V	4	-4
							8	-8
					0.2V	V_{CCO}-0.2V	0.1	-0.1
LVCMOS12	-0.3V	0.35 x V_{CCO}	0.65 x V_{CCO}	3.6V	0.4V	V_{CCO}-0.4V	2	-2
							6	-6
					0.2V	V_{CCO}-0.2V	0.1	-0.1
PCI33	-0.3V	0.3 x V_{CCO}	0.5 x V_{CCO}	3.6V	0.1 x V_{CCO}	0.9 x V_{CCO}	1.5	-0.5
SSTL33_I	-0.3V	V_{REF}-0.2V	V_{REF}+0.2V	3.6V	0.7	V_{CCO}-1.1V	8	-8
SSTL25_I	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	0.54V	V_{CCO}-0.62V	8	-8
SSTL25_II	-0.3V	V_{REF}-0.18V	V_{REF}+0.18V	3.6V	NA	NA	NA	NA
SSTL18_II	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	NA	NA	NA	NA
SSTL18_I	-0.3V	V_{REF}-0.125V	V_{REF}+0.125V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
SSTL15	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL18_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA
HSTL15_I	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	0.40V	V_{CCO}-0.40V	8	-8
HSTL15_II	-0.3V	V_{REF}-0.1V	V_{REF}+ 0.1V	3.6V	NA	NA	NA	NA

4.4 Switching Characteristic

4.4.1 CFU Block Internal Timing Parameters

Table 4-13 CFU Block Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{LUT4_CFU}	LUT4 delay	-	0.674	ns
t_{LUT5_CFU}	LUT5 delay	-	1.388	ns
t_{LUT6_CFU}	LUT6 delay	-	2.01	ns
t_{LUT7_CFU}	LUT7 delay	-	2.632	ns
t_{LUT8_CFU}	LUT8 delay	-	3.254	ns
t_{SR_CFU}	Set/Reset to Register output	-	1.86	ns
t_{CO_CFU}	Clock to Register output	-	0.76	ns

4.4.2 Clock and I/O Switching Characteristics

Table 4-14 Clock and I/O Switching Characteristics

Name	Description	Device	-5		-6		Unit
			Min	Max	Min	Max	
Clocks	TBD	TBD	TBD	TBD	TBD	TBD	
Pin-LUT-Pin Delay	TBD	TBD	TBD	TBD	TBD	TBD	
General I/O Pin Parameters	TBD	TBD	TBD	TBD	TBD	TBD	

4.4.3 B-SRAM Switching Characteristics

Table 4-15 B-SRAM Internal Timing Parameters

Name	Description	Speed Grade		Unit
		Min	Max	
t_{COAD_BSRAM}	Clock to output from read address/data	-	5.10	ns
t_{COOR_BSRAM}	Clock to output from output register	-	0.56	ns

4.4.4 On chip Oscillator Output Frequency

Table 4-16 On chip Oscillator Output Frequency

Name	Description	Min.	Typ.	Max.
f_{MAX}	Output Frequency (0 to 85℃)	106.25MHz	125MHz	143.75MHz
	Output Frequency (-40 to +100℃)	100MHz	125MHz	150MHz
t_{DT}	Output Clock Duty Cycle	43%	50%	57%
t_{OPJIT}	Output Clock Period Jitter	0.01UIPP	0.012UIPP	0.02UIPP

4.4.5 PLL Switching Characteristics

Table 4-17 PLL Switching Characteristics

Device	LV/ZV	Speed Grade	Name	Min.	最大值
GW1NZ-1	LV	C6/I5	CLKIN	3MHZ	400MHZ
			PFD	3MHZ	400MHZ
			VCO	400MHZ	800MHZ
			CLKOUT	3.125MHZ	400MHZ
		C5/I4	CLKIN	3MHZ	320MHZ
			PFD	3MHZ	320MHZ
			VCO	320MHZ	640MHZ
			CLKOUT	2.5MHZ	360MHZ
	ZV	C5/I4	CLKIN	3MHZ	200MHZ
			PFD	3MHZ	200MHZ
			VCO	200MHZ	400MHZ
			CLKOUT	1.5625MHZ	200MHZ
		I3	CLKIN	3MHZ	150MHZ
			PFD	3MHZ	150MHZ
			VCO	150MHZ	300MHZ
			CLKOUT	1.171875MHZ	150MHZ
		I2	CLKIN	3MHZ	100MHZ
			PFD	3MHZ	100MHZ
			VCO	100MHZ	200MHZ
			CLKOUT	0.78125MHZ	100MHZ

4.5 User Flash Characteristic

4.5.1 DC Characteristic

Table 4-18 User Flash DC Characteristics

Name	Parameter	Max.		Unit	Wake-up Time	Condition
		V_{CC}[3]	V_{CCX}			
Read mode (w/I 25ns)[1]	I_{CC1}[2]	2.19	0.5	mA	NA	Min. Clcok period, duty cycle 100%, VIN = “1/0”
Write mode		0.1	12	mA	NA	
Erase mode		0.1	12	mA	NA	
Page Erasure Mode		0.1	12	mA	NA	
Read mode static current (25-50ns)	I_{CC2}	980	25	μA	NA	XE=YE=SE=“1”, between T=Tacc and T=50ns, I/O=0mA; later than T=50ns, read mode is turned off, and I/O current is the current of standby mode.
Standby mode	I_{SB}	5.2	20	μA	0	V_{SS}, V_{CCX}, and V_{CC}

Floating mode[3]	I_{PD}	0	0	μA	7us	V_{CCX}=0
Typical Value (Room temperature: 25℃)						
Standby mode	I_{SB}	0.4	7.5	μA	0	V_{SS}, V_{CCX}, and V_{CC}
Floating mode[3]	I_{PD}	0	0	μA	3.5us	V_{CCX}=0

Note!

- [1] means the average current, and the peak value is higher than the average one.
- [2] Calculated in different T_{new} clock periods.
  - $T_{new} < T_{acc}$ is not allowed
  - $T_{new} = T_{acc}$
  - $T_{acc} < T_{new}$ - 50ns: I_{CC1} (new) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + I_{CC2}
  - T_{new}>50ns: I_{CC1} (new) = (I_{CC1} - I_{CC2})(T_{acc}/T_{new}) + 50ns x I_{CC2}/T_{new} + I_{SB}
  - t > 50ns, $I_{CC2} = I_{SB}$
- [3] Only supported in user flash in sleep mode.

4.5.2 Timing Parameters

Table 4-19 User Flash Timing Parameters

User Modes	Parameter	Name	Min.	Max.	Unit
Access time[2]	WC1	T_{acc}[3]	-	25	ns
	TC		-	22	ns
	BC		-	21	ns
	LT		-	21	ns
	WC		-	25	ns
Program/Erase to data storage		T_{nvs}	5	-	μs
Data storage hold time		T_{nvh}	5	-	μs
Data storage hold time (Overall erase)		T_{nvh1}	100	-	μs
Time from data storage to program setup		T_{pgs}	10	-	μs
Program hold time		T_{pgh}	20	-	ns
Write time		T_{prog}	8	16	μs
Write ready time		T_{wpr}	>0	-	ns
Erase hold time		T_{whd}	>0	-	ns
Time from control signal to write/Erase setup		T_{cps}	-10	-	ns
Time from SE to read setup		T_{as}	0.1	-	ns
E pulse high level time		T_{pws}	5	-	ns
Adress/data setup time		T_{ads}	20	-	ns
Adress/data hold time		T_{adh}	20	-	ns
Data hold-up time		T_{dh}	0.5	-	ns
Read mode address hold time[3]	WC1	T_{ah}	25	-	ns
	TC		22	-	ns
	BC		21	-	ns
	LT		21	-	ns
	WC		25	-	ns
SE pulse low level time		T_{nws}	2	-	ns
Recovery time		T_{rcv}	10	-	μs
Data storage time		T_{hv}[4]	-	6	ms
Erasure time		T_{erase}	100	120	ms
Overall erase time		T_{me}	100	120	ms
Wake-up time from power down to standby mode		T_{wk_pd}	7	-	μs
Standby hold time		T_{sbh}	100	-	ns
V_{CC} setup time		T_{ps}	0	-	ns
V_{CCX} hold time		T_{ph}	0	-	ns

Note!

- [1] The parameter values may change;
- [2] The values are simulation data only.

- [3]After XADR, YADR, XE, and YE are valid, T_{acc} start time is SE rising edge. DOUT is kept until the next valid read operation;
- [4]T_{hv} is the time between write and the next erasure.The same address can not be written twice before erasure, so does the same register. This limitation is for safety;
- [5]Both the rising edge time and falling edge time for all waveform is 1ns;
- [6] TX, YADR, XE, and YE hold time need to be T_{acc} at leaset, and T_{acc} start from SE rising edge.

4.5.3 Operation Timing Diagrams

Figure 4-1 Read Mode

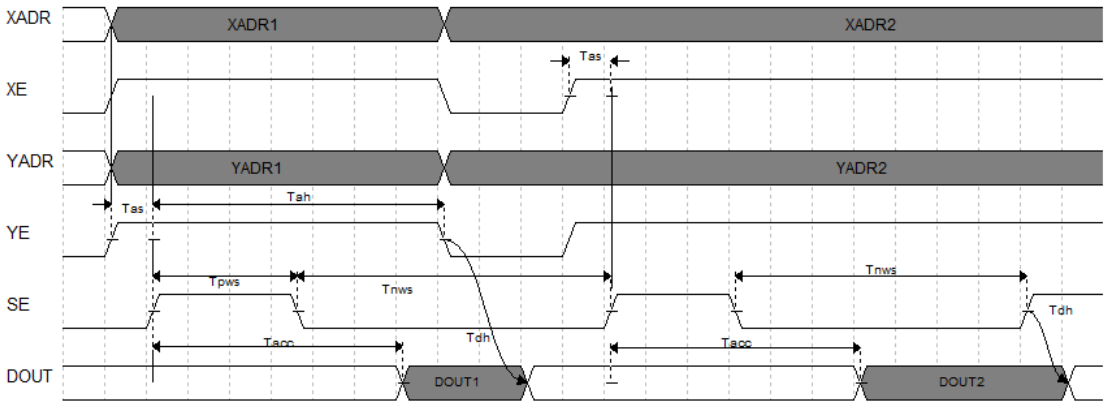


Figure 4-2 Write Mode

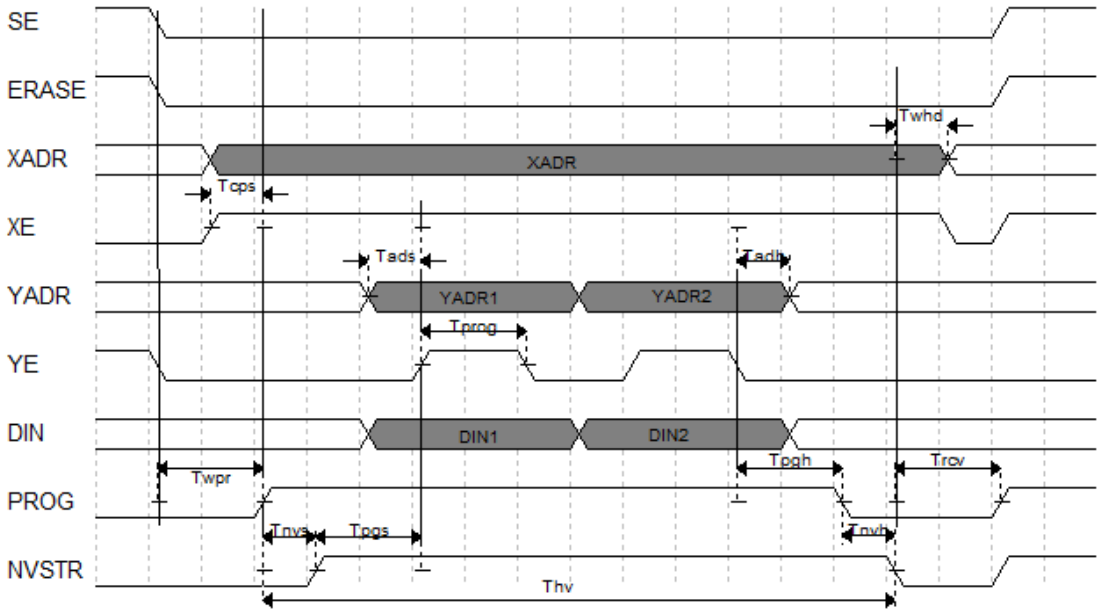
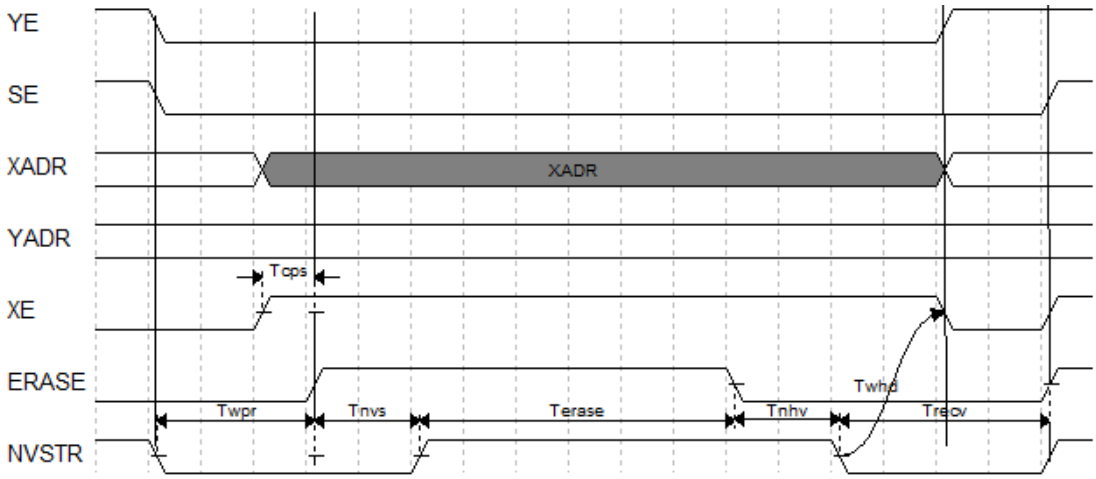


Figure 4-3 Erasure Mode



4.6 Configuration Interface Timing Specification

The GW1NZ series of FPGA products GowinCONFIG support six configuration modes: AUTO BOOT, DUAL BOOT, MSPI, SSPI, SERIAL, and CPU. For more detailed information, please refer to UG290, *Gowin FPGA Products Programming and Configuration* User Guide.

5 Ordering Information

5.1 Part Name

Figure 5-1 Part Naming Example–ES

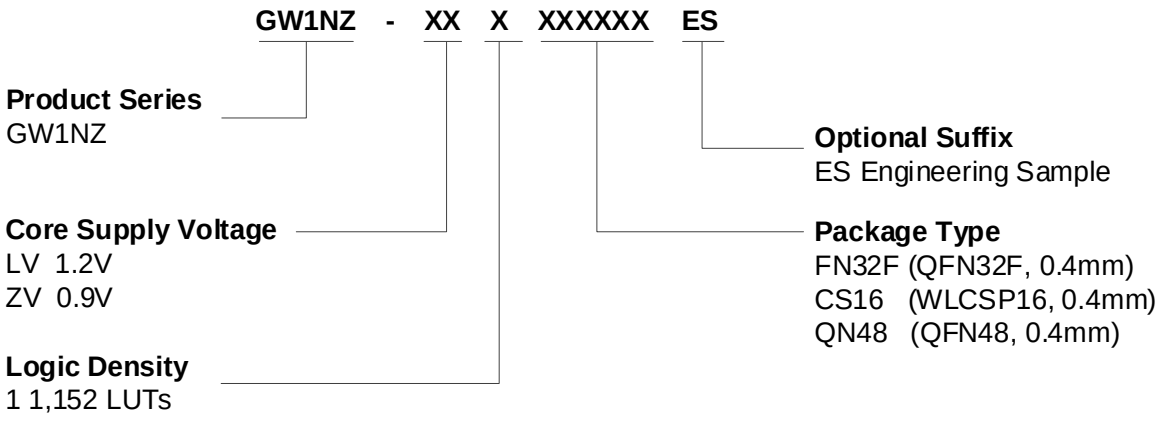
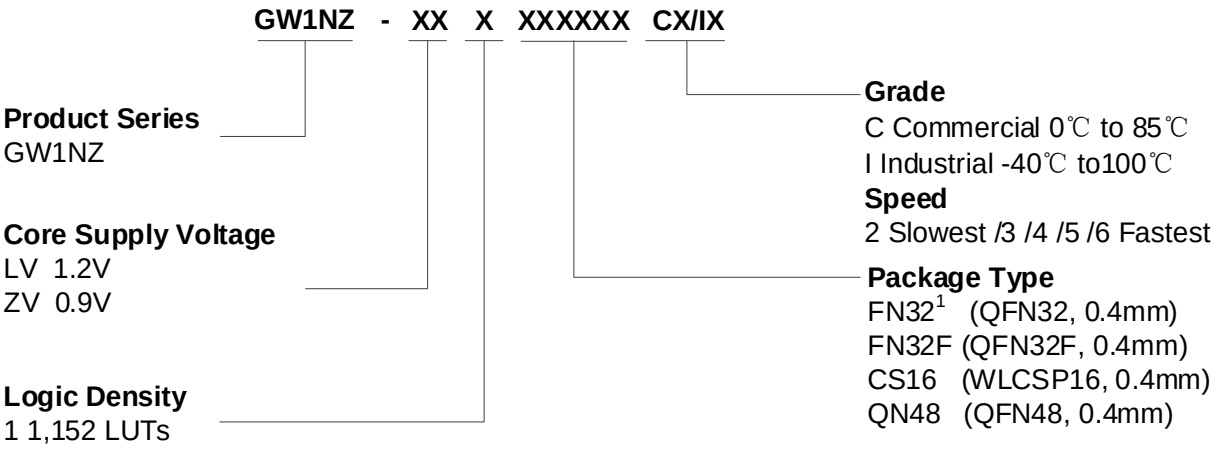


Figure 5-2 Part Naming Example–Production



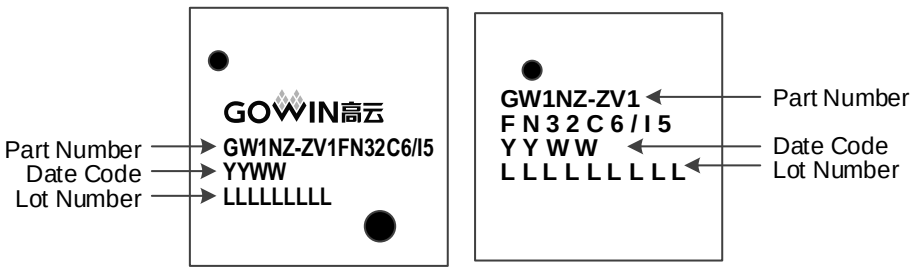
Note!

- [1] FN32 is the legacy version.
- For the further detailed information about the package type and pin number, please refer to 2.2 Product Resources and 2.3 Package Information.
- The LittleBee® family devices and Arora family devices of the same speed level have different speed.
- Both “C” and “I” are used in partial GW1NZ device part name marking. GOWIN devices are screened using industrial standards, so one same device can be used for both industrial (I) and commercial (C) applications. The maximum temperature of the industrial grade is 100℃, and the maximum temperature of the commercial grade is 85℃. Therefore, if the same chip meets the speed level 5 in the commercial grade application, the speed level is 4 in the industrial grade application.

5.2 Package Mark

The device information of GOWINSEMI is marked on the chip surface, as shown in Figure 5-3.

Figure 5-3 Package Mark



Note!

The first two lines in the right figure above are the “Part Number”.