



Gowin UART Master and Slave IP **User Guide**

IPUG511-1.4E, 09/29/2019

Copyright©2019 Guangdong Gowin Semiconductor Corporation. All Rights Reserved.

No part of this document may be reproduced or transmitted in any form or by any denotes, electronic, mechanical, photocopying, recording or otherwise, without the prior written consent of GOWINSEMI.

Disclaimer

GOWINSEMI[®], LittleBee[®], Arora[™], and the GOWINSEMI logos are trademarks of GOWINSEMI and are registered in China, the U.S. Patent and Trademark Office and other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders, as described at www.gowinsemi.com.cn. GOWINSEMI assumes no liability and provides no warranty (either expressed or implied) and is not responsible for any damage incurred to your hardware, software, data, or property resulting from usage of the materials or intellectual property except as outlined in the GOWINSEMI Terms and Conditions of Sale. All information in this document should be treated as preliminary. GOWINSEMI may make changes to this document at any time without prior notice. Anyone relying on this documentation should contact GOWINSEMI for the current documentation and errata.

Revision

| Date | Revision | Description |
|------------|----------|--|
| 12/20/2018 | 1.0E | Initial version published. |
| 03/28/2019 | 1.1E | Supported products updated. |
| 05/08/2019 | 1.2E | Changed AXI interface to SRAM interface. |
| 07/22/2019 | 1.3E | Interface configuration added. |
| 09/29/2019 | 1.4E | UART Master released as an IP; UART Slave released as an open source reference design. |

Contents

| | |
|--|------------|
| Contents | i |
| List of Figures | iii |
| List of Tables | iv |
| 1 About This Manual | 1 |
| 1.1 Manual Content | 1 |
| 1.2 Applicable Products | 1 |
| 1.3 Related Documents | 1 |
| 1.4 Terms and Abbreviations | 1 |
| 1.5 Technical Support and Feedback | 2 |
| 2 Function Introduction | 3 |
| 2.1 Overview | 3 |
| 2.2 Features..... | 3 |
| 2.2.1 Gowin UART Master IP | 3 |
| 2.2.2 Gowin UART Slave IP | 3 |
| 3 Signal Definition | 4 |
| 3.1 Gowin UART Master IP | 4 |
| 3.1.1 SRAM Interface Signal | 4 |
| 3.1.2 UART Side Signal..... | 4 |
| 3.2 Gowin UART Slave IP | 5 |
| 4 Working Principle | 6 |
| 4.1 System Diagram | 6 |
| 4.2 Gowin UART Master IP Register | 6 |
| 4.2.1 Receive Buffer Register (RBR)..... | 7 |
| 4.2.2 Transmit Holding Register (THR) | 7 |
| 4.2.3 Interrupt Enable Register (IER) | 7 |
| 4.2.4 Interrupt Identification Register (IIR)..... | 8 |
| 4.2.5 Line Control Register (LCR) | 9 |
| 4.2.6 Modem Control Register (MCR) | 9 |
| 4.2.7 Line Status Register (LSR) | 10 |
| 4.2.8 Modem Status Register (MSR)..... | 11 |
| 4.3 Gowin UART Slave Implementation | 12 |
| 5 Interface Configuration | 13 |
| 5.1 UART MASTER IP Core Interface..... | 13 |
| 5.2 UART SLAVE IP Core Interface | 14 |

6 Reference Design 15

List of Figures

| | |
|--|----|
| Figure 4-1 System Diagram | 6 |
| Figure 4-2 Receive Buffer Register..... | 7 |
| Figure 4-3 Transmit Holding Register | 7 |
| Figure 4-4 Interrupt Enable Register..... | 8 |
| Figure 4-5 Interrupt Identification Register | 8 |
| Figure 4-6 Line Control Register..... | 9 |
| Figure 4-7 Modem Control Register..... | 9 |
| Figure 4-8 Line Status Register | 10 |
| Figure 4-9 Modem Status Register | 11 |
| Figure 4-10 UART Slave Implementation Block Diagram..... | 12 |
| Figure 5-1 UART MASTER Configuration Interface | 13 |
| Figure 5-2 UART SLAVE Configuration Interface | 14 |

List of Tables

| | |
|--|----|
| Table 1-1 Terms and Abbreviations | 1 |
| Table3-1 SRAM Interface Signal Definition..... | 4 |
| Table3-2 UART Side Signal Definition | 4 |
| Table3-3 UART Slave Signal Definition | 5 |
| Table4-1 Gowin UART Master IP Register | 7 |
| Table4-2 Receive Buffer Register Bit Definition | 7 |
| Table4-3 Transmit Holding Register Bit Definitions..... | 7 |
| Table4-4 Interrupt Enable Register Bit Definition | 8 |
| Table4-5 Interrupt Identification Register Bit Definition..... | 8 |
| Table4-6 Line Control Register | 9 |
| Table4-7 Modem Control Register | 9 |
| Table4-8 Line Status Register | 10 |
| Table4-9 Modem Status Register..... | 11 |

1 About This Manual

1.1 Manual Content

The Gowin UART Master and Slave User Guide mainly includes function introduction, signal definition, working principle, GUI call, etc., which are designed to help users quickly understand the features and usage of Gowin UART Master IP and Slave reference design.

1.2 Applicable Products

The information described in this manual applies to the following products:

- GW1N series of FPGA products: GW1N-1, GW1N-1S, GW1N-2, GW1N-2B, GW1N-4, GW1N-4B, GW1N-6, GW1N-9
- GW1NR series of FPGA products: GW1NR-4, GW1NR-4B, GW1NR-9
- GW1NS series of FPGA products: GW1NS-2, GW1NS-2C
- GW1NSR series of FPGA products: GW1NSR-2, GW1NSR-2C
- GW1NZ series of FPGA products: GW1NZ-1
- GW2A series of FPGA products: GW2A-18, GW2A-55
- GW2AR series of FPGA products: GW2AR-18

1.3 Related Documents

The latest user guides are available on the Gowin website. Refer to the related documents at www.gowinsemi.com

- [DS100](#), GW1N Series of FPGA Product Data Sheet
- [DS117](#), GW1NR Series of FPGA Product Data Sheet
- [DS821](#), GW1NS Series of FPGA Product Data Sheet
- [DS861](#), GW1NSR Series of FPGA Product Data Sheet
- [DS841](#), GW1NZ Series of FPGA Product Data Sheet
- [DS102](#), GW2A Series of FPGA Product Data Sheet
- [DS226](#), GW2AR Series of FPGA Product Data Sheet
- [SUG100](#), Gowin YunYuan Software User Guide

1.4 Terms and Abbreviations

The abbreviations and terminology used in this manual are as shown in Table 1-1 below.

Table 1-1 Terms and Abbreviations

| Terms and abbreviations | Full name |
|-------------------------|-------------------------------|
| FPGA | Field Programmable Gate Array |

| Terms and abbreviations | Full name |
|-------------------------|---|
| SRAM | Static Random Access Memory |
| UART | Universal Asynchronous Receiver/Transmitter |

1.5 Technical Support and Feedback

Gowin Semiconductor provides customers with comprehensive technical support. If you have any questions, comments, or suggestions, please feel free to contact us directly using the information provided below.

URL: www.gowinsemi.com

E-mail: support@gowinsemi.com

Tel: +86 755 8262 0391

2Function Introduction

2.1 Overview

The Universal Asynchronous Receiver/Transmitter, commonly referred to as the UART, is an asynchronous transceiver.

Gowin UART Master IP is a UART Master controller with synchronous SRAM interface, and the external connection standard RS-232 interface. Data is converted between serial communication and parallel communication.

The Gowin UART Slave reference design has the function of receiving and transmitting data, and is mainly used to communicate with the UART Master.

2.2 Features

2.2.1 Gowin UART Master IP

- Support 5-bit, 6-bit, 7-bit or 8-bit data bits;
- Support odd parity, even parity or no parity;
- Support 1 stop bit, 1.5 stop bit or 2 stop bits;
- Built-in baud rate generator;
- With modem control
- A transmit and receive FIFO with a depth of 16 bytes.

2.2.2 Gowin UART Slave Reference Design

With sending and receiving functions;

- Support 5-bit, 6-bit, 7-bit or 8-bit data bits;
- Support odd parity, even parity or no parity;
- Support 1 stop bit, 1.5 stop bit or 2 stop bits.

3 Signal Definition

3.1 Gowin UART Master IP

3.1.1 SRAM Interface Signal

Table3-1 SRAM Interface Signal Definition

| No. | Signal name | I/O | Description | Remarks |
|-----|-------------|-----|-------------------------------------|-----------------------------------|
| 1 | I_CLK | I | Working clock, rising edge sampling | - |
| 2 | I_RESETN | I | Reset signal | - |
| 3 | I_TX_EN | I | Write enable signal | SRAM write address channel signal |
| 4 | I_WADDR | I | Write data signal | |
| 5 | I_WDATA | O | Write address preparation | RSAM read address channel signal |
| 6 | I_RX_EN | I | Read enable signal | |
| 7 | I_RADDR | I | Read address signal | |
| 8 | O_RDATA | O | Read data signal | |

3.1.2 UART Side Signal

Table3-2 UART Side Signal Definition

| No. | Signal name | I/O | Description | Remarks |
|-----|------------------|-----|--|-----------------|
| 1 | SIN | I | Serial data input | - |
| 2 | RxRDYn | O | Ready to receive | - |
| 3 | SOUT | O | Serial data output | - |
| 4 | TxRDYn | O | Ready to send | - |
| 5 | DDIS | O | Disable driver | - |
| 6 | INTR | O | Interrupt signal | - |
| 7 | DCDn | I | Data carrier detection, low effective | Modem interface |
| 8 | CTS _n | I | Run send, low effective | |
| 9 | DSR _n | I | Data communication equipment is ready, low effective | |
| 10 | RI _n | I | Ringing prompt, low effective | |
| 11 | DTR _n | O | Data terminal is ready, low effective | |

| No. | Signal name | I/O | Description | Remarks |
|-----|-------------|-----|--------------------------------|---------|
| 12 | RTSn | O | Request to send, low effective | |

3.2 Gowin UART Slave

Table3-3 UART Slave Signal Definition

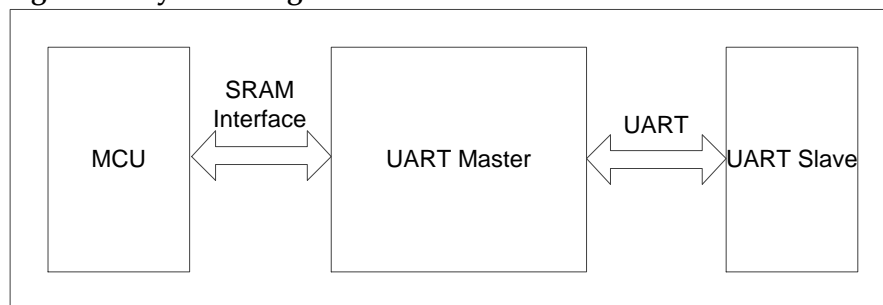
| No. | Signal name | I/O | Description | Remarks |
|-----|-------------|-----|----------------------|---------|
| 1 | SCLK | I | Clock signal | - |
| 2 | RSTN | I | Reset signal | - |
| 3 | TXD | O | Serial output signal | - |
| 4 | RXD | I | Serial input signal | - |

4 Working Principle

4.1 System Diagram

The UART Master IP acts as a "bridge." The main controller transmits the command or data to the UART Master IP through synchronous SRAM interface, and then the UART Master IP is sent to the UART Slave through the UART; or uploads the UART Slave data to the main controller through synchronous SRAM interface shown in Figure 4-1.

Figure 4-1 System Diagram



4.2 Gowin UART Master IP Register

Gowin UART Master IP has 8 registers:

- Receive Buffer Register (RBR)
- Transmit Holding Register (THR)
- Interrupt Enable Register (IER)
- Interrupt Identification Register (IIR)
- Line Control Register (LCR)
- Modem Control Register (MCR)
- Line Status Register (LSR)
- Modem Status Register (MSR)

Note!

The receive buffer register (RBR) and the transmit hold register (THR) have the same address, both of which are 0x00.

Table4-1 Gowin UART Master IP Register

| Register name | Register address | Register bit width | Types | Description |
|---------------|------------------|--------------------|-------|-----------------------------------|
| RBR | 0x00 | 8 | read | Receive Buffer Register |
| THR | 0x00 | 8 | write | Transmit Holding Register |
| IER | 0x01 | 8 | write | Interrupt Enable Register |
| IIR | 0x02 | 8 | read | Interrupt Identification Register |
| LCR | 0x03 | 7 | write | Line Control Register |
| MCR | 0x04 | 8 | write | Modem Control Register |
| LSR | 0x05 | 7 | read | Line State Register |
| MSR | 0x06 | 8 | read | Modem Status Register |

4.2.1 Receive Buffer Register (RBR)

The receive buffer register is shown in Figure4-2. The specific bit definition of the register is shown in Table4-2.

Figure4-2 Receive Buffer Register

| | | | |
|----------|---|-----|---|
| 31 | 8 | 7 | 0 |
| Reserved | | RBR | |

Table4-2 Receive Buffer Register Bit Definition

| Bit | Name | Defaults | Access type | Description |
|------|----------|----------|-------------|------------------------------|
| 31:8 | Reserved | N/A | N/A | Reserved |
| 7:0 | RBR | 0x0 | read | Cache the last received byte |

4.2.2 Transmit Holding Register (THR)

The transmit holding register is shown in Figure4-3. The transmit holding register contains the data to be sent next time. The specific bit definitions are shown in Table4-3.

Figure4-3 Transmit Holding Register

| | | | |
|----------|---|-----|---|
| 31 | 8 | 7 | 0 |
| Reserved | | THR | |

Table4-3 Transmit Holding Register Bit Definitions

| Bit | Name | Defaults | Access type | Description |
|------|----------|----------|-------------|-------------------------|
| 31:8 | Reserved | N/A | N/A | Reserved |
| 7:0 | THR | 0x0 | write | Keep the last sent byte |

4.2.3 Interrupt Enable Register (IER)

The interrupt enable register is shown in Figure4-4. The interrupt enable register contains the bits that make the interrupt valid. The bit definition is shown in Table4-4.

Figure4-4 Interrupt Enable Register

| | | | | | | | |
|----------|---|------|---|-----|------|------|------|
| 31 | 8 | 7 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | 0000 | | MSI | RLSI | THRI | RHRI |

Table4-4 Interrupt Enable Register Bit Definition

| Bit | Name | Defaults | Access type | Description |
|-----|------|----------|-------------|--|
| 31 | 4 | Reserved | N/A | Reserved |
| 3 | MSI | 0x0 | write | Modem status interrupt enable <ul style="list-style-type: none"> ● 0: Disable Modem status interrupt ● 1: Enable Modem status interrupt |
| 2 | RLSI | 0x0 | write | Receive line status interrupt enable <ul style="list-style-type: none"> ● 0: Disable receive line status interrupt ● 1: Enable Receive Line Status Interrupt |
| 1 | THRI | 0x0 | write | Transmit Holding Register Empty Interrupt Enable <ul style="list-style-type: none"> ● 0: Disable transmit hold register empty interrupt ● 1: Enable transmit hold register empty interrupt |
| 0 | RBRI | 0x0 | write | Receive data valid interrupt enable <ul style="list-style-type: none"> ● 0: Disable receive data valid interrupt ● 1: Enable receive data valid interrupt |

4.2.4 Interrupt Identification Register (IIR)

The interrupt identification register is shown in Figure4-5. The interrupt identifier register contains the priority of the interrupt identifier. The bit definition is shown in Table4-5.

Figure4-5 Interrupt Identification Register

| | | | | | | | |
|----------|---|------|---|------|------|------|----------|
| 31 | 8 | 7 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | 0000 | | INT2 | INT1 | INT0 | INT STAT |

Table4-5 Interrupt Identification Register Bit Definition

| Bit | Name | Defaults | Access type | Description |
|------|----------|----------|-------------|---|
| 31:4 | Reserved | N/A | N/A | Reserved |
| 3 | INT2 | 0x0 | read | FIFO enable <ul style="list-style-type: none"> ● 0:16450 mode ● 1:16550 mode |
| 2 | INT1 | 0x0 | read | Interrupt identifier <ul style="list-style-type: none"> ● 11: Receive line status (highest priority) ● 10: Receive data available (Level 2) ● 01: Send Hold Register Empty (Level 3) ● 00: Modem status (Level 4) |
| 1 | INT0 | | | |
| 0 | INT STAT | 0x1 | read | 0: Interrupt waiting |

| Bit | Name | Defaults | Access type | Description |
|-----|------|----------|-------------|----------------------------|
| | | | | 1: No interruption waiting |

4.2.5 Line Control Register (LCR)

The line control register is shown in Figure4-6. The line control register contains the serial communication configuration bits as defined in Table4-6.

Figure4-6 Line Control Register

| | | | | | | | | |
|----------|---|----|----|-----|-----|-----|-----|---|
| 31 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | SB | SP | EPS | EPN | STB | WLS | |

Table4-6 Line Control Register

| Bit | Name | Defaults | Access type | Description |
|------|----------|----------|-------------|---|
| 31:7 | Reserved | N/A | write | Reserved |
| 6 | SB | 0x0 | write | Setup interruption <ul style="list-style-type: none"> ● 1: Start interrupt ● 0: Disable interrupt |
| 5 | SP | 0x0 | write | Forced parity <ul style="list-style-type: none"> ● 1: When the 3, 4 bits are logic 1, the parity bit is transmitted and forced to logic 0; When bit 4 is logic 0 and bit 3 is logic 1, the parity bit is transmitted and forced to logic 1 ● 0: Disable forced parity |
| 4 | EPS | 0x0 | write | Check selection <ul style="list-style-type: none"> ● 1: Select even parity ● 0: Select odd parity |
| 3 | PEN | 0x0 | write | Parity enable <ul style="list-style-type: none"> ● 1: Enable parity ● 0: Disable parity |
| 2 | STB | 0x0 | write | Number of stop bits <ul style="list-style-type: none"> ● 0: 1 stop bit ● 1: 2 stop bits, select 1.5 stop bits when transferring 5 data bits. The reception only detects one stop bit and does not care about the number of selected stop bits. |
| 1:0 | WLS | 0x0 | write | Byte length selection <ul style="list-style-type: none"> ● 00: 5-bit data ● 01: 6-bit data ● 10: 7-bit data ● 11: 8-bit data |

4.2.6 Modem Control Register (MCR)

The modem control register is shown in Figure4-7. The modem control register contains the modem signal configuration bits. The bit definitions are shown in Table4-7.

Figure4-7 Modem Control Register

| | | | | | |
|----------|---|--------|---|-----|-----|
| 31 | 8 | 7 | 2 | 1 | 0 |
| Reserved | | 000000 | | RTS | DTR |

Table4-7 Modem Control Register

| Bit | Name | Defaults | Access type | Description |
|------|----------|----------|-------------|-----------------|
| 31:8 | Reserved | N/A | N/A | Reserved |
| 7:2 | N/A | 0x0 | write | Always "000000" |

| Bit | Name | Defaults | Access type | Description |
|-----|------|----------|-------------|--|
| 1 | RTS | 0x0 | write | Request to send <ul style="list-style-type: none"> ● 1: Drive RTS_n signal is low ● 0: Drive RTS_n signal is high |
| 0 | DTR | 0x0 | write | The data terminal is ready <ul style="list-style-type: none"> ● 1: Drive DTR_n signal is low ● 0: Drive DTR_n signal is high |

4.2.7 Line Status Register (LSR)

The line status register is shown in Figure4-8. The line status register contains the current transmit and receive status. The bit definitions are shown in Table4-8.

Figure4-8 Line Status Register

| | | | | | | | | |
|----------|---|------|------|----|----|----|----|-------|
| 31 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | TEMT | THRE | BI | FE | PE | OE | RxRDY |

Table4-8 Line Status Register

| Bit | Name | Defaults | Access type | Description |
|------|----------|----------|-------------|---|
| 31:7 | Reserved | N/A | N/A | Reserved |
| 6 | TEMT | 0x1 | read | Send empty <ul style="list-style-type: none"> ● 0: THR or Transmit Shift Register contains data ● 1: THR or Transmit Shift Register is empty. In FIFO mode, both transmit FIFO and shift register are empty. |
| 5 | THRE | 0x1 | read | Transmit Holding Register (THR) is <ul style="list-style-type: none"> ● 0: THR or FIFO has data to send ● 1: THR is empty. In FIFO mode, the transmit FIFO is empty. |
| 4 | BI | 0x0 | read | Break Interrupt. Set this interrupt when SIN is held low for the entire data transfer (start bit + data bit + parity + stop bit) |
| 3 | FE | 0x0 | read | Frame error. The transmission loses a stop bit. After the frame error, the UART assumes that the frame error is caused by the start bit of the next transmission. Try to resynchronize by sampling the start bit twice and receiving the next data. |
| 2 | PE | 0x0 | read | Parity error |

| Bit | Name | Defaults | Access type | Description |
|-----|-------|----------|-------------|---|
| | | | | It means that the received data does not have the correct even or odd number, which is inconsistent with the setting by the check selection bit. |
| 1 | OE | 0x0 | read | Overflow error The RBR was not read before the next data reception, thus destroying the previous data. In FIFO mode, the overflow error is sent as the FIFO is full, and the receive shift register has completed the next data reception. |
| 0 | RxRDY | 0x0 | read | Data is ready <ul style="list-style-type: none"> ● 0: All RBR and FIFO have been read ● 1: The data has been received and transferred to the RBR FIFO |

4.2.8 Modem Status Register (MSR)

The modem status register is shown in Figure4-9. The modem status register contains the status of the current modem interface. The bit definitions are shown in Table4-9.

Figure4-9 Modem Status Register

| | | | | | | | | | |
|----------|---|-----|----|-----|-----|------|------|------|------|
| 31 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Reserved | | DCD | RI | DSR | CTS | DDCD | TERI | DDSR | DCTS |

Table4-9 Modem Status Register

| Bit | Name | Defaults | Access type | Description |
|------|----------|----------|-------------|---|
| 31:8 | Reserved | N/A | N/A | Reserved |
| 7 | DCD | X | Read/write | Data carrier detection (low effective) 0: The data carrier has been detected by the modem or data device. |
| 6 | RI | X | Read/write | Ringing prompt |
| 5 | DSR | X | Read/write | Data communication equipment is ready (low effective) 0: The modem or data device is ready to establish a connection with the UART |
| 4 | CTS | X | Read/write | Allow to send (low effective) 0: Modem or data device is ready to exchange data |
| 3 | DDCD | 0x0 | Read/write | Delta Data Carrier Detect. Change in DCDN after last MSR read. |
| 2 | TERI | 0x0 | Read/write | Trailing Edge Ring Indicator. RIN has changed from a low to |

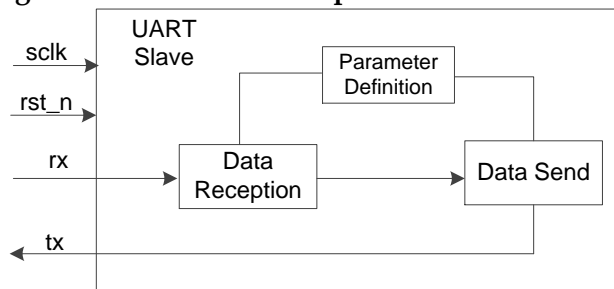
| Bit | Name | Defaults | Access type | Description |
|-----|------|----------|-------------|---|
| | | | | a High. |
| 1 | DDSR | 0x0 | Read/write | Delta Data Set Ready. Change in DSRN after last MSR read. |
| 0 | DCTS | 0x0 | Read/write | Delta Clear To Send. Change in CTSN after last MSR read. |

Note!

The default value is X: indicates that this bit is driven by an external input signal.

4.3 Gowin UART Slave Implementation

Figure4-10 UART Slave Implementation Block Diagram



The UART Slave reference design mainly includes a data receiving module and a data transmitting module. The data receiving module is configured to receive the serial data sent by the Master and convert it into parallel data transmission to the data sending module. The data sending module receives the parallel data sent by the data receiving module and converts it into serial data for transmission to the Master.

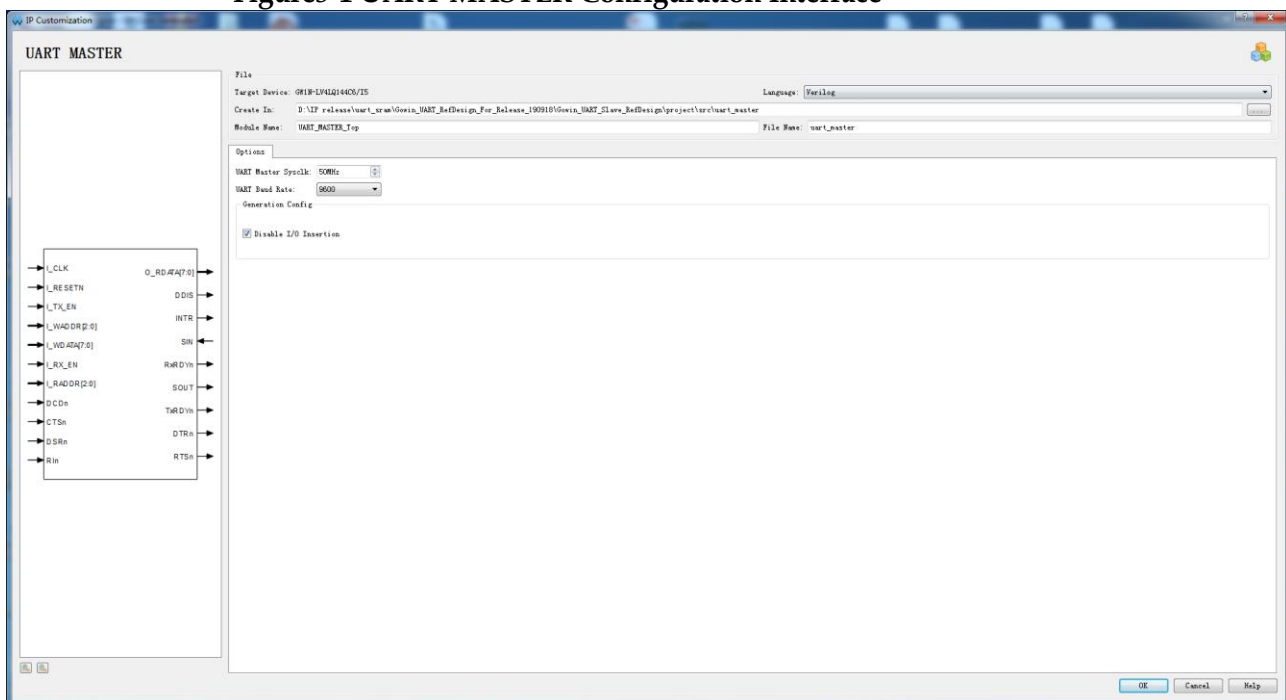
Parameter definitions are used to set the system clock frequency, baud rate, and data frame format.

5 Interface Configuration

Users can use the IP core generator tool in the IDE to call and configure Gowin UART MASTER IP.

5.1 UART MASTER IP Core Interface

UART MASTER configuration interface is as shown in Figure5-1.
Figure5-1 UART MASTER Configuration Interface

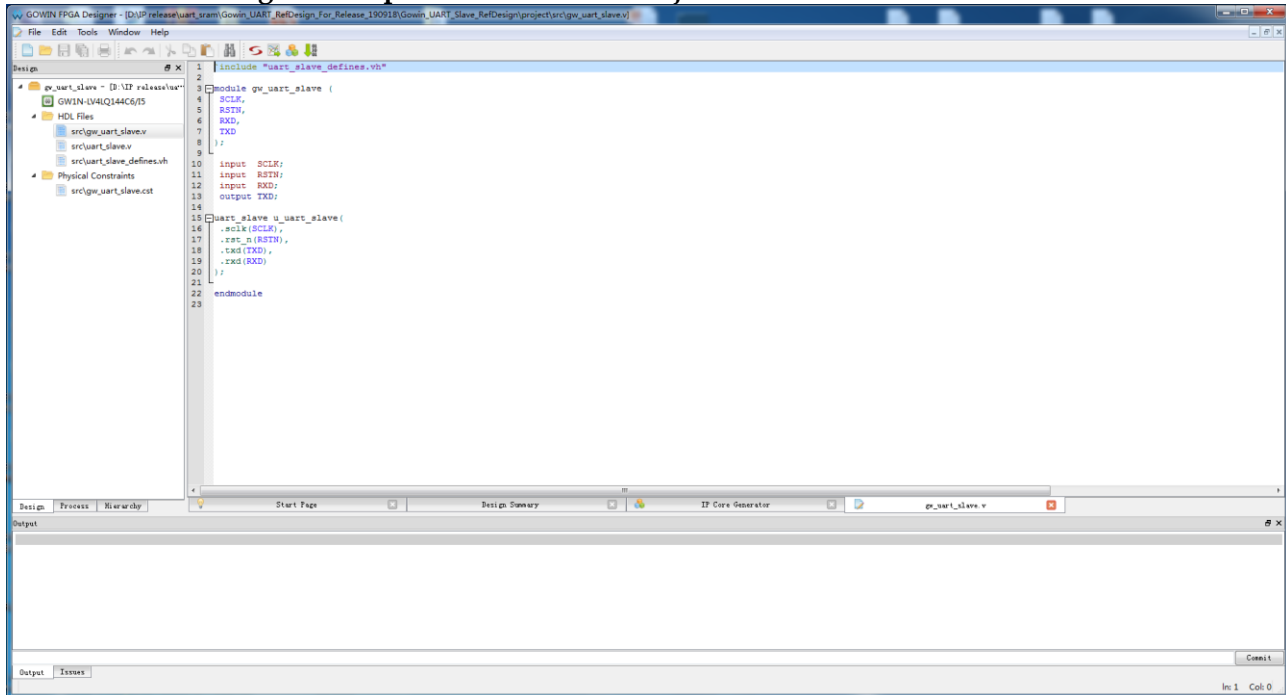


5.2 UART SLAVE Reference Design Project

Open Gowin YunYuan software, click “File > Open” to open the “Open File” dialog box, select the project file (*.gprj), and then open the project, as shown in Figure5-2.

There are three methods to open the project. Please refer to [SUG100, Gowin YunYuan Software User Guide > 5 Operation > Open an Existing Project.](#)

Figure5-2 Open UART SLAVE Project



5.3 Bitstream File Generation

Under necessary constraints, bitstream file can be generated after synthesis, placement and routing. Download the bitstream file to the development board or test board via Gowin USB cable. Observe the communication via the test interface.

6 Reference Design

For more details, please refer to the UART reference design at Gowin official website.