

# HCPL-1930, HCPL-1931, HCPL-193K, 5962-89572<sup>1</sup>



## Dual-Channel Line Receiver Hermetically Sealed Optocoupler

### Data Sheet

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#### Description

The HCPL-193x devices are dual-channel, hermetically sealed, high CMR, line receiver optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either a commercial product or with full MIL-PRF-38534 Class Level H or K testing, or from the DLA Standard Microcircuit Drawing (SMD) 5962-89572. This 16-pin DIP may be purchased with a variety of lead bend and plating options. See [Selection Guide — Lead Configuration Options](#) for details. Standard Microcircuit Drawing (SMD) parts are available for each lead style.

**CAUTION** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

#### Features

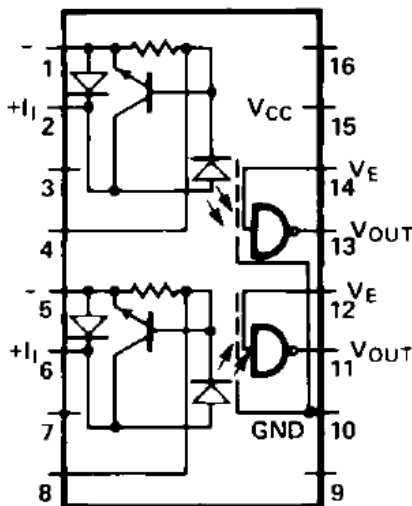
- Dual marked with device part number and DLA Standard Microcircuit Drawing (SMD)
- Manufactured and tested on a MIL-PRF-38534 certified line
- QML-38534, Class H and Class K
- Hermetically sealed 16-pin dual in-line package
- Performance guaranteed over full military temperature range:  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$
- High speed: 10 Mb/s
- Accepts a broad range of drive conditions
- Adaptive line termination included
- Internal shield provides excellent common mode rejection
- External base lead allows LED Peaking and LED current adjustment
- 1500 Vdc withstand test voltage
- High radiation immunity
- HCPL-2602 function compatibility
- Reliability data available

#### Applications

- Military and space
- High reliability systems
- Isolated line receiver
- Simplex/multiplex data transmission
- Computer-peripheral interface
- Microprocessor system interface
- Harsh environmental environments
- Digital isolation for A/D, D/A conversion
- Current sensing
- Instrument input/output isolation
- Ground loop elimination
- Pulse transformer replacement

1. See [Selection Guide — Lead Configuration Options](#) for available extensions.

## Functional Diagram



### Truth Table (Positive Logic)

| Input | Enable | Output |
|-------|--------|--------|
| On    | H      | L      |
| Off   | H      | H      |
| On    | L      | H      |
| Off   | L      | H      |

**NOTE** The connection of a 0.1- $\mu$ F bypass capacitor between pins 15 and 10 is recommended.

All devices are manufactured and tested on a MIL-PRF-38534 certified line and Class H and K devices are included in the DLA Qualified Manufacturers List QML-38534 for Hybrid Microcircuits.

Each unit contains two independent channels, consisting of a GaAsP light emitting diode, an input current regulator, and an integrated high gain photon detector. The input regulator serves as a line termination for line receiver applications. It clamps the line voltage and regulates the LED current so line reflections do not interfere with circuit performance. The regulator allows a typical LED current of 12.5 mA before it starts to shunt excess current. The output of the detector IC is an open collector Schottky clamped transistor. An enable input gates the detector. The internal detector shield provides a guaranteed common mode transient immunity specification of +1000 V/ $\mu$ s.

DC specifications are compatible with TTL logic and are guaranteed from  $-55^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  allowing trouble-free interfacing with digital logic circuits. An input current of 10 mA will sink a six gate fan-out (TTL) at the output with a typical propagation delay from input to output of only 45 ns.

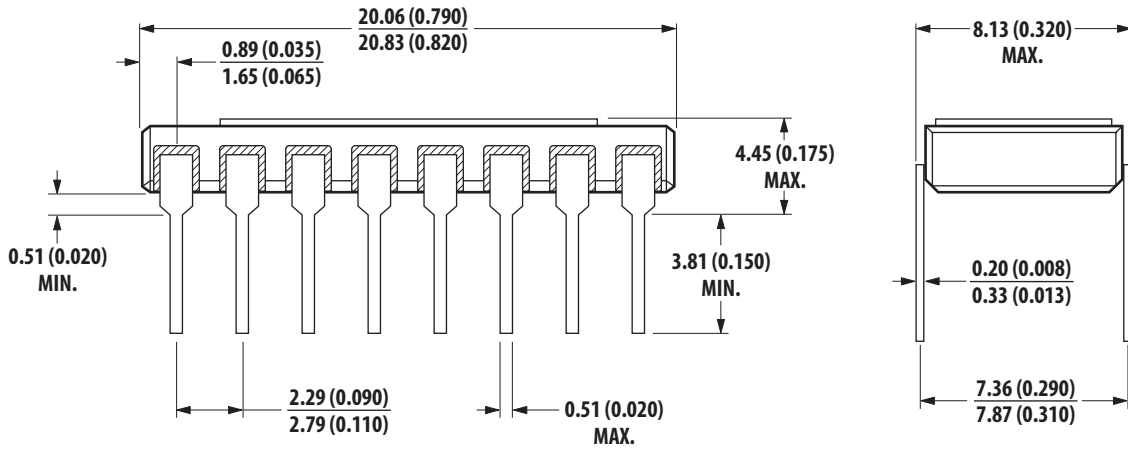
## Selection Guide — Lead Configuration Options

| Part Number and Options            |             |
|------------------------------------|-------------|
| Commercial                         | HCPL-1930   |
| MIL-PRF-38534 Class H              | HCPL-1931   |
| MIL-PRF-38534 Class K              | HCPL-193K   |
| Standard Lead Finish <sup>a</sup>  | Gold        |
| Solder Dipped <sup>b</sup>         | Option #200 |
| Butt Joint/Gold Plate <sup>a</sup> | Option #100 |
| Gull Wing/Soldered <sup>b</sup>    | Option #300 |
| Crew Cut/Gold Plate <sup>a</sup>   | Option #600 |
| <b>Class H SMD Part Number</b>     |             |
| <i>Prescript for all below</i>     | 5962-       |
| Gold Plate <sup>a</sup>            | 8957201EC   |
| Solder Dipped <sup>b</sup>         | 8957201EA   |
| Butt Joint/Gold Plate <sup>a</sup> | 8957201YC   |
| Butt Joint/Soldered <sup>b</sup>   | 8957201YA   |
| Gull Wing/Soldered <sup>b</sup>    | 8957201XA   |
| Crew Cut/Gold Plate <sup>a</sup>   | Available   |
| Crew Cut/Soldered <sup>b</sup>     | Available   |
| <b>Class K SMD Part Number</b>     |             |
| <i>Prescript for all below</i>     | 5962-       |
| Gold Plate <sup>a</sup>            | 8957202KEC  |
| Solder Dipped <sup>b</sup>         | 8957202KEA  |
| Butt Joint/Gold Plate <sup>a</sup> | 8957202KYC  |
| Butt Joint/Soldered <sup>b</sup>   | 8957202KYA  |
| Gull Wing/Soldered <sup>b</sup>    | 8957202KXA  |

- a. Gold Plate lead finish: Maximum gold thickness of leads is <100 micro inches. Typical is 60 to 90 micro inches.
- b. Solder lead finish: Sn63/Pb37.

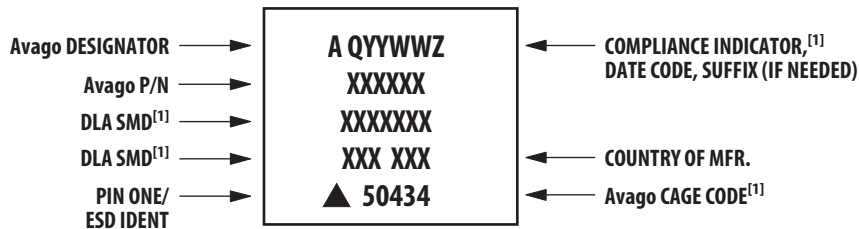
## Outline Drawings

### 16-Pin DIP Through Hole, 2 Channels



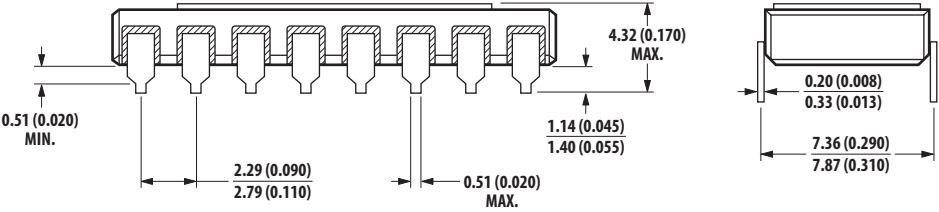
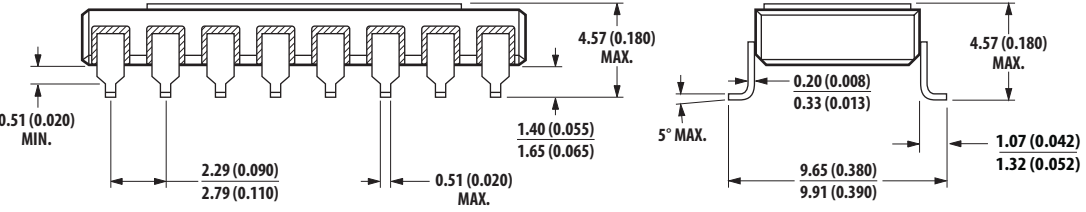
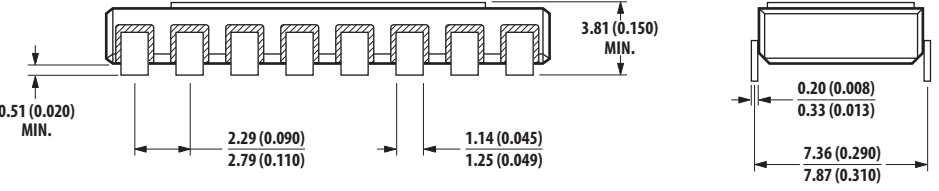
Note: Dimensions in millimeters (inches).

## Device Marking



[1] QML PARTS ONLY

## Hermetic Optocoupler Options

| Option | Description   |
|--------|---|
| 100    | <p>Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on Commercial, Class H, and Class K product.</p>   |
| 200    | <p>Lead finish is solder dipped rather than gold plated. This option is available on Commercial, Class H, and Class K product. DLA Drawing (SMD) part numbers contain provisions for lead finish.</p>   |
| 300    | <p>Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on Commercial, Class H, and Class K product. This option has solder-dipped leads.</p>                                  |
| 600    | <p>Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on Commercial, Class H, and Class K product. Contact factory for the availability of this option on DLA part types.</p>  |

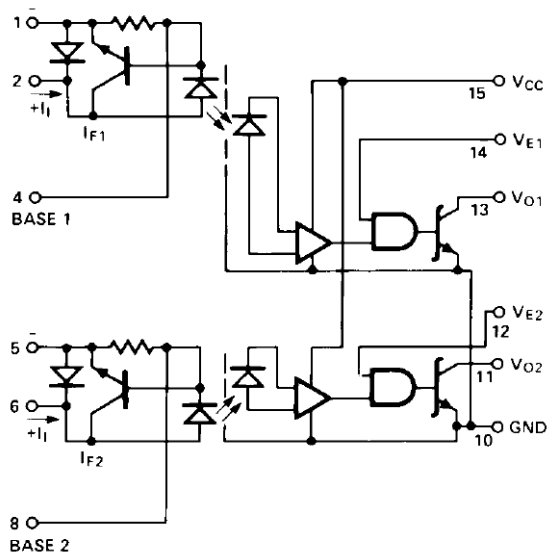
Note: Dimensions in millimeters (inches).

## Absolute Maximum Ratings

| Parameter   | Symbol   | Min | Max              | Unit | Note |
|---|----------|-----|------------------|------|------|
| Storage Temperature                               | $T_S$    | -65 | +150             | °C   |      |
| Operating Temperature                             | $T_A$    | -55 | +125             | °C   |      |
| Lead Solder Temperature                           |          | —   | 260 for 10 sec   | °C   |      |
| Forward Input Current (each channel)              | $I_I$    | —   | 60               | mA   | a    |
| Reverse Input Current                             | $I_R$    | —   | 60               | mA   |      |
| Supply Voltage (1 minute max)                     | $V_{CC}$ | —   | 7.0              | V    |      |
| Enable Input Voltage (each channel)               | $V_E$    | —   | 5.5 <sup>b</sup> | V    |      |
| Output Collector Current (each channel)           | $I_O$    | —   | 25               | mA   |      |
| Output Collector Power Dissipation (each channel) | $P_O$    | —   | 40               | mW   |      |
| Output Collector Voltage (each channel)           | $V_O$    | —   | 7                | V    |      |
| Total Package Power Dissipation                   |          | —   | 564              | mW   |      |
| Input Power Dissipation (each channel)            |          | —   | 168              | mW   |      |

- a. Derate linearly at 1.2 mA/°C above  $T_A = 100^\circ\text{C}$ .
- b. Not to exceed  $V_{CC}$  by more than 500 mV.

## Schematic



Notes: The connection of a 0.1- $\mu\text{F}$  bypass capacitor between pins 15 and 10 is recommended. Bypassing of the power supply line is required, with a 0.1- $\mu\text{F}$  ceramic disc capacitor adjacent to each isolator. The power supply bus for the isolators should be separate from the bus for any active loads, otherwise additional bypass capacitance may be needed to suppress regenerative feedback via the power supply.

## ESD Classification

|                            |            |
|----------------------------|------------|
| (MIL-STD-883, Method 3015) | ▲, Class 1 |
|----------------------------|------------|

## Recommended Operating Conditions

| Parameter                              | Symbol   | Min  | Max      | Unit               |
|--|----------|------|----------|--------------------|
| Input Current, Low Level               | $I_{IL}$ | 0    | 250      | $\mu\text{A}$      |
| Input Current, High Level <sup>a</sup> | $I_{IH}$ | 12.5 | 60       | mA                 |
| Supply Voltage, Output                 | $V_{CC}$ | 4.5  | 5.5      | V                  |
| High Level Enable Voltage              | $V_{EH}$ | 2.0  | $V_{CC}$ | V                  |
| Low Level Enable Voltage               | $V_{EL}$ | 0    | 0.8      | V                  |
| Fan Out (at $R_L = 4\text{ k}\Omega$ ) | N        | —    | 5        | TTL Loads          |
| Operating Temperature                  | $T_A$    | -55  | 125      | $^{\circ}\text{C}$ |

a. 12.5-mA condition permits at least 20% guardband for optical coupling variation. Initial switching threshold is 10 mA or less.

## Electrical Specifications

$T_A = -55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$  unless otherwise stated.

| Parameter                                   | Symbol    | Test Conditions  | Group A Subgroups <sup>a</sup> | Limits |                  |      | Unit          | Fig  | Note |
|---|-----------|--|--------------------------------|--------|------------------|------|---------------|------|------|
|   |           |  |                                | Min    | Typ <sup>b</sup> | Max  |               |      |      |
| High Level Output Current                   | $I_{OH}$  | $V_{CC} = 5.5\text{V}, V_O = 5.5\text{V}$<br>$I_I = 250\ \mu\text{A}, V_E = 2.0\text{V}$         | 1, 2, 3                        | —      | 20               | 250  | $\mu\text{A}$ | 3    | c    |
| Low Level Output Voltage                    | $V_{OL}$  | $V_{CC} = 5.5\text{V}; I_I = 10\text{ mA}$<br>$V_E = 2.0\text{V},$<br>$I_{OL}$ (Sinking) = 10 mA | 1, 2, 3                        | —      | 0.3              | 0.6  | V             | 1    | c    |
| Input Voltage                               | $V_I$     | $I_I = 10\text{ mA}$   | 1, 2, 3                        | —      | 2.2              | 2.6  | V             | 2    | c    |
|   |           | $I_I = 60\text{ mA}$   |                                | —      | 2.35             | 2.75 |               |      |      |
| Input Reverse Voltage                       | $V_R$     | $I_R = 10\text{ mA}$   | 1, 2, 3                        | —      | 0.8              | 1.10 | V             |      | c    |
| Low Level Enable Current                    | $I_{EL}$  | $V_{CC} = 5.5\text{V}, V_E = 0.5\text{V}$  | 1, 2, 3                        | —      | -1.45            | -2.0 | mA            |      | c    |
| High Level Enable Current                   | $I_{EH}$  | $V_{CC} = 5.5\text{V}, V_E = 1.7\text{V}$  | 1, 2, 3                        | —      | —                | -1.5 | mA            |      | c    |
| High Level Enable Voltage                   | $V_{EH}$  | —  | 1, 2, 3                        | 2.0    | —                | —    | V             |      | c, d |
| Low Level Enable Voltage                    | $V_{EL}$  | —  | 1, 2, 3                        | —      | —                | 0.8  | V             |      | c    |
| High Level Supply Current                   | $I_{CCH}$ | $V_{CC} = 5.5\text{V}; I_I = 0,$<br>$V_E = 0.5\text{V}$ both channels                            | 1, 2, 3                        | —      | 21               | 28   | mA            |      |      |
| Low Level Supply Current                    | $I_{CCL}$ | $V_{CC} = 5.5\text{V}; I_I = 60\text{ mA},$<br>$V_E = 0.5\text{V}$ both channels                 | 1, 2, 3                        | —      | 27               | 36   | mA            |      |      |
| Input-Output Insulation Leakage Current     | $I_{I-O}$ | Relative Humidity $\leq 65,$<br>$t = 5\text{ s}, V_{I-O} = 1500\text{ Vdc}$                      | 1                              | —      | —                | 1    | $\mu\text{A}$ |      | e    |
| Propagation Delay Time to High Output Level | $t_{PLH}$ | $R_L = 510\Omega; C_L = 50\text{ pF},$<br>$I_I = 13\text{ mA}, V_{CC} = 5.0\text{ V}$            | 9                              | —      | 55               | 100  | ns            | 4, 5 | c, f |
|   |           |  | 10, 11                         | —      | —                | 140  |               |      |      |

| Parameter   | Symbol    | Test Conditions   | Group A Subgroups <sup>a</sup> | Limits |                  |     | Unit       | Fig  | Note    |
|---|-----------|---|--------------------------------|--------|------------------|-----|------------|------|---------|
|   |           |   |                                | Min    | Typ <sup>b</sup> | Max |            |      |         |
| Propagation Delay Time to Low Output Level          | $t_{PHL}$ | $R_L = 510\Omega; C_L = 50 \text{ pF}, I_I = 13 \text{ mA}, V_{CC} = 5.0V$                                    | 9                              | —      | 60               | 100 | ns         | 4, 5 | c, g    |
|   |           |   | 10, 11                         | —      | —                | 120 |            |      |         |
| Common Mode Transient Immunity at High Output Level | $ CM_H $  | $V_{CM} = 50V \text{ (peak)}, V_O \text{ (min.)} = 2V, R_L = 510\Omega; I_I = 0 \text{ mA}, V_{CC} = 5.0V$    | 9, 10, 11                      | 1000   | 10,000           | —   | V/ $\mu$ s | 8, 9 | c, h, i |
| Common Mode Transient Immunity at Low Output Level  | $ CM_L $  | $V_{CM} = 50V \text{ (peak)}, V_O \text{ (max.)} = 0.8V, R_L = 510\Omega; I_I = 10 \text{ mA}, V_{CC} = 5.0V$ | 9, 10, 11                      | 1000   | 10,000           | —   | V/ $\mu$ s | 8, 9 | c, j, i |

- a. Commercial parts receive 100% testing at 25°C (Subgroups 1 and 9). Class H and K parts receive 100% testing at 25, 125, and -55° C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
- b. All typical values are at  $V_{CC} = 5V, T_A = 25^\circ\text{C}$ .
- c. Each channel.
- d. No external pull-up is required for a high logic state on the enable input.
- e. Device considered a two terminal device: pins 1 through 8 are shorted together, and pins 9 through 16 are shorted together.
- f. The  $t_{PLH}$  propagation delay is measured from the 6.5-mA point on the trailing edge of the input pulse to the 1.5V point on the trailing edge of the output pulse.
- g. The  $t_{PHL}$  propagation delay is measured from the 6.5-mA point on the leading edge of the input pulse to the 1.5V point on the leading edge of the output pulse.
- h.  $CM_H$  is the maximum tolerable rate of rise of the common mode voltage to assure that the output remains in a high logic state, i.e.,  $V_{OUT} > 2.0V$ .
- i. Parameters shall be tested as part of device initial characterization and after process changes. Parameters shall be guaranteed to the limits specified for all lots not specifically tested.
- j.  $CM_L$  is the maximum tolerable rate of fall of the common mode voltage to assure that the output remains in a low logic state, i.e.,  $V_{OUT} < 0.8V$ .

## Typical Specifications

$T_A = 25^\circ\text{C}, V_{CC} = 5V.$

| Parameter  | Symbol    | Typ       | Unit     | Test Conditions   | Fig. | Note |
|--|-----------|-----------|----------|---|------|------|
| Resistance (Input-Output)                                  | $R_{I-O}$ | $10^{12}$ | $\Omega$ | $V_{I-O} = 500 \text{ Vdc}$   |      | a, b |
| Capacitance (Input-Output)                                 | $C_{I-O}$ | 1.7       | pF       | $f = 1 \text{ MHz}$   |      | a, b |
| Input-Input Insulation Leakage Current                     | $I_{I-I}$ | 0.5       | nA       | $\leq 65\% \text{ Relative Humidity}, V_{I-I} = 500 \text{ Vdc}, t = 5s$                |      | c    |
| Resistance (Input-Input)                                   | $R_{I-I}$ | 1012      | $\Omega$ | $V_{I-I} = 500 \text{ Vdc}$   |      | c    |
| Capacitance (Input-Input)                                  | $C_{I-I}$ | 0.55      | pF       | $f = 1 \text{ MHz}$   |      | c    |
| Propagation Delay Time of Enable from $V_{EH}$ to $V_{EL}$ | $t_{ELH}$ | 35        | ns       | $R_L = 510\Omega, C_L = 15 \text{ pF}, I_I = 13 \text{ mA}, V_{EH} = 3V, V_{EL} = 0V$   | 6, 7 | a, d |
| Propagation Delay Time of Enable from $V_{EL}$ to $V_{EH}$ | $t_{EHL}$ | 35        | ns       |   | 6, 7 | a, e |
| Output Rise Time (10% to 90%)                              | $t_r$     | 30        | ns       | $R_L = 510\Omega, C_L = 15 \text{ pF}, I_I = 13 \text{ mA}$                             |      | a    |
| Output Fall Time (90% to 10%)                              | $t_f$     | 24        | ns       |   |      | a    |
| Input Capacitance  | $C_I$     | 60        | pF       | $f = 1 \text{ MHz}, V_I = 0, \text{ PINS } 1 \text{ to } 2 \text{ or } 5 \text{ to } 6$ |      | a    |

- a. Each channel.
- b. Measured between pins 1 and 2 or 5 and 6 shorted together, and pins 10 through 15 shorted together.
- c. Measured between adjacent input leads shorted together, i.e., between 1, 2, and 4 shorted together and pins 5, 6, and 8 shorted together.
- d. The  $t_{ELH}$  enable propagation delay is measured from the 1.5V point on the trailing edge of the enable input pulse to the 1.5V point on the trailing edge of the output pulse.
- e. The  $t_{EHL}$  enable propagation delay is measured from the 1.5V point on the leading edge of the enable input pulse to the 1.5V point on the leading edge of the output pulse.

Figure 1 Input-Output Characteristics

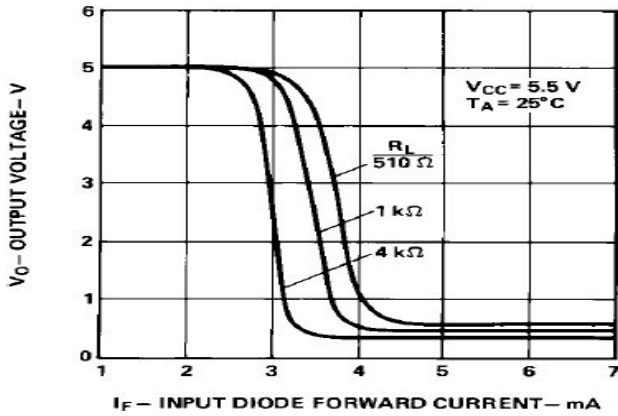


Figure 2 Input Characteristics

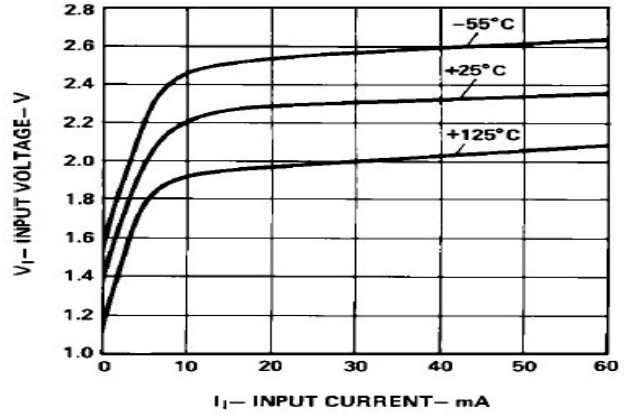


Figure 3 High Level Output Current vs. Temperature

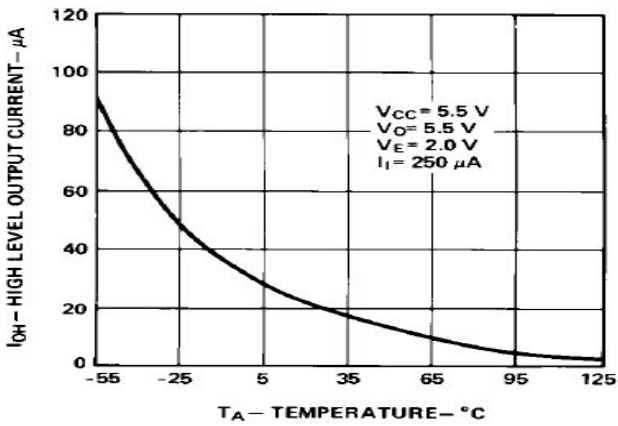


Figure 4 Propagation Delay vs. Temperature

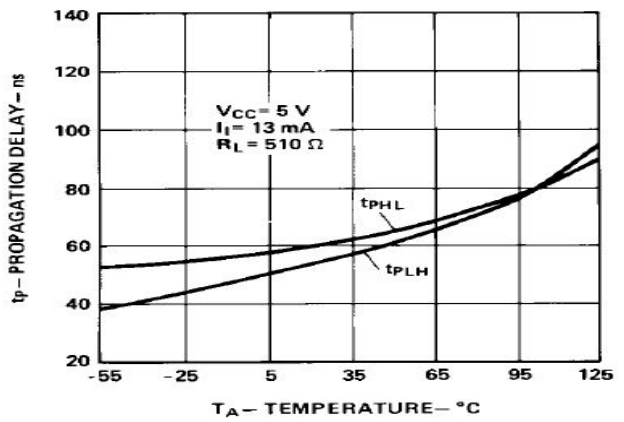


Figure 5 Enable Propagation Delay vs. Temperature

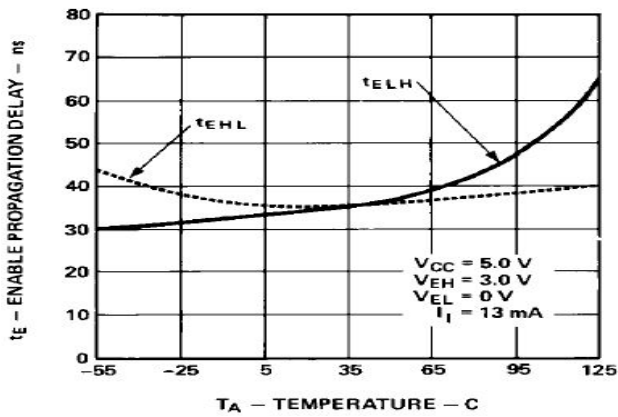




Figure 6 Test Circuit for  $t_{PHL}$  and  $t_{PLH}$

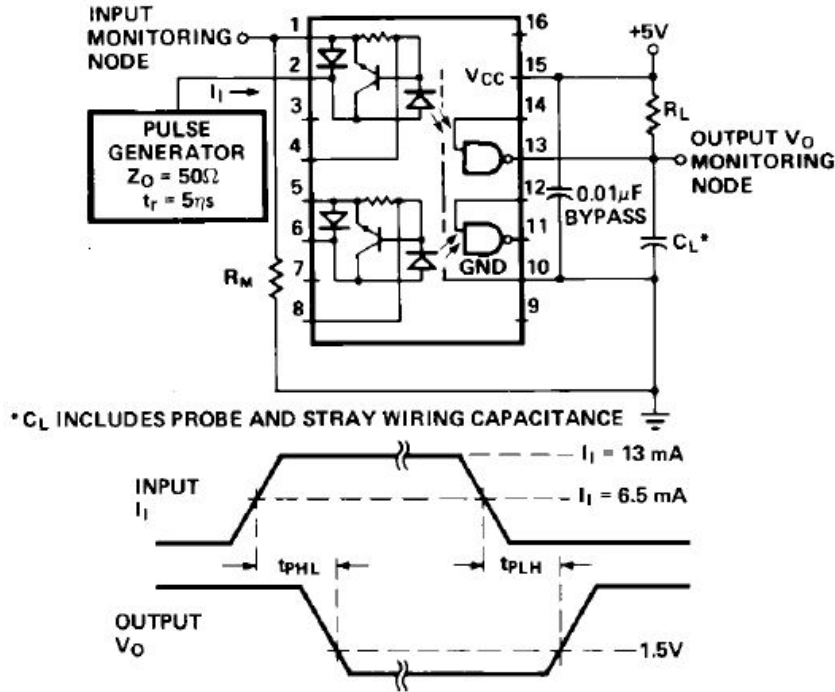


Figure 7 Test Circuit for  $t_{EHL}$  and  $t_{ELH}$

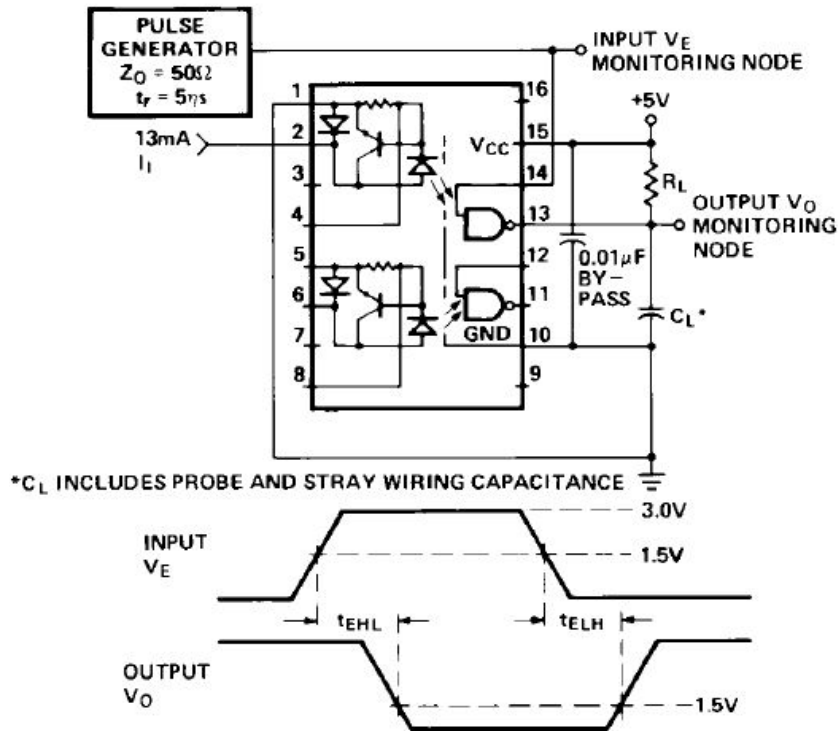


Figure 8 Typical Common Mode Transient Immunity

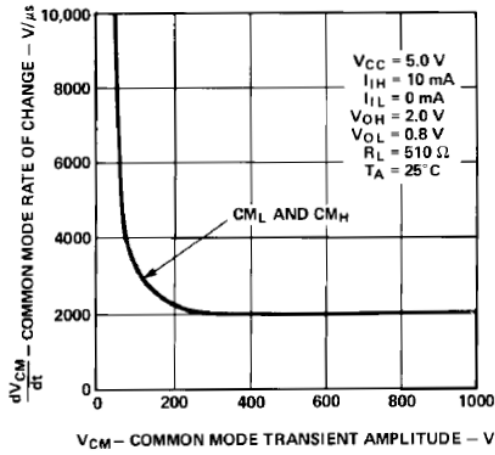


Figure 9 Test Circuit for Common Mode Transient Immunity and Typical Waveforms

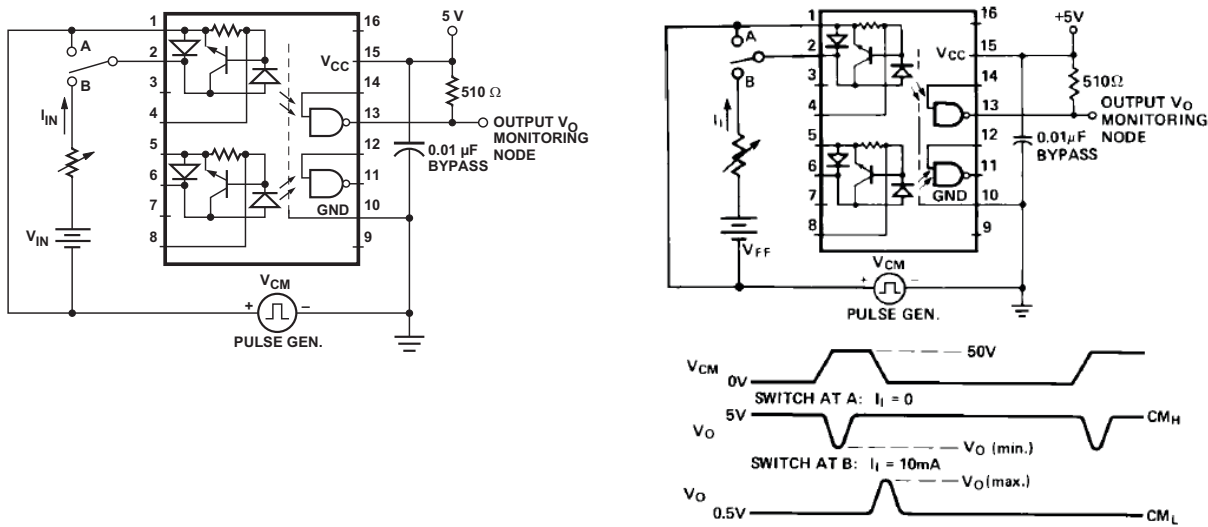
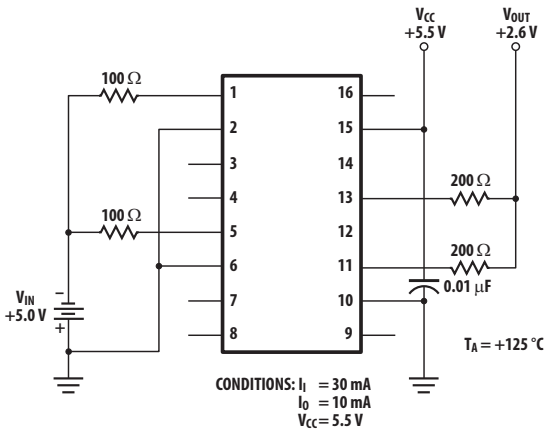
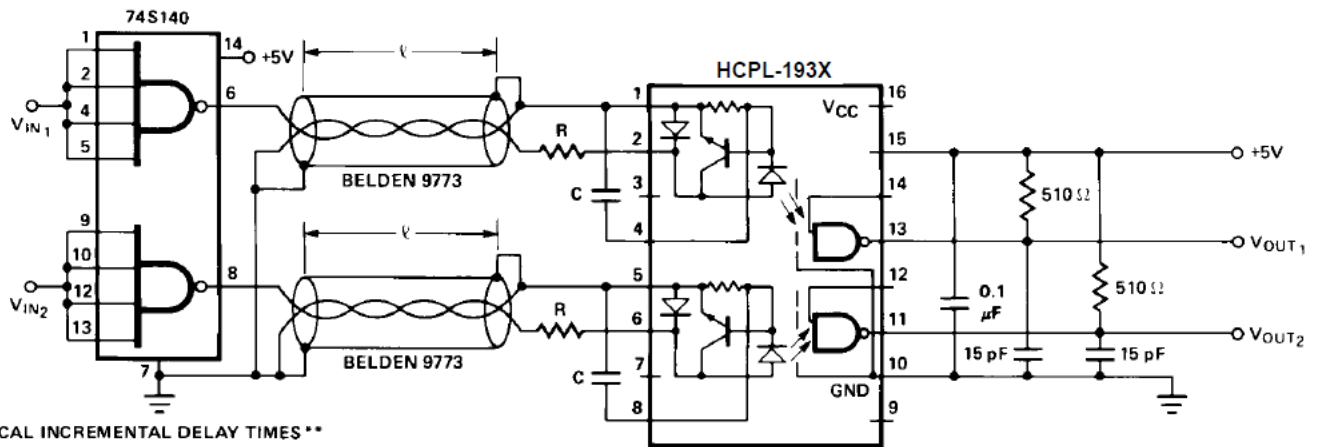


Figure 10 Burn In Circuit



## Application Circuits

Figure 11 Polarity Non-Reversing

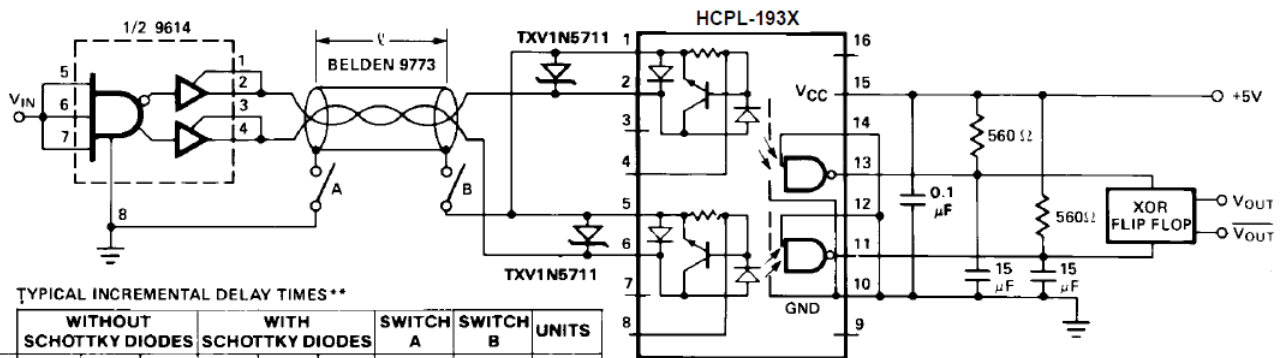


TYPICAL INCREMENTAL DELAY TIMES\*\*

| ℓ                | R = 0, C = OPEN |     |     | R = 33Ω, C = OPEN |     |     | R = 33Ω, C = 390pF |     |     | UNITS |
|------------------|-----------------|-----|-----|-------------------|-----|-----|--------------------|-----|-----|-------|
|                  | <1              | 150 | 300 | <1                | 150 | 300 | <1                 | 150 | 300 |       |
| t <sub>PHL</sub> | 42              | 27  | 121 | 43                | 47  | 171 | 28                 | 37  | 146 | nsec  |
| t <sub>PLH</sub> | 31              | 121 | 296 | 31                | 31  | 71  | 26                 | 11  | 46  | nsec  |

PROPAGATION DELAY TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS.

Figure 12 Polarity Reversing, Split Phase

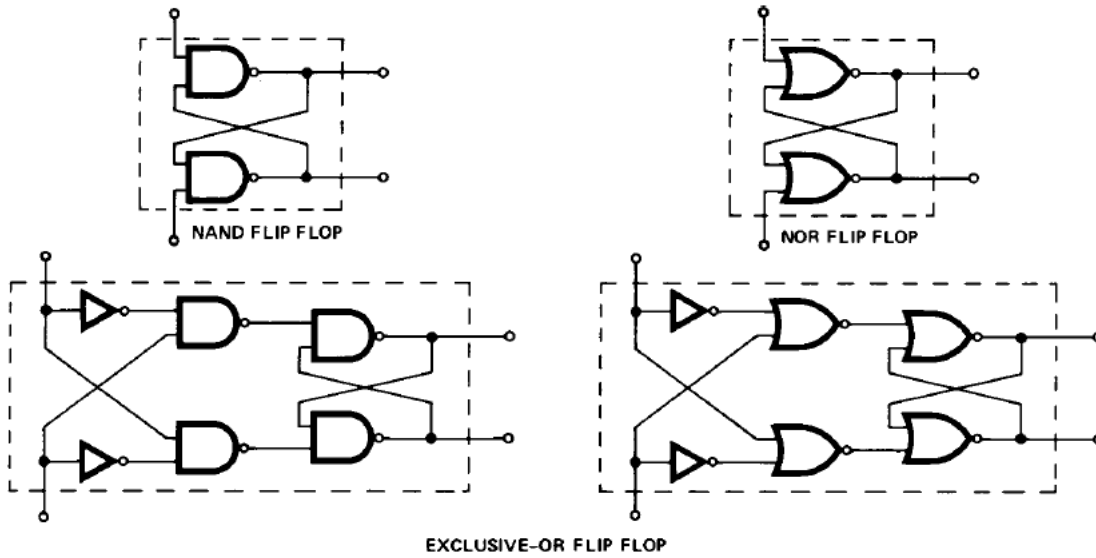


TYPICAL INCREMENTAL DELAY TIMES\*\*

| ℓ              | WITHOUT SCHOTTKY DIODES |     |     | WITH SCHOTTKY DIODES |     |     | SWITCH A | SWITCH B | UNITS |
|----------------|-------------------------|-----|-----|----------------------|-----|-----|----------|----------|-------|
|                | <1                      | 150 | 300 | <1                   | 150 | 300 |          |          |       |
| t <sub>p</sub> | 112                     | 455 | 820 | 78                   | 365 | 700 | OPEN     | OPEN     | nsec  |
|                | 52                      | 410 | 730 | 54                   | 305 | 580 | OPEN     | CLOSED   | nsec  |
|                | 52                      | 410 | 490 | 54                   | 395 | 490 | CLOSED   | CLOSED   | nsec  |

PROPAGATION DELAY TIMES SHOWN EXCLUDE DRIVER AND LINE DELAYS USING 1/3 74LS04 INVERTERS AND 74LS00 QUAD NAND

Figure 13 Flop-Flop Configurations



NAND flip flop tolerates simultaneously HIGH inputs; NOR flip flop tolerates simultaneously LOW inputs; EXCLUSIVE-OR flip flop tolerates simultaneously HIGH OR LOW inputs without causing either of the outputs to change.

\*FOR A DESCRIPTION OF THESE CIRCUITS SEE HCPL-2602 DATA SHEET.