

# HCPL-3150 (Single Channel), HCPL-315J (Dual Channel)

## 0.5 Amp Output Current IGBT Gate Drive Optocoupler

### Overview

The Broadcom<sup>®</sup> HCPL-315X consists of an LED optically coupled to an integrated circuit with a power output stage. This optocoupler is ideally suited for driving power IGBTs and MOSFETs used in motor control inverter applications. The high operating voltage range of the output stage provides the drive voltages required by gate-controlled devices. The voltage and current supplied by this optocoupler makes it ideally suited for directly driving IGBTs with ratings up to 1200V/50A. For IGBTs with higher ratings, the HCPL-3150/315J can be used to drive a discrete power stage which drives the IGBT gate.

### Applications

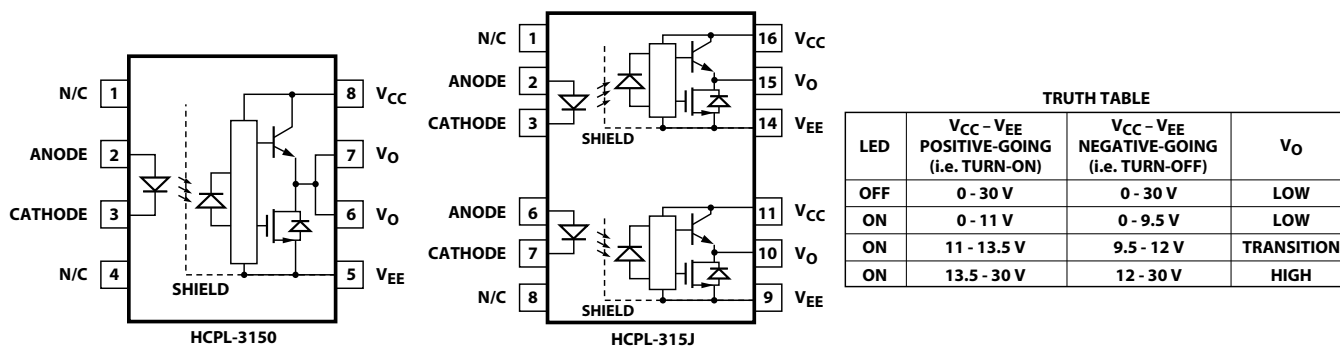
- Isolated IGBT/MOSFET gate drive
- AC and brushless DC motor drives
- Industrial inverters
- Switch mode power supplies (SMPSs)
- Uninterruptable power supplies (UPSs)

### Features

- 0.6A maximum peak output current
- 0.5A minimum peak output current
- 15-kV/ $\mu$ s minimum Common Mode Rejection (CMR) at  $V_{CM} = 1500V$
- 1.0V maximum low level output voltage ( $V_{OL}$ ) eliminates need for negative gate drive
- $I_{CC} = 5$  mA maximum supply current
- Under voltage lock-out protection (UVLO) with hysteresis
- Wide operating  $V_{CC}$  range: 15V to 30V
- 0.5- $\mu$ s maximum propagation delay
- $\pm 0.35$ - $\mu$ s maximum delay between devices/channels
- Industrial temperature range:  $-40^{\circ}C$  to  $100^{\circ}C$
- HCPL-315J: channel one to channel two output isolation = 1500 Vrms/1 min.
- Safety and regulatory approval:
  - UL recognized (UL1577),  
3750 Vrms/1 min. (HCPL-3150)  
5000 Vrms/1 min. (HCPL-315J)
  - IEC/EN/DIN EN 60747-5-5 approved  
 $V_{IORM} = 630 V_{peak}$  (HCPL-3150 option 060 only)  
 $V_{IORM} = 1414 V_{peak}$  (HCPL-315J) CSA certified

**CAUTION!** It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation that may be induced by ESD. The components featured in this data sheet are not to be used in military or aerospace applications or environments.

## Functional Diagram



**NOTE:** A 0.1- $\mu$ F bypass capacitor must be connected between the  $V_{CC}$  and  $V_{EE}$  pins for each channel.

## Selection Guide: Inverter Gate Drive Optoisolators

Package Type	8-Pin DIP (300 mil)				Widebody (400 mil)	Small Outline SO-16		
Part Number	HCPL-3150	HCPL-3120	HCPL-J312	HCPL-J314	HCNW-3120	HCPL-315J	HCPL-316J	HCPL-314J
Number of Channels	1	1	1	1	1	2	1	2
IEC/EN/DIN EN 60747-5-5 Approvals	$V_{IORM}$ 630 V <sub>peak</sub> Option 060		$V_{IORM}$ 1230 V <sub>peak</sub>		$V_{IORM}$ 1414 V <sub>peak</sub>	$V_{IORM}$ 1414 V <sub>peak</sub>		
UL Approval	5000 Vrms/1 min.		5000 Vrms/1min.		5000 Vrms/ 1 min.	5000 Vrms/1 min.		
Output Peak Current	0.5A	2A	2A	0.4A	2A	0.5A	2A	0.4A
CMR (Minimum)	15 kV/ $\mu$ s			10 kV/ $\mu$ s	15 kV/ $\mu$ s			10 kV/ $\mu$ s
UVLO	Yes			No	Yes			No
Fault Status	No					Yes		No

## Ordering Information

HCPL-3150 is UL Recognized with 3750 Vrms for 1 minute per UL1577. HCPL-315J is UL Recognized with 5000 Vrms for 1 minute per UL1577.

Part Number	Option		Package	Surface Mount	Gull Wing	Tape & Reel	IEC/EN/DIN EN 60747-5-5	Quantity
	RoHS Compliant	Non RoHS Compliant						
HCPL-3150	-000E	No option	300 mil DIP-8					50 per tube
	-300E	#300		X	X			50 per tube
	-500E	#500		X	X	X		1000 per reel
	-060E	#060					X	50 per tube
	-360E	#360		X	X		X	50 per tube
	-560E	#560		X	X	X	X	1000 per reel
	-560ME	No option		X	X	X	X	1000 per reel
HCPL-315J	-000E	No option	SO-16	X			X	45 per tube
	-500E	#500		X		X	X	850 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-3150-560E to order product of 300 mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-5 Safety Approval in RoHS compliant.

Example 2:

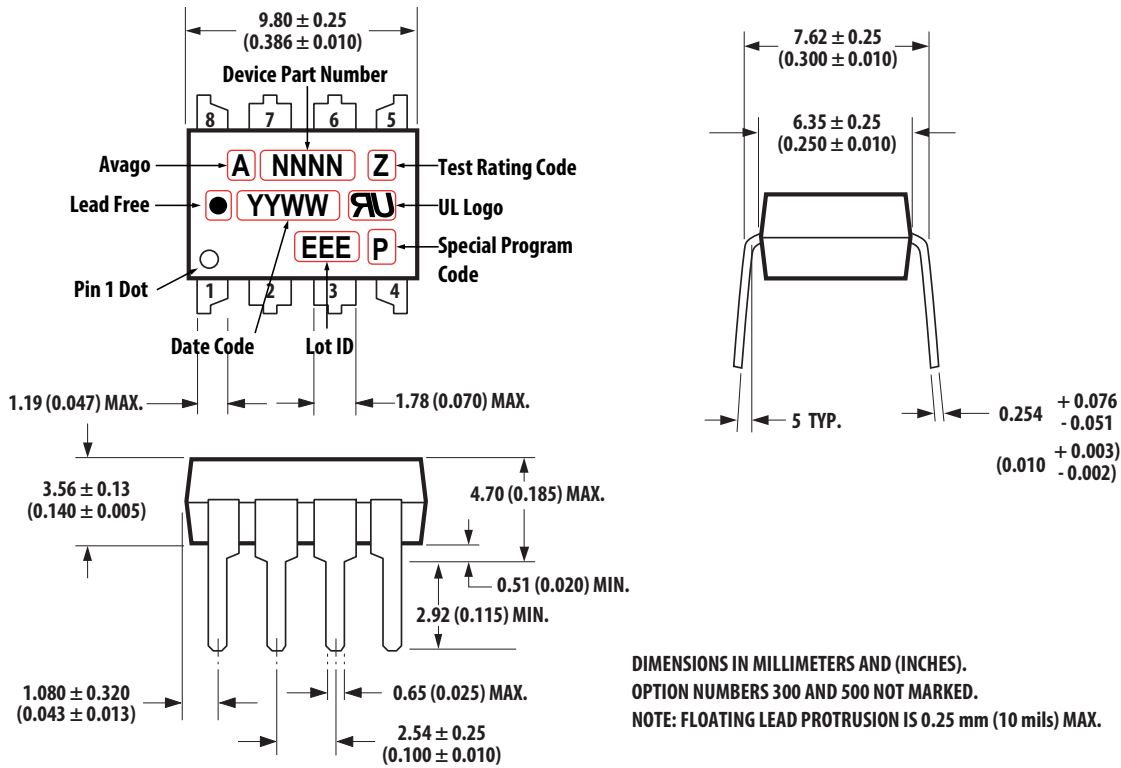
HCPL-3150 to order product of 300 mil DIP package in tube packaging and non RoHS compliant.

Option data sheets are available. Contact your Broadcom sales representative or authorized distributor for information.

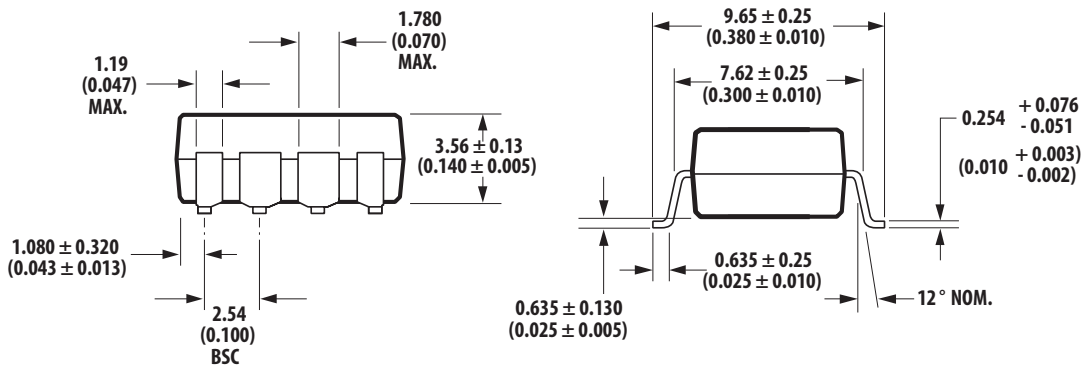
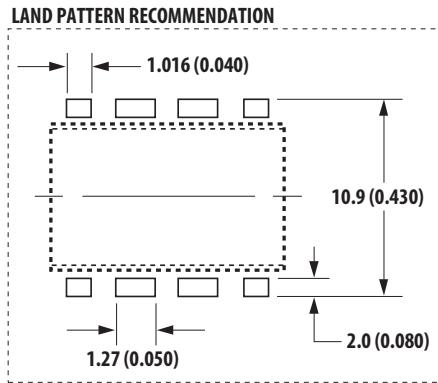
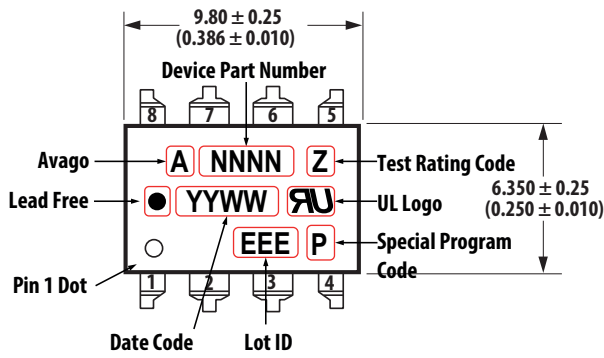
**NOTE:** The notation “#XXX” is used for existing products, while (new) products launched since July 15, 2001 and RoHS compliant option use “-XXE.”

# Package Outline Drawings

## Standard DIP Package

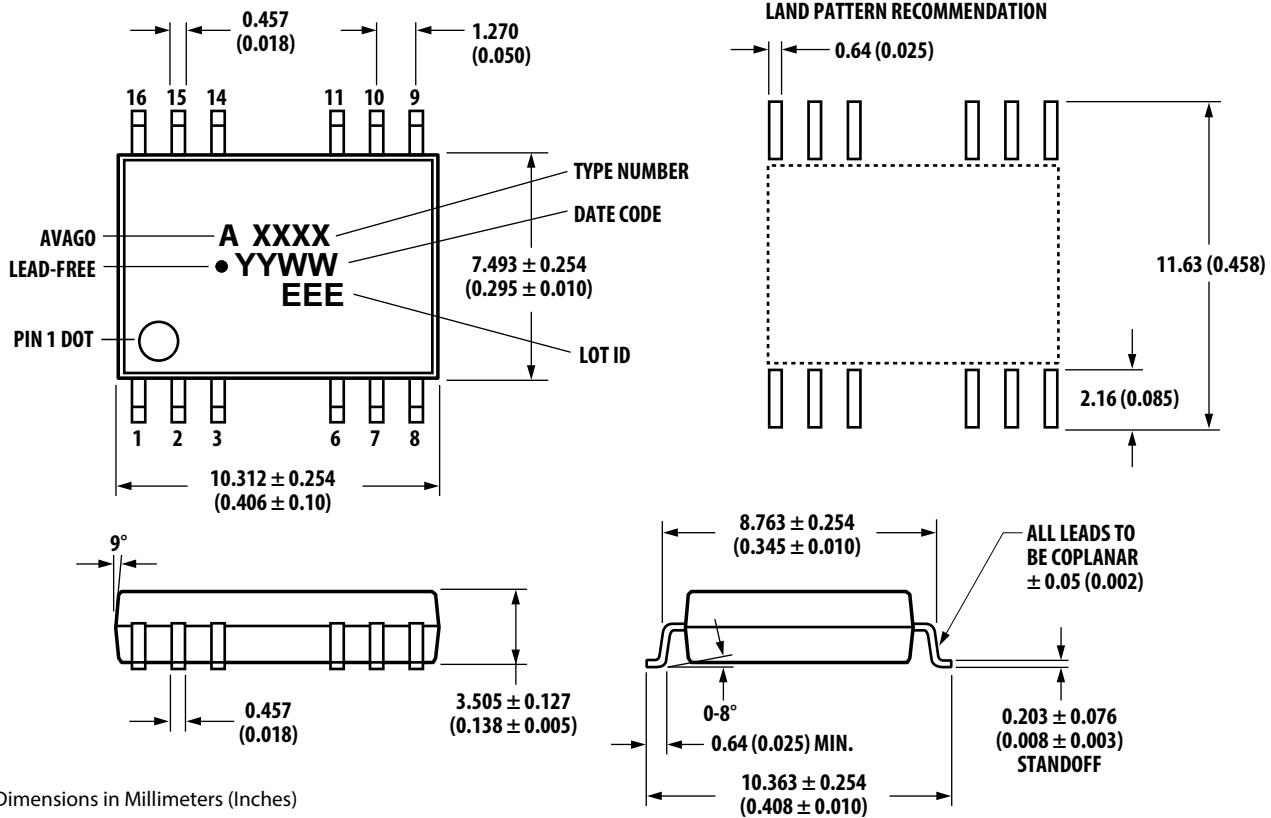


# Gull-Wing Surface-Mount Option 300



DIMENSIONS IN MILLIMETERS (INCHES).  
 LEAD COPLANARITY = 0.10 mm (0.004 INCHES).  
 NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

## 16-Lead Surface Mount Package



Dimensions in Millimeters (Inches)

Floating lead protrusion is 0.25 mm (10 mils) Max.

Note: Initial and continued variation in color of the white mold compound is normal and does not affect performance or reliability of the device

## Recommended Pb-Free IR Profile

Recommended reflow condition as per JEDEC Standard, J-STD-020 (latest revision). Non-halide flux should be used.

## Regulatory Information

The HCPL-3150 and HCPL-315J have been approved by the following organizations.

<b>UL</b>	Recognized under UL 1577, Component Recognition Program, File E55361.
<b>CSA</b>	Approved under CSA Component Acceptance Notice #5, File CA 88324.
<b>IEC/EN/DIN EN 60747-5-5</b>	Approved under: DIN EN 60747-5-5(VDE 0884-5):2011-11 (Option 060 and HCPL-315J only)

## IEC/EN/DIN EN 60747-5-5 Insulation Characteristics

Description	Symbol	HCPL-3150#060	HCPL-315J	Units
Installation classification per DIN VDE 0110/1.89, Table 1 For rated mains voltage $\leq 150$ Vrms For rated mains voltage $\leq 300$ Vrms For rated mains voltage $\leq 600$ Vrms For rated mains voltage $\leq 1000$ Vrms			I - IV I - IV I - IV I-III	
Climatic Classification		55/100/21	55/100/21	
Pollution Degree (DIN VDE 0110/1.89)		2	2	
Maximum Working Insulation Voltage	$V_{IORM}$	630	1414	Vpeak
Input to Output Test Voltage, Method b <sup>a</sup> $V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Test with $t_m = 1$ second, Partial discharge $< 5$ pC	$V_{PR}$	1181	2652	Vpeak
Input to Output Test Voltage, Method a <sup>a</sup> $V_{IORM} \times 1.6 = V_{PR}$ , Type and Sample Test, $t_m = 10$ seconds, Partial discharge $< 5$ pC	$V_{PR}$	945	2262	Vpeak
Highest Allowable Overvoltage <sup>a</sup> (Transient Overvoltage $t_{ini} = 60$ seconds)	$V_{IOTM}$	6000	8000	Vpeak
Safety-Limiting Values – Maximum Values Allowed in the Event of a Failure, Also See <a href="#">Figure 41</a> and <a href="#">Figure 42</a> .				
Case Temperature	$T_S$	175	175	°C
Input Current	$I_{S, INPUT}$	230	400	mA
Output Power	$P_{S, OUTPUT}$	600	1200	mW
Insulation Resistance at $T_S$ , $V_{IO} = 500V$	$R_S$	$\geq 10^9$	$\geq 10^9$	$\Omega$

a. Refer to IEC/EN/DIN EN 60747-5-5 Optoisolator Safety Standard section of the Broadcom Regulatory Guide to Isolation Circuits, AV02-2041EN for a detailed description of Method a and Method b partial discharge test profiles.

**NOTE:** Isolation characteristics are guaranteed only within the safety maximum ratings that must be ensured by protective circuits in application.

## Insulation and Safety Related Specifications

Parameter	Symbol	HCPL-3150	HCPL-315J	Units	Conditions
Minimum External Air Gap (External Clearance)	L(101)	7.1	8.3	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	8.3	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	≥ 0.5	mm	Through insulation distance conductor to conductor.
Tracking Resistance (Comparative Tracking Index)	CTI	≥ 175	≥ 175	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

Option 300 – surface mount classification is Class A in accordance with CECC 00802.

## Absolute Maximum Ratings

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	$T_S$	-55	125	°C	
Operating Temperature	$T_A$	-40	100	°C	
Average Input Current	$I_{F(AVG)}$	—	25	mA	a, b
Peak Transient Input Current (<1- $\mu$ s pulse width, 300 pps)	$I_{F(TRAN)}$	—	1.0	A	
Reverse Input Voltage	$V_R$	—	5	Volts	
“High” Peak Output Current	$I_{OH(PEAK)}$	—	0.6	A	b, c
“Low” Peak Output Current	$I_{OL(PEAK)}$	—	0.6	A	b, c
Supply Voltage	$(V_{CC} - V_{EE})$	0	35	Volts	
Output Voltage	$V_{O(PEAK)}$	0	$V_{CC}$	Volts	
Output Power Dissipation	$P_O$	—	250	mW	b, d
Total Power Dissipation	$P_T$	—	295	mW	b, e
Lead Solder Temperature	260°C for 10 seconds, 1.6 mm below seating plane				
Solder Reflow Temperature Profile	See Package Outline Drawings Section				

- Derate linearly above 70°C free-air temperature at a rate of 0.3 mA/°C.
- Each channel.
- Maximum pulse width = 10  $\mu$ s, maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with  $I_O$  peak minimum = 0.5A. See the Applications section for additional details on limiting  $I_{OH}$  peak.
- Derate linearly above 70°C free-air temperature at a rate of 4.8 mW/°C.
- Derate linearly above 70°C free-air temperature at a rate of 5.4 mW/°C. The maximum LED junction temperature should not exceed 125°C.



## Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Power Supply Voltage	$(V_{CC} - V_{EE})$	15	30	V
Input Current (ON)	$I_{F(ON)}$	7	16	mA
Input Voltage (OFF)	$V_{F(OFF)}$	-3.6	0.8	V
Operating Temperature	$T_A$	-40	100	°C

## Electrical Specifications (DC)

Over recommended operating conditions ( $T_A = -40^\circ\text{C}$  to  $100^\circ\text{C}$ ,  $I_{F(\text{ON})} = 7\text{ mA}$  to  $16\text{ mA}$ ,  $V_{F(\text{OFF})} = -3.6\text{V}$  to  $0.8\text{V}$ ,  $V_{CC} = 15\text{V}$  to  $30\text{V}$ ,  $V_{EE} = \text{Ground}$ , each channel) unless otherwise specified.

Parameter	Symbol	Min.	Typ. <sup>a</sup>	Max.	Units	Test Conditions	Figure	Note
High Level Output Current	$I_{OH}$	0.1	0.4	—	A	$V_O = (V_{CC} - 4\text{V})$	2, 3, 5	
		0.5	—	—		$V_O = (V_{CC} - 15\text{V})$	17	b
Low Level Output Current	$I_{OL}$	0.1	0.6	—	A	$V_O = (V_{EE} + 2.5\text{V})$	5, 6	c
		0.5	—	—		$V_O = (V_{EE} + 15\text{V})$	18	b
High Level Output Voltage	$V_{OH}$	$(V_{CC} - 4)$	$(V_{CC} - 3)$	—	V	$I_O = -100\text{ mA}$	1, 3, 19	d, e
Low Level Output Voltage	$V_{OL}$	—	0.4	1.0	V	$I_O = 100\text{ mA}$	4, 6, 20	
High Level Supply Current	$I_{CCH}$	—	2.5	5.0	mA	Output Open, $I_F = 7$ to $16\text{ mA}$	7, 8	f
Low Level Supply Current	$I_{CCL}$	—	2.7	5.0	mA	Output Open, $V_F = -3.0$ to $+0.8\text{V}$		
Threshold Input Current Low to High	$I_{FLH}$	—	2.2	5.0	mA	HCPL-3150	9, 15, 21	
		—	2.6	6.4		HCPL-315J		
Threshold Input Voltage High to Low	$V_{FHL}$	0.8	—	—	V			
Input Forward Voltage	$V_F$	1.2	1.5	1.8	V	HCPL-3150	16	
			1.6	1.95	V	HCPL-315J		
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$	—	-1.6	—	mV/°C	$I_F = 10\text{ mA}$		
Input Reverse Breakdown Voltage	$BV_R$	5	—	—	V	HCPL-3150		
		3				HCPL-315J		
Input Capacitance	$C_{IN}$	—	70	—	pF	$f = 1\text{ MHz}$ , $V_F = 0\text{V}$		
UVLO Threshold	$V_{UVLO+}$	11.0	12.3	13.5	V	$V_O > 5\text{ V}$	22, 40	
	$V_{UVLO-}$	9.5	10.7	12.0		$I_F = 10\text{ mA}$		
UVLO Hysteresis	$UVLO_{HYS}$	—	1.6	—	V			

- All typical values at  $T_A = 25^\circ\text{C}$  and  $V_{CC} - V_{EE} = 30\text{V}$ , unless otherwise noted.
- Maximum pulse width =  $10\ \mu\text{s}$ , maximum duty cycle = 0.2%. This value is intended to allow for component tolerances for designs with  $I_O$  peak minimum = 0.5 A. See Applications section for additional details on limiting  $I_{OH}$  peak.
- Maximum pulse width =  $50\ \mu\text{s}$ , maximum duty cycle = 0.5%.
- In this test,  $V_{OH}$  is measured with a dc load current. When driving capacitive loads  $V_{OH}$  will approach  $V_{CC}$  as  $I_{OH}$  approaches zero amps.
- Maximum pulse width = 1 ms, maximum duty cycle = 20%.
- Each channel.

## Switching Specifications (AC)

Over recommended operating conditions ( $T_A = -40$  to  $100^\circ\text{C}$ ,  $I_{F(ON)} = 7$  mA to 16 mA,  $V_{F(OFF)} = -3.6$  V to 0.8 V,  $V_{CC} = 15$  V to 30 V,  $V_{EE} = \text{Ground}$ , each channel) unless otherwise specified.

Parameter	Symbol	Min.	Typ. <sup>a</sup>	Max.	Units	Test Conditions	Figure	Note	
Propagation Delay Time to High Output Level	$t_{PLH}$	0.10	0.30	0.50	$\mu\text{s}$	$R_g = 47 \Omega$ , $C_g = 3 \text{ nF}$ , $f = 10 \text{ kHz}$ , Duty Cycle = 50%	10, 11, 12, 13, 14, 23	b	
Propagation Delay Time to Low Output Level	$t_{PHL}$	0.10	0.3	0.50	$\mu\text{s}$				
Pulse Width Distortion	PWD			0.3	$\mu\text{s}$				
Propagation Delay Difference Between Any Two Parts or Channels	PDD ( $t_{PHL} - t_{PLH}$ )	-0.35	—	0.35	$\mu\text{s}$			38, 39	d
Rise Time	$t_r$	—	0.1	—	$\mu\text{s}$			23	
Fall Time	$t_f$	—	0.1	—	$\mu\text{s}$				
UVLO Turn On Delay	$t_{UVLO ON}$	—	0.8	—	$\mu\text{s}$	$V_O > 5\text{V}$ , $I_F = 10 \text{ mA}$	22		
UVLO Turn Off Delay	$t_{UVLO OFF}$	—	0.6	—	$\mu\text{s}$	$V_O < 5\text{V}$ , $I_F = 10 \text{ mA}$			
Output High Level Common Mode Transient Immunity	$ CM_H $	15	30	—	kV/ $\mu\text{s}$	$T_A = 25^\circ\text{C}$ , $I_F = 10$ to 16 mA, $V_{CM} = 1500\text{V}$ , $V_{CC} = 30 \text{ V}$	24	e, f	
Output Low Level Common Mode Transient Immunity	$ CM_L $	15	30	—	kV/ $\mu\text{s}$	$T_A = 25^\circ\text{C}$ , $V_{CM} = 1500\text{V}$ , $V_F = 0 \text{ V}$ , $V_{CC} = 30\text{V}$		e, g	

- a. All typical values at  $T_A = 25^\circ\text{C}$  and  $V_{CC} - V_{EE} = 30\text{V}$ , unless otherwise noted.
- b. This load condition approximates the gate load of a 1200 V/25 A IGBT
- c. Pulse Width Distortion (PWD) is defined as  $|t_{PHL} - t_{PLH}|$  for any given device.
- d. The difference between  $t_{PHL}$  and  $t_{PLH}$  between any two parts or channels under the same test condition.
- e. Pins 1 and 4 (HCPL-3150) and pins 3 and 4 (HCPL-315J) need to be connected to LED common.
- f. Common mode transient immunity in the high state is the maximum tolerable  $|dV_{CM}/dt|$  of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in the high state (that is,  $V_O > 15.0\text{V}$ ).
- g. Common mode transient immunity in a low state is the maximum tolerable  $|dV_{CM}/dt|$  of the common mode pulse,  $V_{CM}$ , to assure that the output will remain in a low state (that is,  $V_O < 1.0\text{V}$ ).

## Package Characteristics

Each channel, unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ. <sup>a</sup>	Max.	Units	Test Conditions	Figure	Note
Input-Output Momentary Withstand Voltage <sup>b</sup>	$V_{ISO}$	HCPL-3150	3750	—	—	Vrms	RH < 50%, t = 1 min., T <sub>A</sub> = 25°C		c, d
		HCPL-315J	5000						
Output-Output Momentary Withstand Voltage <sup>b</sup>	$V_{O-O}$	HCPL-315J	1500	—	—	Vrms	RH < 50%, t = 1 min., T <sub>A</sub> = 25°C		e
Resistance (Input-Output)	$R_{I-O}$		—	10 <sup>12</sup>	—	Ω	V <sub>I-O</sub> = 500 V <sub>DC</sub>		f
Capacitance (Input-Output)	$C_{I-O}$	HCPL-3150	—	0.6	—	pF	f = 1 MHz		
		HCPL-315J		1.3					
LED-to-Case Thermal Resistance	$\theta_{LC}$	HCPL-3150	—	391	—	°C/W	Thermocouple located at center underside of package	29, 30	g
LED-to-Detector Thermal Resistance	$\theta_{LD}$	HCPL-3150	—	439	—	°C/W			
Detector-to-Case Thermal Resistance	$\theta_{DC}$	HCPL-3150	—	119	—	°C/W			

- a. All typical values at T<sub>A</sub> = 25°C and V<sub>CC</sub> – V<sub>EE</sub> = 30V, unless otherwise noted.
- b. The Input-Output/Output-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output/output-output continuous voltage rating. For the continuous voltage rating, refer to your equipment level safety specification or Broadcom Application Note 1074, *Optocoupler Input-Output Endurance Voltage*.
- c. In accordance with UL1577, each HCPL-3150 optocoupler is proof tested by applying an insulation test voltage ≥ 4500 Vrms (≥ 6000 Vrms for the HCPL-315J) for 1 second. This test is performed before the 100% production test for partial discharge (method b) shown in the IEC/EN/DIN EN 60747-5-5 Insulation Characteristics Table, if applicable.
- d. Device considered a two-terminal device: pins on input side shorted together and pins on output side shorted together.
- e. Device considered a two terminal device: Channel one output side pins shorted together, and channel two output side pins shorted together.
- f. Device considered a two-terminal device: pins on input side shorted together and pins on output side shorted together.
- g. See the thermal model for the HCPL-315J in the application section of this data sheet.

Figure 1:  $V_{OH}$  vs. Temperature

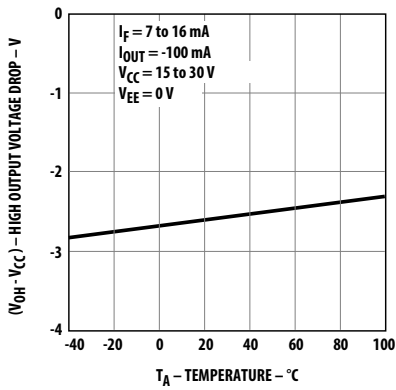


Figure 2:  $I_{OH}$  vs. Temperature

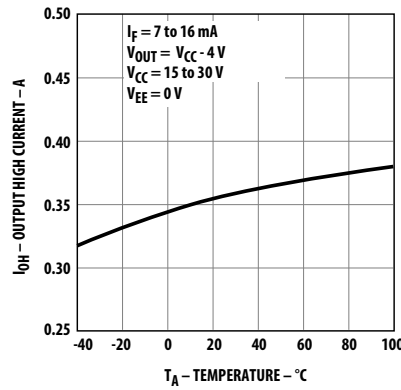


Figure 3:  $V_{OH}$  vs.  $I_{OH}$

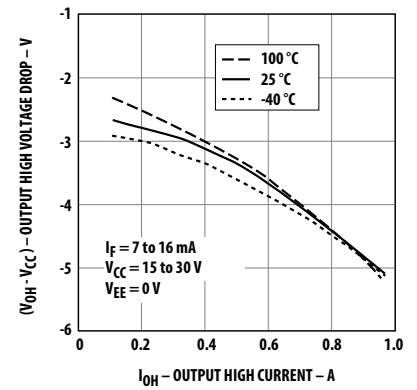


Figure 4:  $V_{OL}$  vs. Temperature

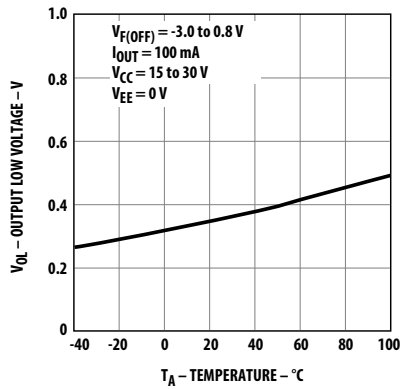


Figure 5:  $I_{OL}$  vs. Temperature

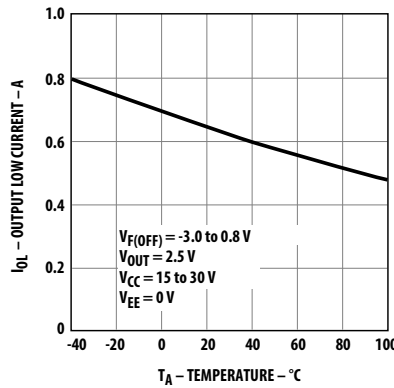


Figure 6:  $V_{OL}$  vs.  $I_{OL}$

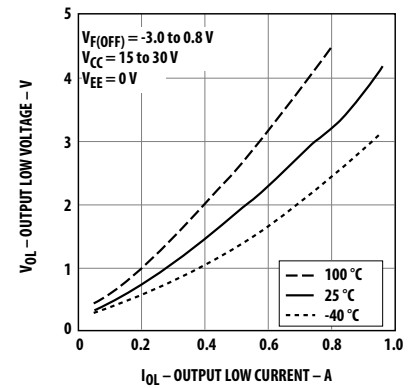


Figure 7:  $I_{CC}$  vs. Temperature

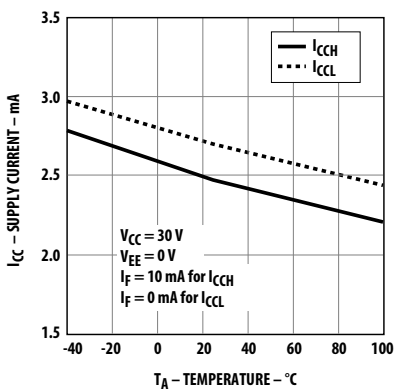


Figure 8:  $I_{CC}$  vs.  $V_{CC}$

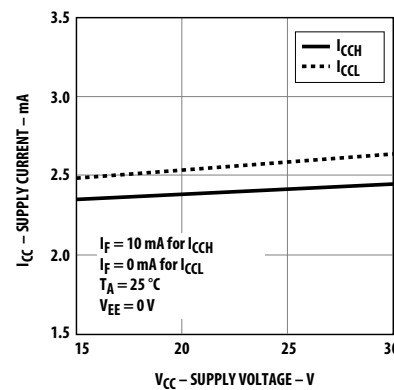


Figure 9:  $I_{FLH}$  vs. Temperature

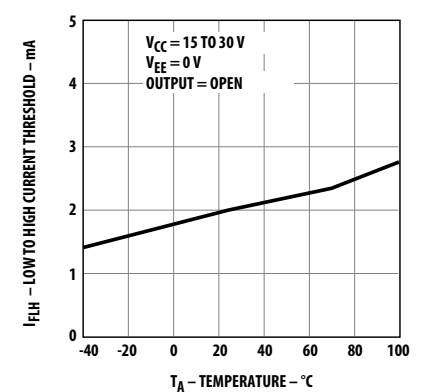


Figure 10: Propagation Delay vs.  $V_{CC}$

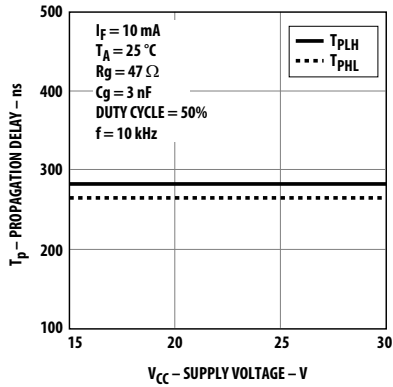


Figure 11: Propagation Delay vs.  $I_F$

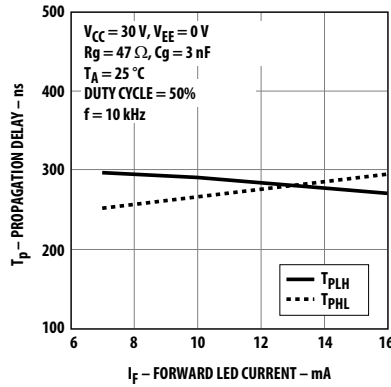


Figure 12: Propagation Delay vs. Temperature

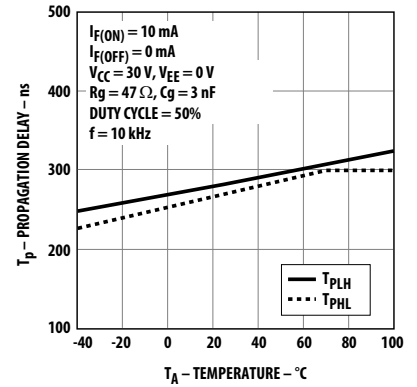


Figure 13: Propagation Delay vs.  $R_g$

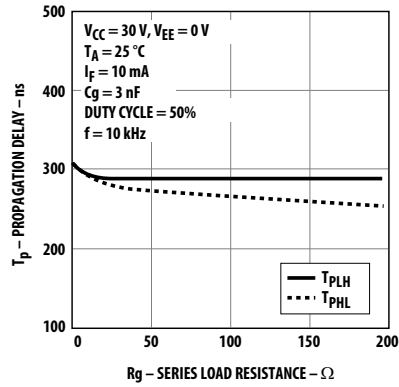


Figure 14: Propagation Delay vs.  $C_g$

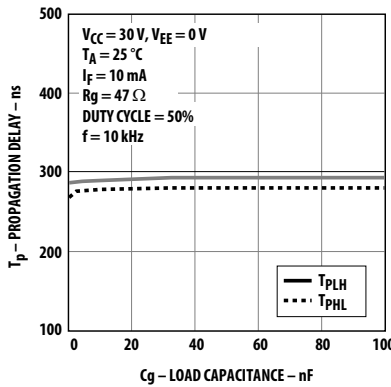


Figure 15: Transfer Characteristics

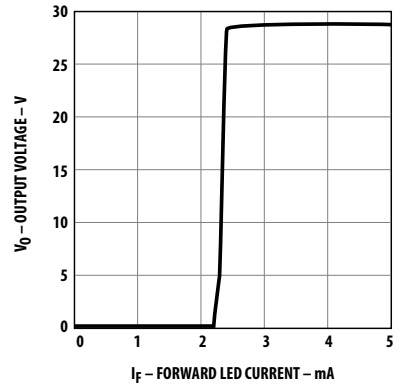


Figure 16: Input Current vs. Forward Voltage

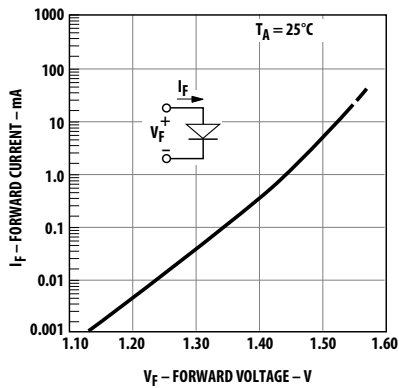


Figure 17:  $I_{OH}$  Test Circuit

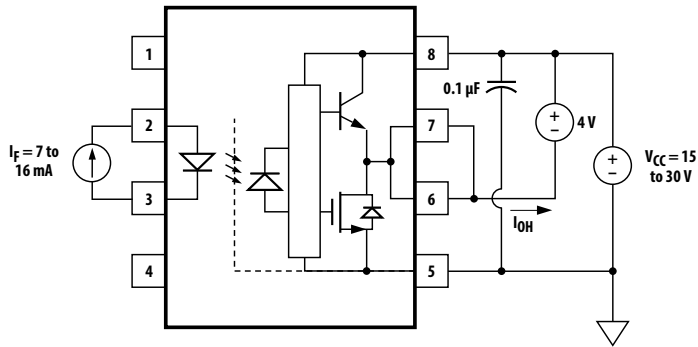


Figure 18:  $I_{OL}$  Test Circuit

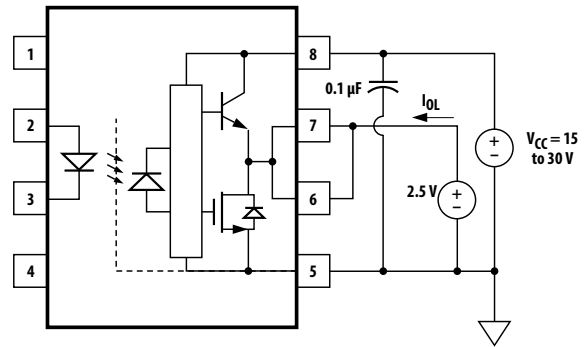


Figure 19:  $V_{OH}$  Test Circuit

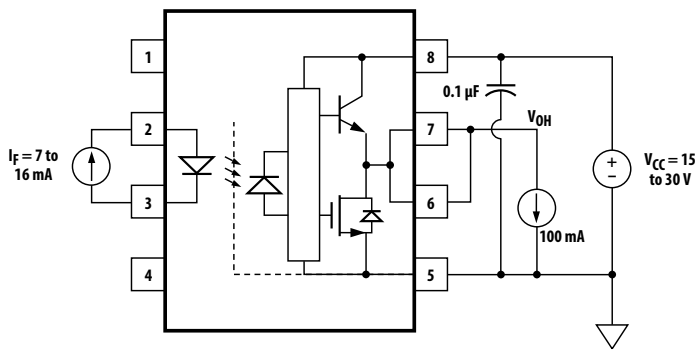


Figure 20:  $V_{OL}$  Test Circuit

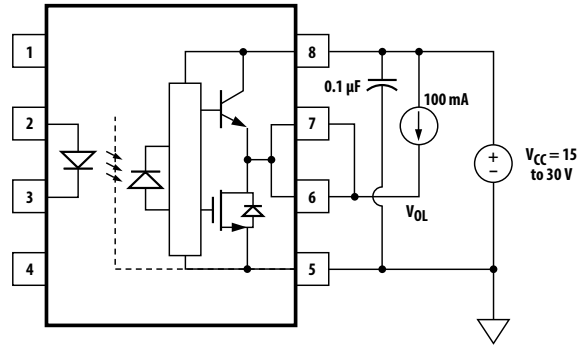


Figure 21:  $I_{FLH}$  Test Circuit

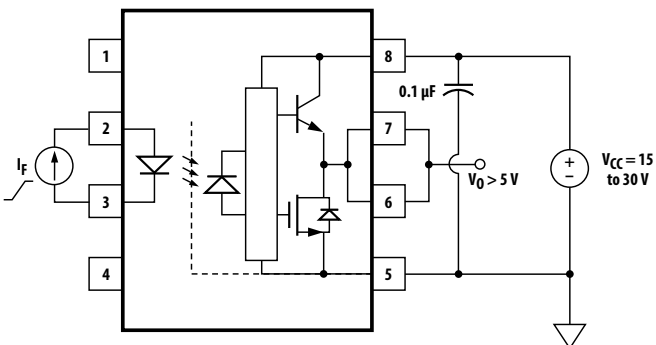


Figure 22: UVLO Test Circuit

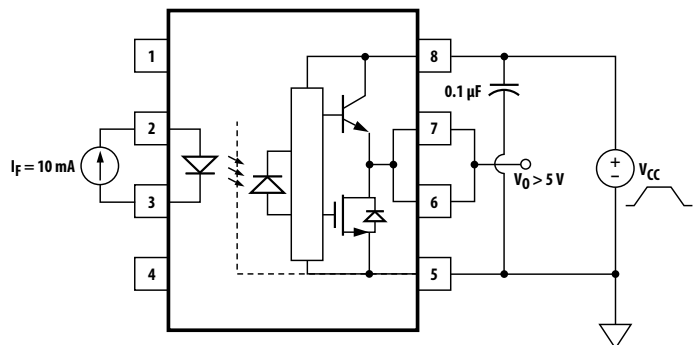


Figure 23:  $t_{PLH}$ ,  $t_{PHL}$ ,  $t_r$ , and  $t_f$  Test Circuit and Waveforms

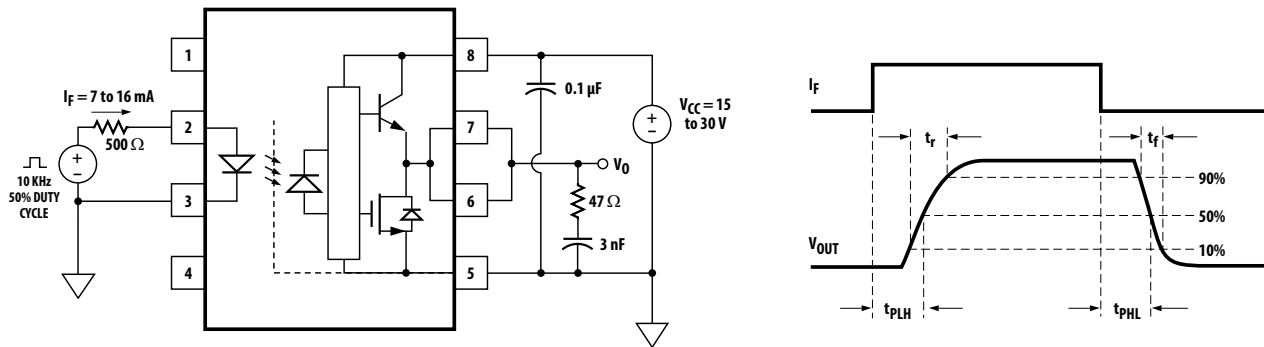
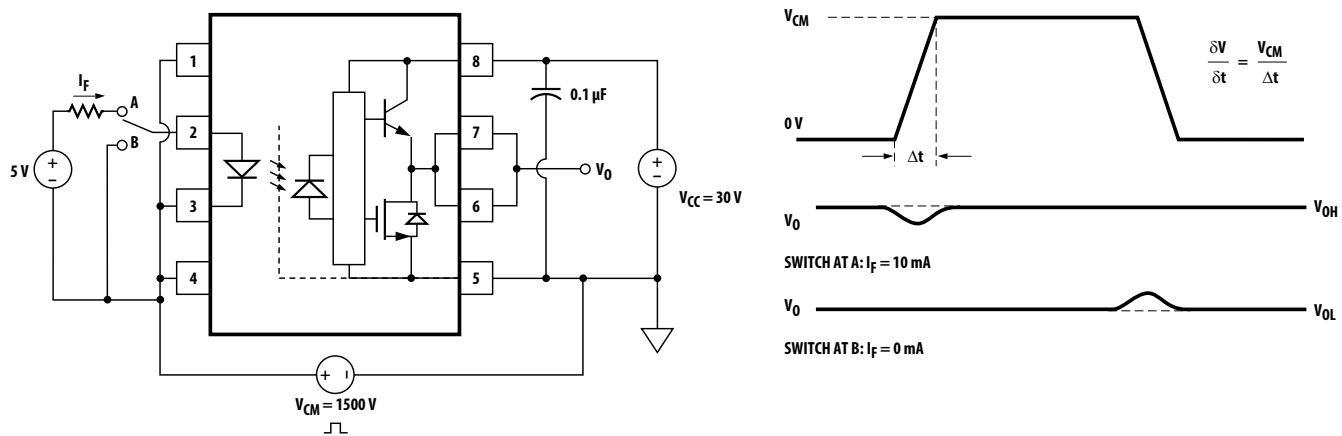


Figure 24: CMR Test Circuit and Waveforms



## Applications Information

### Eliminating Negative IGBT Gate Drive

To keep the IGBT firmly off, the HCPL-3150/315J has a very low maximum  $V_{OL}$  specification of 1.0V. The HCPL-3150/315J realizes this very low  $V_{OL}$  by using a DMOS transistor with 4Ω (typical) on resistance in its pull-down circuit. When the HCPL3150/315J is in the low state, the IGBT gate is shorted to the emitter by  $R_g + 4\Omega$ . Minimizing  $R_g$  and the lead inductance from the HCPL-3150/315J to the IGBT gate and emitter (possibly by mounting the HCPL-3150/315J on a small PC board directly above the IGBT) can eliminate the need for negative IGBT gate drive in many applications as shown in [Figure 25](#) and [Figure 26](#). Care should be taken with such a PC board design to avoid routing the IGBT collector or emitter traces close to the HCPL-3150/315J and degrade performance. (If the IGBT drain must be routed near the HCPL-3150/315J input, then the LED should be reverse-biased when in the off state, to prevent the transient signals coupled from the IGBT drain from turning on the HCPL-3150/315J.)



Figure 25: Recommended LED Drive and Application Circuit

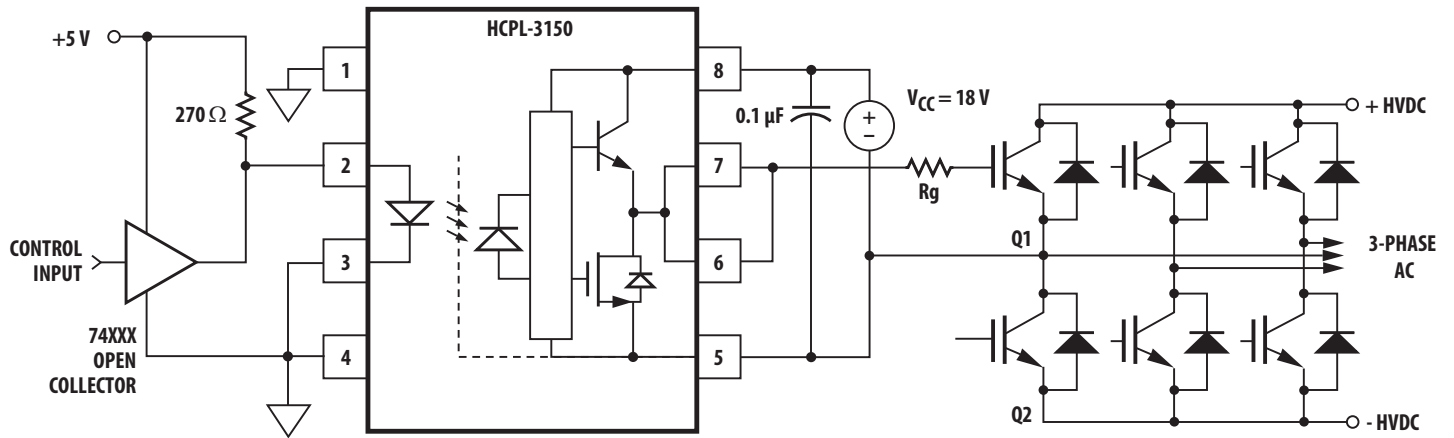
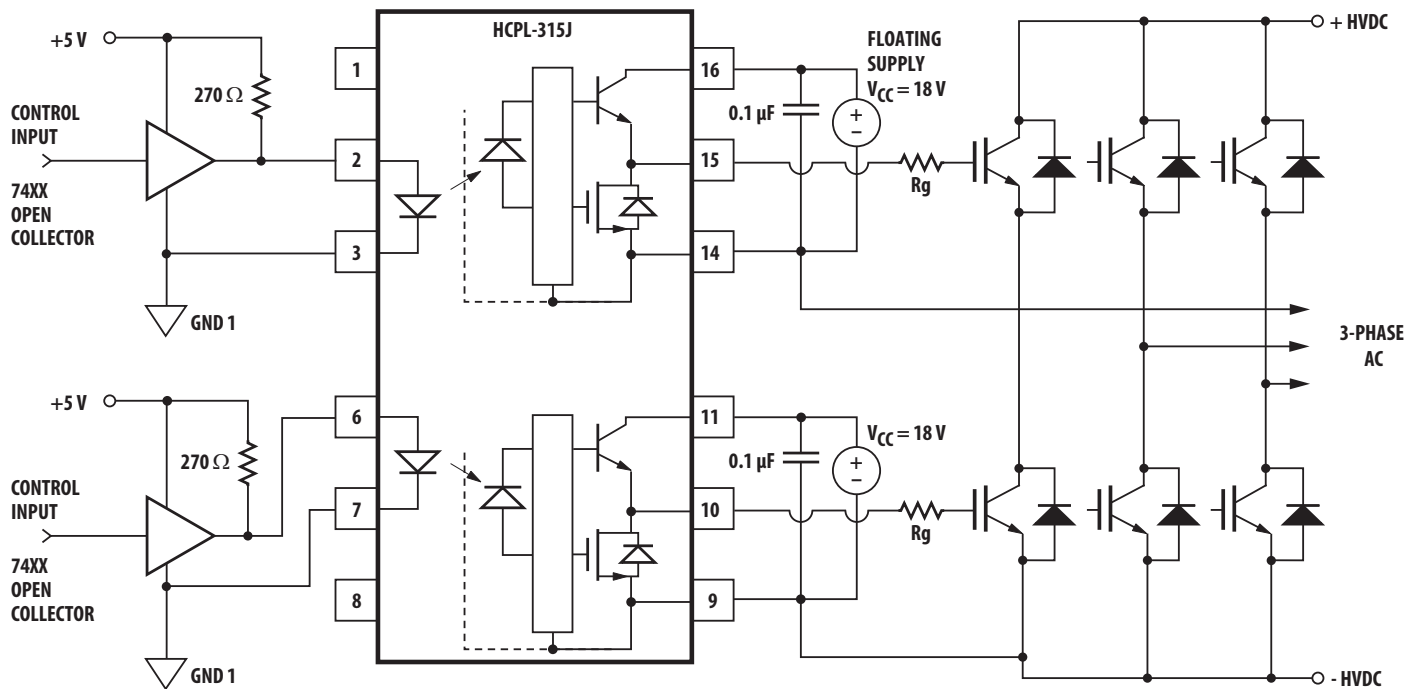


Figure 26: Recommended LED Drive and Application Circuit (HCPL-315J)



## Selecting the Gate Resistor (Rg) to Minimize IGBT Switching Losses

**Step 1: Calculate Rg Minimum From the IOL Peak Specification.** The IGBT and Rg in [Figure 27](#) and [Figure 28](#) can be analyzed as a simple RC circuit with a voltage supplied by the HCPL-3150/315J.

$$\begin{aligned}
 R_g &\geq \frac{(V_{CC} - V_{EE} - V_{OL})}{I_{OLPEAK}} \\
 &= \frac{(V_{CC} - V_{EE} - 1.7 V)}{I_{OLPEAK}} \\
 &= \frac{(15 V + 5 V - 1.7 V)}{0.6 A} \\
 &= 30.5 \Omega
 \end{aligned}$$

The  $V_{OL}$  value of 2V in the previous equation is a conservative value of  $V_{OL}$  at the peak current of 0.6A (see [Figure 6](#)). At lower Rg values the voltage supplied by the HCPL-3150/315J is not an ideal voltage step. This results in lower peak currents (more margin) than predicted by this analysis. When negative gate drive is not used  $V_{EE}$  in the previous equation is equal to zero volts.

**Step 2: Check the HCPL-3150/315J Power Dissipation and Increase Rg if Necessary.** The HCPL-3150/315J total power dissipation ( $P_T$ ) is equal to the sum of the emitter power ( $P_E$ ) and the output power ( $P_O$ ):

$$\begin{aligned}
 P_T &= P_E + P_O \\
 P_E &= I_F \cdot V_F \cdot \text{Duty Cycle} \\
 P_O &= P_{O(BIAS)} + P_{O(SWITCHING)} \\
 &= I_{CC} \cdot (V_{CC} - V_{EE}) + E_{SW} (R_G Q_G) \cdot f
 \end{aligned}$$

For the circuit in [Figure 27](#) and [Figure 28](#) with  $I_F$  (worst case) = 16 mA,  $R_g = 30.5\Omega$ , Max Duty Cycle = 80%,  $Q_g = 500$  nC,  $f = 20$  kHz, and  $T_{Amax} = 90^\circ\text{C}$ :

$$\begin{aligned}
 P_E &= 16 \text{ mA} \cdot 1.8 \text{ V} \cdot 0.8 = 23 \text{ mW} \\
 P_O &= 4.25 \text{ mA} \cdot 20 \text{ V} + 4.0 \mu\text{J} \cdot 20 \text{ kHz} \\
 &= 85 \text{ mW} + 80 \text{ mW} \\
 &= 165 \text{ mW} > 154 \text{ mW} (P_{O(MAX)} @ 90^\circ\text{C}) \\
 &= 250 \text{ mW} - 20\text{C} \cdot 4.8 \text{ mW/C}
 \end{aligned}$$

Figure 27: HCPL-3150 Typical Application Circuit with Negative IGBT Gate Drive

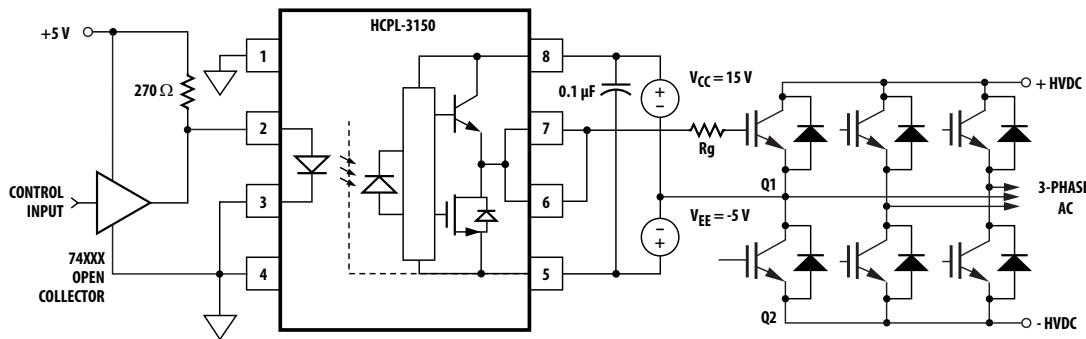


Figure 28: HCPL-315J Typical Application Circuit with Negative IGBT Gate Drive

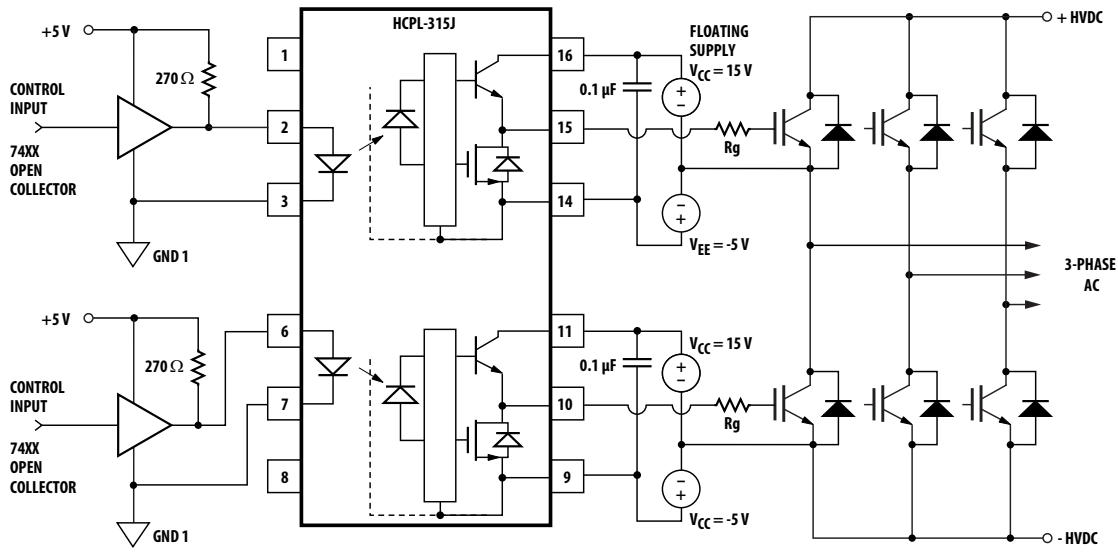


Table 1:  $P_E$  and  $P_O$  Parameters

$P_E$ Parameter	Description	$P_O$ Parameter	Description
$I_F$	LED Current	$I_{CC}$	Supply Current
$V_F$	LED On Voltage	$V_{CC}$	Positive Supply Voltage
Duty Cycle	Maximum LED Duty Cycle	$V_{EE}$	Negative Supply Voltage
		$E_{SW}(R_g, Q_g)$	Energy Dissipated in the HCPL-3150/315J for each IGBT Switching Cycle (see <a href="#">Figure 32</a> )
		$f$	Switching Frequency

The value of 4.25 mA for  $I_{CC}$  in the previous equation was obtained by derating the  $I_{CC}$  max of 5 mA (which occurs at  $-40^{\circ}\text{C}$ ) to  $I_{CC}$  max at  $90^{\circ}\text{C}$  (see Figure 7).

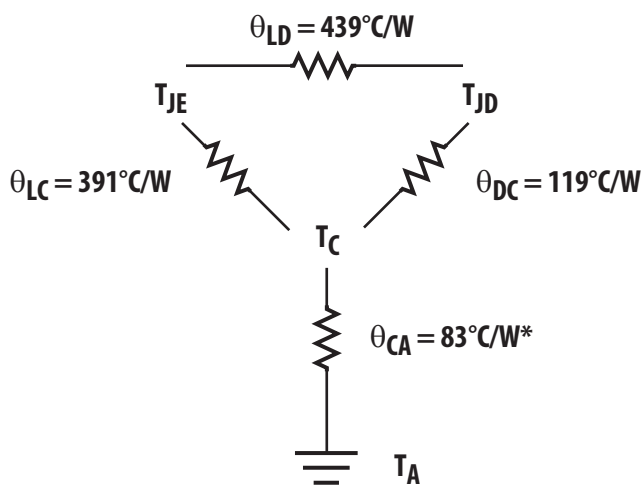
Since  $P_O$  for this case is greater than  $P_{O(MAX)}$ ,  $R_g$  must be increased to reduce the HCPL-3150 power dissipation.

$$\begin{aligned} P_{O(SWITCHING\ MAX)} &= P_{O(MAX)} - P_{O(BIAS)} \\ &= 154\text{ mW} - 85\text{ mW} \\ &= 69\text{ mW} \end{aligned}$$

$$\begin{aligned} E_{SW(MAX)} &= \frac{P_{O(SWITCHING\ MAX)}}{f} \\ &= \frac{69\text{ mW}}{20\text{ kHz}} = 3.45\ \mu\text{J} \end{aligned}$$

For  $Q_g = 500\text{ nC}$ , from Table 1, a value of  $E_{SW} = 3.45\ \mu\text{J}$  gives a  $R_g = 41\ \Omega$ .

Figure 29: Thermal Model



**$T_{JE}$  = LED JUNCTION TEMPERATURE**  
 **$T_{JD}$  = DETECTOR IC JUNCTION TEMPERATURE**  
 **$T_C$  = CASE TEMPERATURE MEASURED AT THE CENTER OF THE PACKAGE BOTTOM**  
 **$\theta_{LC}$  = LED-TO-CASE THERMAL RESISTANCE**  
 **$\theta_{LD}$  = LED-TO-DETECTOR THERMAL RESISTANCE**  
 **$\theta_{DC}$  = DETECTOR-TO-CASE THERMAL RESISTANCE**  
 **$\theta_{CA}$  = CASE-TO-AMBIENT THERMAL RESISTANCE**  
**\* $\theta_{CA}$  WILL DEPEND ON THE BOARD DESIGN AND THE PLACEMENT OF THE PART.**

From the thermal mode in Figure 29, the LED and detector IC junction temperatures can be expressed as:

$$T_{JE} = P_E \cdot (\theta_{LC} \parallel (\theta_{LD} + \theta_{DC}) + \theta_{CA}) + P_D \cdot \left( \frac{\theta_{LC} \cdot \theta_{DC}}{\theta_{LC} + \theta_{DC} + \theta_{LD}} + \theta_{CA} \right) + T_A$$

$$T_{JD} = P_E \cdot \left( \frac{\theta_{LC} \cdot \theta_{DC}}{\theta_{LC} + \theta_{DC} + \theta_{LD}} + \theta_{CA} \right) + P_D \cdot (\theta_{DC} \parallel (\theta_{LD} + \theta_{LC}) + \theta_{CA}) + T_A$$

Inserting the values for  $\theta_{LC}$  and  $\theta_{DC}$  shown in Figure 29 gives:

$$T_{JE} = P_E \cdot (230^\circ\text{C/W} + \theta_{CA}) + P_D \cdot (49^\circ\text{C/W} + \theta_{CA}) + T_A$$

$$T_{JD} = P_E \cdot (49^\circ\text{C/W} + \theta_{CA}) + P_D \cdot (104^\circ\text{C/W} + \theta_{CA}) + T_A$$

For example, given  $P_E = 45 \text{ mW}$ ,  $P_O = 250 \text{ mW}$ ,  $T_A = 70^\circ\text{C}$  and  $\theta_{CA} = 83^\circ\text{C/W}$ :

$$T_{JE} = P_E \cdot 313^\circ\text{C/W} + P_D \cdot 132^\circ\text{C/W} + T_A$$

$$= 45 \text{ mW} \cdot 313^\circ\text{C/W} + 250 \text{ mW} \cdot 132^\circ\text{C/W} + 70^\circ\text{C} = 117^\circ\text{C}$$

$$T_{JD} = P_E \cdot 132^\circ\text{C/W} + P_D \cdot 187^\circ\text{C/W} + T_A$$

$$= 45 \text{ mW} \cdot 132^\circ\text{C/W} + 250 \text{ mW} \cdot 187^\circ\text{C/W} + 70^\circ\text{C} = 123^\circ\text{C}$$

$T_{JE}$  and  $T_{JD}$  should be limited to  $125^\circ\text{C}$  based on the board layout and part placement ( $\theta_{CA}$ ) specific to the application.

## Thermal Model Dual-Channel (SOIC-16) HCPL-315J Optoisolator

### Definitions

$\theta_1, \theta_2, \theta_3, \theta_4, \theta_5, \theta_6, \theta_7, \theta_8, \theta_9, \theta_{10}$ : Thermal impedances between nodes as shown in Figure 30. Ambient Temperature: Measured approximately 1.25 cm above the optocoupler with no forced air.

Figure 30: Thermal Impedance Model for HCPL-315J

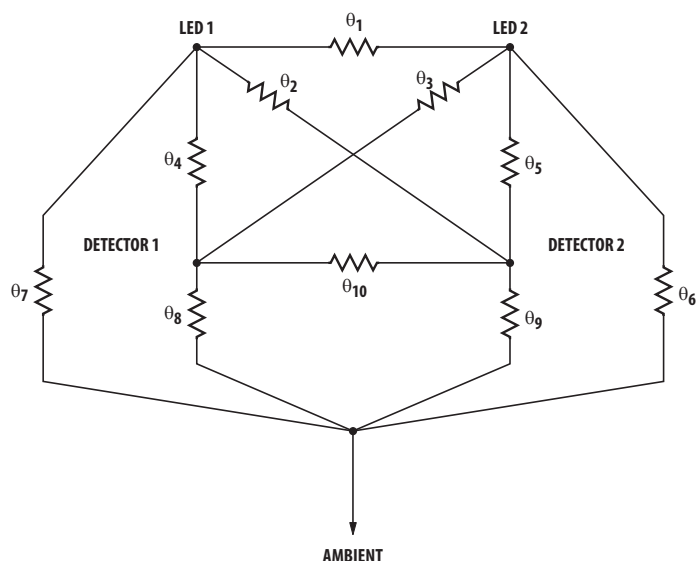
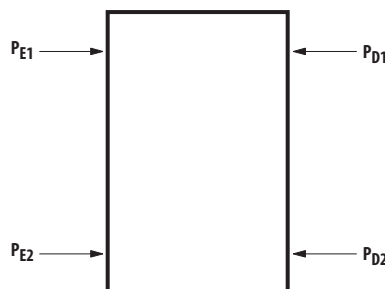


Figure 31: Power Dissipation



### Description

This thermal model assumes that a 16-pin dual-channel (SOIC-16) optocoupler is soldered into an 8.5 cm x 8.1 cm printed circuit board (PCB). These optocouplers are hybrid devices with four die: two LEDs and two detectors. The temperature at the LED and the detector of the optocoupler can be calculated by using the equations below.

$$\Delta T_{E1A} = A_{11} P_{E1} + A_{12} P_{E2} + A_{13} P_{D1} + A_{14} P_{D2}$$

$$\Delta T_{E2A} = A_{21} P_{E1} + A_{22} P_{E2} + A_{23} P_{D1} + A_{24} P_{D2}$$

$$\Delta T_{D1A} = A_{31} P_{E1} + A_{32} P_{E2} + A_{33} P_{D1} + A_{34} P_{D2}$$

$$\Delta T_{D2A} = A_{41} P_{E1} + A_{42} P_{E2} + A_{43} P_{D1} + A_{44} P_{D2}$$

where:

$\Delta T_{E1A}$  = Temperature difference between ambient and LED 1

$\Delta T_{E2A}$  = Temperature difference between ambient and LED 2

$\Delta T_{D1A}$  = Temperature difference between ambient and detector 1

$\Delta T_{D2A}$  = Temperature difference between ambient and detector 2

$P_{E1}$  = Power dissipation from LED 1;

$P_{E2}$  = Power dissipation from LED 2;

$P_{D1}$  = Power dissipation from detector 1;

$P_{D2}$  = Power dissipation from detector 2

$A_{xy}$  thermal coefficient (units in °C/W) is a function of thermal impedances  $\theta_1$  through  $\theta_{10}$ .

**Table 2: Thermal Coefficient Data (units in °C/W)**

Part Number	$A_{11}, A_{22}$	$A_{12}, A_{21}$	$A_{13}, A_{31}$	$A_{24}, A_{42}$	$A_{14}, A_{41}$	$A_{23}, A_{32}$	$A_{33}, A_{44}$	$A_{34}, A_{43}$
HCPL-315J	198	64	62	64	83	90	137	69

**NOTE:** Maximum junction temperature for above part: 125°C.

## LED Drive Circuit Considerations for Ultra High CMR Performance

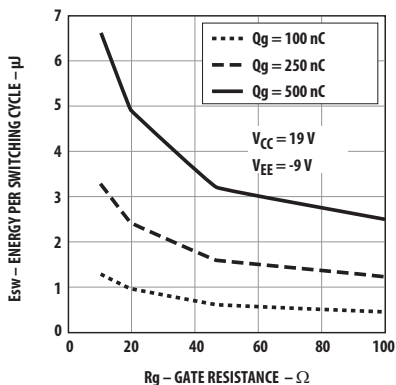
Without a detector shield, the dominant cause of optocoupler CMR failure is capacitive coupling from the input side of the optocoupler, through the package, to the detector IC as shown in Figure 33. The HCPL-3150/315J improves CMR performance by using a detector IC with an optically transparent Faraday shield, which diverts the capacitively coupled current away from the sensitive IC circuitry. However, this shield does not eliminate the capacitive coupling between the LED and optocoupler pins 5 to 8 as shown in Figure 34. This capacitive coupling causes perturbations in the LED current during common mode transients and becomes the major source of CMR failures for a shielded optocoupler. The main design objective of a high CMR LED drive circuit becomes keeping the LED in the proper state (on or off) during common mode transients. For example, the recommended application circuit (Figure 25 and Figure 26), can achieve 15kV/μs CMR while minimizing component complexity.

Techniques to keep the LED in the proper state are discussed in the next two sections.

### CMR with the LED On (CMR<sub>H</sub>)

A high CMR LED drive circuit must keep the LED on during common mode transients. This is achieved by overdriving the LED current beyond the input threshold so that it is not pulled below the threshold during a transient. A minimum LED current of 10 mA provides adequate margin over the maximum I<sub>FLH</sub> of 5 mA to achieve 15kV/μs CMR.

**Figure 32: Energy Dissipated in the HCPL-3150 for Each IGBT Switching Cycle.**



### CMR with the LED Off (CMR<sub>L</sub>)

A high CMR LED drive circuit must keep the LED off ( $V_F \leq V_{F(OFF)}$ ) during common mode transients. For example, during a  $-dV_{CM}/dt$  transient in Figure 35, the current flowing through  $C_{LEDP}$  also flows through the  $R_{SAT}$  and  $V_{SAT}$  of the logic gate. As long as the low state voltage developed across the logic gate is less than  $V_{F(OFF)}$ , the LED will remain off and no common mode failure will occur.

The open collector drive circuit, shown in Figure 36, cannot keep the LED off during a  $+dV_{CM}/dt$  transient, since all the current flowing through  $C_{LEDN}$  must be supplied by the LED, and it is not recommended for applications requiring ultra-high CMR<sub>L</sub> performance. Figure 37 is an alternative drive circuit which, like the recommended application circuit (Figure 25 and Figure 26), does achieve ultra-high CMR performance by shunting the LED in the off state.

### Under Voltage Lockout Feature

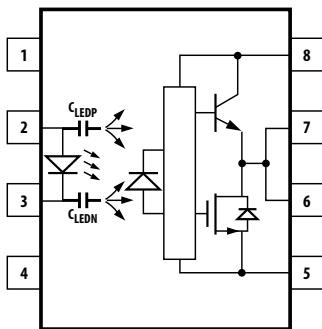
The HCPL-3150/315J contains an under voltage lockout (UVLO) feature that is designed to protect the IGBT under fault conditions that cause the HCPL-3150/315J supply voltage (equivalent to the fully-charged IGBT gate voltage) to drop below a level necessary to keep the IGBT in a low resistance state. When the HCPL-3150/315J output is in the high state and the supply voltage drops below the HCPL-3150/315J  $V_{UVLO-}$  threshold ( $9.5 < V_{UVLO-} < 12.0$ ), the optocoupler output will go into the low state with a typical delay, UVLO Turn Off Delay, of 0.6 μs. When the HCPL-3150/315J output is in the low state and the supply voltage rises above the HCPL-3150/315J  $V_{UVLO+}$  threshold ( $11.0 < V_{UVLO+} < 13.5$ ), the optocoupler will go into the high state (assuming LED is "ON") with a typical delay, UVLO TURN On Delay, of 0.8 μs.

## IPM Dead Time and Propagation Delay Specifications

The HCPL-3150/315J includes a Propagation Delay Difference (PDD) specification intended to help designers minimize “dead time” in their power inverter designs. Dead time is the time period during which both the high and low side power transistors (Q1 and Q2 in Figure 38) are off. Any overlap in Q1 and Q2 conduction will result in large currents flowing through the power devices from the high- to the low-voltage motor rails.

To minimize dead time in a given design, the turn on of LED2 should be delayed (relative to the turn off of LED1) so that under worst-case conditions, transistor Q1 has just turned off when transistor Q2 turns on, as shown in Figure 38. The amount of delay necessary to achieve this condition is equal to the maximum value of the propagation delay difference specification,  $PDD_{MAX}$ , which is specified to be 350 ns over the operating temperature range of  $-40^{\circ}\text{C}$  to  $100^{\circ}\text{C}$ .

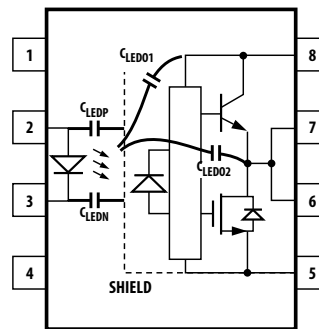
**Figure 33: Optocoupler Input to Output Capacitance Model for Unshielded Optocouplers**



Delaying the LED signal by the maximum propagation delay difference ensures that the minimum dead time is zero, but it does not tell a designer what the maximum dead time will be. The maximum dead time is equivalent to the difference between the maximum and minimum propagation delay difference specifications as shown in Figure 39. The maximum dead time for the HCPL-3150/315J is 700 ns ( $= 350 \text{ ns} - (-350 \text{ ns})$ ) over an operating temperature range of  $-40^{\circ}\text{C}$  to  $100^{\circ}\text{C}$ .

Note that the propagation delays used to calculate PDD and dead time are taken at equal temperatures and test conditions since the optocouplers under consideration are typically mounted in close proximity to each other and are switching identical IGBTs.

**Figure 34: Optocoupler Input to Output Capacitance Model for Shielded Optocouplers**



**Figure 35: Equivalent Circuit for Figure 25 During Common Mode Transient**

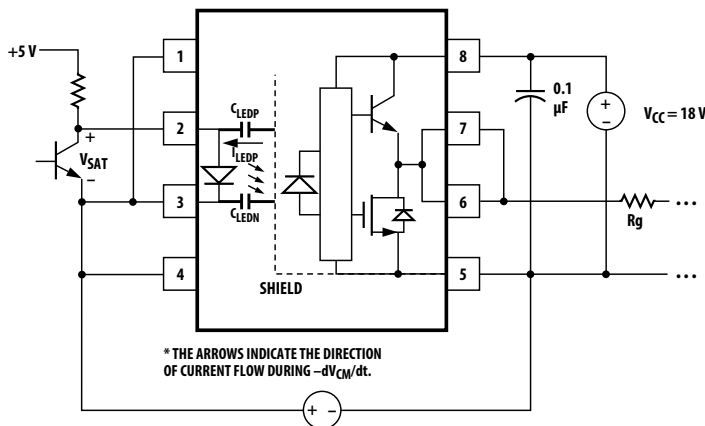




Figure 36: Not Recommended Open Collector Drive Circuit

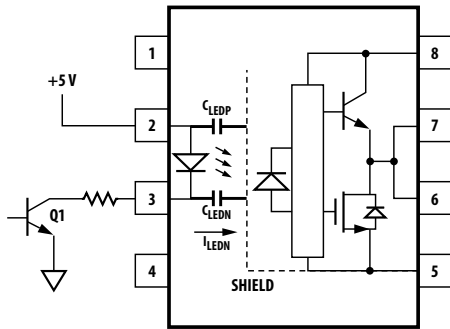


Figure 37: Recommended LED Drive Circuit for Ultra-High CMR

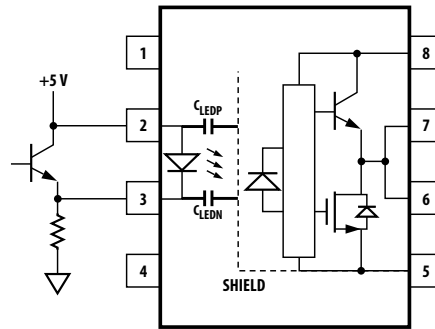
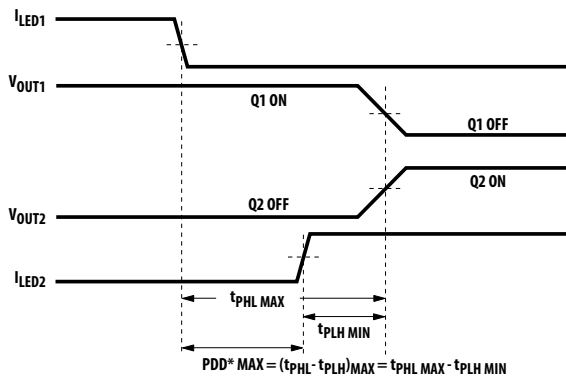
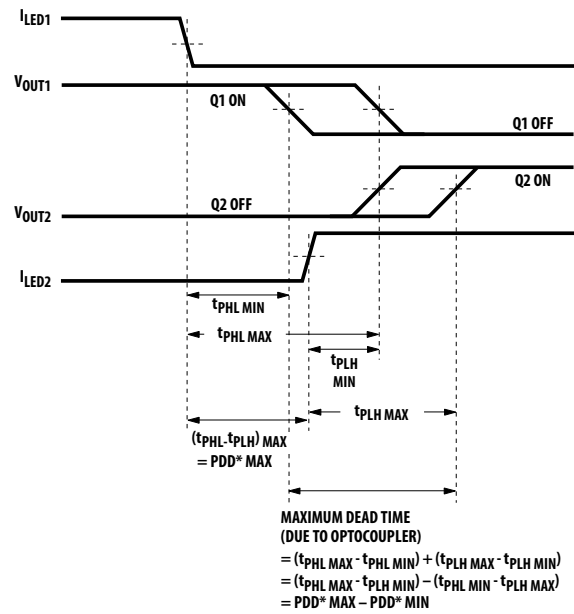


Figure 38: Minimum LED Skew for Zero Dead Time



\*PDD = PROPAGATION DELAY DIFFERENCE  
 NOTE: FOR PDD CALCULATIONS THE PROPAGATION DELAYS  
 ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 39: Waveforms for Dead Time



\*PDD = PROPAGATION DELAY DIFFERENCE  
 NOTE: FOR DEAD TIME AND PDD CALCULATIONS ALL PROPAGATION  
 DELAYS ARE TAKEN AT THE SAME TEMPERATURE AND TEST CONDITIONS.

Figure 40: Under Voltage Lock Out

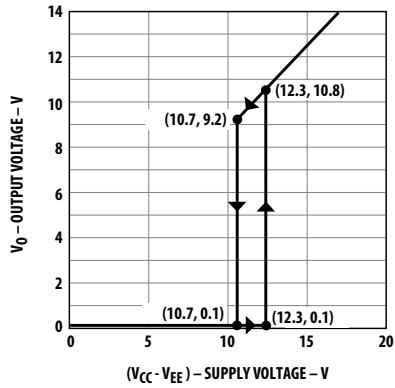


Figure 41: HCPL-3150: Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per IEC/EN/DIN EN 60747-5-5

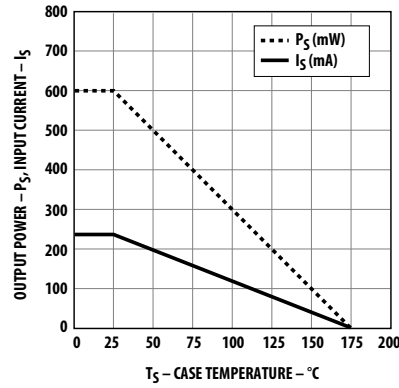


Figure 42: HCPL-315J: Thermal Derating Curve, Dependence of Safety Limiting Value with Case Temperature per IEC/EN/DIN EN 60747-5-5

