HCPL-4504/J454/0454, HCNW4504
High CMR, High Speed Optocouplers

AVAGO TECHNOLOGIES

Data Sheet

Lead (Pb) Free
RoHS 6 fully compliant

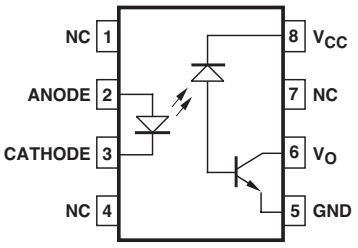
RoHS 6 fully compliant options available;
-xxxE denotes a lead-free product

Description

The HCPL-4504 and HCPL-0454 contain a GaAsP LED while the HCPL-J454 and HCNW4504 contain an AlGaAs LED. The LED is optically coupled to an integrated high gain photo detector.

The HCPL-4504 series has short propagation delays and high CTR. The HCPL-4504 series also has a guaranteed propagation delay difference (t_{PLH}-t_{PHL}). These features make the HCPL-4504 series an excellent solution to IPM inverter dead time and other switching problems. The CTR, propagation delay, and CMR are specified both for TTL and IPM conditions which are provided for ease of application. These single channel, diode-transistor optocouplers are available in 8-Pin DIP, SO-8, and Widebody package configurations. An insulating layer between a LED and an integrated photodetector provide electrical insulation between input and output. Separate connections for the photodiode bias and output-transistor collector increase the speed up to a hundred times that of a conventional phototransistor coupler by reducing the base collector capacitance.

Functional Diagram

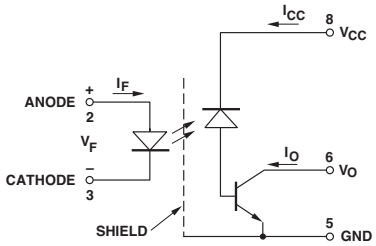


TRUTH TABLE

LED	VO
ON	LOW
OFF	HIGH

A 0.1 µF bypass capacitor between pins 5 and 8 is recommended.

Schematic



Features

- Short propagation delays for TTL and IPM applications
- 15 kV/µs minimum Common Mode Transient immunity at V_{CM} = 1500 V for TTL/load drive
- High CTR at T_A = 25°C
  - >25% for HCPL-4504/0454
  - >23% for HCNW4504
  - >19% for HCPL-J454
- Electrical specifications for common IPM applications
- TTL compatible
- Open collector output
- Safety approval:
  UL recognized
  – 3750 V rms/1min. for HCPL-4504/0454/J454
  – 5000 V rms/1min. for HCPL-4504 Option 020 and HCNW4504
  CSA approved
  IEC/EN/DIN EN 60747-5-2 approved
  – V_{IORM} = 560 Vpeak for HCPL-0454 Option 060
  – V_{IORM} = 630 Vpeak for HCPL-4504 Option 060
  – V_{IORM} = 891 Vpeak for HCPL-J454
  – V_{IORM} = 1414 Vpeak for HCNW4504

Applications

- Inverter circuits and Intelligent Power Module (IPM) interfacing: High Common Mode Transient immunity (> 10 kV/µs for an IPM load/drive) and (t_{PLH} - t_{PHL}) Specified (see Power Inverter Dead Time section)
- Line receivers: Short propagation delays and low input-output capacitance
- High speed logic ground isolation: TTL/TTL, TTL/CMOS, TTL/LSTTL
- Replaces pulse transformers: Save board space and weight
- Analog signal ground isolation: Integrated photodetector provides improved linearity over phototransistors

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Ordering Information

HCPL-0454, HCPL-4504 and HCPL-J454 are UL Recognized with 3750 Vrms for 1 minute per UL1577.

HCNW4504 is UL Recognized with 5000 Vrms for 1 minute per UL1577. HCPL-0454, HCPL-4504, HCPL-J454 and HCNW4504 are approved under CSA Component Acceptance Notice #5, File CA 88324.

Part Number	Option		Package	Surface Mount	Gull Wing	Tape & Reel	UL 1577 5000 Vrms/ 1 Minute rating	IEC/EN/DIN EN 60747-5-2	Quantity
	RoHS Compliant	non RoHS Compliant							
HCPL-4504	-000E	no option	300 mil DIP-8						50 per tube
	-300E	#300		X	X				50 per tube
	-500E	#500		X	X	X			1000 per reel
	-020E	#020					X		50 per tube
	-320E	#320		X	X		X		50 per tube
	-520E	#520		X	X	X	X		1000 per reel
	-060E	#060						X	50 per tube
	-360E	#360		X	X			X	50 per tube
	-560E	#560		X	X	X		X	1000 per reel
HCPL-J454	-000E	no option	300 mil DIP-8					X	50 per tube
	-300E	#300		X	X			X	50 per tube
	-400E	NA		X	X			X	50 per tube
	-500E	#500		X	X	X		X	1000 per reel
	-600E	NA		X	X	X		X	750 per reel
HCPL-0454	-000E	no option	SO-8	X					100 per tube
	-500E	#500		X		X			1500 per reel
	-060E	#060		X				X	100 per tube
	-560E	#560		X		X		X	1500 per reel
HCNW4504	-000E	no option	400 mil Widebody DIP-8				X	X	42 per tube
	-300E	#300		X	X		X	X	42 per tube
	-500E	#500		X	X	X	X	X	750 per reel

To order, choose a part number from the part number column and combine with the desired option from the option column to form an order entry.

Example 1:

HCPL-4504-560E to order product of 300 mil DIP Gull Wing Surface Mount package in Tape and Reel packaging with IEC/EN/DIN EN 60747-5-2 Safety Approval and RoHS compliant.

Example 2:

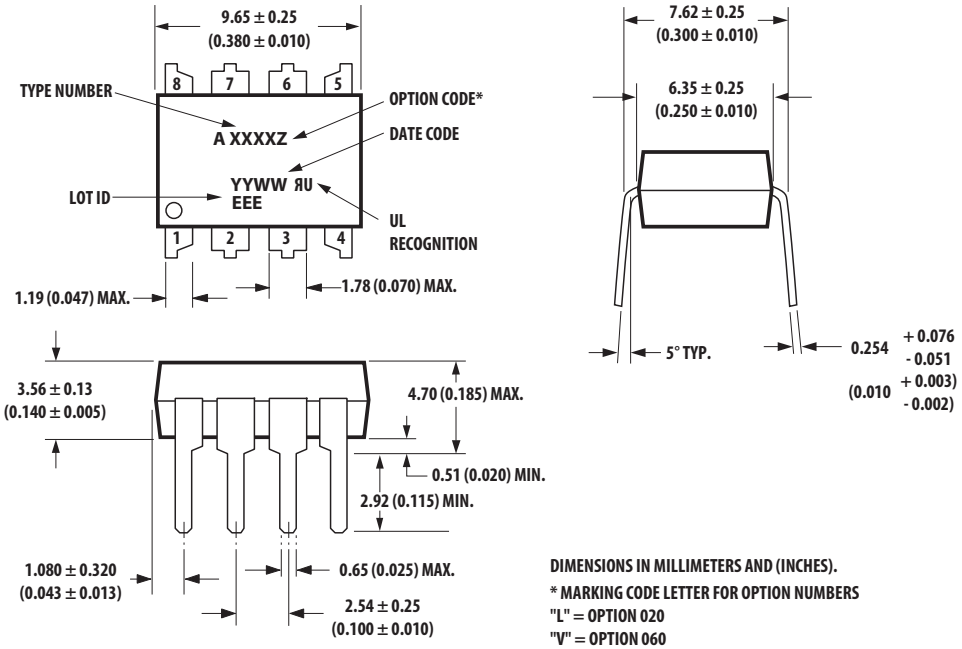
HCPL-4504 to order product of 300 mil DIP package in Tube packaging and non RoHS compliant.

Option datasheets are available. Contact your Avago sales representative or authorized distributor for information.

Remarks: The notation '#XXX' is used for existing products, while (new) products launched since July 15, 2001 and RoHS compliant will use '–XXXE.'

Package Outline Drawings

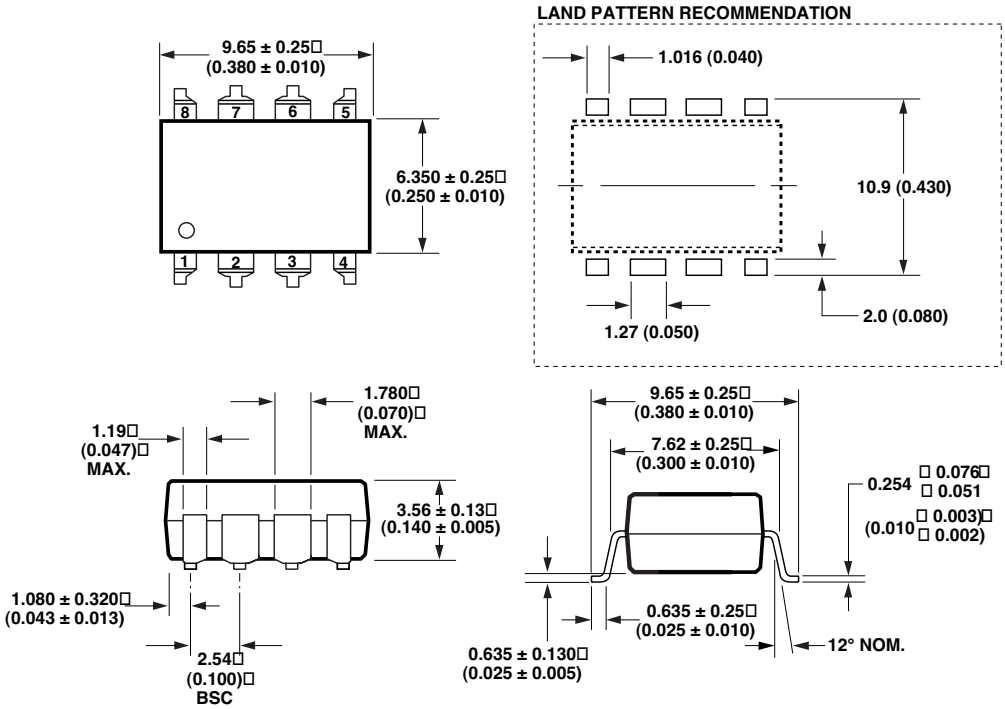
HCPL-4504 Outline Drawing



DIMENSIONS IN MILLIMETERS AND (INCHES).
* MARKING CODE LETTER FOR OPTION NUMBERS
"L" = OPTION 020
"V" = OPTION 060
OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

HCPL-4504 Gull Wing Surface Mount Option 300 Outline Drawing

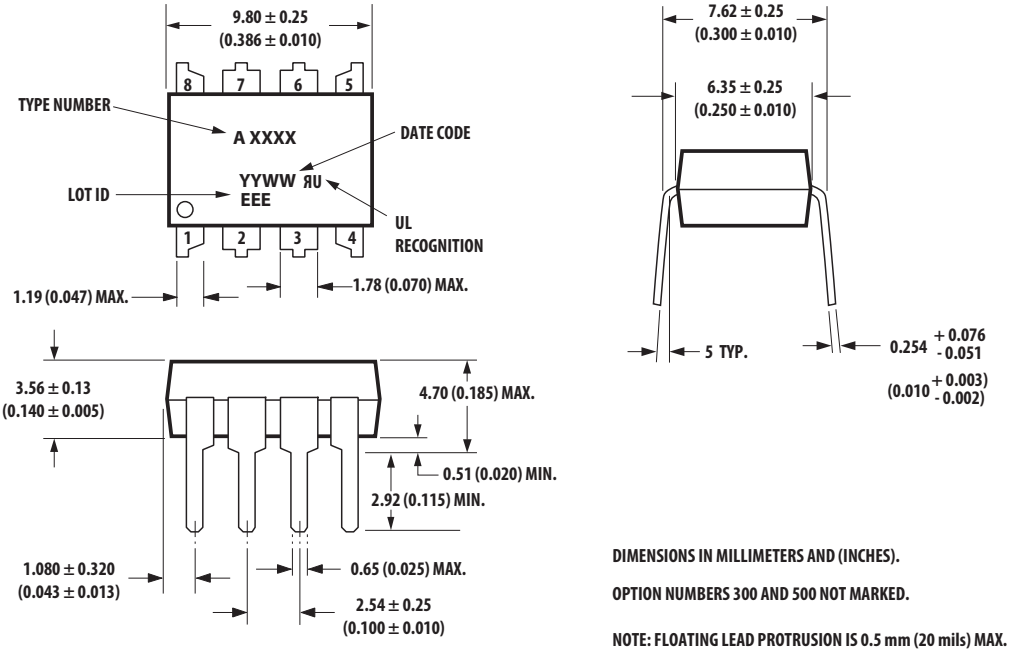


DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARIT 0.10 (0.004 INCHES).

NOTE LOATIN LEAD PROTRSION IS 0.25 (10)

Package Outline Drawings

HCPL-J454 Outline Drawing

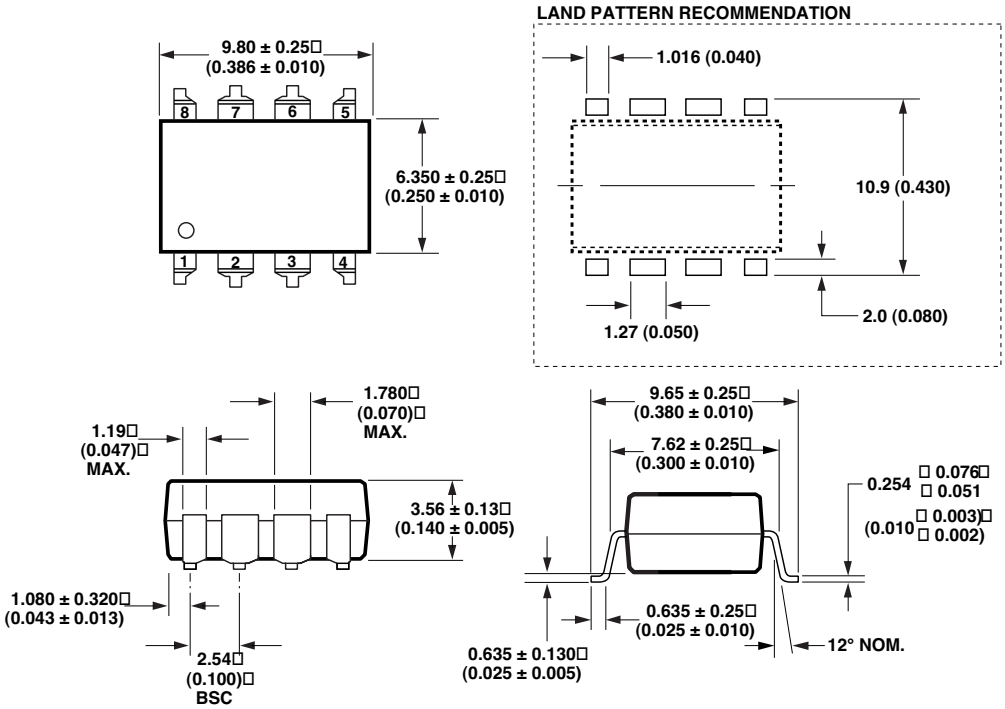


DIMENSIONS IN MILLIMETERS AND (INCHES).

OPTION NUMBERS 300 AND 500 NOT MARKED.

NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

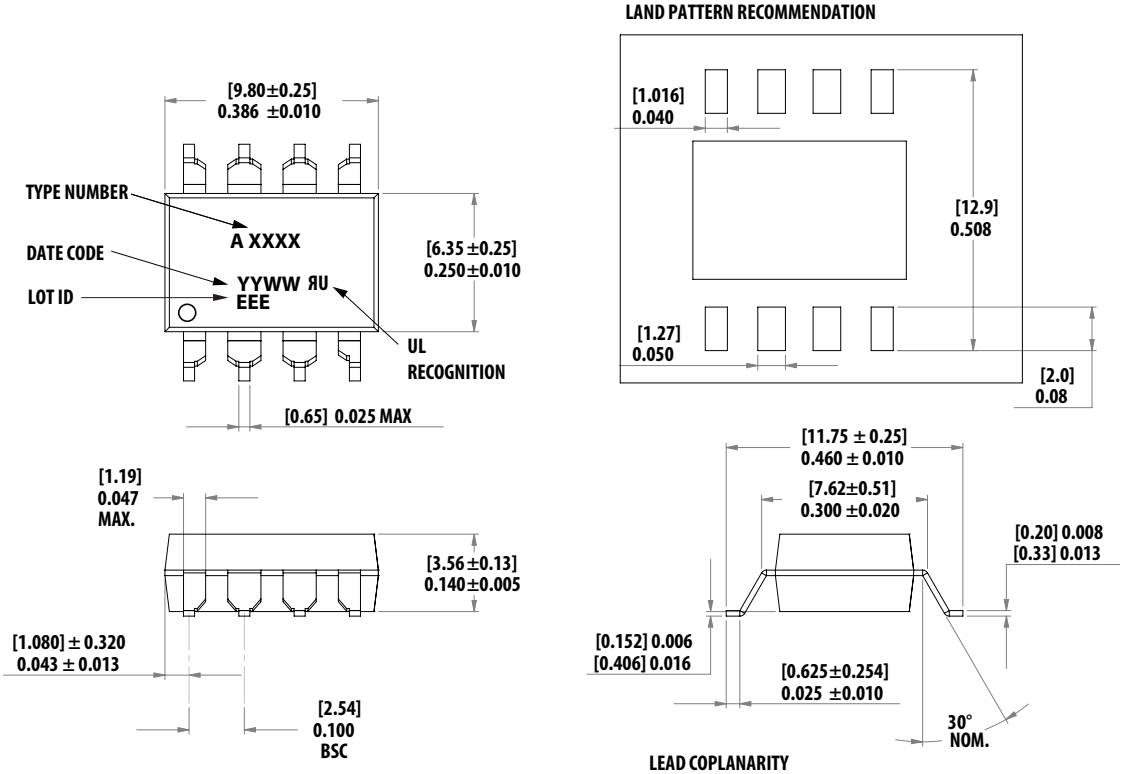
HCPL-J454 Gull Wing Surface Mount Option 300 Outline Drawing



DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

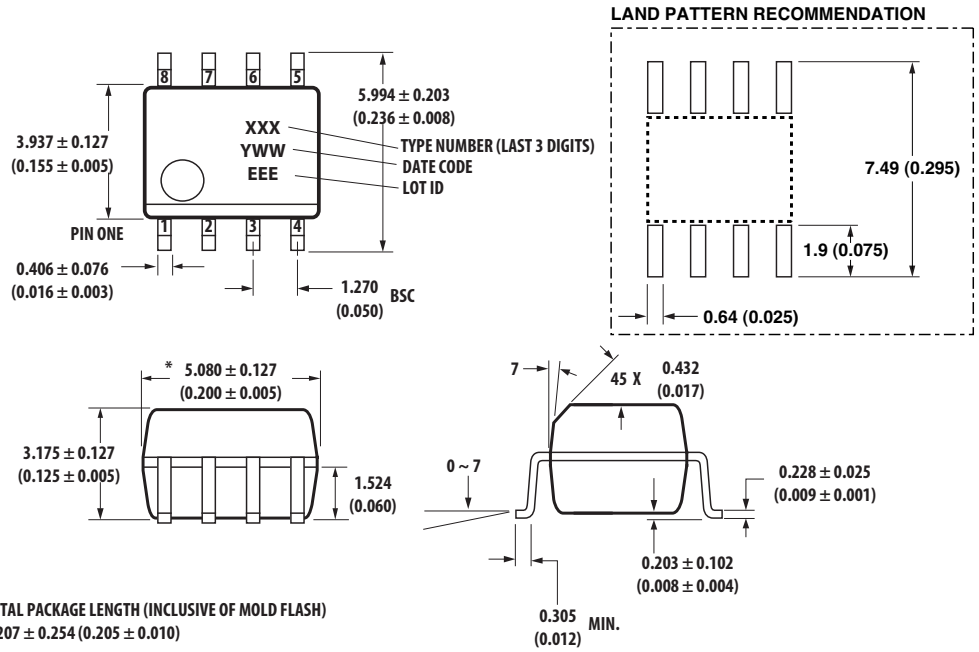
NOTE LOATIN LEAD PROTRSION IS 0.5 mm (20 m) MAX.

HCPL-J454-400E/600E Widelead Gullwing Surface Mount Outline Drawing



DIMENSIONS IN [MILLIMETERS] INCHES
OPTION NUMBERS 400 AND 600 NOT MARKED.
NOTE: FLOATING LEAD PROTRUSION IS 0.5 mm (20 mils) MAX.

HCPL-0454 Outline Drawing (8-Pin Small Outline Package)

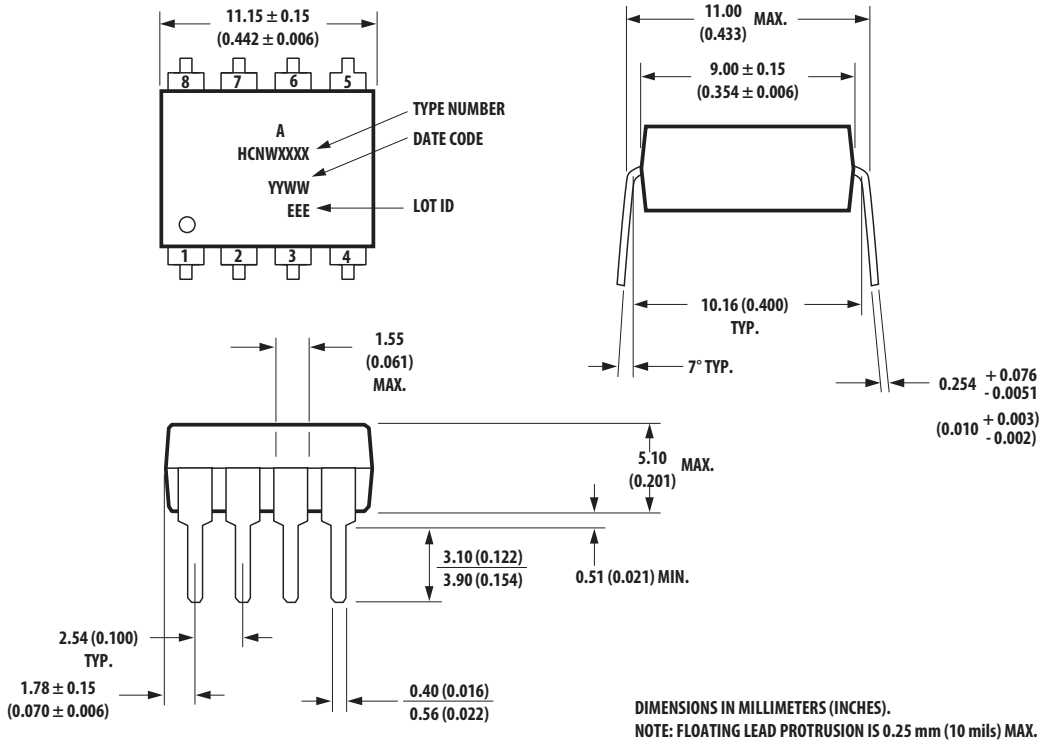


* TOTAL PACKAGE LENGTH (INCLUSIVE OF MOLD FLASH)
5.207 ± 0.254 (0.205 ± 0.010)

DIMENSIONS IN MILLIMETERS (INCHES).
LEAD COPLANARITY = 0.10 mm (0.004 INCHES) MAX.

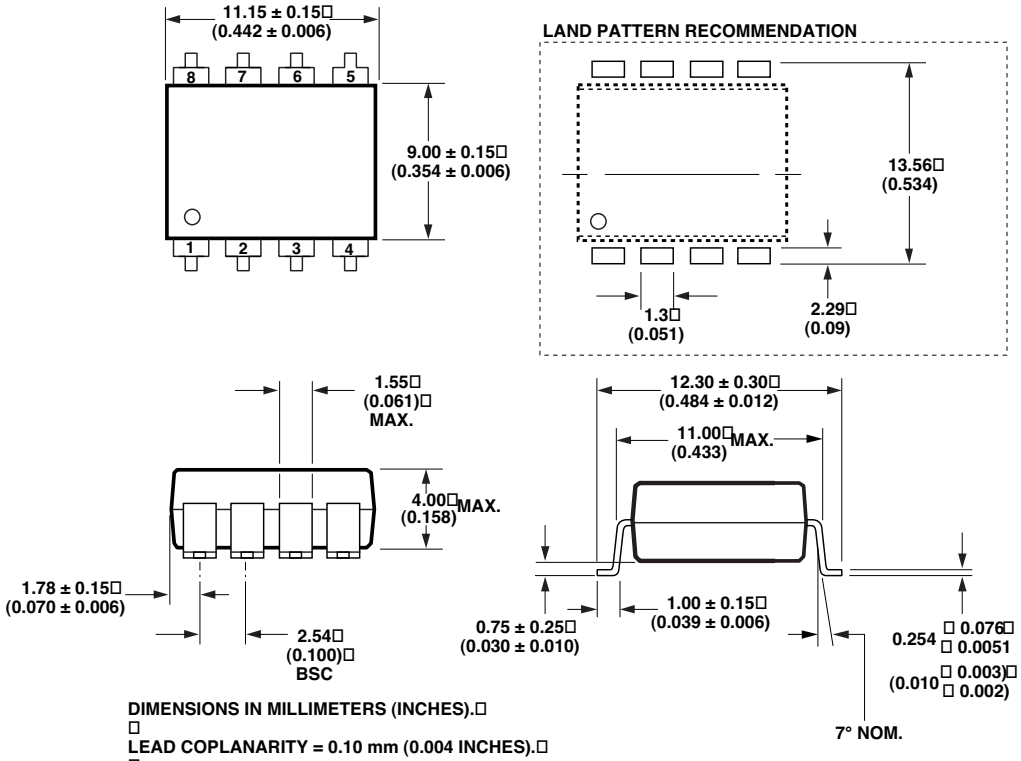
NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

HCNW4504 Outline Drawing (8-Pin Widebody Package)



DIMENSIONS IN MILLIMETERS (INCHES).
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

HCNW4504 Gull Wing Surface Mount Option 300 Outline Drawing

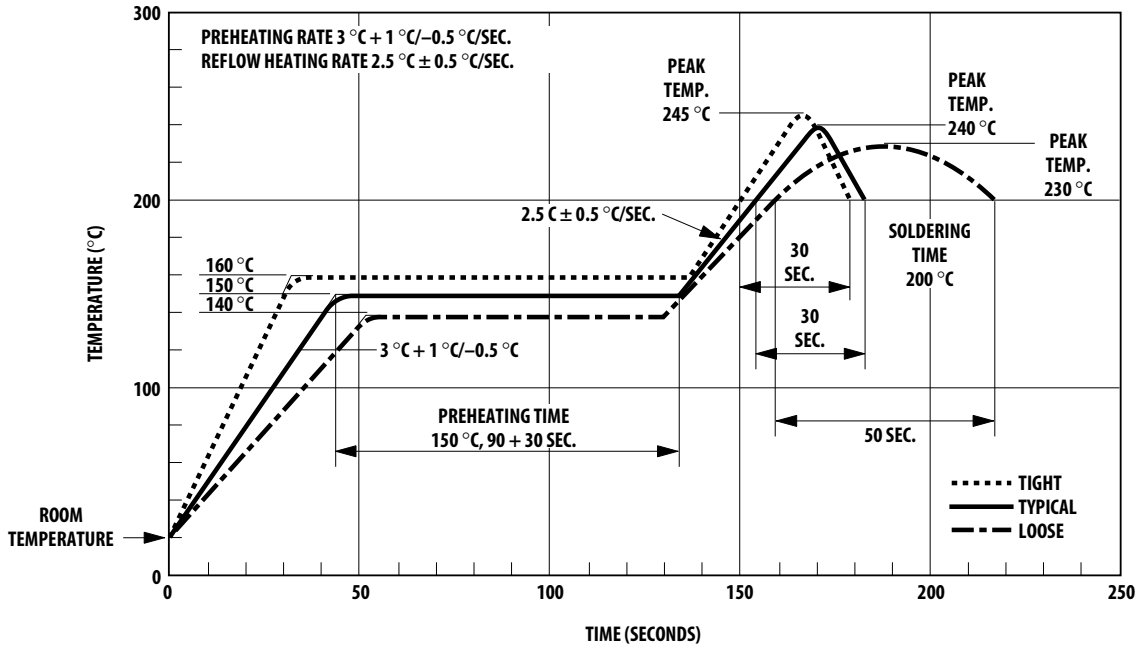


DIMENSIONS IN MILLIMETERS (INCHES).

LEAD COPLANARITY = 0.10 mm (0.004 INCHES).

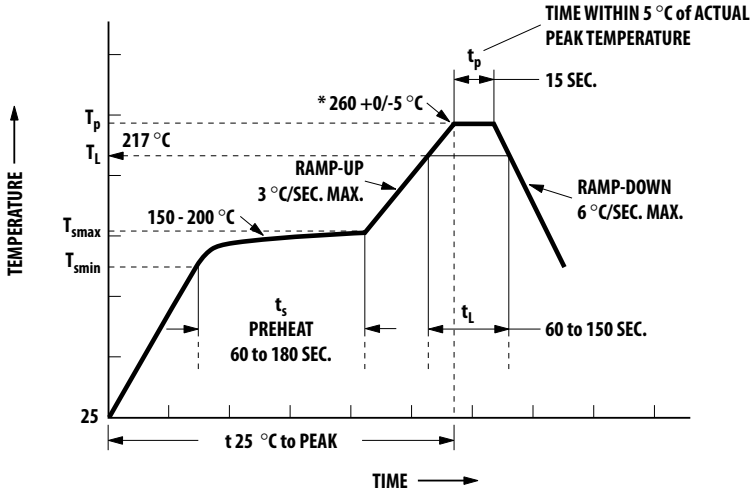
NOTE: FLOATING LEAD PROTRUSION IS 0.25 mm (10 mils) MAX.

Solder Reflow Temperature Profile



NOTE: NON-HALIDE FLUX SHOULD BE USED.

Recommended Pb-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

NOTE: NON-HALIDE FLUX SHOULD BE USED.

* RECOMMENDED PEAK TEMPERATURE FOR WIDEBODY 400mils PACKAGE IS 245 °C

Regulatory Information

The devices contained in this data sheet have been approved by the following agencies:

Agency/Standard		HCPL-4504	HCPL-J454	HCPL-0454	HCNW4504
Underwriters Laboratories (UL) Recognized under UL1577, Component Recognition Program, Category FPQU2, File E55361	UL1577	3750 Vrms / 1 minute, Option 020 5000 Vrms / 1 minute	3750 Vrms / 1 minute	3750 Vrms / 1 minute	5000 Vrms / 1 minute
Canadian Standards Association (CSA) File CA88324	Component Acceptance Notice #5	3750 Vrms / 1 minute, Option 020 5000 Vrms / 1 minute	3750 Vrms / 1 minute	3750 Vrms / 1 minute	5000 Vrms / 1 minute
IEC/EN/DIN EN 60747-5-2 Approved under: IEC 60747-5-2:1997 + A1:2002 EN 60747-5-2:2001 + A1:2002 DIN EN 60747-5-2 (VDE 0884 Teil 2):2003-01		Option 060 V_{IORM} = 630 Vpeak	V_{IORM} = 891 Vpeak	Option 060 V_{IORM} = 560 Vpeak	V_{IORM} = 1414 Vpeak

Insulation and Safety Related Specifications

		Value						
Parameter	**Symbol**	**HCPL-4504**	**HCPL-J454 -400E/-600E**	**HCPL-J454 All other options**	**HCPL-0454**	**HCNW 4504**	**Units**	**Conditions**
Minimum External Air Gap (External Clearance)	L(101)	7.1	8.0	7.4	4.9	9.6	mm	Measured from input terminals to output terminals, shortest distance through air.
Minimum External Tracking (External Creepage)	L(102)	7.4	8.0	8.0	4.8	10.0	mm	Measured from input terminals to output terminals, shortest distance path along body.
Minimum Internal Plastic Gap (Internal Clearance)		0.08	0.5	0.5	0.08	1.0	mm	Through insulation distance, conductor to conductor, usually the direct distance between the photoemitter and photodetector inside the optocoupler cavity.
Minimum Internal Tracking (Internal Creepage)		NA	NA	NA	NA	4.0	mm	Measured from input terminals to output terminals, along internal cavity.
Tracking Resistance (Comparative Tracking Index)	CTI	≥175	≥175	≥175	≥175	≥200	Volts	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa	IIIa	IIIa	IIIa	IIIa		Material Group (DIN VDE 0110, 1/89, Table 1)

All Avago data sheets report the creepage and clearance inherent to the optocoupler component itself. These dimensions are needed as a starting point for the equipment designer when determining the circuit insulation requirements.

However, once mounted on a printed circuit board, minimum creepage and clearance requirements must be met as specified for individual equipment standards. For creepage, the shortest distance path along the surface of a printed circuit board between the solder fillets of the input and output leads must be considered. There are recommended techniques such as grooves and ribs which may be used on a printed circuit board to achieve desired creepage and clearances. Creepage and clearance distances will also change depending on factors such as pollution degree and insulation level.

IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics

Description	Symbol	HCPL-0454 OPTION 060	HCPL-4504 OPTION 060	HCPL-J454	HCNW4504	Unit
Installation classification per DIN VDE 0110/1.89, Table 1						
for rated mains voltage ≤150 V rms		I-IV	I-IV	I-IV	I-IV	
for rated mains voltage ≤300 V rms		I-III	I-IV	I-IV	I-IV	
for rated mains voltage ≤450 V rms			I-III	I-III	I-IV	
for rated mains voltage ≤600 V rms				I-III	I-IV	
for rated mains voltage ≤1000 V rms					I-III	
Climatic Classification		55/100/21	55/100/21	55/100/21	55/85/21	
Pollution Degree (DIN VDE 0110/1.89)		2	2	2	2	
Maximum Working Insulation Voltage	V_{IORM}	560	630	891	1414	V_{peak}
Input to Output Test Voltage, Method b* V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 sec, Partial Discharge < 5 pC	V_{PR}	1050	1181	1670	2652	V_{peak}
Input to Output Test Voltage, Method a* V_{IORM} x 1.5 = V_{PR}, Type and Sample Test, t_m = 60 sec, Partial Discharge < 5 pC	V_{PR}	840	945	1336	2121	V_{peak}
Highest Allowable Overvoltage* (Transient Overvoltage, t_{ini} = 10 sec)	V_{IOTM}	4000	6000	6000	8000	V_{peak}
Safety Limiting Values - Maximum Values Allowed in the Event of a Failure, also see Thermal Derating curve						
Case Temperature	T_S	150	175	175	150	°C
Input Current	$I_{S,INPUT}$	150	230	400	400	mA
Output Power	$P_{S,OUTPUT}$	600	600	600	700	mW
Insulation Resistance at T_S, V_{IO} = 500 V	R_S	$\geq 10^9$	$\geq 10^9$	$\geq 10^9$	$\geq 10^9$	Ω

*Refer to the optocoupler section of the Designer's Catalog, under regulatory information (IEC/EN/DIN EN 60747-5-2) for a detailed description of Method a and Method b partial discharge test profiles.

NOTE: These optocouplers are suitable for "safe electrical isolation" only within the safety limit data. Maintenance of the safety data shall be ensured by means of protective circuits.

NOTE: Insulation Characteristics are per IEC/EN/DIN EN 60747-5-2.

NOTE: Surface mount classification is Class A in accordance with CECC 00802.

Absolute Maximum Ratings

Parameter	Symbol	Device	Min.	Max.	Units	Note
Storage Temperature	T_S		-55	125	°C	
Operating Temperature	T_A	HCPL-4504 HCPL-0454 HCPL-J454	-55	100	°C	
		HCNW4504	-55	85		
Average Forward Input Current	$I_{F(AVG)}$			25	mA	1
Peak Forward Input Current (50% duty cycle, 1 ms pulse width)	$I_{F(PEAK)}$	HCPL-4504 HCPL-0454		50	mA	2
		HCPL-J454 HCNW4504		40		
Peak Transient Input Current (≤1 µs pulse width, 300 pps)	$I_{F(TRANS)}$	HCPL-4504 HCPL-0454		1	A	
		HCPL-J454 HCNW4504		0.1		
Reverse LED Input Voltage (Pin 3-2)	V_R	HCPL-4504 HCPL-0454		5	V	
		HCPL-J454 HCNW4504		3		
Input Power Dissipation	P_{IN}	HCPL-4504 HCPL-0454		45	mW	3
		HCPL-J454 HCNW4504		40		
Average Output Current (Pin 6)	$I_{O(AVG)}$			8	mA	
Peak Output Current	$I_{O(PEAK)}$			16	mA	
Supply Voltage (Pin 8-5)	V_{CC}		-0.5	30	V	
Output Voltage (Pin 6-5)	V_O		-0.5	20	V	
Output Power Dissipation	P_O			100	mW	4
Lead Solder Temperature (Through-Hole Parts Only) 1.6 mm below seating plane, 10 seconds	T_{LS}	HCPL-4504 HCPL-J454		260	°C	
Up to seating plane, 10 seconds		HCNW4504		260		
Reflow Temperature Profile	T_{RP}	HCPL-0454, Option 300 , Option 500, Option 400E & Option 600E.	See **Package Outline Drawings** section			

Electrical Specifications (DC)

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. See note 12.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions			Fig.	Note
Current Transfer Ratio	CTR	HCPL-4504 HCPL-0454	25	32	60	%	T_A = 25°C	V_O = 0.4 V	I_F = 16 mA, V_{CC} = 4.5 V	1, 2, 4	5
			21	34				V_O = 0.5 V			
		HCPL-J454	19	37	60		T_A = 25°C	V_O = 0.4 V			
			13	39				V_O = 0.5 V			
		HCNW4504	23	29	60		T_A = 25°C	V_O = 0.4 V			
			19	31	63			V_O = 0.5 V			
Current Transfer Ratio	CTR	HCPL-4504 HCPL-0454	26	35	65	%	T_A = 25°C	V_O = 0.4 V	I_F = 12 mA, V_{CC} = 4.5 V	1, 2, 4	5
			22	37				V_O = 0.5 V			
		HCPL-J454	21	43	65		T_A = 25°C	V_O = 0.4 V			
			16	45				V_O = 0.5 V			
		HCNW4504	25	33	65		T_A = 25°C	V_O = 0.4 V			
			21	35	68			V_O = 0.5 V			
Logic Low Output Voltage	V_{OL}	HCPL-4504 HCPL-0454		0.2	0.4	V	T_A = 25°C	I_O = 4.0 mA	I_F = 16 mA, V_{CC} = 4.5 V		
					0.5			I_O = 3.3 mA			
		HCPL-J454		0.2	0.4		T_A = 25°C	I_O = 3.6 mA			
				0.5				I_O = 3.0 mA			
		HCNW4504		0.2	0.4		T_A = 25°C	I_O = 3.6 mA			
				0.5				I_O = 3.0 mA			
Logic High Output Current	I_{OH}			0.003	0.5	µA	T_A = 25°C	V_O = V_{CC} = 5.5 V	I_F = 0 mA	5	
				0.01	1		T_A = 25°C	V_O = V_{CC} = 15 V			
					50						
Logic Low Supply Current	I_{CCL}	HCPL-4504 HCPL-0454 HCNW4504		50	200	µA	I_F = 16 mA, V_O = Open, V_{CC} = 15 V			12	
		HCPL-J454			70						
Logic High Supply Current	I_{CCH}			0.02	1	µA	T_A = 25°C	I_F = 0 mA, V_O = Open,		12	
					2			V_{CC} = 15 V			
Input Forward Voltage	V_F	HCPL-4504 HCPL-0454		1.5	1.7	V	T_A = 25°C	I_F = 16 mA		3	
					1.8						
		HCPL-J454 HCNW4504	1.45	1.59	1.85		T_A = 25°C	I_F = 16 mA			
			1.35		1.95						
Input Reverse Breakdown Voltage	BV_R	HCPL-4504 HCPL-0454	5			V	I_R = 10 µA				
		HCPL-J454 HCNW4504	3				I_R = 100 µA				
Temperature Coefficient of Forward Voltage	$\frac{\Delta V_F}{\Delta T_A}$	HCPL-4504 HCPL-0454		-1.6		mV/°C	I_F = 16 mA				
		HCPL-J454 HCNW4504		-1.4							
Input Capacitance	C_{IN}	HCPL-4504 HCPL-0454		60		pF	f = 1 MHz, V_F = 0 V				
		HCPL-J454 HCNW4504			70						

*All typicals at T_A = 25°C.

AC Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.	Max.	Units	Test Conditions		Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}			0.2	0.3	µs	T_A = 25°C	Pulse: f = 20 kHz, Duty Cycle = 10%, I_F = 16 mA, V_{CC} = 5.0 V, R_L = 1.9 kΩ, C_L = 15 pF, V_{THHL} = 1.5 V	6, 8, 9	9
				0.2	0.5					
	t_{PHL}		0.2	0.5	0.7	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50%, I_F = 12 mA, V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, V_{THHL} = 1.5 V	6, 10-14	10
		HCPL-J454	0.05		1.0					
		Others	0.1							
Propagation Delay Time to Logic High at Output	t_{PLH}			0.3	0.5	µs	T_A = 25°C	Pulse: f = 20 kHz, Duty Cycle = 10%, I_F = 16 mA, V_{CC} = 5.0 V, R_L = 1.9 kΩ, C_L = 15 pF, V_{THLH} = 1.5 V	6, 8, 9	9
				0.3	0.7					
	t_{PLH}		0.3	0.8	1.1	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50%, I_F = 12 mA, V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, V_{THLH} = 2.0 V	6, 10-14	10
			0.2	0.8	1.4					
Propagation Delay Difference Between Any 2 Parts	t_{PLH}-t_{PHL}		-0.4	0.3	0.9	µs	T_A = 25°C	Pulse: f = 10 kHz, Duty Cycle = 50%, I_F = 12 mA, V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, V_{THHL} = 1.5 V, V_{THLH} = 2.0 V	6, 10-14	17
			-0.7	0.3	1.3					
Common Mode Transient Immunity at Logic High	$\|CM_H\|$		15	30		kV/µs	T_A = 25°C, V_{CM} = 1500 V_{P-P}	V_{CC} = 5.0 V, R_L = 1.9 kΩ, C_L = 15 pF, I_F = 0 mA	7	7, 9
	$\|CM_H\|$		15	30		kV/µs		V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, I_F = 0 mA	7	8, 10
Level Output Common Mode Transient Immunity at Logic Low Level Output	$\|CM_L\|$		15	30		kV/µs	T_A = 25°C, V_{CM} = 1500 V_{P-P}	V_{CC} = 5.0 V, R_L = 1.9 kΩ, C_L = 15 pF, I_F = 16 mA	7	7, 9
	$\|CM_L\|$	HCPL-J454	15	30		kV/µs		V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, I_F = 12 mA	7	8, 10
		Others	10							
	$\|CM_L\|$		15	30		kV/µs		V_{CC} = 15.0 V, R_L = 20 kΩ, C_L = 100 pF, I_F = 16 mA	7	8, 10

*All typicals at T_A = 25°C.

Package Characteristics

Over recommended temperature (T_A = 0°C to 25°C) unless otherwise specified.

Parameter	Symbol	Device	Min.	Typ.*	Max.	Units	Test Conditions	Figure	Note
Input-Output Momentary Withstand Voltage†	V_{ISO}	HCPL-4504 HCPL-0454	3750			V rms	RH ≤50%, t = 1 min., T_A = 25°C		6, 13, 16
		HCPL-J454	3750						6, 14, 16
		HCPL-4504 Option 020	5000						6, 11, 15
		HCNW4504	5000						6, 15, 16
Input-Output Resistance	R_{I-O}	HCPL-4504 HCPL-0454 HCPL-J454		10^{12}		Ω	V_{I-O} = 500 Vdc		6
		HCNW4504	10^{12}	10^{13}			T_A = 25°C		
			10^{11}				T_A = 100°C		
Capacitance (Input-Output)	C_{I-O}	HCPL-4504 HCPL-0454		0.6		pF	f = 1 MHz		6
		HCPL-J454		0.8					
		HCNW4504		0.5	0.6				

All typicals at T_A = 25°C..

†The Input-Output Momentary Withstand Voltage is a dielectric voltage rating that should not be interpreted as an input-output continuous voltage rating. For the continuous voltage rating refer to the IEC/EN/DIN EN 60747-5-2 Insulation Related Characteristics Table (if applicable), your equipment level safety specification or Avago Application Note 1074 entitled "Optocoupler Input-Output Endurance Voltage."

Notes:

1. Derate linearly above 70°C free-air temperature at a rate of 0.8 mA/°C (8-Pin DIP).
   Derate linearly above 85°C free-air temperature at a rate of 0.5 mA/°C (SO-8).
2. Derate linearly above 70°C free-air temperature at a rate of 1.6 mA/°C (8-Pin DIP).
   Derate linearly above 85°C free-air temperature at a rate of 1.0 mA/°C (SO-8).
3. Derate linearly above 70°C free-air temperature at a rate of 0.9 mW/°C (8-Pin DIP).
   Derate linearly above 85°C free-air temperature at a rate of 1.1 mW/°C (SO-8).
4. Derate linearly above 70°C free-air temperature at a rate of 2.0 mW/°C (8-Pin DIP).
   Derate linearly above 85°C free-air temperature at a rate of 2.3 mW/°C (SO-8).
5. CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
6. Device considered a two-terminal device: Pins 1, 2, 3, and 4 shorted together and Pins 5, 6, 7, and 8 shorted together.
7. Under TTL load and drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 2.0$ V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 0.8$ V).
8. Under IPM (Intelligent Power Module) load and LED drive conditions: Common mode transient immunity in a Logic High level is the maximum tolerable dV_{CM}/dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., $V_O > 3.0$ V). Common mode transient immunity in a Logic Low level is the maximum tolerable dV_{CM}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., $V_O < 1.0$ V).
9. The 1.9 kΩ load represents 1 TTL unit load of 1.6 mA and the 5.6 kΩ pull-up resistor.
10. The R_L = 20 kΩ, C_L = 100 pF load represents an IPM (Intelligent Power Module) load.
11. See Option 020 data sheet for more information.
12. Use of a 0.1 µF bypass capacitor connected between Pins 5 and 8 is recommended.
13. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥4500 V rms for 1 second (leakage detection current limit, I_{i-o} ≤5 µA).
14. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥4500 V rms for 1 second (leakage detection current limit, I_{i-o} ≤ 5 µA).
15. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥6000 V rms for 1 second (leakage detection current limit, I_{i-o} ≤5 µA).
16. This test is performed before the 100% Production test shown in the VDE 0884 Insulation Related Characteristics Table, if applicable.
17. The difference between t_{PLH} and t_{PHL} between any two devices (same part number) under the same test condition. (See Power Inverter Dead Time and Propagation Delay Specifications section.)

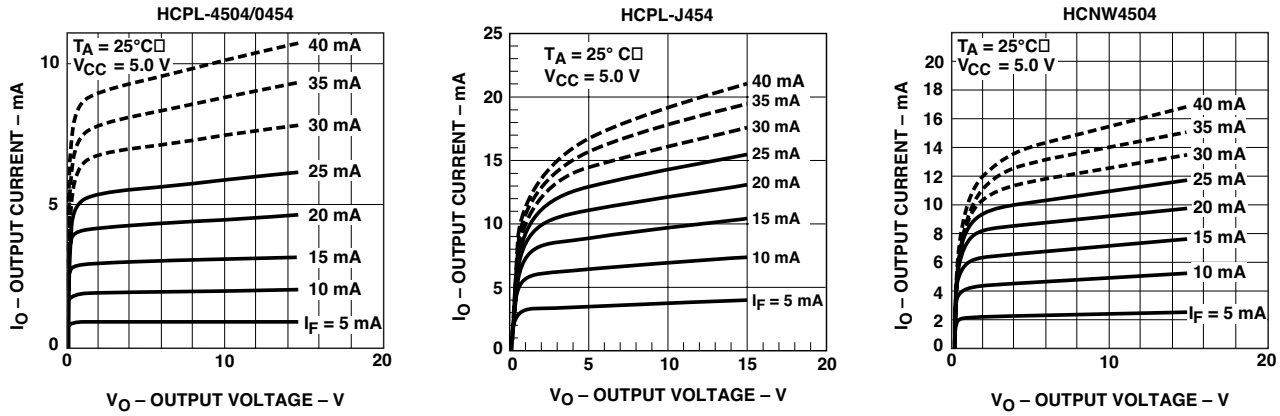


Figure 1. DC and pulsed transfer characteristics.

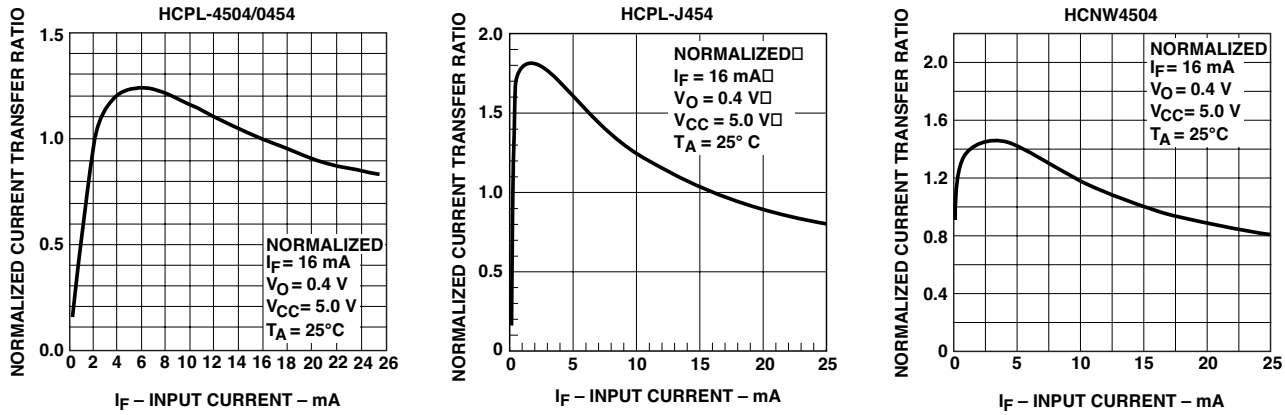


Figure 2. Current transfer ratio vs. input current.

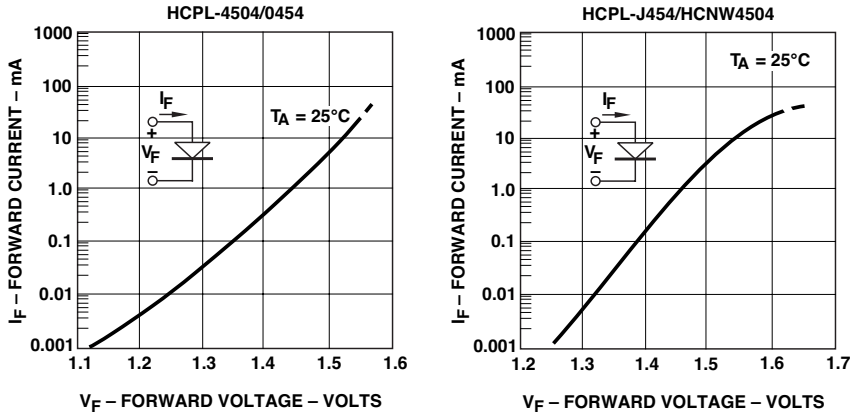


Figure 3. Input current vs. forward voltage.

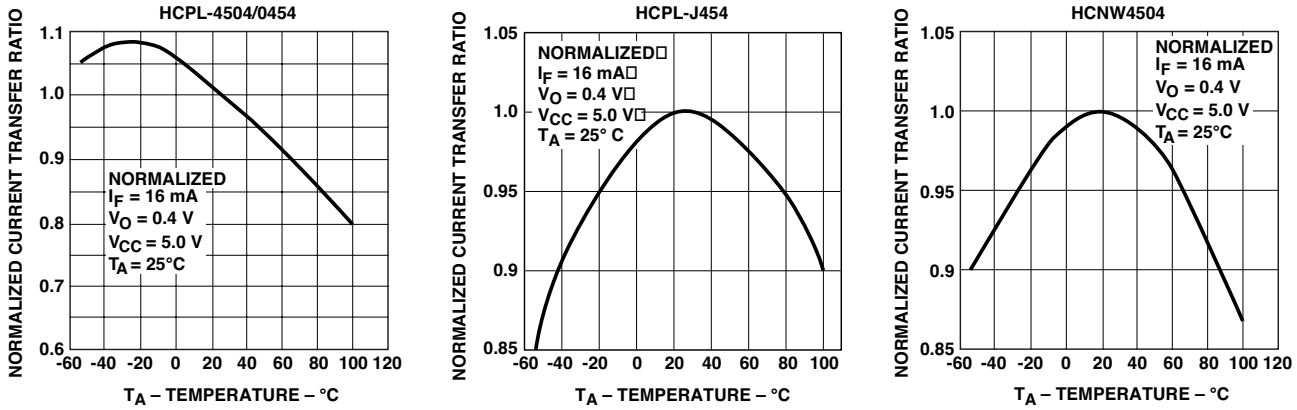


Figure 4. Current transfer ratio vs. temperature.

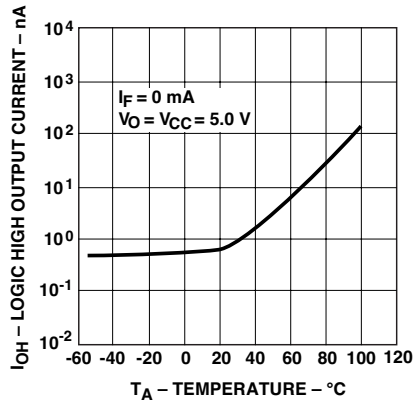


Figure 5. Logic high output current vs. temperature.

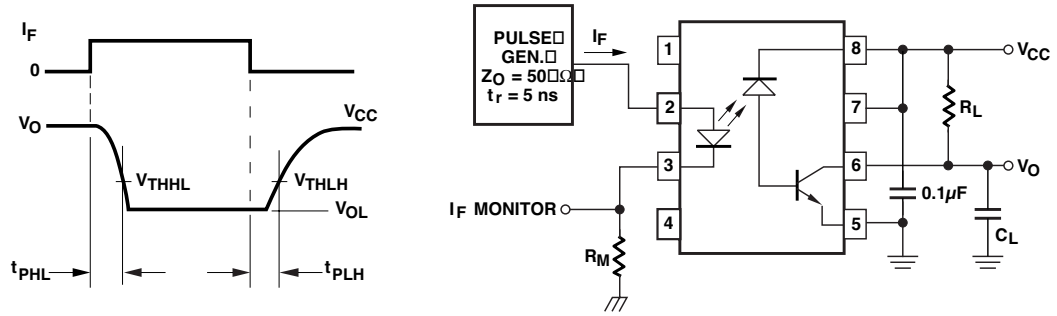


Figure 6. Switching test circuit.

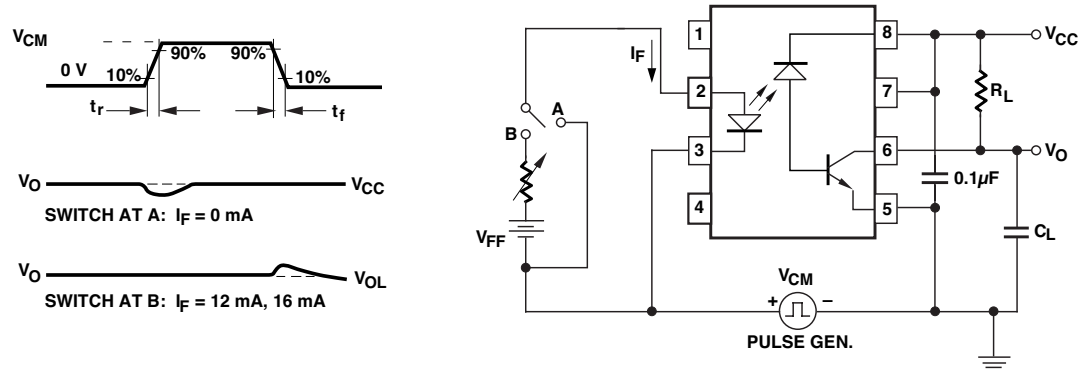
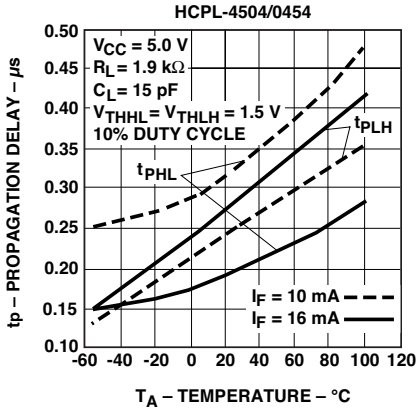


Figure 7. Test circuit for transient immunity and typical waveforms.



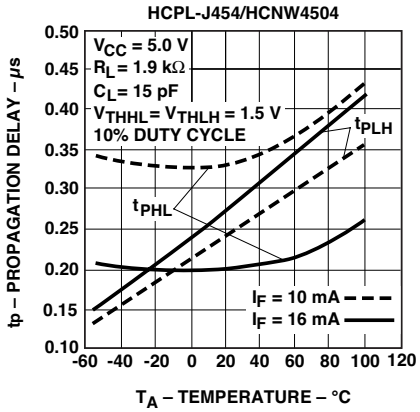


Figure 8. Propagation delay time vs. temperature.

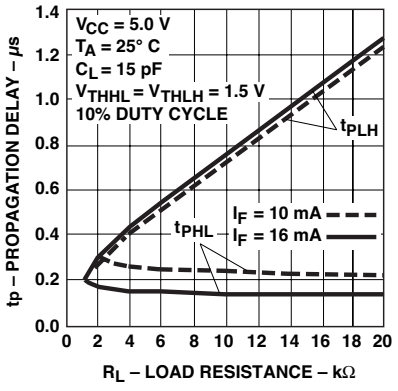


Figure 9. Propagation delay time vs. load resistance.

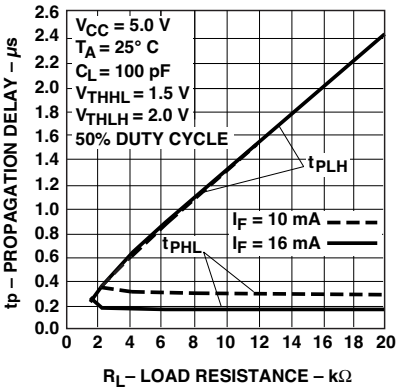


Figure 10. Propagation delay time vs. load resistance.

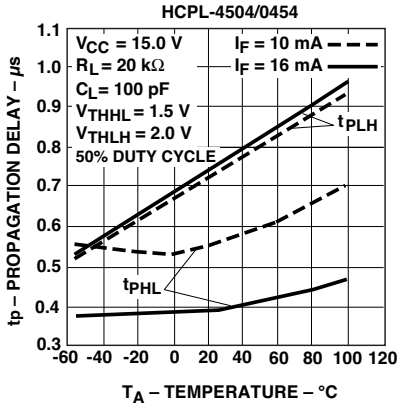
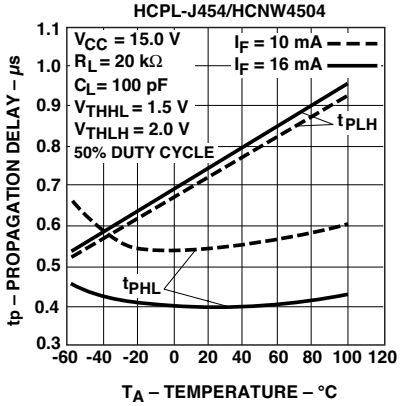


Figure 11. Propagation delay time vs. temperature.



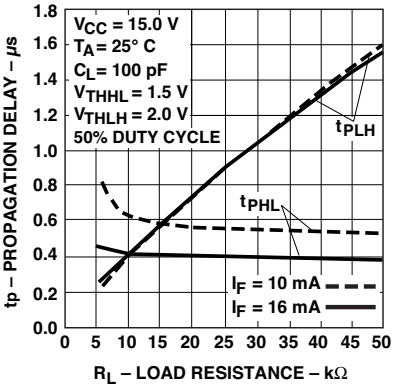


Figure 12. Propagation delay time vs. load resistance.

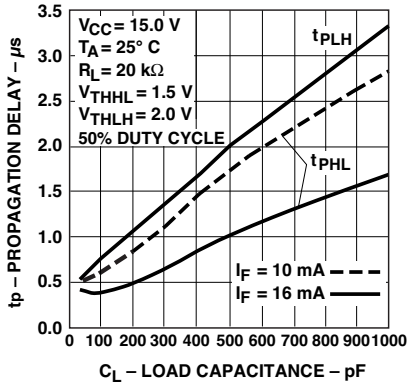


Figure 13. Propagation delay time vs. load capacitance.

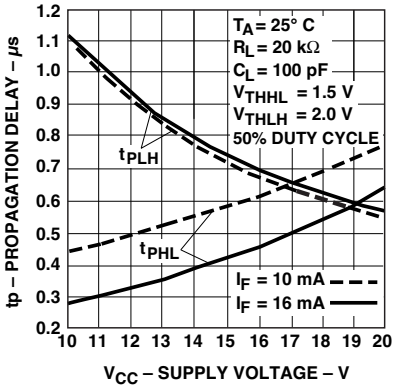


Figure 14. Propagation delay time vs. supply voltage.

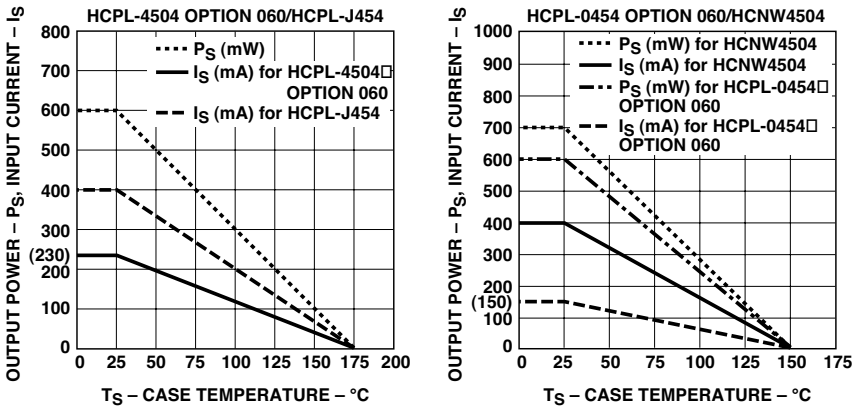


Figure 15. Thermal derating curve, dependence of safety limiting valve with case temperature per IEC/EN/DIN EN 60747-5-2.

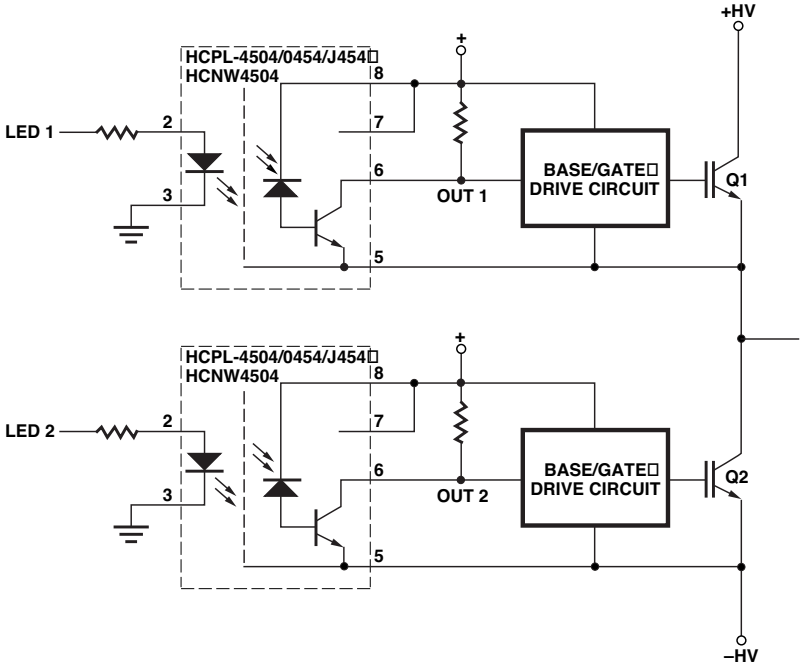


Figure 16. Typical power inverter.

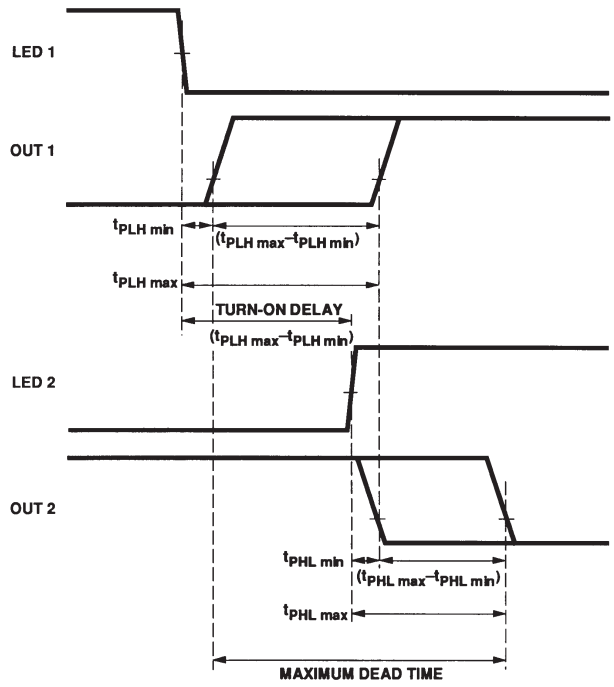


Figure 17. LED delay and dead time diagram.

Power Inverter Dead Time and Propagation Delay Specifications

The HCPL-4504/0454/J454 and HCNW4504 include a specification intended to help designers minimize "dead time" in their power inverter designs. The new "propagation delay difference" specification ($t_{PLH} - t_{PHL}$) is useful for determining not only how much optocoupler switching delay is needed to prevent "shoot-through" current, but also for determining the best achievable worst-case dead time for a given design.

When inverter power transistors switch (Q1 and Q2 in Figure 17), it is essential that they never conduct at the same time. Extremely large currents will flow if there is any overlap in their conduction during switching transitions, potentially damaging the transistors and even the surrounding circuitry. This "shoot-through" current is eliminated by delaying the turn-on of one transistor (Q2) long enough to ensure that the opposing transistor (Q1) has completely turned off. This delay introduces a small amount of "dead time" at the output of the inverter during which both transistors are off during switching transitions. Minimizing this dead time is an important design goal for an inverter designer.

The amount of turn-on delay needed depends on the propagation delay characteristics of the optocoupler, as well as the characteristics of the transistor base/gate drive circuit. Considering only the delay characteristics of the optocoupler (the characteristics of the base/gate drive circuit can be analyzed in the same way), it is important to know the minimum and maximum turn-on (t_{PHL}) and turnoff (t_{PLH}) propagation delay specifications, preferably over the desired operating temperature range. The importance of these specifications is illustrated in Figure 17. The waveforms labeled "LED1", "LED2", "OUT1", and "OUT2" are the input and output voltages of the optocoupler circuits driving Q1 and Q2 respectively. Most inverters are designed such that the power transistor turns on when the optocoupler LED turns on; this ensures that both power transistors will be off in the event of a power loss in the control circuit. Inverters can also be designed such that the power transistor turns off when the optocoupler LED turns on; this type of design, however, requires additional fail-safe circuitry to turn off the power transistor if an over-current condition is detected. The timing illustrated in Figure 17 assumes that the power transistor turns on when the optocoupler LED turns on.