

**6N134, 81028, HCPL-563x, HCPL-663x,
HCPL-565x, 5962-98001, HCPL-268K,
HCPL-665x, 5962-90855, HCPL-560x¹**



Hermetically Sealed, High Speed, High CMR,
Logic Gate Optocouplers

Data Sheet

1. See matrix for available extensions.

Description

These units are single, dual and quad channel, hermetically sealed optocouplers. The products are capable of operation and storage over the full military temperature range and can be purchased as either commercial product or with full MIL-PRF-38534 Class Level H or K testing or from the appropriate DLA Drawing. All devices are manufactured and tested on a MIL-PRF-38534 certified line and Class H and K devices are included in the DLA Qualified Manufacturers List QML-38534 for Hybrid Microcircuits. Quad channel devices are available by special order in the 16-pin DIP through hole packages.

CAUTION It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

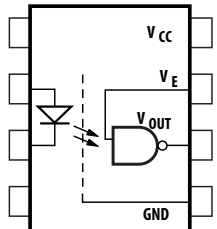
Features

- Dual marked with device part number and DLA Standard Microcircuit Drawing (SMD)
- Manufactured and tested on a MIL-PRF-38534 Certified Line
- QML-38534, Class H and K
- Five hermetically sealed package configurations
- Performance guaranteed over full military temperature range: -55°C to $+125^{\circ}\text{C}$
- High speed: 10 Mbd typical
- CMR: $> 10,000 \text{ V}/\mu\text{s}$ typical
- 1500 Vdc withstand test voltage
- 2500 Vdc withstand test voltage for HCPL-565x
- High radiation immunity
- 6N137, HCPL-2601, HCPL-2630/31 function compatibility
- Reliability data
- TTL circuit compatibility

Applications

- Military and aerospace
- High reliability systems
- Transportation, medical, and life critical systems
- Line receiver
- Voltage level shifting
- Isolated input line receiver
- Isolated output line driver
- Logic ground isolation
- Harsh industrial environments
- Isolation for computer, communication, and test equipment systems

Functional Diagram



Multiple channel devices available.

Truth Table (Positive Logic)

Multichannel Devices

| Input | Output |
|---------|--------|
| On (H) | L |
| Off (L) | H |

Single Channel DIP

| Input | Enable | Output |
|---------|--------|--------|
| On (H) | H | L |
| Off (L) | H | H |
| On (H) | L | H |
| Off (L) | L | H |

NOTE The connection of a 0.1 μF bypass capacitor between V_{CC} and GND is recommended.

Each channel contains a GaAsP light emitting diode that is optically coupled to an integrated high speed photon detector. The output of the detector is an open collector Schottky clamped transistor. Internal shields provide a guaranteed common mode transient immunity specification of 1000 V/ μs . For Isolation Voltage applications requiring up to 2500 Vdc, the HCPL-5650 family is also available. Package styles for these parts are 8- and 16-pin DIP through hole (case outlines P and E, respectively), and 16-pin surface mount DIP flat pack (case outline F), leadless ceramic chip carrier (case outline 2). Devices may be purchased with a variety of lead bend and plating options. See the Selection Guide table for details. Standard Microcircuit Drawing (SMD) parts are available for each package and lead style.

Because the same electrical die (emitters and detectors) are used for each channel of each device listed in this data sheet, absolute maximum ratings, recommended operating conditions, electrical specifications, and performance characteristics shown in the figures are identical for all parts. Occasional exceptions exist due to package variations and limitations, and are as noted. Additionally, the same package assembly processes and materials are used in all devices. These similarities give justification for the use of data obtained from one part to represent other parts' performance for reliability and certain limited radiation test results.

Selection Guide – Package Styles and Lead Configuration Options

| Package | 16-Pin DIP | 8-Pin DIP | 8-Pin DIP | 8-Pin DIP | 16-Pin Flat Pack | 20-Pad LCCC |
|-----------------------------------|-------------------------|-------------------------|-------------------------|-------------------------|-------------------------|--------------------------|
| Lead Style | Through Hole | Through Hole | Through Hole | Through Hole | Unformed Leads | Surface Mount |
| Channels | 2 | 1 | 2 | 2 | 4 | 2 |
| Common Channel Wiring | V _{CC} , GND | None | V _{CC} , GND | V _{CC} , GND | V _{CC} , GND | None |
| Withstand Test Voltage | 1500 Vdc | 1500 Vdc | 1500 Vdc | 2500 Vdc | 1500 Vdc | 1500 Vdc |
| Avago Part # & Options | | | | | | |
| Commercial | 6N134 | HCPL-5600 | HCPL-5630 | HCPL-5650 | HCPL-6650 | HCPL-6630 |
| MIL-PRF-38534, Class H | 6N134/883B | HCPL-5601 | HCPL-5631 | HCPL-5651 | HCPL-6651 | HCPL-6631 |
| MIL-PRF-38534, Class K | HCPL-268K | HCPL-560K | HCPL-563K | | HCPL-665K | HCPL-663K |
| Standard Lead Finish | Gold Plate ^a | Gold Plate ^a | Gold Plate ^a | Gold Plate ^a | Gold Plate ^a | Solder Pads ^b |
| Solder Dipped ^b | Option #200 | Option #200 | Option #200 | Option #200 | | |
| Butt Cut/Gold Plate ^a | Option #100 | Option #100 | Option #100 | | | |
| Gull Wing/Soldered ^b | Option #300 | Option #300 | Option #300 | | | |
| Class H SMD Part # | | | | | | |
| <i>Prescript for all below</i> | <i>None</i> | <i>5962-</i> | <i>None</i> | <i>None</i> | <i>None</i> | <i>None</i> |
| Gold Plate ^a | 8102801EC | 9085501HPC | 8102802PC | 8102805PC | 8102804FC | |
| Solder Dipped ^b | 8102801EA | 9085501HPA | 8102802PA | 8102805PA | | 81028032A |
| Butt Cut/Gold Plate ^a | 8102801UC | 9085501HYC | 8102802YC | | | |
| Butt Cut/Soldered ^b | 8102801UA | 9085501HYA | 8102802YA | | | |
| Gull Wing/Soldered ^b | 8102801TA | 9085501HXA | 8102802ZA | | | |
| Class K SMD Part # | | | | | | |
| <i>Prescript for all below</i> | <i>5962-</i> | <i>5962-</i> | <i>5962-</i> | | <i>5962-</i> | <i>5962-</i> |
| Gold Plate ^a | 9800101KEC | 9085501KPC | 9800102KPC | | 9800104KFC | |
| Solder Dipped ^b | 9800101KEA | 9085501KPA | 9800102KPA | | | 9800103K2A |
| Butt Cut/Gold Plate ^a | 9800101KUC | 9085501KYC | 9800102KYC | | | |
| Butt Cut/Soldered ^b | 9800101KUA | 9085501KYA | 9800102KYA | | | |
| Gull Wing/Soldered ^b | 9800101KTA | 9085501KXA | 9800102KZA | | | |

- a. Gold Plate lead finish: Maximum gold thickness of leads is <100 micro inches. Typical is 60 to 90 micro inches.
b. Solder lead finish: Sn63/Pb37.

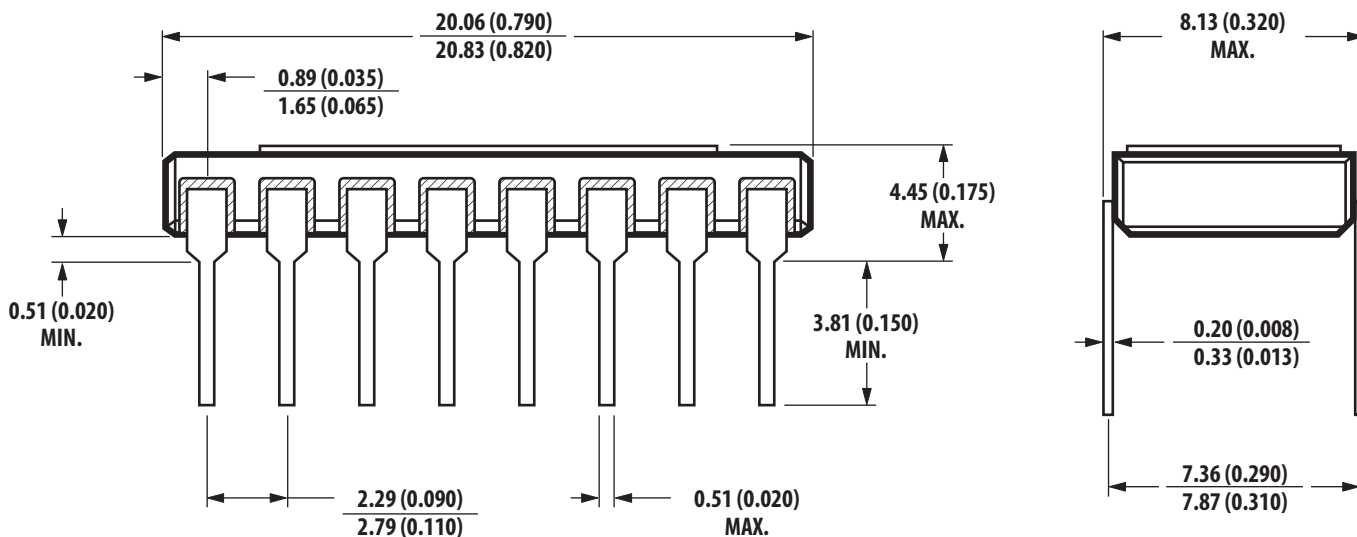
Functional Diagrams

| 16-Pin DIP | 8-Pin DIP | 8-Pin DIP | 16-Pin Flat Pack | 20-Pad LCCC |
|--------------|--------------|--------------|------------------|---------------|
| Through Hole | Through Hole | Through Hole | Unformed Leads | Surface Mount |
| 2 Channels | 1 Channel | 2 Channels | 4 Channels | 2 Channels |
| | | | | |

NOTE All DIP and flat pack devices have common V_{CC} and ground. Single channel DIP has an enable pin 7. LCCC (leadless ceramic chip carrier) package has isolated channels with separate V_{CC} and ground connections. All diagrams are "top view."

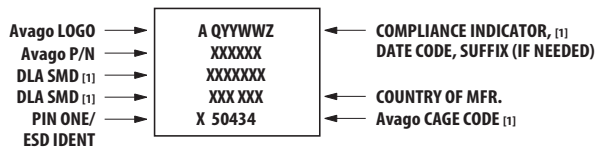
Outline Drawings

16-Pin DIP, Through Hole, 2 Channels



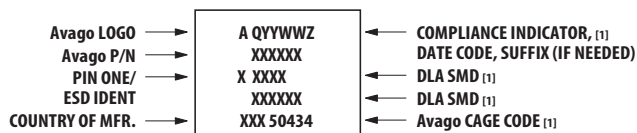
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

Leaded Device Marking (8- and 16-Pin DIPS, Flat Pack)



[1] QML PARTS ONLY

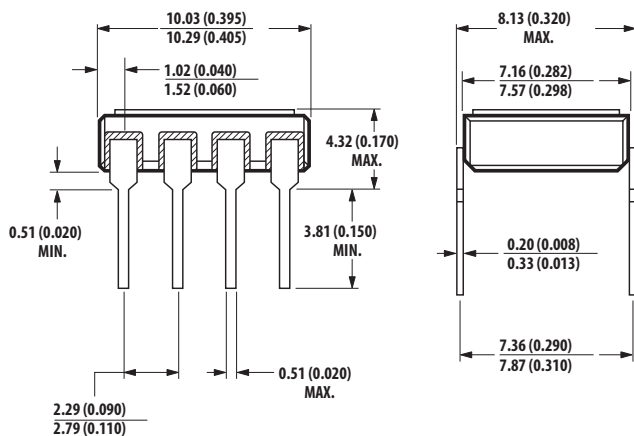
Leadless Device Marking (20 LCCC)



[1] QML PARTS ONLY

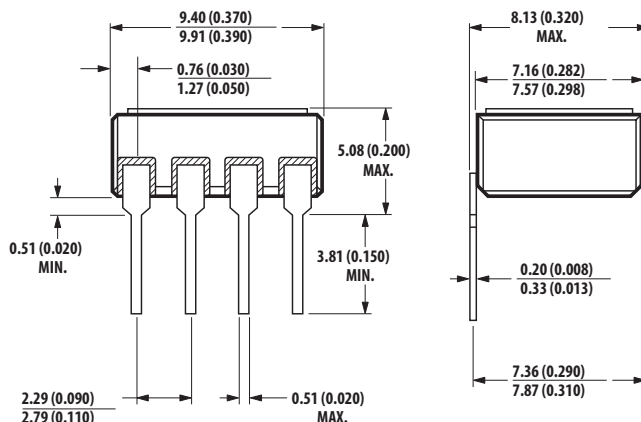
Outline Drawings (Continued)

8-Pin DIP, Through Hole, 1 and 2 Channels



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

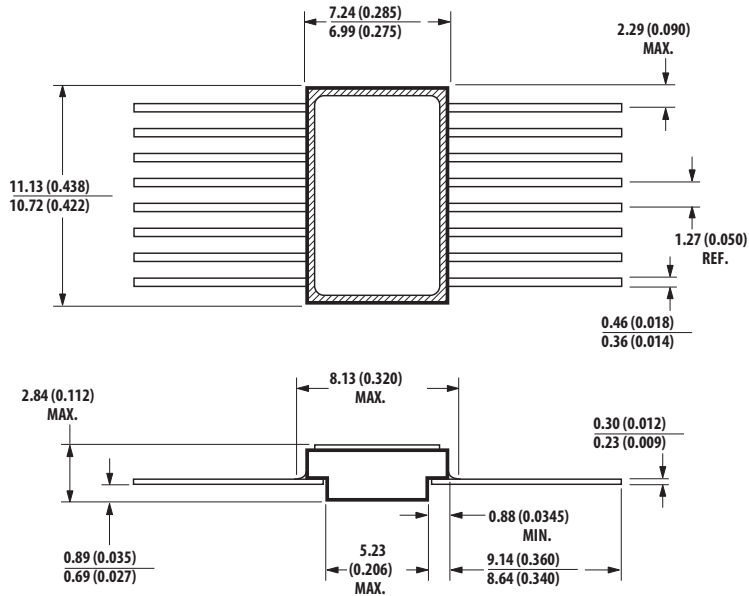
8-Pin DIP, Through Hole, 2 Channels, 2500 Vdc Withstand Test Voltage



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

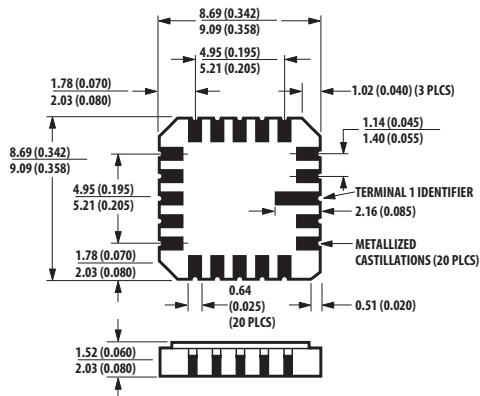
Outline Drawings (Continued)

16-Pin Flat Pack, 4 Channels



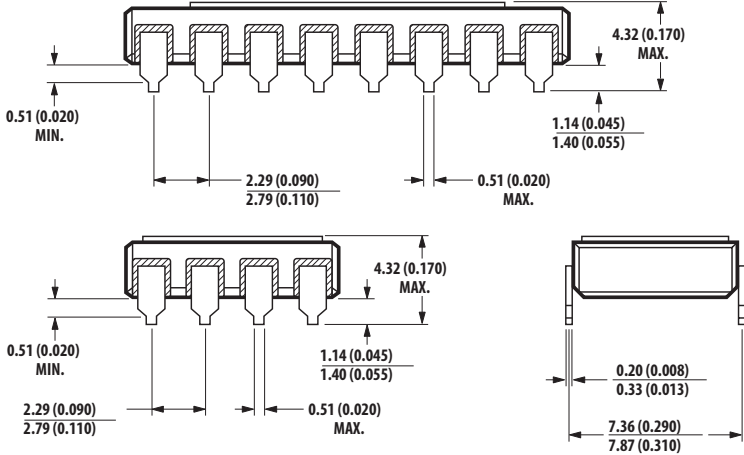
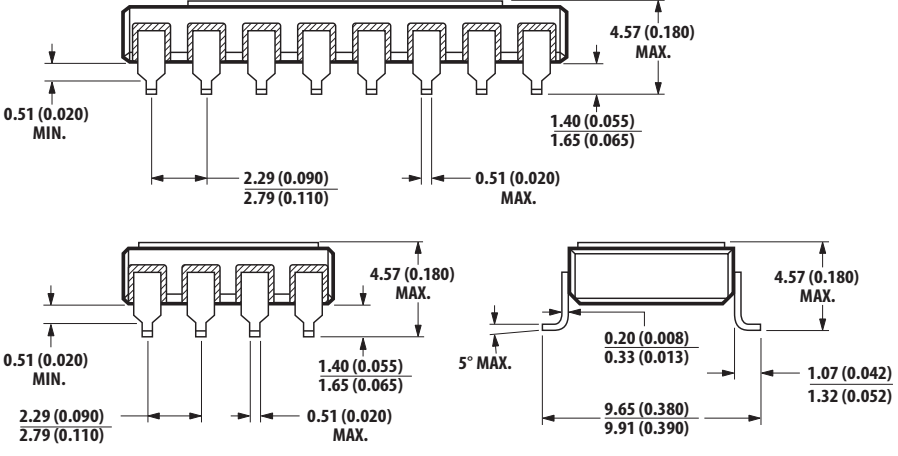
NOTE: DIMENSIONS IN MILLIMETERS (INCHES).

20-Terminal LCCC, Surface Mount, 2 Channels



NOTE: DIMENSIONS IN MILLIMETERS (INCHES).
 SOLDER THICKNESS 0.127 (0.005) MAX.

Hermetic Optocoupler Options

| Option | Description |
|--------|--|
| 100 | <p>Surface mountable hermetic optocoupler with leads trimmed for butt joint assembly. This option is available on Commercial, Class H and K products in 8- and 16-pin DIP (see the following drawings for details).</p>  <p style="text-align: center;">NOTE: DIMENSIONS IN MILLIMETERS (INCHES).</p> |
| 200 | <p>Lead finish is solder dipped rather than gold plated. This option is available on Commercial, Class H and K products in 8- and 16-pin DIP. DLA Drawing part numbers contain provisions for lead finish. All leadless chip carrier devices are delivered with solder dipped terminals as a standard feature.</p> |
| 300 | <p>Surface mountable hermetic optocoupler with leads cut and bent for gull wing assembly. This option is available on Commercial, Class H and K products in 8- and 16-pin DIP (see the following drawings for details). This option has solder dipped leads.</p>  <p style="text-align: center;">NOTE: DIMENSIONS IN MILLIMETERS (INCHES).</p> |

Absolute Maximum Ratings

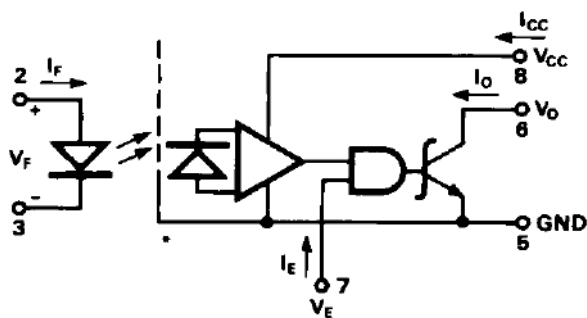
No derating required up to +125°C.

| Parameter | Symbol | Min. | Max. | Units |
|--|---------------|------|----------------|-------|
| Storage Temperature | T_S | -65 | +150 | °C |
| Operating Temperature | T_A | -55 | +125 | °C |
| Case Temperature | T_C | | +170 | °C |
| Junction Temperature | T_J | | +175 | °C |
| Lead Solder Temperature | | | 260 for 10 sec | °C |
| Peak Forward Input Current (each channel, 1 ms duration) | $I_{F(PEAK)}$ | | 40 | mA |
| Average Input Forward Current (each channel) | $I_{F(AVG)}$ | | 20 | mA |
| Input Power Dissipation (each channel) | | | 35 | mW |
| Reverse Input Voltage (each channel) | V_R | | 5 | V |
| Supply Voltage (1 minute maximum) | V_{CC} | | 7.0 | V |
| Output Current (each channel) | I_O | | 25 | mA |
| Output Voltage (each channel) | V_O | | 7 | V |
| Output Power Dissipation (each channel) | P_O | | 40 | mW |
| Package Power Dissipation (each channel) | P_D | | 200 | mW |

Single Channel Product Only

| Parameter | Symbol | Min. | Max. | Units |
|----------------------|--------|------|------|-------|
| Enable Input Voltage | V_E | | 5.5 | V |



8-Pin Ceramic DIP Single Channel Schematic



Note enable pin 7. An external 0.01 μ F to 0.1 μ F bypass capacitor must be connected between V_{CC} and ground for each package type.

ESD Classification

(MIL-STD-883, Method 3015)

| | |
|---|---|
| HCPL-5600/01/0K |  , Class 1 |
| 6N134, 6N134/883B, HCPL-5630/31/3K, HCPL-5650/51, HCPL-6630/31/3K and HCPL-6650/51/5K |  , Class 3 |

Recommended Operating Conditions

| Parameter | Symbol | Min. | Max. | Units |
|--|----------|------|------|---------|
| Input Current, Low Level, Each Channel | I_{FL} | 0 | 250 | μ A |
| Input Current, High Level, Each Channel ^a | I_{FH} | 10 | 20 | mA |
| Supply Voltage, Output | V_{CC} | 4.5 | 5.5 | V |
| Fan Out (TTL Load) Each Channel | N | | 6 | |

a. Meets or exceeds DLA SMD.

Single Channel Product Only (see Note)

| Parameter | Symbol | Min. | Max. | Units |
|---------------------------|----------|------|----------|-------|
| High Level Enable Voltage | V_{EH} | 2.0 | V_{CC} | V |
| Low Level Enable Voltage | V_{EL} | 0 | 0.8 | V |

NOTE No external pull up is required for a high logic state on the enable input.

Electrical Characteristics ($T_A = -55^\circ\text{C}$ to $+125^\circ\text{C}$, unless Otherwise Specified)

| Parameter | Symbol | Test Conditions | Group A ^a Subgroups | Limits | | | Units | Fig. | Note |
|---|----------------|---|-----------------------------------|--------|-------------------|------|------------------|---------|---------|
| | | | | Min. | Typ. ^b | Max. | | | |
| High Level Output Current | I_{OH} | $V_{CC} = 5.5\text{ V}, V_O = 5.5\text{ V}, I_F = 250\ \mu\text{A}$ | 1, 2, 3 | | 20 | 250 | μA | 1 | c |
| Low Level Output Voltage | V_{OL} | $V_{CC} = 5.5\text{ V}, I_F = 10\text{ mA}, I_{OL} (\text{Sinking}) = 10\text{ mA}$ | 1, 2, 3 | | 0.3 | 0.6 | V | 2 | c, d |
| Current Transfer Ratio | h_F CTR | $V_O = 0.6\text{ V}, I_F = 10\text{ mA}, V_{CC} = 5.5\text{ V}$ | 1, 2, 3 | 100 | | | % | | c |
| Logic High Supply Current | Single Channel | $V_{CC} = 5.5\text{ V}, I_F = 0\text{ mA}$ | 1, 2, 3 | | 9 | 14 | mA | | c |
| | Dual Channel | | | | 18 | 28 | mA | | e |
| | Quad Channel | | | | 25 | 42 | mA | | |
| Logic Low Supply Current | Single Channel | $V_{CC} = 5.5\text{ V}, I_F = 20\text{ mA}$ | 1, 2, 3 | | 13 | 18 | mA | | c |
| | Dual Channel | | | | 26 | 36 | mA | | e |
| | Quad Channel | | | | 33 | 50 | mA | | |
| Input Forward Voltage | V_F | $I_F = 20\text{ mA}$ | 1, 2, 3 | | 1.5 | 1.9 | V | 3 | c, f |
| | | | 1, 2 | | 1.55 | 1.75 | V | 3 | c, g |
| | | | 3 | | | 1.85 | | | |
| Input Reverse Breakdown Voltage | BV_R | $I_R = 10\ \mu\text{A}$ | 1, 2, 3 | 5 | | | V | | c |
| Input-Output Leakage Current | I_{I-O} | $R_H \leq 65\%, T_A = 25^\circ\text{C}, t = 5\text{ s}$ | $V_{I-O} = 1500\text{ Vdc}$ | 1 | | 1.0 | μA | | h, i, j |
| | | | $V_{I-O} = 2500\text{ Vdc}$ | 1 | | 1.0 | μA | | k |
| Capacitance Between Input/Output | C_{I-O} | $f = 1\text{ MHz}, T_C = 25^\circ\text{C}$ | 4 | | 1.0 | 4.0 | pF | | c, l, m |
| Propagation Delay Time to High Output Level | t_{PLH} | $V_{CC} = 5\text{ V}, R_L = 510\ \Omega, C_L = 50\text{ pF}, I_F = 13\text{ mA}$ | 9 | | 60 | 100 | ns | 4, 5, 6 | c, n |
| | | | 10, 11 | | | 140 | | | |
| Propagation Delay Time to Low Output Level | t_{PHL} | | 9 | | 55 | 100 | ns | | |
| | | | 10, 11 | | | 120 | | | |
| Output Rise Time | t_{LH} | $R_L = 510\ \Omega, C_L = 50\text{ pF}, I_F = 13\text{ mA}$ | 9, 10, 11 | | 35 | 90 | ns | | c |
| Output Fall Time | t_{HL} | | | | 35 | 40 | | | |
| Common Mode Transient Immunity at High Output Level | $ CM_H $ | $V_{CM} = 50\text{ V (PEAK)}, V_{CC} = 5\text{ V}, V_O (\text{min.}) = 2\text{ V}, R_L = 510\ \Omega, I_F = 0\text{ mA}$ | 9, 10, 11 | 1000 | >10000 | | V/ μs | 7 | c, m, o |
| Common Mode Transient Immunity at Low Output Level | $ CM_L $ | $V_{CM} = 50\text{ V (PEAK)}, V_{CC} = 5\text{ V}, V_O (\text{max.}) = 0.8\text{ V}, R_L = 510\ \Omega, I_F = 10\text{ mA}$ | 9, 10, 11 | 1000 | >10000 | | V/ μs | 7 | c, m, o |

- a. Commercial parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and 883B parts receive 100% testing at 25, 125, and 55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
- b. All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.
- c. Each channel.
- d. It is essential that a bypass capacitor (0.01 to 0.1 μF ceramic) be connected from V_{CC} to ground. Total lead length between both ends of this external capacitor and the isolator connections should not exceed 20 mm.
- e. The HCPL-6630, HCPL-6631, and HCPL-663K dual channel parts function as two independent single channel units. Use the single channel parameter limits for each channel.
- f. Not required for 6N134, 6N134/883B, 8102801, HCPL-268K, and 5962-9800101 types.
- g. Required for 6N134, 6N134/883B, 8102801, HCPL-268K, and 5962-9800101 types.
- h. All devices are considered two-terminal devices; I_{LO} is measured between all input leads or terminals shorted together and all output leads or terminals shorted together.
- i. This is a momentary withstand test, not an operating condition.
- j. Not required for HCPL-5650, HCPL-5651, and 8102805 types.
- k. Required for HCPL-5650, HCPL-5651, and 8102805 types only.
- l. Measured between each input pair shorted together and all output connections for that channel shorted together.
- m. Parameters are tested as part of device initial characterization and after design and process changes. Parameters are guaranteed to limits specified for all lots not specifically tested.
- n. t_{PHL} propagation delay is measured from the 50% point on the leading edge of the input pulse to the 1.5 V point on the leading edge of the output pulse. The t_{PLH} propagation delay is measured from the 50% point on the trailing edge of the input pulse to the 1.5 V point on the trailing edge of the output pulse.
- o. CM_L is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic low state ($V_O < 0.8\text{ V}$). CM_H is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic high state ($V_O > 2.0\text{ V}$).

Single Channel Product Only

| Parameter | Symbol | Test Conditions | Group A ^a Subgroups | Limits | | | Units | Fig. | Note |
|---------------------------|----------|---|-----------------------------------|--------|-------------------|------|-------|------|--------------|
| | | | | Min. | Typ. ^b | Max. | | | |
| Low Level Enable Current | I_{EL} | $V_{CC} = 5.5\text{ V}$, $V_E = 0.5\text{ V}$ | 1, 2, 3 | -2.0 | -1.45 | | mA | | |
| High Level Enable Voltage | V_{EH} | | 1, 2, 3 | 2.0 | | | V | | ^c |
| Low Level Enable Voltage | V_{EL} | | 1, 2, 3 | | | 0.8 | V | | |

- a. Standard parts receive 100% testing at 25°C (Subgroups 1 and 9). SMD and 883B parts receive 100% testing at 25, 125, and 55°C (Subgroups 1 and 9, 2 and 10, 3 and 11, respectively).
- b. All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$.
- c. No external pull up is required for a high logic state on the enable input.

Typical Characteristics, $T_A = 25^\circ\text{C}$, $V_{CC} = 5\text{ V}$

| Parameter | Sym. | Typ. | Units | Test Conditions | Fig. | Note |
|-------------------------------------|---------------------------|-----------|----------------------|---|------|------|
| Input Capacitance | C_{IN} | 60 | pF | $V_F = 0\text{ V}$, $f = 1\text{ MHz}$ | | a |
| Input Diode Temperature Coefficient | $\Delta V_F / \Delta T_A$ | -1.5 | mV/ $^\circ\text{C}$ | $I_F = 20\text{ mA}$ | | a |
| Resistance (Input-Output) | R_{I-O} | 10^{12} | Ω | $V_{I-O} = 500\text{ V}$ | | b |

- Each channel.
- All devices are considered two-terminal devices; I_{I-O} is measured between all input leads or terminals shorted together and all output leads or terminals shorted together.

Single Channel Product Only

| Parameter | Sym. | Typ. | Units | Test Conditions | Fig. | Note |
|--|-----------|------|-------|--|------|------|
| Propagation Delay Time of Enable from V_{EH} to V_{EL} | t_{ELH} | 35 | ns | $R_L = 510\ \Omega$, $C_L = 50\text{ pF}$, $I_F = 13\text{ mA}$, $V_{EH} = 3\text{ V}$, $V_{EL} = 0\text{ V}$ | 8, 9 | a, b |
| Propagation Delay Time of Enable from V_{EL} to V_{EH} | t_{EHL} | 35 | ns | | | a, c |

- Each channel.
- The t_{ELH} enable propagation delay is measured from the 1.5 V point on the trailing edge of the enable input pulse to the 1.5V point on the trailing edge of the output pulse.
- The t_{EHL} enable propagation delay is measured from the 1.5 V point on the leading edge of the enable input pulse to the 1.5V point on the leading edge of the output pulse.

Dual and Quad Channel Product Only

| Parameter | Sym. | Typ. | Units | Test Conditions | Fig. | Note |
|-----------------------------|-----------|-----------|----------|--|------|------|
| Input-Input Leakage Current | I_{I-I} | 0.5 | nA | Relative Humidity $\leq 65\%$ $V_{I-I} = 500\text{ V}$, $t = 5\text{ s}$ | | a |
| Resistance (Input-Input) | R_{I-I} | 10^{12} | Ω | $V_{I-I} = 500\text{ V}$ | | a |
| Capacitance (Input-Input) | C_{I-I} | 0.55 | pF | $f = 1\text{ MHz}$ | | a |

- Measured between adjacent input pairs shorted together for each multichannel device.

Figure 1 High Level Output Current vs. Temperature

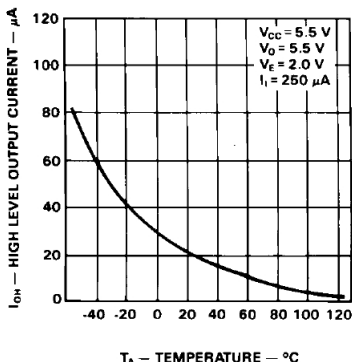


Figure 2 Input-Output Characteristics

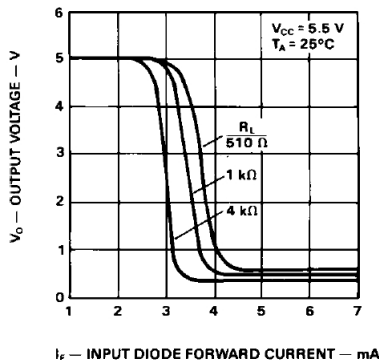


Figure 3 Input Diode Forward Characteristics

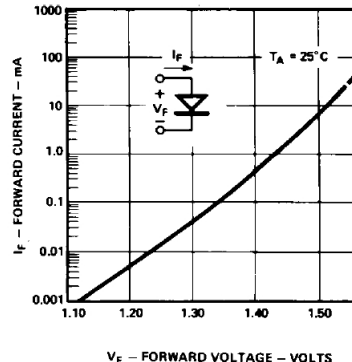


Figure 4 Test Circuit for t_{PHL} and t_{PLH}

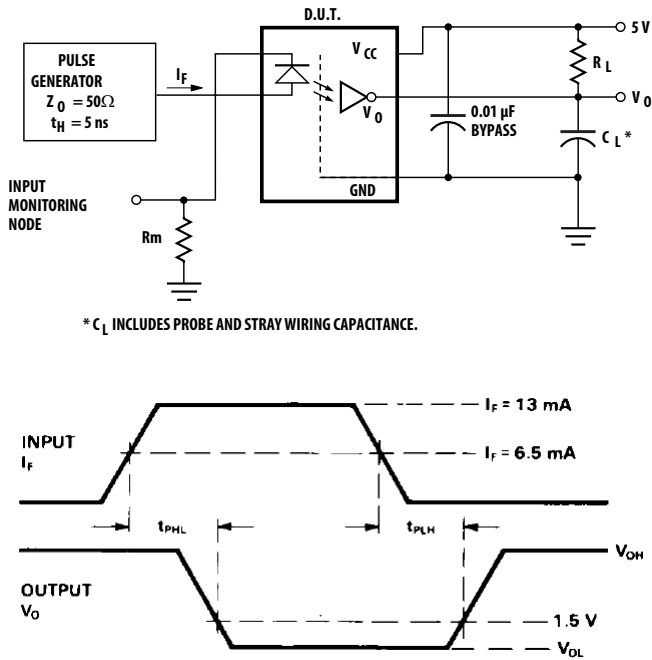


Figure 5 Propagation Delay, t_{PHL} and t_{PLH} vs. Pulse Input Current, I_{FH}

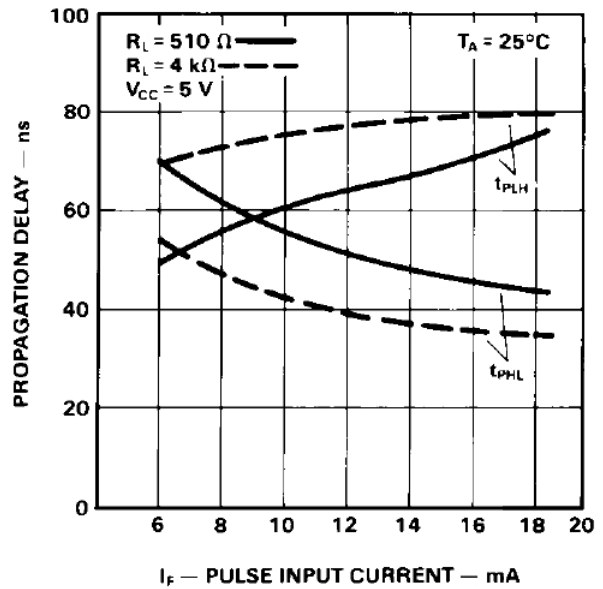


Figure 6 Propagation Delay vs. Temperature

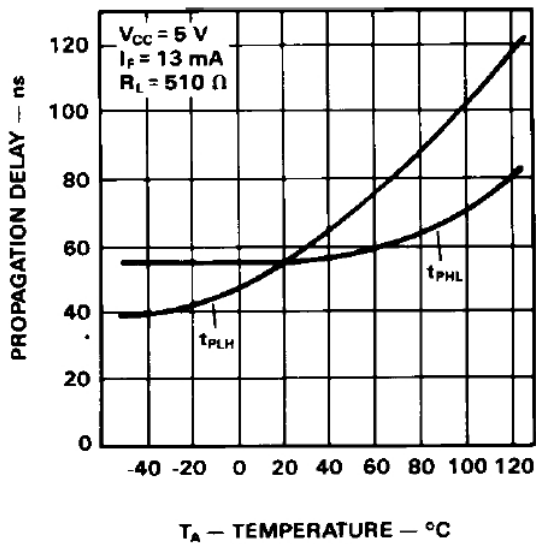


Figure 7 Test Circuit for Common Mode Transient Immunity and Typical Waveforms

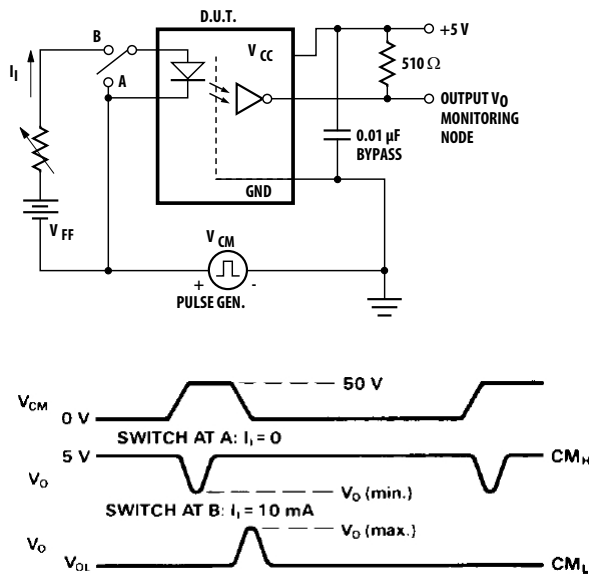


Figure 8 Test Circuit for t_{EHL} and t_{ELH}

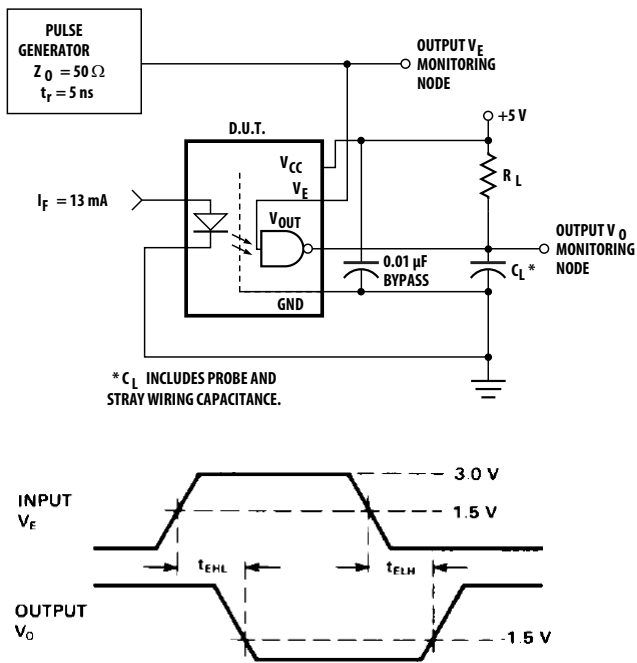


Figure 9 Enable Propagation Delay vs. Temperature

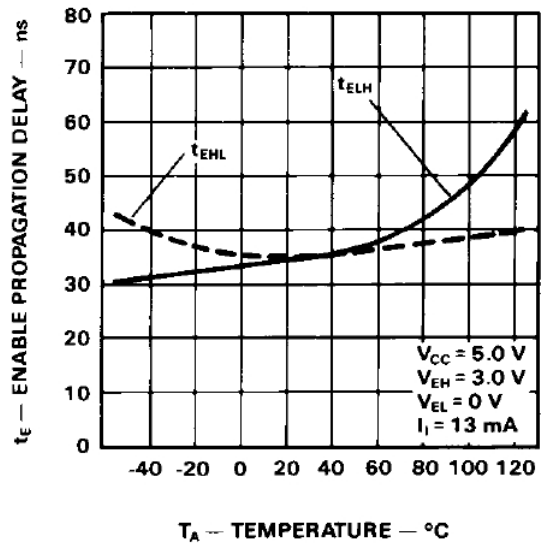


Figure 10 Operating Circuit for Burn-In and Steady State Life Tests

