

8-Pin DIP High Speed Transistor Optocouplers

Single-Channel: 6N135M, 6N136M, HCPL4503M Dual-Channel: HCPL2530M, HCPL2531M

Description

The 6N135M, 6N136M, HCPL4503M, HCPL2530M, and HCPL2531M optocouplers consist of an AlGaAs LED optically coupled to a high speed photodetector transistor for each channel.

A separate connection for the bias of the photodiode improves the speed by several orders of magnitude over conventional phototransistor optocouplers by reducing the base-collector capacitance of the input transistor.

The HCPL4503M has no internal connection to the phototransistor base for improved noise immunity. An internal noise shield provides superior common mode rejection of up to 50,000 V/μs.

Features

- High Speed – 1 MBit/s
- Dual-Channel: HCPL2530M, HCPL2531M
- CTR Guaranteed 0°C to 70°C
- No Base Connection for Improved Noise Immunity (HCPL4503M)
- Superior CMR of 15,000 V/μs Minimum (HCPL4503M)
- Safety and Regulatory Approvals
 - ♦ UL1577, 5,000 VAC_{RMS} for 1 Minute
 - ♦ DIN EN/IEC60747-5-5
- These are Pb-Free Devices

Applications

- Line Receivers
- Pulse Transformer Replacement
- Output Interface to CMOS-LSTTL-TTL
- Wide-Bandwidth Analog Coupling

Related Resources

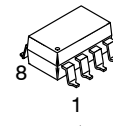
- <https://www.onsemi.com/products/interfaces/high-performance-optocouplers>
- <https://www.onsemi.com/products/interfaces/high-performance-optocouplers/high-performance-transistor-optocouplers/hcpl0500>
- <https://www.onsemi.com/products/interfaces/high-performance-optocouplers/high-performance-transistor-optocouplers/fodm452>
- <https://www.onsemi.com/products/interfaces/high-performance-optocouplers/low-voltage-high-performance-optocouplers/fod0501>



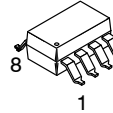
PDIP8 6.6x3.81, 2.54P
CASE 646BW



PDIP8 9.655x6.61, 2.54P
CASE 646CQ

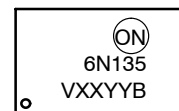


PDIP8 GW
CASE 709AC



PDIP8 GW
CASE 709AD

MARKING DIAGRAM



- 6N135 = Device Number
- V = DIN EN/IEC60747-5-5 Option (only appears on component ordered with this option)
- XX = Two Digit Year Code, e.g., '15'
- YY = Two Digit Work Week Ranging from '01' to '53'
- B = Assembly Package Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 11 of this data sheet.

Single-Channel: 6N135M, 6N136M, HCPL4503M Dual-Channel: HCPL2530M, HCPL2531M

SCHEMATICS

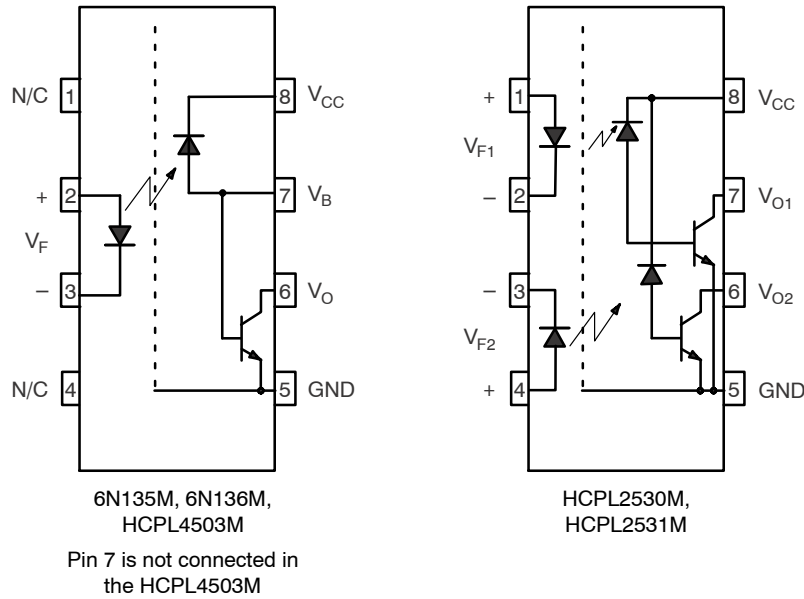


Figure 1. Schematics

SAFETY AND INSULATION RATINGS (As per DIN EN/IEC 60747-5-5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.)

Parameter		Characteristics
Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	<150 V _{RMS}	I-IV
	<300 V _{RMS}	I-IV
	<450 V _{RMS}	I-III
	<600 V _{RMS}	I-III
Climatic Classification		40/100/21
Pollution Degree (DIN VDE 0110/1.89)		2
Comparative Tracking Index		175

Symbol	Parameter	Value	Unit
V _{PR}	Input-to-Output Test Voltage, Method A, V _{IORM} × 1.6 = V _{PR} , Type and Sample Test with t _m = 10 s, Partial Discharge < 5 pC	1,335	V _{peak}
	Input-to-Output Test Voltage, Method B, V _{IORM} × 1.875 = V _{PR} , 100% Production Test with t _m = 1 s, Partial Discharge < 5 pC	1,669	V _{peak}
V _{IORM}	Maximum Working Insulation Voltage	890	V _{peak}
V _{IOTM}	Highest Allowable Over-Voltage	6,000	V _{peak}
	External Creepage	≥8.0	mm
	External Clearance	≥7.4	mm
	External Clearance (for Option TV, 0.4" Lead Spacing)	≥10.16	mm
DTI	Distance Through Insulation (Insulation Thickness)	≥0.5	mm
T _S	Case Temperature (Note 1)	150	°C
I _{S,INPUT}	Input Current (Note 1)	200	mA
P _{S,OUTPUT}	Output Power (Duty Factor ≤ 2.7%) (Note 1)	300	mW
R _{IO}	Insulation Resistance at T _S , V _{IO} = 500 V (Note 1)	>10 ⁹	Ω

1. Safety limit value – maximum values allowed in the event of a failure.

**Single-Channel: 6N135M, 6N136M, HCPL4503M Dual-Channel: HCPL2530M,
HCPL2531M**

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Value	Unit
T_{STG}	Storage Temperature		-40 to +125	$^\circ\text{C}$
T_{OPR}	Operating Temperature		-40 to +100	$^\circ\text{C}$
T_J	Junction Temperature		-40 to +125	$^\circ\text{C}$
T_{SOL}	Lead Solder Temperature		260 for 10 s	$^\circ\text{C}$

EMITTER

I_F (avg)	DC/Average Forward Input Current Each Channel (Note 2)		25	mA
I_F (pk)	Peak Forward Input Current Each Channel (Note 3)	50% Duty Cycle, 1 ms P.W.	50	mA
I_F (trans)	Peak Transient Input Current Each Channel	$\leq 1 \mu\text{s}$ P.W., 300 pps	1.0	A
V_R	Reverse Input Voltage Each Channel		5	V
P_D	Input Power Dissipation Each Channel (Note 4)		45	mW

DETECTOR

I_O (avg)	Average Output Current Each Channel		8	mA
I_O (pk)	Peak Output Current Each Channel		16	mA
V_{EBR}	Emitter-Base Reverse Voltage	6N135M and 6N136M	5	V
V_{CC}	Supply Voltage		-0.5 to 30	V
V_O	Output Voltage		-0.5 to 20	V
I_B	Base Current	6N135M and 6N136M	5	mA
P_D	Output Power Dissipation Each Channel (Note 5)		100	mW

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. Derate linearly above 70°C free-air temperature at a rate of $0.8 \text{ mA}/^\circ\text{C}$.
3. Derate linearly above 70°C free-air temperature at a rate of $1.6 \text{ mA}/^\circ\text{C}$.
4. Derate linearly above 70°C free-air temperature at a rate of $0.9 \text{ mW}/^\circ\text{C}$.
5. Derate linearly above 70°C free-air temperature at a rate of $2.0 \text{ mW}/^\circ\text{C}$.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	20.0	V
T_A	Ambient Operating Temperature	0	70	$^\circ\text{C}$
I_{FL}	Input Current, Low Level	0	250	μA
I_{FH}	Input Current, High Level (Note 6)	6.3	20.0	mA

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

6. 6.3 mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0 mA or less.

Single-Channel: 6N135M, 6N136M, HCPL4503M Dual-Channel: HCPL2530M, HCPL2531M

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Device	Test Conditions	Min	Typ	Max	Unit
--------	-----------	--------	-----------------	-----	-----	-----	------

INDIVIDUAL COMPONENT CHARACTERISTICS ($V_{CC} = 5.0\text{ V}$, $T_A = 0^\circ\text{C}$ to 70°C unless otherwise specified.)

EMITTER							
V_F	Input Forward Voltage	All	$I_F = 16\text{ mA}$, $T_A = 25^\circ\text{C}$	-	1.45	1.70	V
		All	$I_F = 16\text{ mA}$	-	-	1.80	
B_{VR}	Input Reverse Breakdown Voltage	All	$I_R = 10\ \mu\text{A}$	5	21	-	V
$\Delta V_F/\Delta T_A$	Temperature Coefficient of Forward Voltage	All	$I_F = 16\text{ mA}$	-	-1.7	-	mV/ $^\circ\text{C}$

DETECTOR							
I_{OH}	Logic High Output Current	All	$I_F = 0\text{ mA}$, $V_O = V_{CC} = 5.5\text{ V}$, $T_A = 25^\circ\text{C}$	-	0.0007	0.5	μA
		6N135M, 6N136M, HCPL4503M	$I_F = 0\text{ mA}$, $V_O = V_{CC} = 15\text{ V}$, $T_A = 25^\circ\text{C}$	-	0.0019	1	
		All	$I_F = 0\text{ mA}$, $V_O = V_{CC} = 15\text{ V}$	-	-	50	
I_{CCL}	Logic Low Supply Current	6N135M, 6N136M, HCPL4503M	$I_F = 16\text{ mA}$, $V_O = \text{Open}$, $V_{CC} = 15\text{ V}$	-	163	200	μA
		HCPL2530M, HCPL2531M	$I_{F1} = I_{F2} = 16\text{ mA}$, $V_O = \text{Open}$, $V_{CC} = 15\text{ V}$	-	-	400	
I_{CCH}	Logic High Supply Current	6N135M, 6N136M, HCPL4503M	$I_F = 0\text{ mA}$, $V_O = \text{Open}$, $V_{CC} = 15\text{ V}$	-	0.0004	2	μA
		HCPL2530M, HCPL2531M	$I_F = 0\text{ mA}$, $V_O = \text{Open}$, $V_{CC} = 15\text{ V}$	-	-	4	

TRANSFER CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C unless otherwise specified.)

COUPLED								
CTR	Current Transfer Ratio (Note 7)	6N135M, HCPL2530M	$I_F = 16\text{ mA}$, $V_O = 0.4\text{ V}$, $V_{CC} = 4.5\text{ V}$, $T_A = 25^\circ\text{C}$	7	38	50	%	
		6N136M, HCPL4503M, HCPL2531M		19	38	50	%	
		6N135M	$I_F = 16\text{ mA}$, $V_{CC} = 4.5\text{ V}$	$V_{OL} = 0.4\text{ V}$	5	-	-	%
		HCPL2530M		$V_{OL} = 0.5\text{ V}$				
		6N136M, HCPL4503M		$V_{OL} = 0.4\text{ V}$	15	-	-	%
		HCPL2531M		$V_{OL} = 0.5\text{ V}$				
V_{OL}	Logic LOW Output Voltage	6N135M	$I_F = 16\text{ mA}$, $I_O = 1.1\text{ mA}$, $V_{CC} = 4.5\text{ V}$, $T_A = 25^\circ\text{C}$	-	0.12	0.4	V	
		HCPL2530M				0.5		
		6N136M, HCPL4503M	$I_F = 16\text{ mA}$, $I_O = 3\text{ mA}$, $V_{CC} = 4.5\text{ V}$, $T_A = 25^\circ\text{C}$	-	0.20	0.4		
		HCPL2531M				0.5		
		6N135M, HCPL2530M	$I_F = 16\text{ mA}$, $I_O = 0.8\text{ mA}$, $V_{CC} = 4.5\text{ V}$	-	0.11	0.5		
		HCPL4503M, HCPL2531M	$I_F = 16\text{ mA}$, $I_O = 2.4\text{ mA}$, $V_{CC} = 4.5\text{ V}$	-	0.18	0.5		

Single-Channel: 6N135M, 6N136M, HCPL4503M Dual-Channel: HCPL2530M, HCPL2531M

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Device	Test Conditions	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS ($T_A = 0^\circ\text{C}$ to 70°C unless otherwise specified.)							
t_{pHL}	Propagation Delay Time to Logic LOW	6N135M	$T_A = 25^\circ\text{C}$, $R_L = 4.1\text{ k}\Omega$, $I_F = 16\text{ mA}$ (Note 8) (Figure 14)	-	0.23	1.5	μs
		HCPL2530M			0.25		
		6N136M, HCPL4503M	$T_A = 25^\circ\text{C}$, $R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$ (Note 9) (Figure 14)	-	0.25	0.8	μs
		HCPL2531M			0.28		
		6N135M, HCPL2530M	$R_L = 4.1\text{ k}\Omega$, $I_F = 16\text{ mA}$ (Note 8) (Figure 14)	-	-	2.0	μs
		6N136M, HCPL4503M, HCPL2531M	$R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$ (Note 9) (Figure 14)	-	-	1.0	μs
t_{pLH}	Propagation Delay Time to Logic HIGH	6N135M	$T_A = 25^\circ\text{C}$, $R_L = 4.1\text{ k}\Omega$, $I_F = 16\text{ mA}$ (Note 8) (Figure 14)	-	0.45	1.5	μs
		HCPL2530M			0.29		
		6N136M, HCPL4503M	$T_A = 25^\circ\text{C}$, $R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$ (Note 9) (Figure 14)	-	0.26	0.8	μs
		HCPL2531M			0.18		
		6N135M, HCPL2530M	$R_L = 4.1\text{ k}\Omega$, $I_F = 16\text{ mA}$ (Note 8) (Figure 14)	-	-	2.0	μs
		6N136M, HCPL4503M, HCPL2531M	$R_L = 1.9\text{ k}\Omega$, $I_F = 16\text{ mA}$ (Note 9) (Figure 14)	-	-	1.0	μs
CM_H	Common Mode Transient Immunity at Logic High	6N135M, HCPL2530M	$I_F = 0\text{ mA}$, $V_{CM} = 10\text{ V}_{P-P}$, $R_L = 4.1\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ (Note 10) (Figure 15)	-	10,000	-	$\text{V}/\mu\text{s}$
		6N136M, HCPL2531M	$I_F = 0\text{ mA}$, $V_{CM} = 10\text{ V}_{P-P}$, $R_L = 1.9\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ (Note 10) (Figure 15)	-	10,000	-	
		HCPL4503M	$I_F = 0\text{ mA}$, $V_{CM} = 1,500\text{ V}_{P-P}$, $R_L = 4.1\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ (Note 10) (Figure 15)	15,000	50,000	-	
CM_L	Common Mode Transient Immunity at Logic Low	6N135M, HCPL2530M	$I_F = 16\text{ mA}$, $V_{CM} = 10\text{ V}_{P-P}$, $R_L = 4.1\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ (Note 10) (Figure 16)	-	10,000	-	$\text{V}/\mu\text{s}$
		6N136M, HCPL2531M	$I_F = 16\text{ mA}$, $V_{CM} = 10\text{ V}_{P-P}$, $R_L = 1.9\text{ k}\Omega$ (Note 10) (Figure 15)	-	10,000	-	
		HCPL4503M	$I_F = 16\text{ mA}$, $V_{CM} = 1,500\text{ V}_{P-P}$, $R_L = 4.1\text{ k}\Omega$, $T_A = 25^\circ\text{C}$ (Note 10) (Figure 15)	15,000	50,000	-	

**Single-Channel: 6N135M, 6N136M, HCPL4503M Dual-Channel: HCPL2530M,
HCPL2531M**

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Device	Test Conditions	Min	Typ	Max	Unit
ISOLATION CHARACTERISTICS ($T_A = 25^\circ\text{C}$, unless otherwise noted.)							
V_{ISO}	Withstand Isolation Test Voltage	All	$RH \leq 50\%$, $I_{I-O} \leq 10 \mu\text{A}$ $t = 1$ minute, $f = 50$ Hz (Note 11) (Note 13)	5,000	–	–	V_{ACRMS}
R_{I-O}	Resistance (Input to Output)	All	$V_{I-O} = 500 V_{DC}$ (Note 11)	–	10^{11}	–	Ω
C_{I-O}	Capacitance (Input to Output)	All	$f = 1$ MHz, $V_{I-O} = 0 V_{DC}$ (Note 11)	–	1	–	pF
I_{I-I}	Input-Input Insulation Leakage Current	HCPL2530M, HCPL2531M	$RH \leq 45\%$, $V_{I-I} = 500 V_{DC}$, $t = 5$ s (Note 12)	–	<1	–	nA
R_{I-I}	Input-Input Resistance	HCPL2530M, HCPL2531M	$V_{I-I} = 500 V_{DC}$ (Note 12)	–	10^{12}	–	Ω
C_{I-I}	Input-Input Capacitance	HCPL2530M, HCPL2531M	$f = 1$ MHz (Note 12)	–	0.2	–	pF

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. Current Transfer Ratio is defined as a ratio of output collector current, I_O , to the forward LED input current, I_F , times 100%.

8. The 4.1 k Ω load represents 1 LSTTL unit load of 0.36 mA and 6.1 k Ω pull-up resistor.

9. The 1.9 k Ω load represents 1 TTL unit load of 1.6 mA and 5.6 k Ω pull-up resistor.

10. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic high state (i.e., $V_O > 2.0$ V).

Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM} , to assure that the output will remain in a logic low state (i.e., $V_O < 0.8$ V).

11. Device is considered a two terminal device: pins 1, 2, 3 and 4 are shorted together and pins 5, 6, 7 and 8 are shorted together.

12. Measured between pins 1 and 2 shorted together, and pins 3 and 4 shorted together.

13. 5000 V_{RMS} for 1 minute duration is equivalent to 6000 V_{RMS} for 1 second duration.

Single-Channel: 6N135M, 6N136M, HCPL4503M Dual-Channel: HCPL2530M, HCPL2531M

TYPICAL PERFORMANCE CURVES

(For single-channel devices; 6N135M, 6N136M, and HCPL4503M.)



Figure 2. Normalized CTR vs. Forward Current

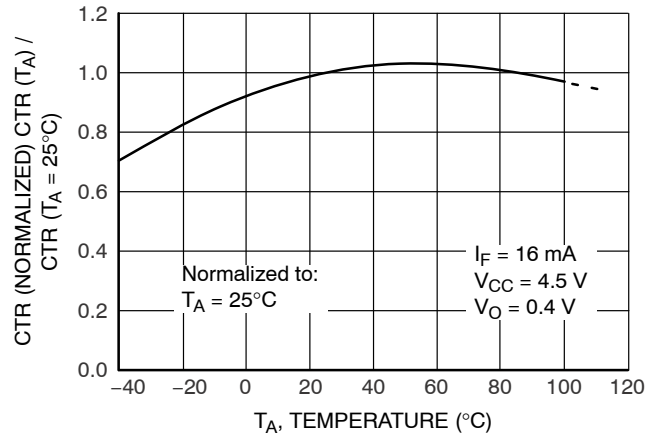


Figure 3. Normalized CTR vs. Temperature

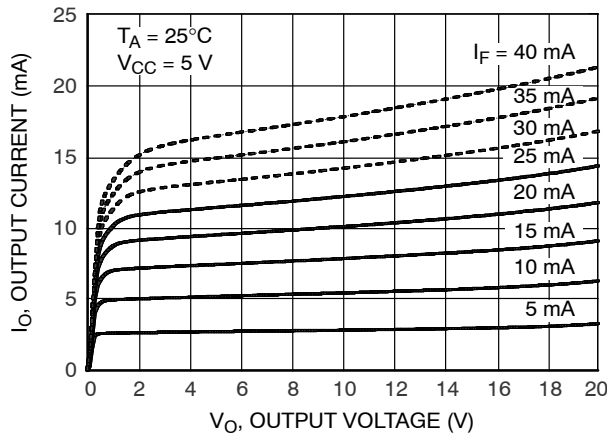


Figure 4. Output Current vs. Output Voltage

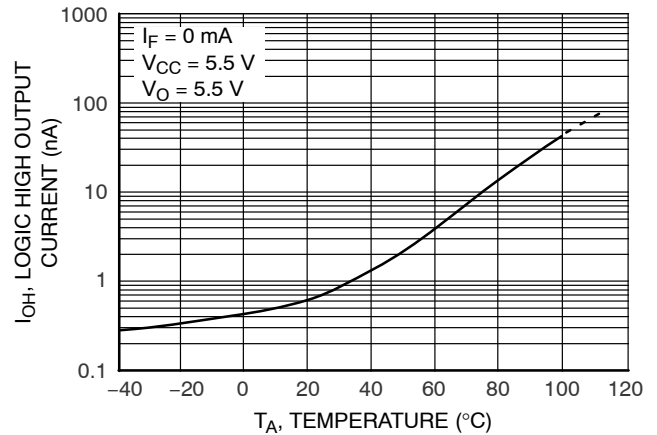


Figure 5. Logic High Output Current vs. Temperature



Figure 6. Propagation Delay vs. Temperature

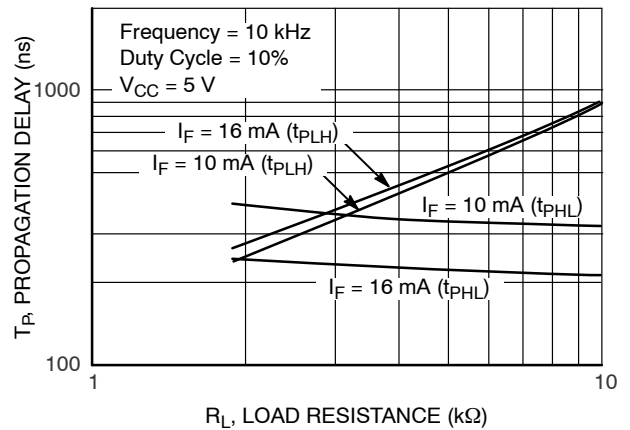


Figure 7. Propagation Delay vs. Load Resistance

Single-Channel: 6N135M, 6N136M, HCPL4503M Dual-Channel: HCPL2530M, HCPL2531M

TYPICAL PERFORMANCE CURVES

(For dual-channel devices; HCPL2530M and HCPL2531M.)

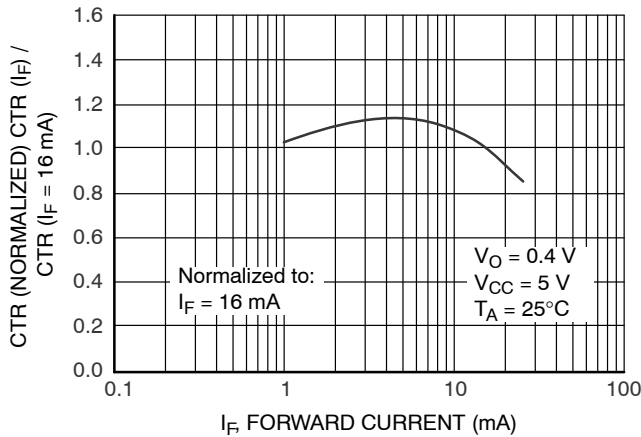


Figure 8. Normalized CTR vs. Forward Current

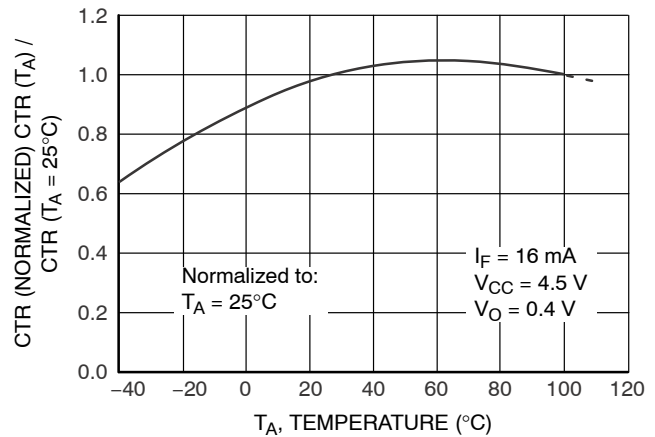


Figure 9. Normalized CTR vs. Temperature

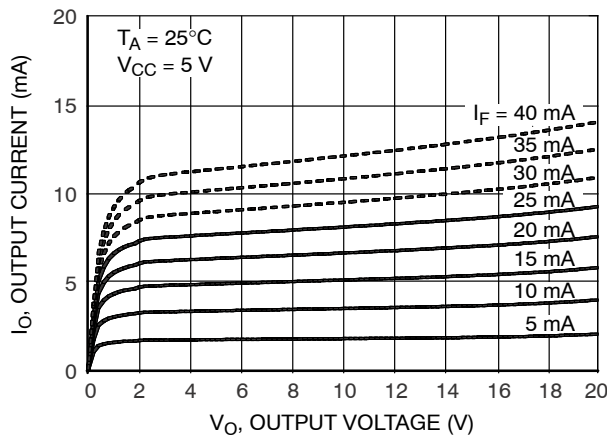


Figure 10. Output Current vs. Output Voltage

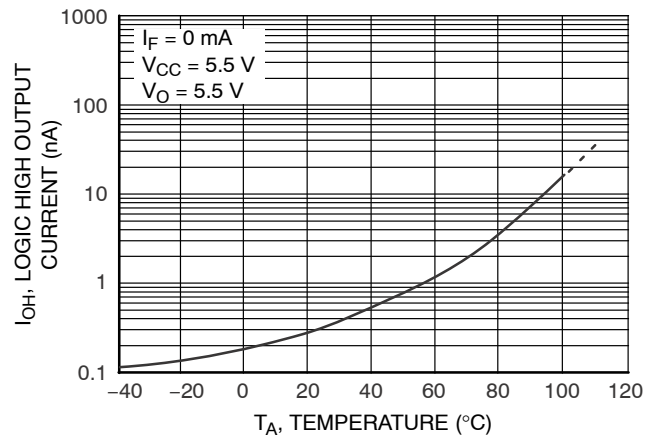


Figure 11. Logic High Output Current vs. Temperature

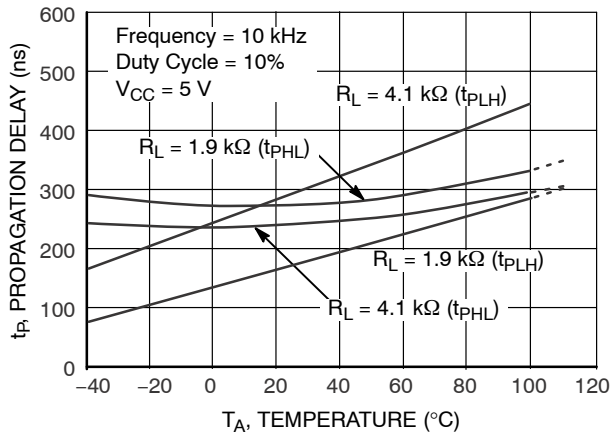


Figure 12. Propagation Delay vs. Temperature

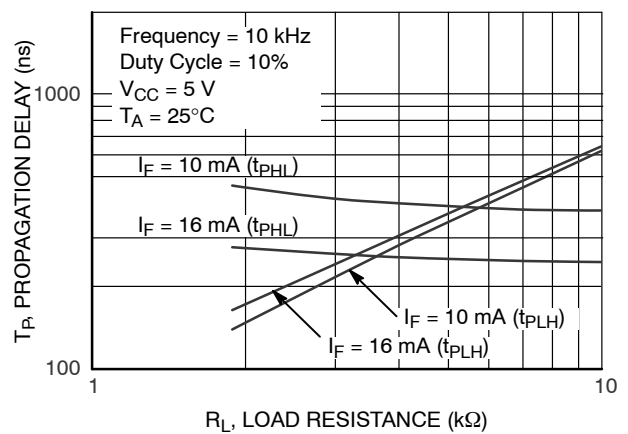
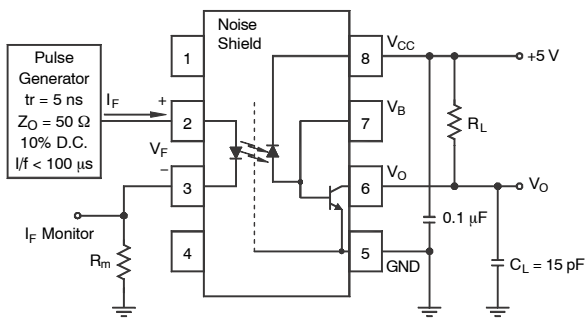


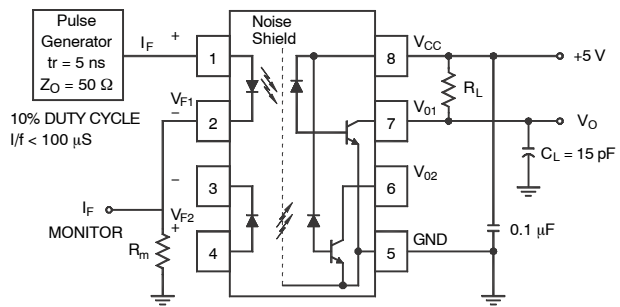
Figure 13. Propagation Delay vs. Load Resistance

Single-Channel: 6N135M, 6N136M, HCPL4503M Dual-Channel: HCPL2530M, HCPL2531M

TEST CIRCUIT



Test Circuit for 6N135M, 6N136M, and HCPL4503M



Test Circuit for HCPL2530M and HCPL2531M

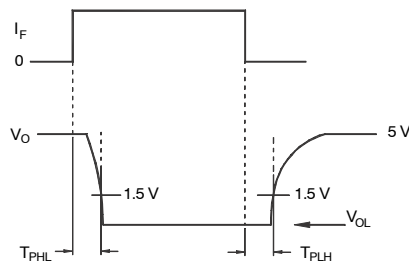
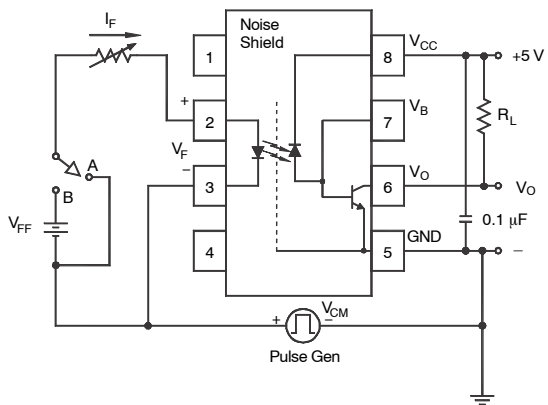
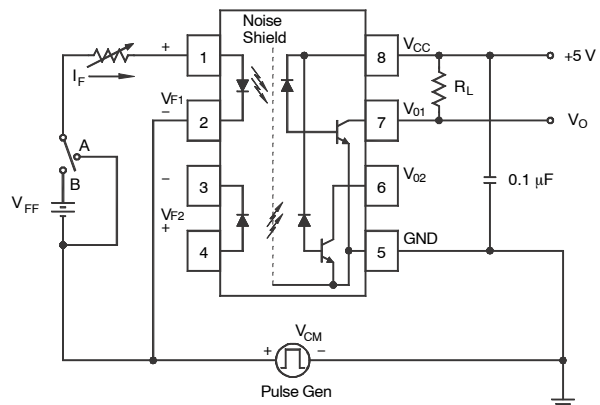


Figure 14. Switching Time Test Circuit



Test Circuit for 6N135M, 6N136M, and HCPL4503M



Test Circuit for HCPL2530M and HCPL2531M

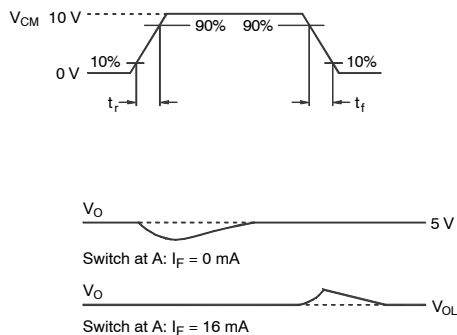
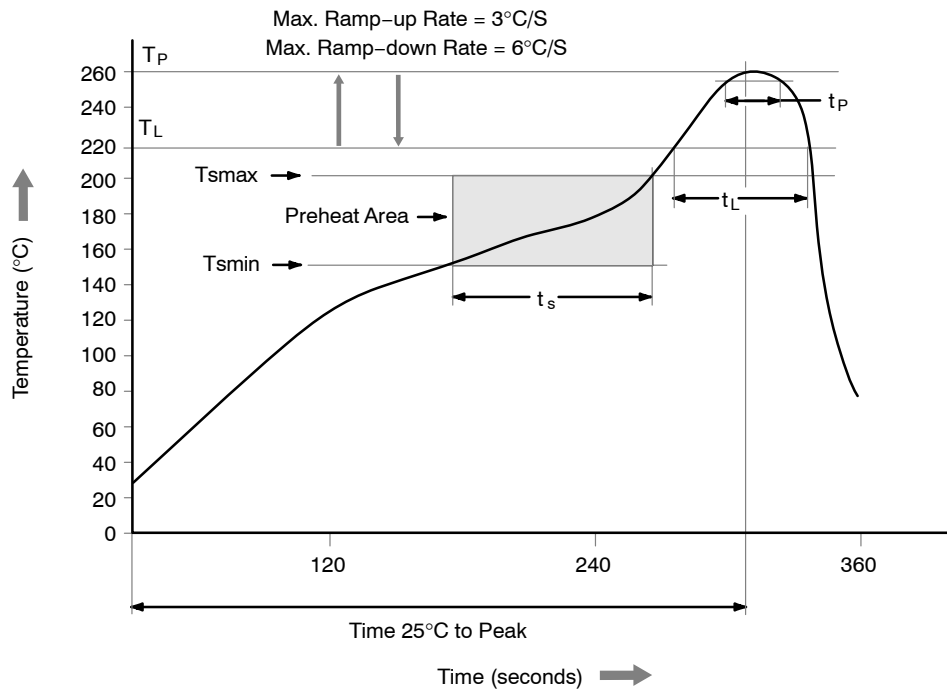


Figure 15. Common Mode Immunity Test Circuit

**Single-Channel: 6N135M, 6N136M, HCPL4503M Dual-Channel: HCPL2530M,
HCPL2531M**

REFLOW PROFILE



Profile Feature	Pb-Free Assembly Profile
Temperature Min. (Tsmín)	150°C
Temperature Max. (Tsmáx)	200°C
Time (ts) from (Tsmín to Tsmáx)	60 to 120 s
Ramp-up Rate (tL to tp)	3°C/second maximum
Liquidous Temperature (TL)	217°C
Time (tL) Maintained Above (TL)	60 to 150 s
Peak Body Package Temperature	260°C +0°C / -5°C
Time (tp) within 5°C of 260°C	30 s
Ramp-down Rate (TP to TL)	6°C/s maximum
Time 25°C to Peak Temperature	8 minutes maximum

Figure 16. Reflow Profile

**Single-Channel: 6N135M, 6N136M, HCPL4503M Dual-Channel: HCPL2530M,
HCPL2531M**

ORDERING INFORMATION

Part Number	Package	Shipping[†]
6N135M	PDIP8 9.655x6.61, 2.54P DIP 8-Pin	50 Units / Tube
6N135SM	PDIP8 GW SMT 8-Pin (Lead Bend)	50 Units / Tube
6N135SDM	PDIP8 GW SMT 8-Pin (Lead Bend)	1,000 / Tape and Reel
6N135VM	PDIP8 9.655x6.61, 2.54P DIP 8-Pin, DIN IEC60747-5-5 Option	50 Units / Tube
6N135SVM	PDIP8 GW SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 Option	50 Units / Tube
6N135SDVM	PDIP8 GW SMT 8-Pin (Lead Bend), DIN EN/IEC 60747-5-5 Option	1,000 / Tape and Reel
6N135TVM	PDIP8 6.6x3.81, 2.54P DIP 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-5 Option	50 Units / Tube
6N135TSVM	PDIP8 GW SMT 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-5 Option	50 Units / Tube
6N135TSR2VM	PDIP8 GW SMT 8-Pin, 0.4" Lead Spacing, DIN EN/IEC 60747-5-2 Option	1,000 / Tape and Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NOTE: The product orderable part number system listed in this table also applies to the 6N136M, HCPL4503M, HCPL2530M and HCPL2531M product families.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®



PDIP8 6.6x3.81, 2.54P
CASE 646BW
ISSUE O

DATE 31 JUL 2016



- NOTES:
A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

DOCUMENT NUMBER:	98AON13445G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PDIP8 6.6X3.81, 2.54P	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

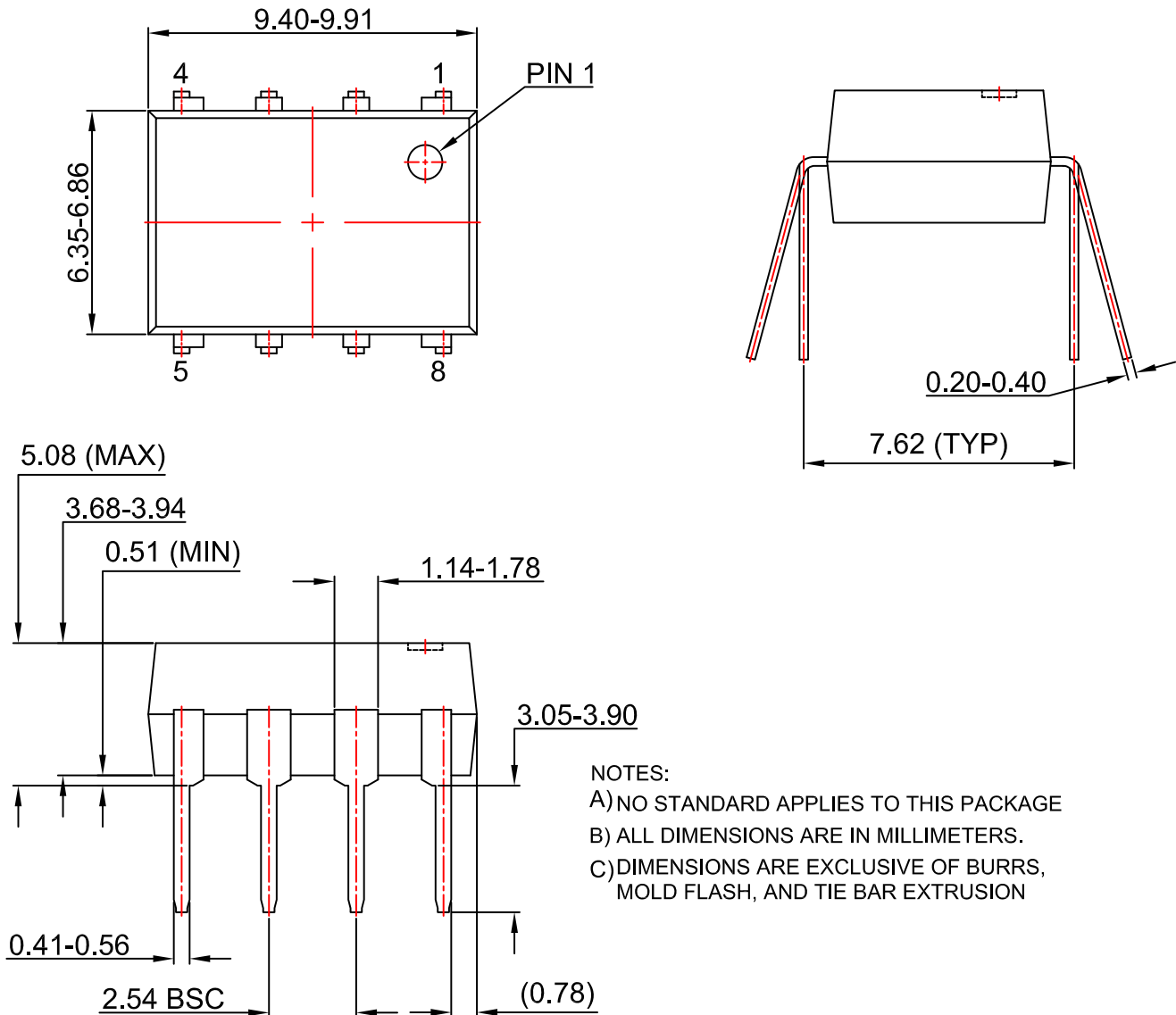
PACKAGE DIMENSIONS

ON Semiconductor®



PDIP8 9.655x6.6, 2.54P
CASE 646CQ
ISSUE O

DATE 18 SEP 2017



NOTES:
A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS,
MOLD FLASH, AND TIE BAR EXTRUSION

DOCUMENT NUMBER:	98AON13446G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PDIP8 9.655X6.6, 2.54P	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

ON Semiconductor®

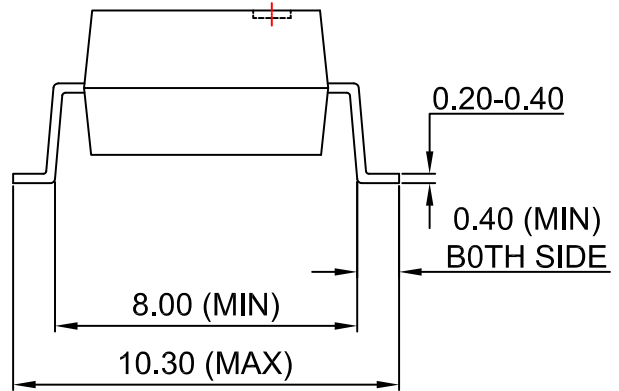


PDIP8 GW
CASE 709AC
ISSUE O

DATE 31 JUL 2016



LAND PATTERN RECOMMENDATION



NOTES:

- A) NO STANDARD APPLIES TO THIS PACKAGE
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

DOCUMENT NUMBER:	98AON13447G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PDIP8 GW	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.

MECHANICAL CASE OUTLINE

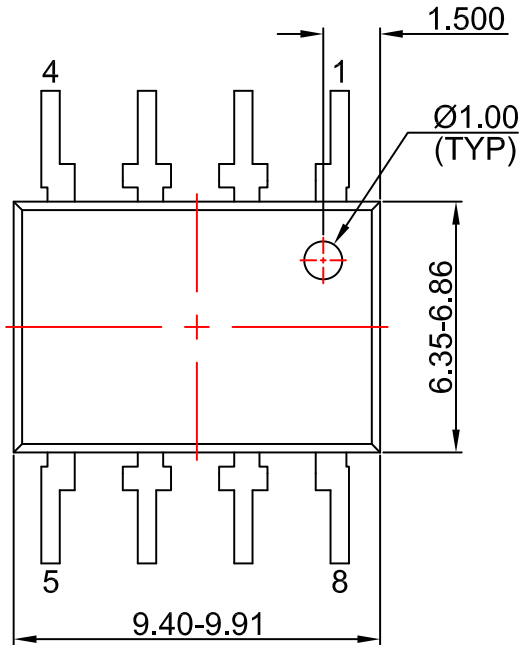
PACKAGE DIMENSIONS

ON Semiconductor®



PDIP8 GW
CASE 709AD
ISSUE O

DATE 31 JUL 2016



LAND PATTERN RECOMMENDATION



NOTES:

- A) NO STANDARD APPLIES TO THIS PACKAGE
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

DOCUMENT NUMBER:	98AON13448G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PDIP8 GW	PAGE 1 OF 1

ON Semiconductor and are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. ON Semiconductor does not convey any license under its patent rights nor the rights of others.