8-Pin DIP High-Speed 10 MBit/s Logic Gate Optocouplers

Single-Channel: 6N137M, HCPL2601M, HCPL2611M Dual-Channel: HCPL2630M, HCPL2631M

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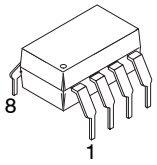
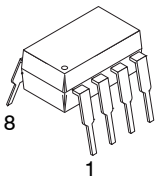
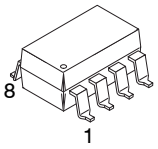


PDIP8 6.6x3.81, 2.54P
CASE 646BW



PDIP8 9.655x6.6, 2.54P
CASE 646CQ



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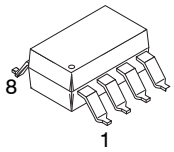
CASE 709AC



PDIP8 GW
CASE 709AD

Description

The 6N137M, HCPL2601M, HCPL2611M single−channel and HCPL2630M, HCPL2631M dual−channel optocouplers consist of a 850 nm AlGaAs LED, optically coupled to a very high speed integrated photo−detector logic gate with a strobable output. This output features an open collector, thereby permitting wired OR outputs. The switching parameters are guaranteed over the temperature range of −40°C to +85°C. A maximum input signal of 5 mA will provide a minimum output sink current of 13 mA (fan out of 8).

An internal noise shield provides superior common mode rejection of typically 10 kV/μs. The HCPL2601M and HCPL2631M has a minimum CMR of 5 kV/μs. The HCPL2611M has a minimum CMR of 10 kV/μs.

Features

- Very High Speed – 10 MBit/s
- Superior CMR – 10 kV/μs
- Fan−out of 8 Over −40°C to +85°C
- Logic Gate Output
- Strobable Output
- Wired OR−open Collector
- Safety and Regulatory Approvals
  - UL1577, 5,000 VAC_{RMS} for 1 Minute
  - DIN EN/IEC60747−5−5
- These are Pb−Free Devices

Applications

- Ground Loop Elimination
- LSTTL to TTL, LSTTL or 5 V CMOS
- Line Receiver, Data Transmission
- Data Multiplexing
- Switching Power Supplies
- Pulse Transformer Replacement
- Computer−peripheral Interface

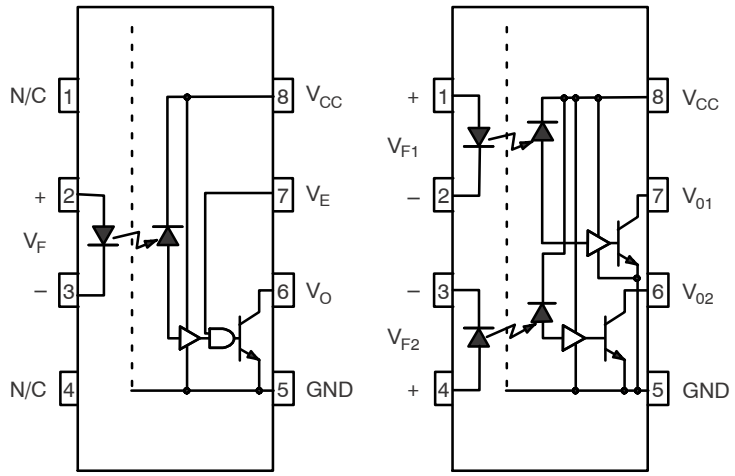
MARKING DIAGRAM

6N137	= Device Number
V	= DIN EN/IEC60747−5−5 Option (only appears on component ordered with this option)
XX	= Two−Digit Year Code, e.g., ‘16’
YY	= Two−Digit Work Week, Ranging from ‘01’ to ‘53’
B	= Assembly Package Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 14 of this data sheet.

SCHEMATICS



6N137M, HCPL2601M, HCPL2611M

HCPL2630M, HCPL2631M

A 0.1 μF bypass capacitor must be connected between pins 8 and 5 (Note 1).

Figure 1. Schematics

TRUTH TABLE (Positive Logic)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H
H	NC	L
L	NC	H

SAFETY AND INSULATION RATINGS (As per DIN EN/IEC 60747−5−5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.)

Parameter		Characteristics
Installation Classifications per DIN VDE 0110/1.89 Table 1, For Rated Mains Voltage	<150 V_{RMS}	I–IV
	<300 V_{RMS}	I–IV
	<450 V_{RMS}	I–III
	<600 V_{RMS}	I–III
Climatic Classification		40/100/21
Pollution Degree (DIN VDE 0110/1.89)		2
Comparative Tracking Index		175

Symbol	Parameter	Value	Unit
V_{PR}	Input−to−Output Test Voltage, Method A, V_{IORM} x 1.6 = V_{PR}, Type and Sample Test with t_m = 10 s, Partial Discharge < 5 pC	1,335	V_{peak}
	Input−to−Output Test Voltage, Method B, V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC	1,669	V_{peak}
V_{IORM}	Maximum Working Insulation Voltage	890	V_{peak}
V_{IOTM}	Highest Allowable Over−Voltage	6,000	V_{peak}
	External Creepage	≥8.0	mm
	External Clearance	≥7.4	mm
	External Clearance (for Option TV, 0.4” Lead Spacing)	≥10.16	mm
DTI	Distance Through Insulation (Insulation Thickness)	≥0.5	mm
T_S	Case Temperature (Note 2)	150	°C
$I_{S,INPUT}$	Input Current (Note 2)	200	mA
$P_{S,OUTPUT}$	Output Power (Duty Factor ≤ 2.7%) (Note 2)	300	mW
R_{IO}	Insulation Resistance at T_S, V_{IO} = 500 V (Note 2)	$>10^9$	Ω

1. The V_{CC} supply to each optoisolator must be bypassed by a 0.1 μF capacitor or larger. This can be either a ceramic or solid tantalum capacitor with good high frequency characteristic and should be connected as close as possible to the package V_{CC} and GND pins of each device.
2. Safety limit value − maximum values allowed in the event of a failure.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Device	Value	Unit
T_{STG}	Storage Temperature		−40 to +125	°C
T_{OPR}	Operating Temperature		−40 to +100	°C
T_J	Junction Temperature		−40 to +125	°C
T_{SOL}	Lead Solder Temperature		260 for 10 s	°C
EMITTER				
I_F (avg)	DC/Average Forward Input Current Per Channel	Single Channel	50	mA
		Dual Channel	30	
V_E	Enable Input Voltage Not to Exceed V_{CC} by More than 500 mV	Single Channel	5.5	V
V_R	Reverse Input Voltage Per Channel	All	5.0	V
P_I	Input Power Dissipation Per Channel	Single Channel	100	mW
		Dual Channel	45	
DETECTOR				
V_{CC}	Supply Voltage	All	−0.5 to 7.0	V
I_O (avg)	Average Output Current Per Channel	All	25	mA
I_O (pk)	Peak Output Current Per Channel	All	50	mA
V_O	Output Voltage Per Channel	All	−0.5 to 7.0	V
P_O	Output Power Dissipation Per Channel	Single Channel	85	mW
		Dual Channel	60	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V_{CC}	Supply Voltage	4.5	5.5	V
I_{FL}	Input Current, Low Level	0	250	μA
I_{FH}	Input Current, High Level	6.3 (Note 3)	20.0	mA
V_{EL}	Enable Voltage, Low Level	0	0.8	V
V_{EH}	Enable Voltage, High Level	2.0	V_{CC}	V
T_A	Ambient Operating Temperature	−40	+85	°C
N	Fan Out (TTL Load)	−	8	

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

3. 6.3 mA is a guard banded value which allows for at least 20% CTR degradation. Initial input current threshold value is 5.0 mA or less.

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	Device	Min	Typ	Max	Unit
INDIVIDUAL COMPONENT CHARACTERISTICS (V_{CC} = 5.5 V, T_A = 0°C to 70°C unless otherwise specified)							
EMITTER							
V_F	Input Forward Voltage	I_F = 10 mA, T_A = 25°C	All	–	1.45	1.70	V
		I_F = 10 mA		–	–	1.80	
B_{VR}	Input Reverse Breakdown Voltage	I_R = 10 μA	All	5.0	–	–	V
C_{IN}	Input Capacitance	V_F = 0, f = 1 MHz	All	–	60	–	pF
$\Delta V_F / \Delta T_A$	Temperature Coefficient of Forward Voltage	I_F = 10 mA	All	–	−1.4	–	mV/°C
DETECTOR							
I_{CCL}	Logic Low Supply Current	I_F = 10 mA, V_O = Open, V_E = 0.5 V	Single Channel	–	8	13	mA
		I_{F1} = I_{F2} = 10 mA, V_O = Open	Dual Channel	–	14	21	
I_{CCH}	Logic High Supply Current	I_F = 0 mA, V_O = Open, V_E = 0.5 V	Single Channel	–	6	10	mA
		I_F = 0 mA, V_O = Open	Dual Channel	–	10	15	
I_{EL}	Low Level Enable Current	V_E = 0.5 V	Single Channel	–	−0.7	−1.6	mA
I_{EH}	High Level Enable Current	V_E = 2.0 V	Single Channel	–	−0.5	−1.6	mA
V_{EL}	Low Level Enable Voltage	I_F = 10 mA (Note 4)	Single Channel	–	–	0.8	V
V_{EH}	High Level Enable Voltage	I_F = 10 mA	Single Channel	2.0	–	–	V
TRANSFER CHARACTERISTICS (V_{CC} = 5.5 V, T_A = −40°C to +85°C unless otherwise specified)							
I_{FT}	Input Threshold Current	V_O = 0.6 V, V_E = 2.0 V, I_{OL} = 13 mA	All	–	3	5	mA
I_{OH}	HIGH Level Output Current	V_O = 5.5 V, I_F = 250 μA, V_E = 2.0 V	All	–	–	100	μA
V_{OL}	LOW Level Output Voltage	I_F = 5 mA, V_E = 2.0 V, I_{OL} = 13 mA	All	–	0.4	0.6	V
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, I_F = 7.5 mA, T_A = −40°C to +85°C unless otherwise specified)							
t_{PHL}	Propagation Delay Time to Logic LOW	R_L = 350 Ω, C_L = 15 pF, T_A = 25°C (Note 5) (Figure 23)	All	25	40	75	ns
		R_L = 350 Ω, C_L = 15 pF (Note 5) (Figure 23)		–	–	100	
t_{PLH}	Propagation Delay Time to Logic HIGH	R_L = 350 Ω, C_L = 15 pF, T_A = 25°C (Note 6) (Figure 23)	All	20	40	75	ns
		R_L = 350 Ω, C_L = 15 pF (Note 6) (Figure 23)		–	–	100	
$\lvert t_{PHL} - t_{PLH} \rvert$	Pulse Width Distortion	R_L = 350 Ω, C_L = 15 pF (Figure 23)	All	–	1	35	ns
t_R	Output Rise Time (10% to 90%)	R_L = 350 Ω, C_L = 15 pF (Note 7) (Figure 23)	All	–	30	–	ns
t_F	Output Fall Time (90% to 10%)	R_L = 350 Ω, C_L = 15 pF(Note 8) (Figure 23)	All	–	10	–	ns
t_{EHL}	Enable Propagation Delay Time to Output LOW Level	V_{EH} = 3.5 V, R_L = 350 Ω, C_L = 15 pF (Note 9) (Figure 24)	Single Channel	–	15	–	ns
t_{ELH}	Enable Propagation Delay Time to Output HIGH Level	V_{EH} = 3.5 V, R_L = 350 Ω, C_L = 15 pF (Note 10) (Figure 24)	Single Channel	–	15	–	ns
$\lvert CM_H \rvert$	Common Mode Transient Immunity at Logic High	I_F = 0 mA, V_{CM} = 50 V_{PEAK}, R_L = 350 Ω, T_A = 25°C (Note 11) (Figure 25)	6N137M, HCPL2630M	–	10,000	–	V/μs
			HCPL2601M, HCPL2631M	5000	10,000	–	
		I_F = 0 mA, V_{CM} = 400 V_{PEAK}, R_L = 350 Ω, T_A = 25°C (Note 11) (Figure 25)	HCPL2611M	10,000	15,000	–	

ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Test Conditions	Device	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS (V_{CC} = 5 V, I_F = 7.5 mA, T_A = −40°C to +85°C unless otherwise specified)							
$\|CM_L\|$	Common Mode Transient Immunity at Logic Low	V_{CM} = 50 V_{PEAK}, R_L = 350 Ω, T_A = 25°C (Note 11) (Figure 25)	6N137M, HCPL2630M	–	10,000	–	V/μs
			HCPL2601M, HCPL2631M	5000	10,000	–	
		V_{CM} = 400 V_{PEAK}, R_L = 350 Ω, T_A = 25°C (Note 11) (Figure 25)	HCPL2611M	10,000	15,000	–	
ISOLATION CHARACTERISTICS (T_A = 25°C, unless otherwise noted)							
V_{ISO}	Withstand Insulation Test Voltage	Relative Humidity ≤ 50%, I_{I-O} ≤ 10 μA, t = 1 min, f = 50 Hz (Note 12) (Note 13)	All	5,000	–	–	VAC_{RMS}
R_{I-O}	Resistance (Input to Output)	V_{I-O} = 500 V_{DC} (Note 12)	All	–	10^{11}	–	Ω
C_{I-O}	Capacitance (Input to Output)	f = 1 MHz, V_{I-O} = 0 V_{DC} (Note 12)	All	–	1	–	pF
I_{I-O}	Input−Output Insulation Leakage Current	Relative Humidity ≤ 45%, V_{I-I} = 3000 V_{DC}, t = 5 s (Note 12)	All	–	–	1.0	μA

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Enable Input − No pull up resistor required as the device has an internal pull up resistor.
5. t_{PHL} − Propagation delay is measured from the 3.75 mA level on the LOW to HIGH transition of the input current pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
6. t_{PLH} − Propagation delay is measured from the 3.75 mA level on the HIGH to LOW transition of the input current pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
7. t_R − Rise time is measured from the 10% to the 90% levels on the LOW to HIGH transition of the output pulse.
8. t_F − Fall time is measured from the 90% to the 10% levels on the HIGH to LOW transition of the output pulse.
9. t_{EHL} − Enable input propagation delay is measured from the 1.5 V level on the LOW to HIGH transition of the input voltage pulse to the 1.5 V level on the HIGH to LOW transition of the output voltage pulse.
10. t_{ELH} − Enable input propagation delay is measured from the 1.5 V level on the HIGH to LOW transition of the input voltage pulse to the 1.5 V level on the LOW to HIGH transition of the output voltage pulse.
11. Common mode transient immunity in logic high level is the maximum tolerable (positive) dV_{cm}/dt on the leading edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic high state (i.e., V_O > 2.0 V). Common mode transient immunity in logic low level is the maximum tolerable (negative) dV_{cm}/dt on the trailing edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a logic low state (i.e., V_O < 0.8 V).
12. Device is considered a two terminal device: pins 1, 2, 3 and 4 are shorted together and pins 5, 6, 7 and 8 are shorted together.
13. 5000 VAC_{RMS} for 1 minute duration is equivalent to 6000 VAC_{RMS} for 1 second duration

TYPICAL PERFORMANCE CURVES

(For Single−Channel Devices: 6N137M, HCPL2601M, and HCPL2611M)

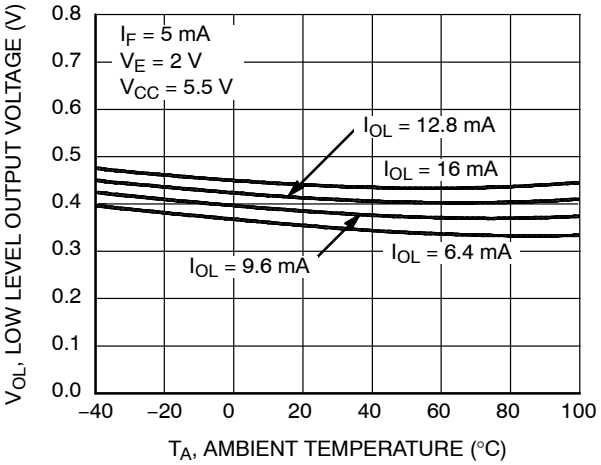


Figure 2. Low Level Output Voltage vs. Ambient Temperature

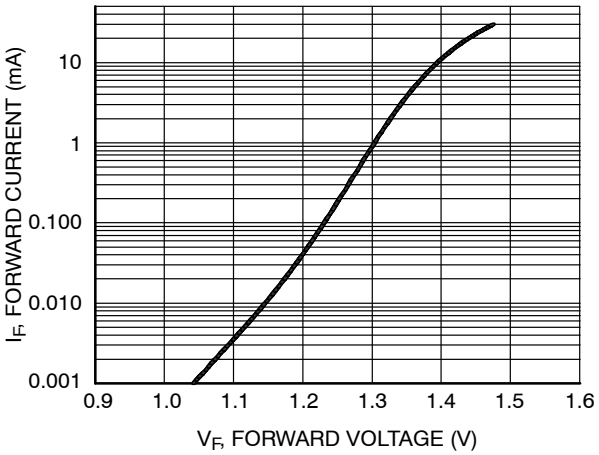


Figure 3. Input Diode Forward Voltage vs. Forward Current

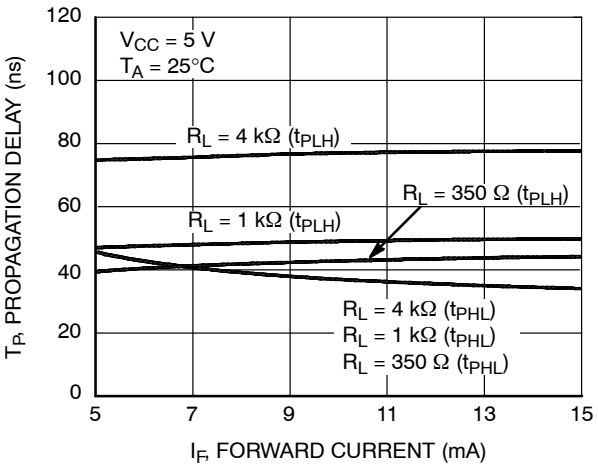


Figure 4. Switching Time vs. Forward Current

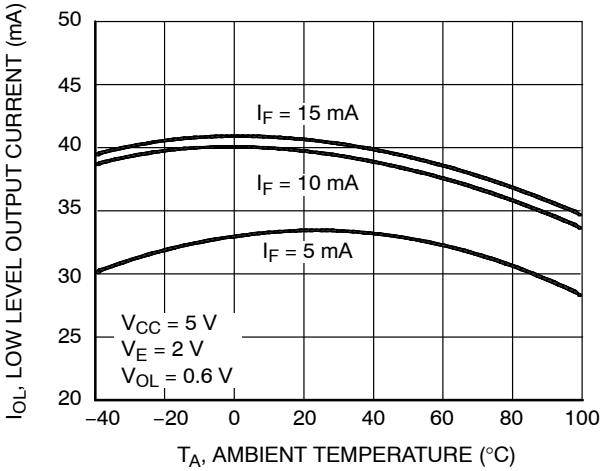


Figure 5. Low Level Output vs. Ambient Temperature

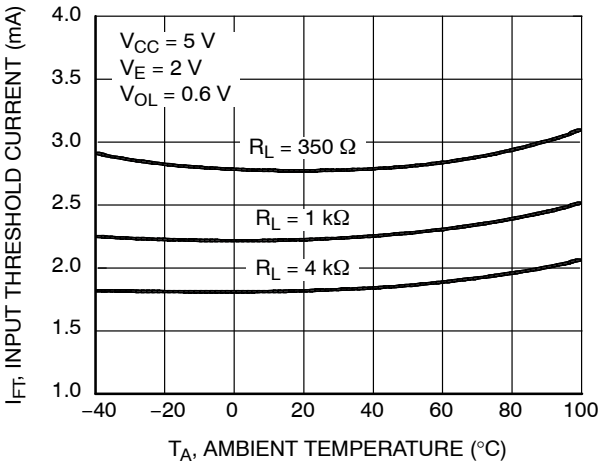


Figure 6. Input Threshold Current vs. Ambient Temperature

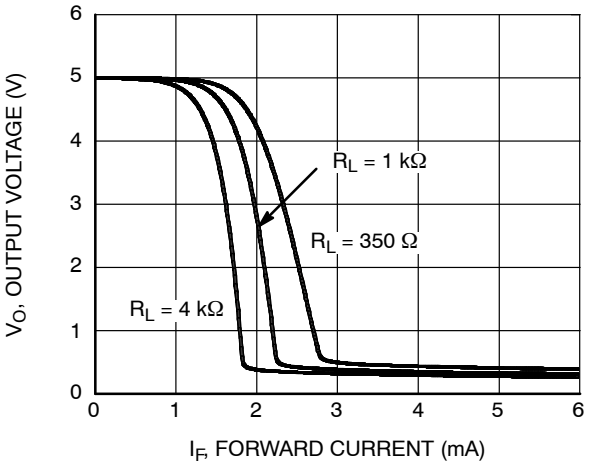


Figure 7. Output Voltage vs. Input Forward Current

TYPICAL PERFORMANCE CURVES (Continued)

(For Single−Channel Devices: 6N137M, HCPL2601M, HCPL2611M)

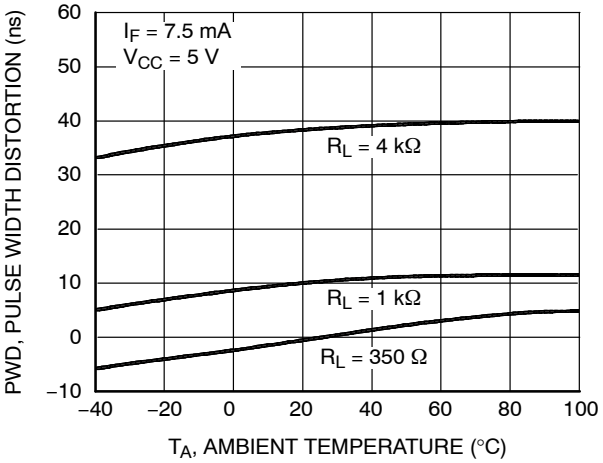


Figure 8. Pulse Width Distortion vs. Temperature

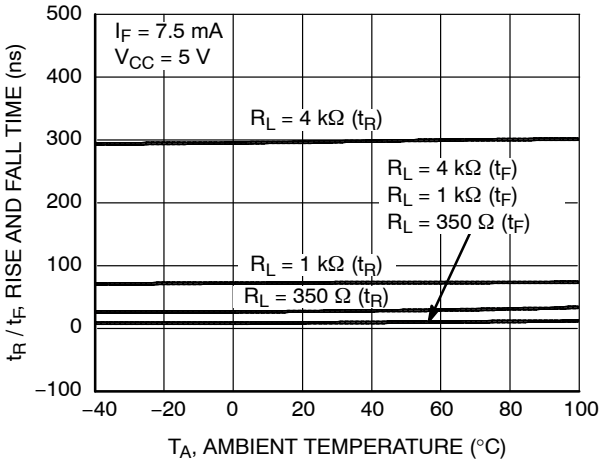


Figure 9. Rise and Fall Time vs. Temperature

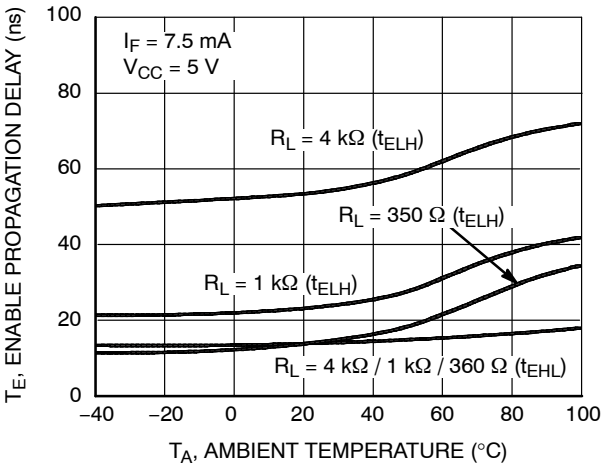


Figure 10. Enable Propagation Delay vs. Temperature

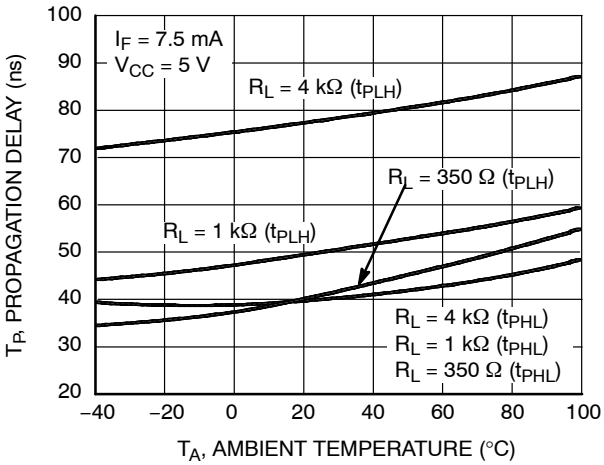


Figure 11. Switching Time vs. Temperature

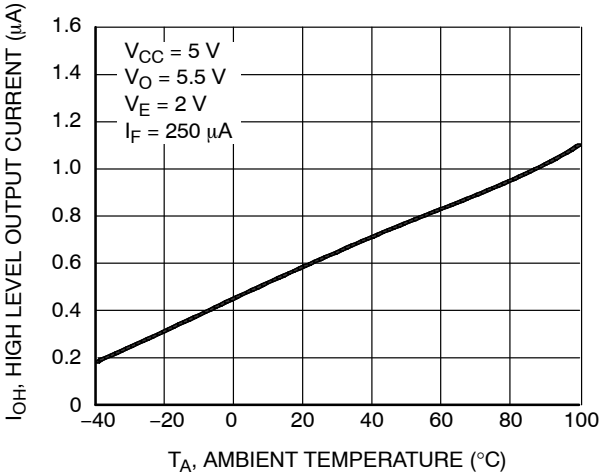


Figure 12. High Level Output Current vs. Temperature

TYPICAL PERFORMANCE CURVES (Continued)

(For Dual−Channel Devices: HCPL2630M and HCPL2631M)

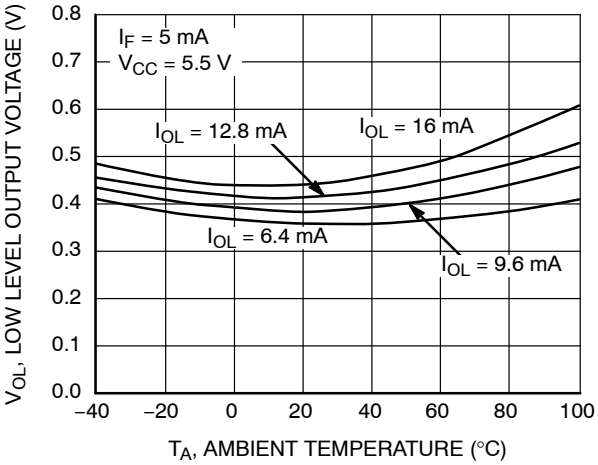


Figure 13. Low Level Output Voltage vs. Ambient Temperature

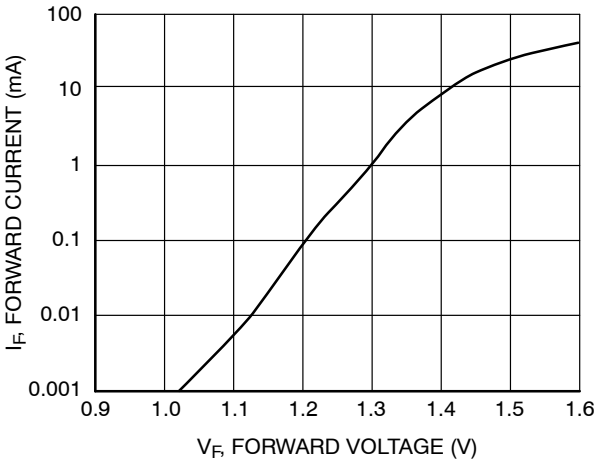


Figure 14. Input Diode Forward Voltage vs. Forward Current

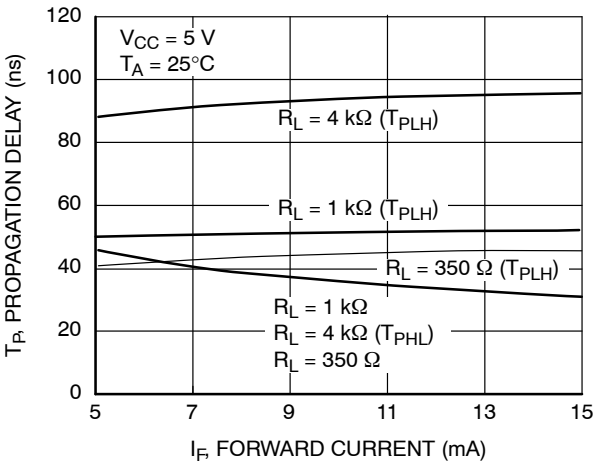


Figure 15. Switching Time vs. Forward Current

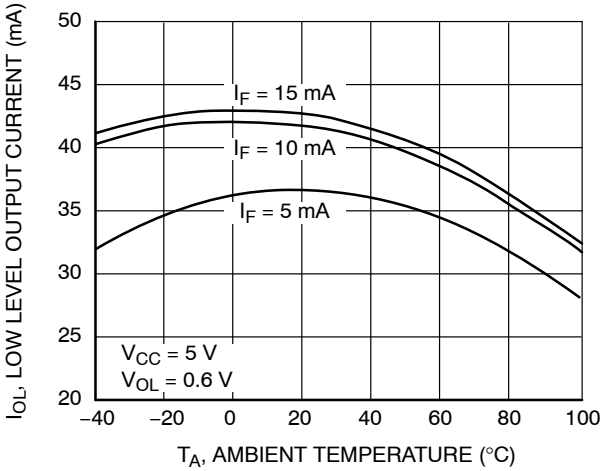


Figure 16. Low Level Output Current vs. Ambient Temperature

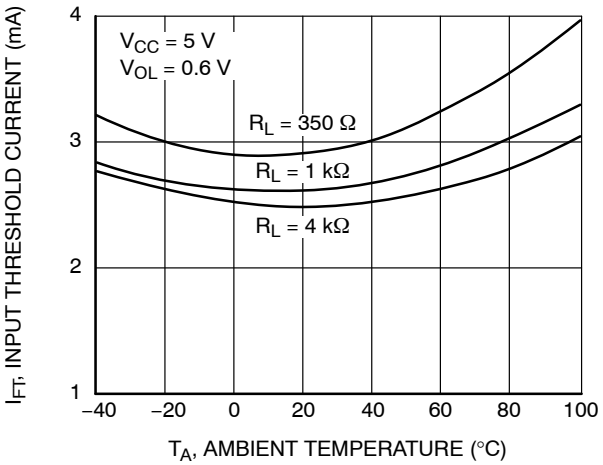


Figure 17. Input Threshold Current vs. Ambient Temperature

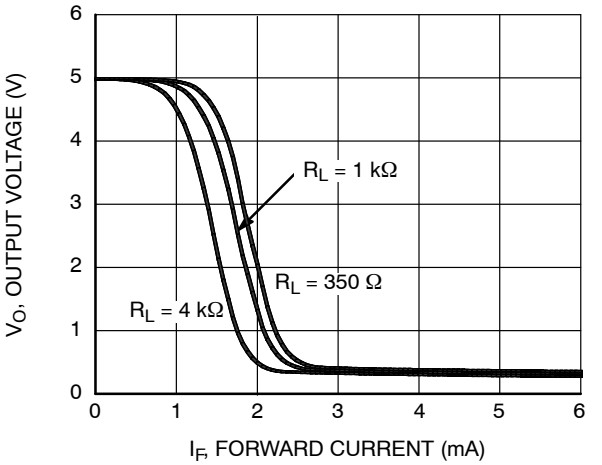


Figure 18. Output Voltage vs. Input Forward Current

TYPICAL PERFORMANCE CURVES (Continued)

(For Dual−Channel Devices: HCPL2630M and HCPL2631M)

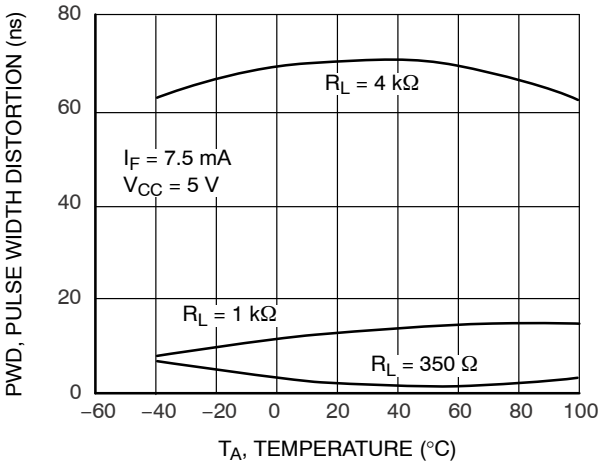


Figure 19. Pulse Width Distortion vs. Temperature

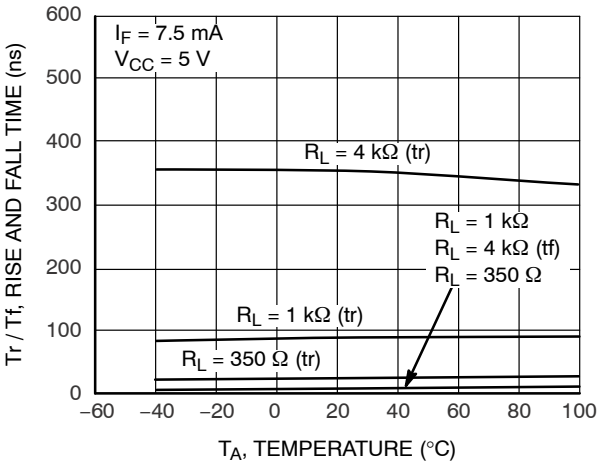


Figure 20. Rise and Fall Time vs. Temperature

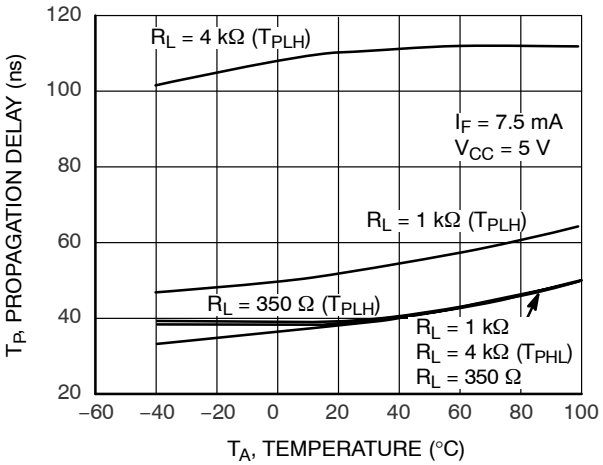


Figure 21. Switching Time vs. Temperature

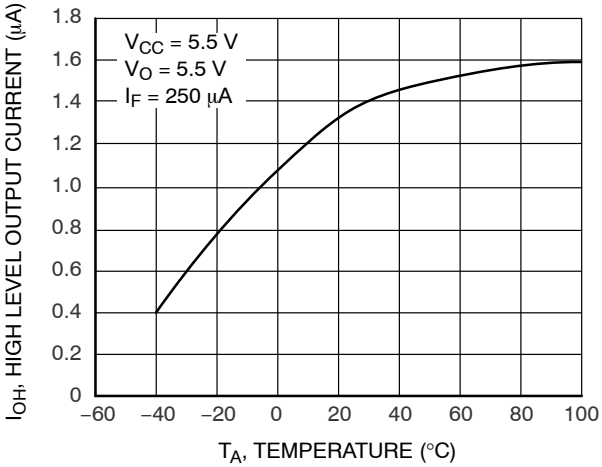


Figure 22. High Level Output Current vs. Temperature

TEST CIRCUITS

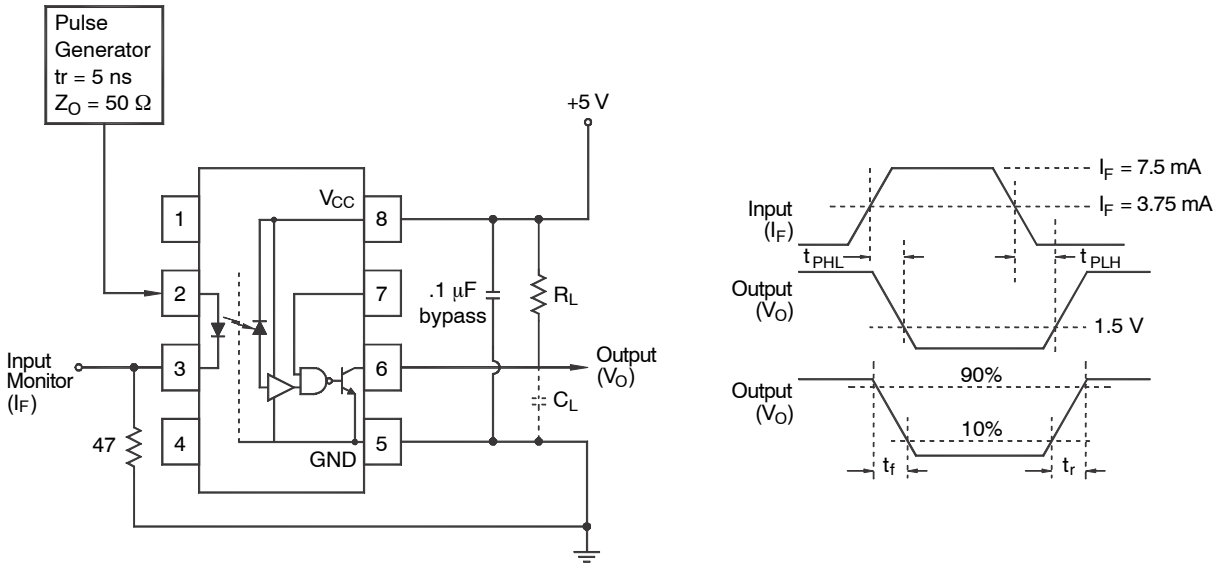


Figure 23. Test Circuit and Waveforms for t_{PLH}, t_{PHL}, t_r and t_f

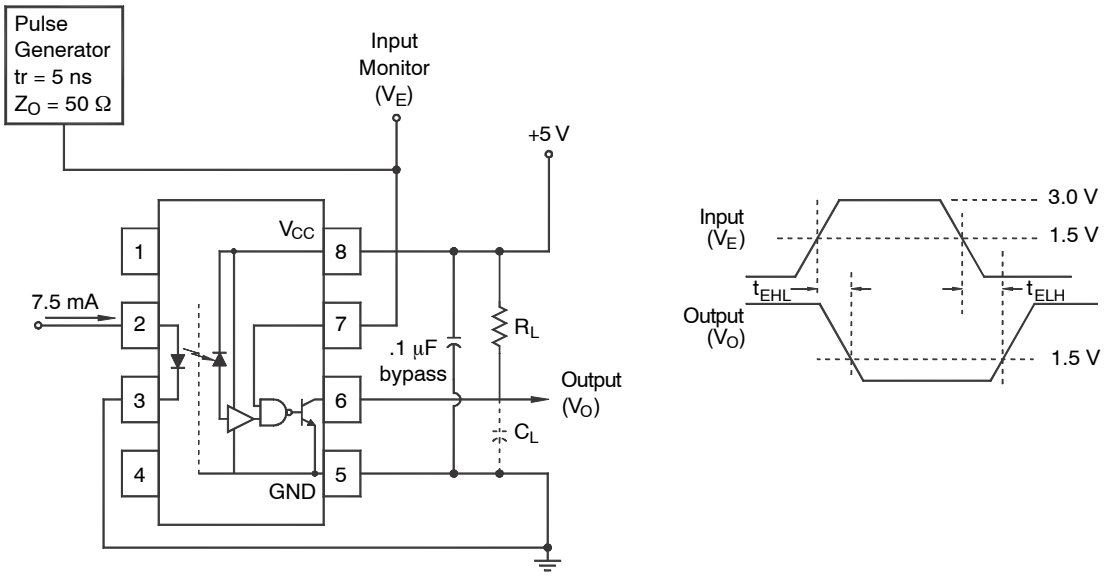


Figure 24. Test Circuit t_{EHL} and t_{ELH}

TEST CIRCUITS (Continued)

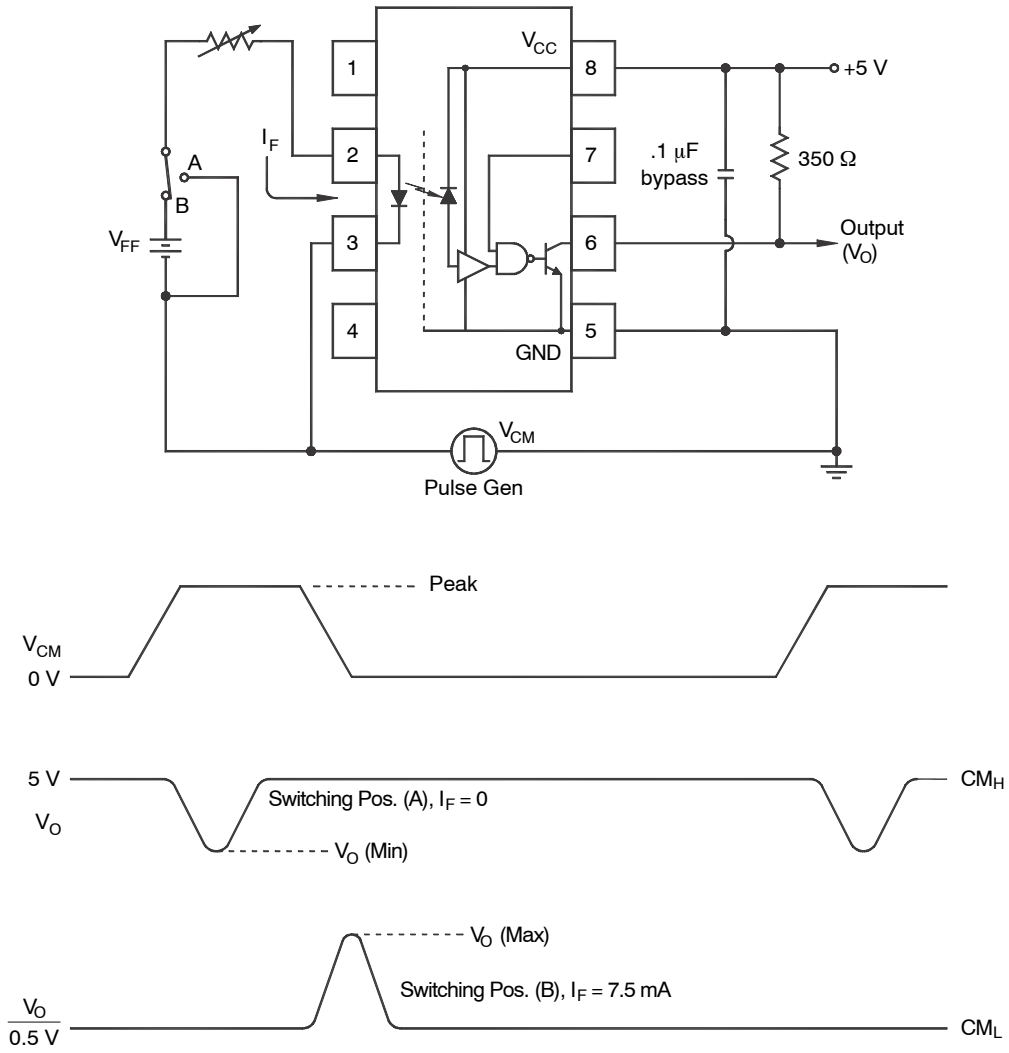
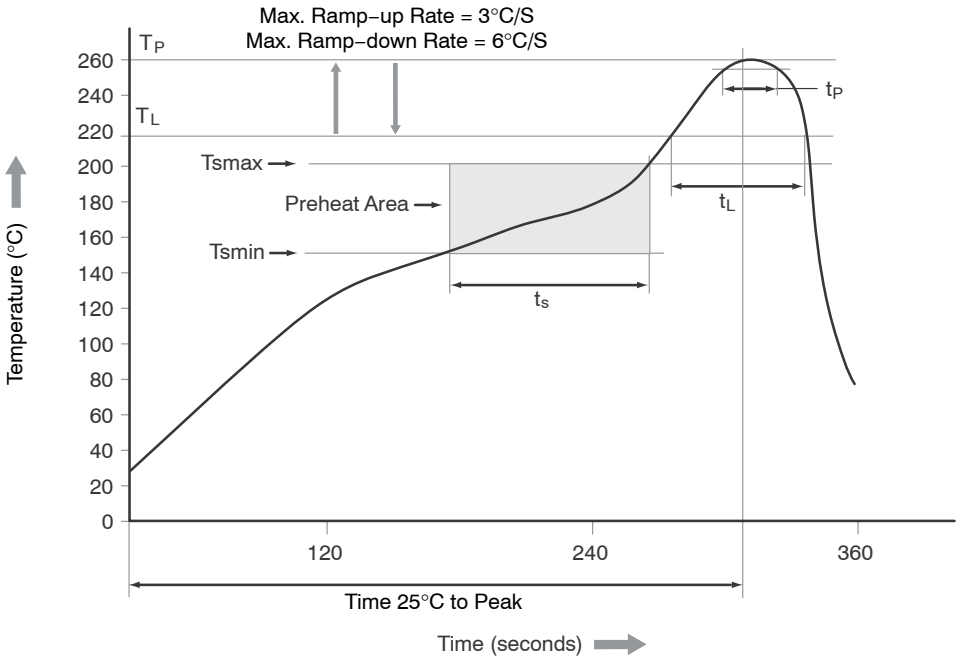


Figure 25. Test Circuit Common Mode Transient Immunity

REFLOW PROFILE



Profile Feature	Pb−Free Assembly Profile
Temperature Minimum (Tsmin)	150°C
Temperature Maximum (Tsmax)	200°C
Time (t_S) from (Tsmin to Tsmax)	60 to 120 s
Ramp−up Rate (t_L to t_P)	3°C/second maximum
Liquidous Temperature (T_L)	217°C
Time (t_L) Maintained Above (T_L)	60 to 150 s
Peak Body Package Temperature	260°C +0°C / −5°C
Time (t_P) within 5°C of 260°C	30 s
Ramp−down Rate (T_P to T_L)	6°C/s maximum
Time 25°C to Peak Temperature	8 minutes maximum

Figure 26. Reflow Profile

ORDERING INFORMATION (Note 14)

Part Number	Package	Shipping†
6N137M	PDIP8 9.655x6.6, 2.54P, CASE 646CQ DIP8−Pin (Pb−Free)	50 Units / Tube
6N137SM	PDIP8 GW, CASE 709AC SMT 8−Pin (Lead Bend) (Pb−Free)	50 Units / Tube
6N137SDM	PDIP8 GW, CASE 709AC SMT 8−Pin (Lead Bend) (Pb−Free)	1000 / Tape & Reel
6N137VM	PDIP8 9.655x6.6, 2.54P, CASE 646CQ DIP 8−Pin, DIN EN/IEC 60747−5−5 Option (Pb−Free)	50 Units / Tube
6N137SVM	PDIP8 GW, CASE 709AC SMT 8−Pin (Lead Bend), DIN EN/IEC 60747−5−5 Option (Pb−Free)	50 Units / Tube
6N137SDVM	PDIP8 GW, CASE 709AC SMT 8−Pin (Lead Bend), DIN EN/IEC 60747−5−5 Option (Pb−Free)	1000 / Tape & Reel
6N137TVM	PDIP8 6.6x3.81, 2.54P, CASE 646BW DIP 8−Pin, 0.4” Lead Spacing, DIN EN/IEC60747−5−5 Option (Pb−Free)	50 Units / Tube
6N137TSVM	PDIP8 GW, CASE 709AD SMT 8−Pin, 0.4” Lead Spacing, DIN EN/IEC60747−5−5 Option (Pb−Free)	50 Units / Tube
6N137TSR2VM	PDIP8 GW, CASE 709AD SMT 8−Pin, 0.4” Lead Spacing, DIN EN/IEC60747−5−5 Option (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

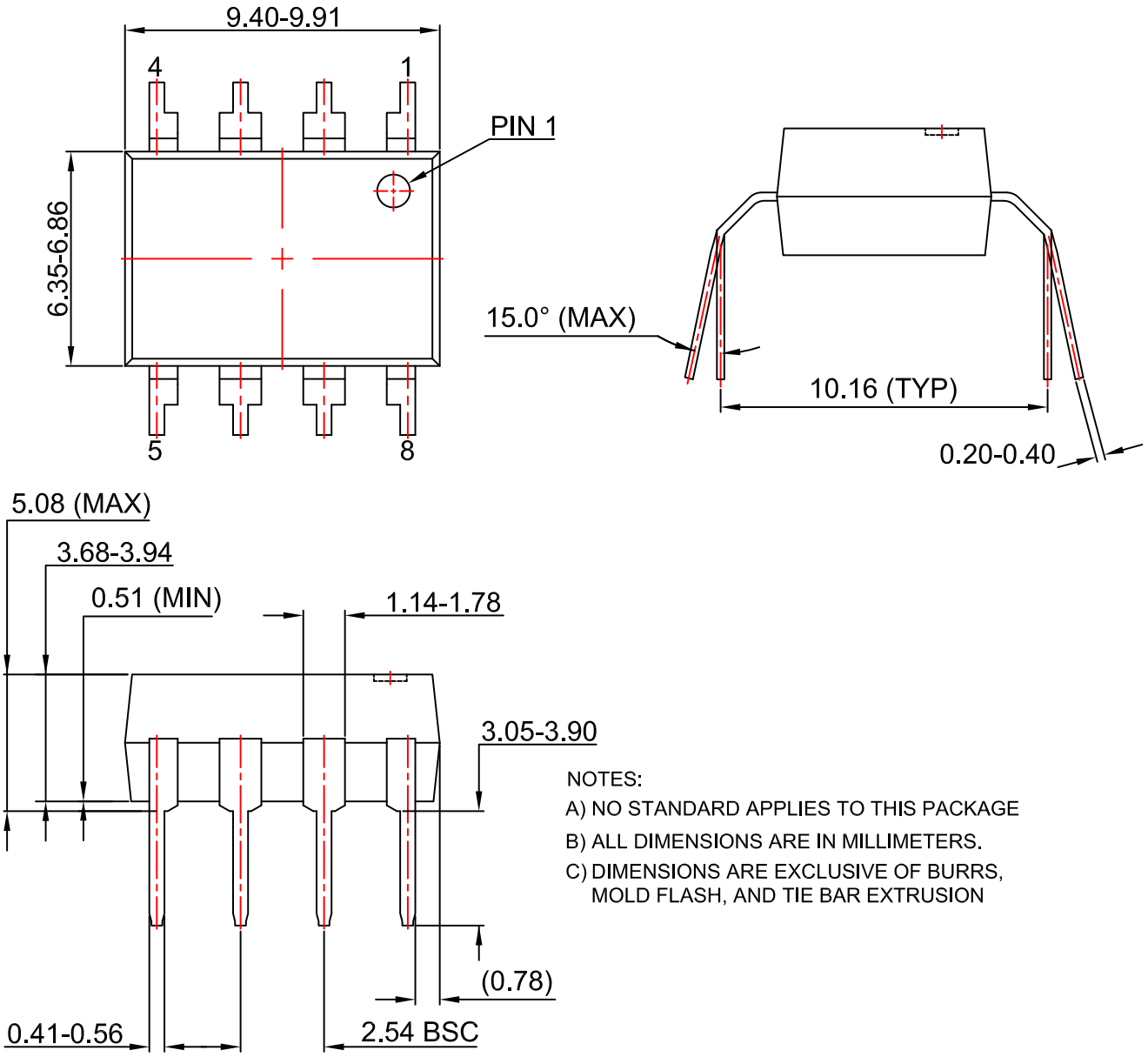
14. The product orderable part number system listed in this table also applies to the HCPL2601M, HCPL2611M, HCPL2630M and HCPL2631M product families.

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

PDIP8 6.6x3.81, 2.54P
CASE 646BW
ISSUE O

DATE 31 JUL 2016



NOTES:
A) NO STANDARD APPLIES TO THIS PACKAGE
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSION

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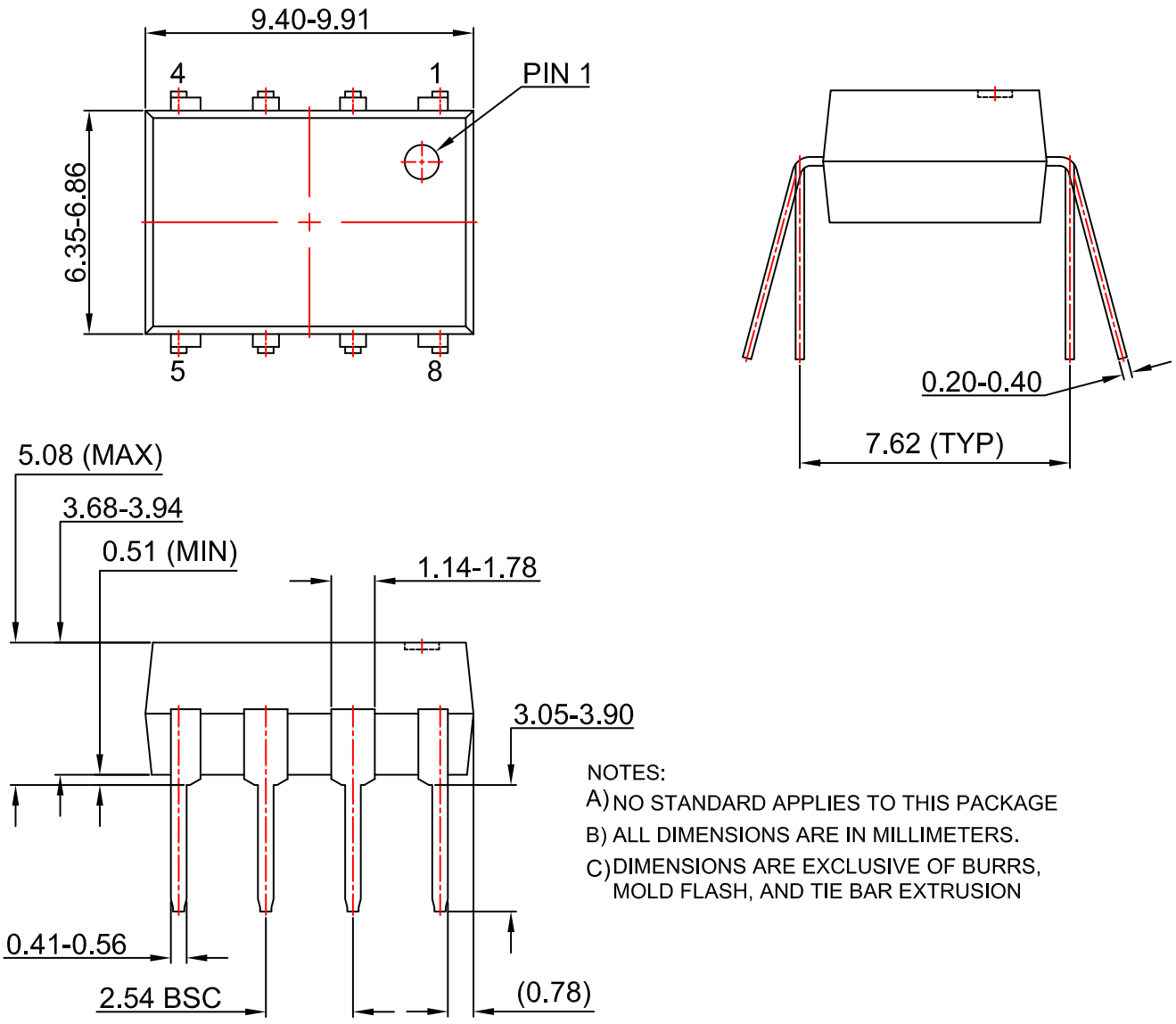
PDIP8 9.655x6.6, 2.54P
CASE 646CQ
ISSUE O

DATE 18 SEP 2017



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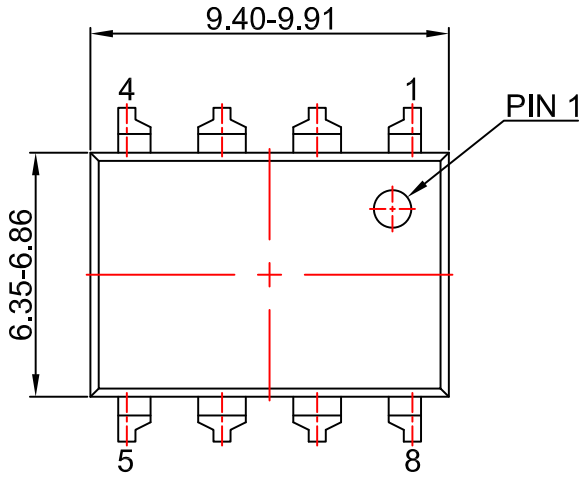
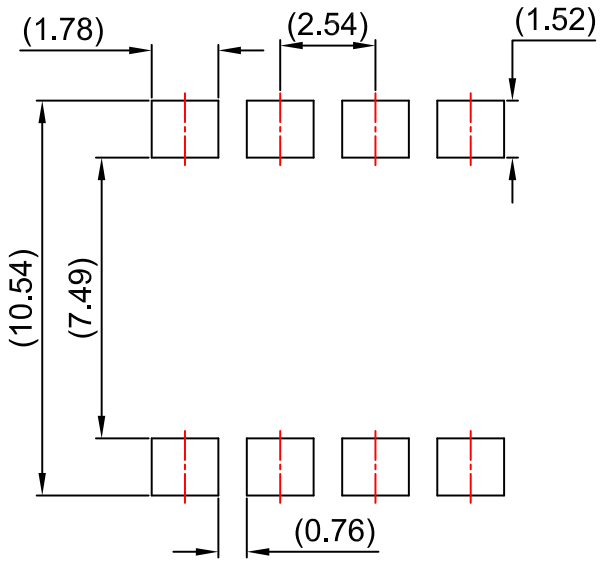
MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

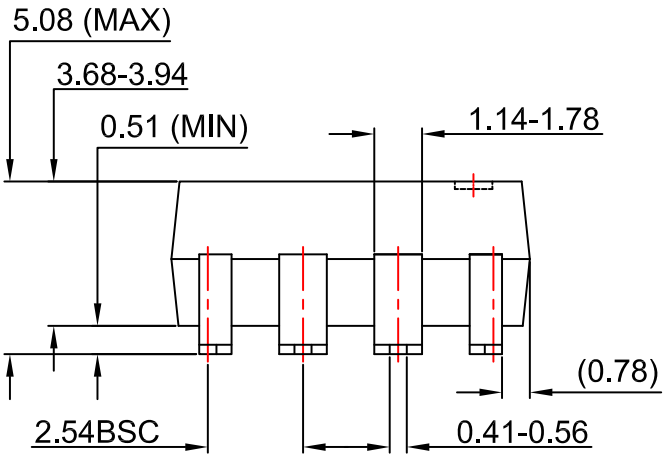
PDIP8 GW
CASE 709AC
ISSUE O

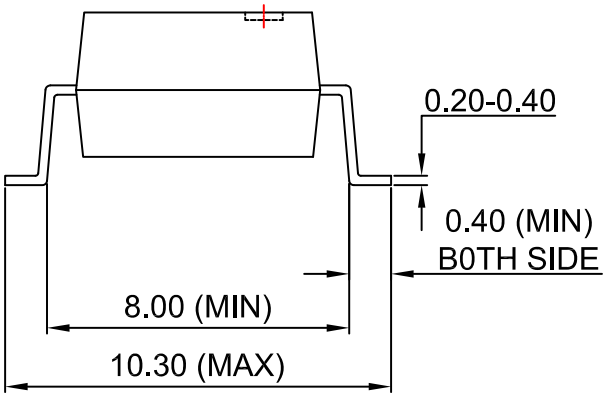
DATE 31 JUL 2016





LAND PATTERN RECOMMENDATION





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DESCRIPTION:	**PDIP8 GW**	**PAGE 1 OF 1**