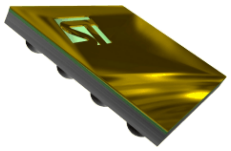
HDMI2C2-5F2

Datasheet

ESD protection and signal booster for HDMI sink control stage interface



WLCSP (10 bumps) package

Features

- For HDMI 1.4, 2.0 & 2.1 application, operating temperature from -40 to 85 °C
- 8 kV contact ESD protection on connector side (IEC 61000-4-2 level 4)
- Supports direct connection to low-voltage HDMI ASIC (down to 1.8 V)
- High integration level in 1 package
- DDC capacitive decoupling between ASIC and HDMI connector and dynamic pull-up for long cable driving
- Enable function to sense 5V power supply presence from HDMI connector and to switch off for power consumption optimization
- Backdrive protection on DDC bus
- Proposed in 500 µm pitch WLCSP package 10 bumps for easy PCB layout

Benefits

- Minimal PCB footprint in tablet, set top box, game console and other consumer application
- Protection of ultra-sensitive HDMI ASICs
- Power consumption optimization thanks to Enable function
- Improved HDMI interface ruggedness and user experience
- Long and/or poor quality cable support with dynamic pull-up on DDC bus

Complies with the following standards

- Dedicated for HDMI 1.4, 2.0 and 2.1 version
- IEC 61000-4-2 level 4
- JESD22-A114D level 2

Product status link
HDMI2C2-5F2

Applications

Consumer and computer electronics HDMI Sink device such as:

- Tablet and smartphone
- HD set-top boxes
- Game console
- DVD and Blu-Ray Disk systems
- Notebook
- PC graphic cards

Description

The HDMI2C2-5F2 is an integrated ESD protection and signal conditioning device for control links of HDMI transmitters (sink).

This device is a simple solution that provides HDMI designers with an easy and fast way to reach full compliance with the stringent HDMI CTS on a wide temperature range.

1 Functional description

The HDMI2C2-5F2 is a fully integrated ESD protection and signal conditioning device for control stage of HDMI receivers (sink).

The component offers two bidirectional buffers, integrating signal conditioning dynamic pull-up on DDC bus for maximum system robustness and signal integrity. These buffers embed also a protection to prevent from connector backdrive current from connector.

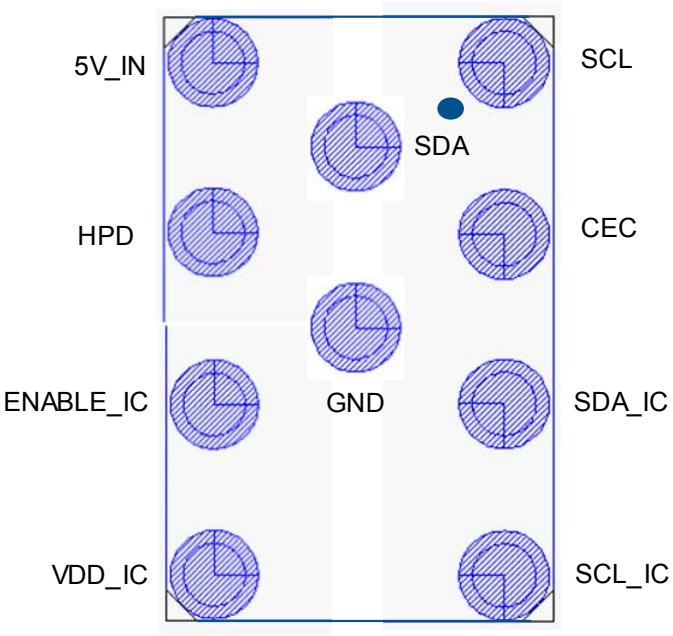
ENABLE_IC function is available to sense 5 V power supply presence from HDMI connector.

On top of 5 V sensing, Enable_IC can be used to switch off our device even if 5V_IN is present.

All these features are provided in a single 10 bumps WLCSP package featuring natural PCB routing, cost optimization and saving space on the board.

The HDMI2C2-5F2 is a simple solution that provides HDMI designers with an easy and fast way to reach full compliance with the stringent HDMI CTS on a wide temperature range. STMicroelectronics proposes also a large range of High Speed ESD protections and common mode filter (ECMF series) dedicated to the TMDS lanes giving the flexibility to the designer to filter and protect these (high speed video link against ESD strikes and EMC issues.

Figure 1. Pin configuration (bump side)



2 Application infomation

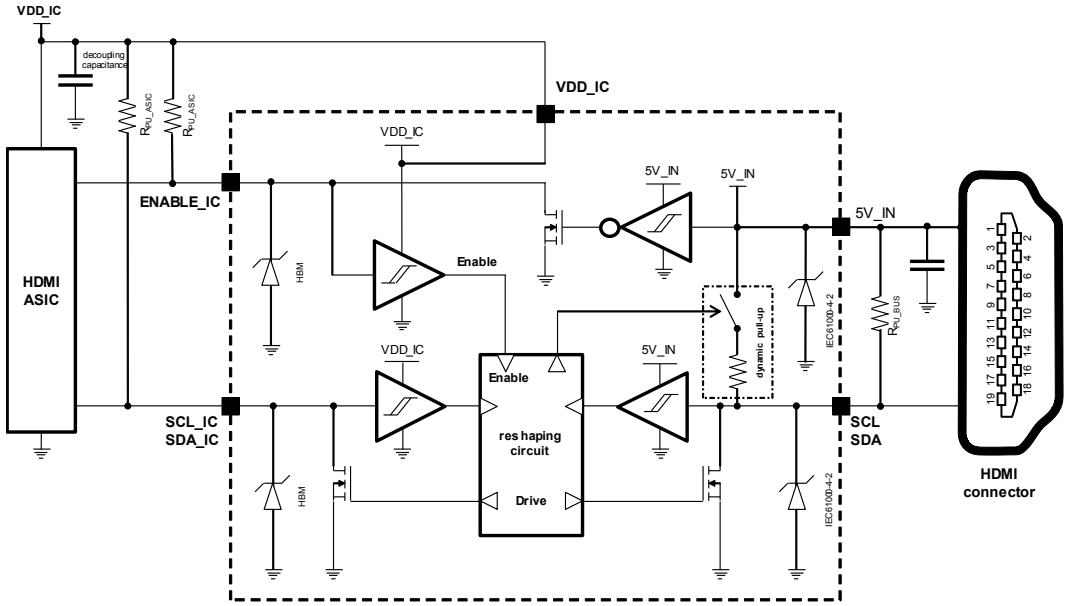
2.1 DDC bus description

The DDC bus is described in the HDMI standards as the display data channel. The topology corresponds to an I2C bus that must be compliant with the I2C bus specification UM10204 revision 5 (October 2012). The DDC bus is made of 2 lines; data line (SDA) and clock line (SCL). It is used to create a point to point communication link from the source to the sink. EEDID and HDCP protocols are especially flowing through this link, making this I2C communication channel a key element in the HDMI application.

The DDC block integrated in the HDMI2C2-5F2 allows a bidirectional communication between the cable and the ASIC. It is fully compliant with the HDMI 2.0 standard (I2C bus specification) and its CTS, and with the I2C bus specification version 2.1. It is shifting the 5 V voltage from the cable (V_{5V_IN}) down to the ASIC voltage level (V_{DD_IC}) that can be as low as 1.8 V.

The Figure 2. DDC buffer functional diagram (SCL and SDA lines) shows the functional diagram of the DDC block integrated in the HDMI2C2-5F2 device.

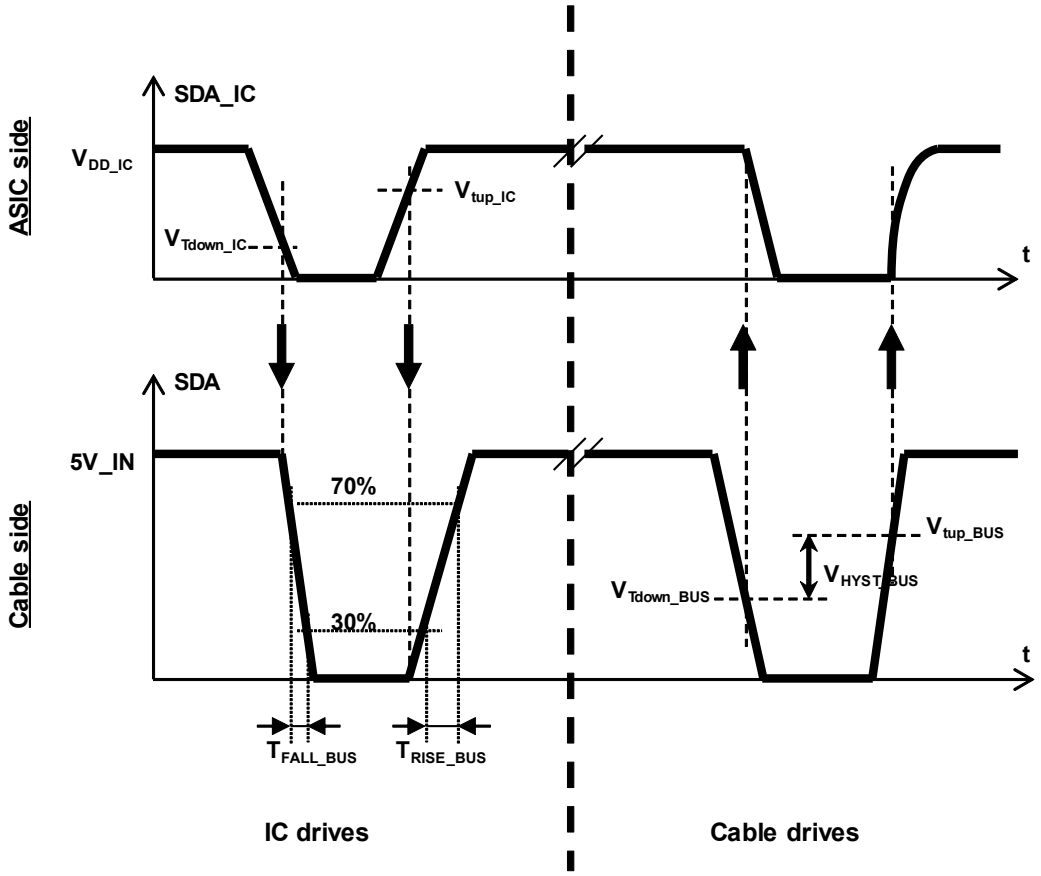
Figure 2. DDC buffer functional diagram (SCL and SDA lines)



ENABLE_IC function is available to sense 5 V power supply presence from HDMI connector and to disable DDC block. The DDC outputs (SCL and SDA on cable side) integrate a protection against ESD which is compliant with IEC61000-4-2 standard, level 4 (8 kV contact).

The Figure 3 illustrates the electrical parameter of the DDC block specified by the Table 6.

Figure 3. **Simplified view of the electrical parameters of the DDC block**



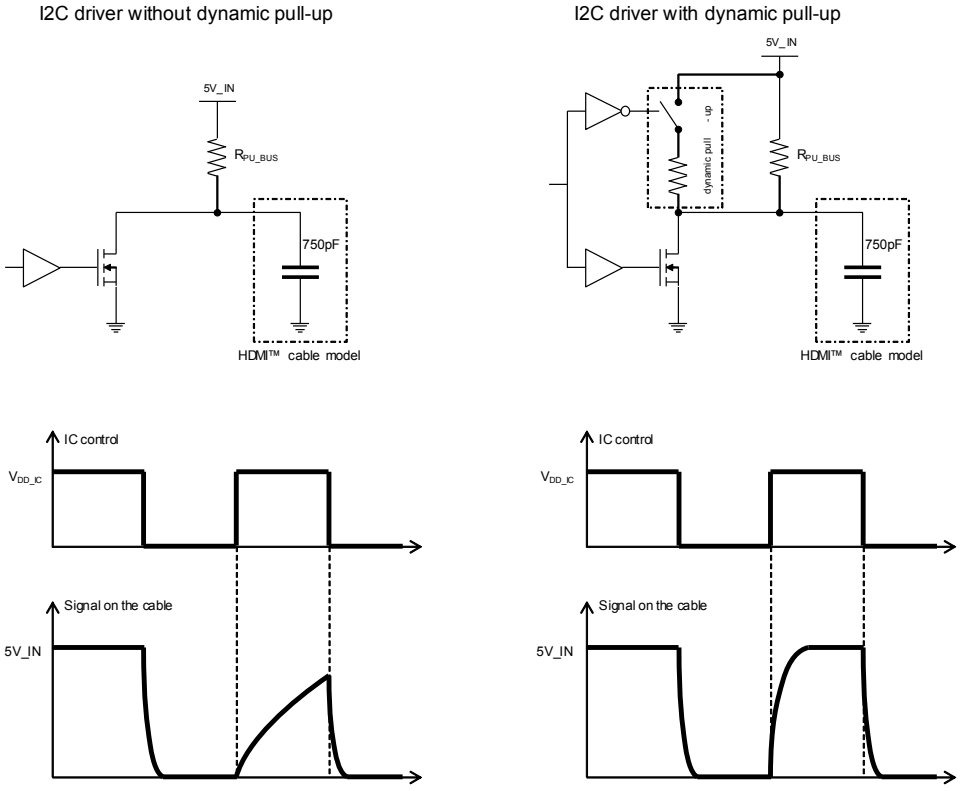
Capacitance measured at the HDMI connector output is equal to the sum of HDMI2C2-5F2 capacitance plus bus capacitance between HDMI2C2-5F2 and HDMI connector output. Thanks to the internal structure of the integrated DDC block, measured capacitance is equal to the input capacitance and then independent from the IC actual capacitance. For compliance test, capacitance on DDC bus must be measured with HDMI2C2-5F2 powered on.

The HDMI standard specifies that the max capacitance of the cable can reach up to 700 pF. Knowing that the max capacitance of the source input can reach up to 50 pF, this means that the I2C buffer must be able to drive a load capacitance up to 750 pF. On the other hand, the I2C standard specifies a maximum rise time (30%-70%) of the signal must be lower than 1 µs in order to keep the signal integrity. Taking into account the max cable capacitance of 750 pF, it is not possible to guarantee a rise time lower than 1µs in worst case.

Therefore, a dynamic pull-up has been integrated at the output of SDA and SCL lines and synchronized with the I2C driver. This signal booster accelerates for a short period the charging time of the equivalent cable capacitance, allowing driving any HDMI cable.

The Figure 4. Benefit of the dynamic pull-up on the DDC bus illustrates the benefit of the dynamic pull-up integrated in the HDMI2C2-5F2 device.

Figure 4. Benefit of the dynamic pull-up on the DDC bus



In order to activate the DDC bus, following conditions must be respected: V_{5V_IN} must be higher than the V_{5V_ON} threshold (see Table 3. Absolute maximum ratings (limiting values)), ENABLE_IC input must be set to a high level and all inputs and outputs (SDA, SCL, SDA_IC, SCL_IC) must be set to a high level at the same time.

The DDC outputs (SCL and SDA on cable side) integrate a protection against ESD which is compliant with IEC61000-4-2 standard, level 4 (8 kV contact).

2.2 ENABLE_IC description

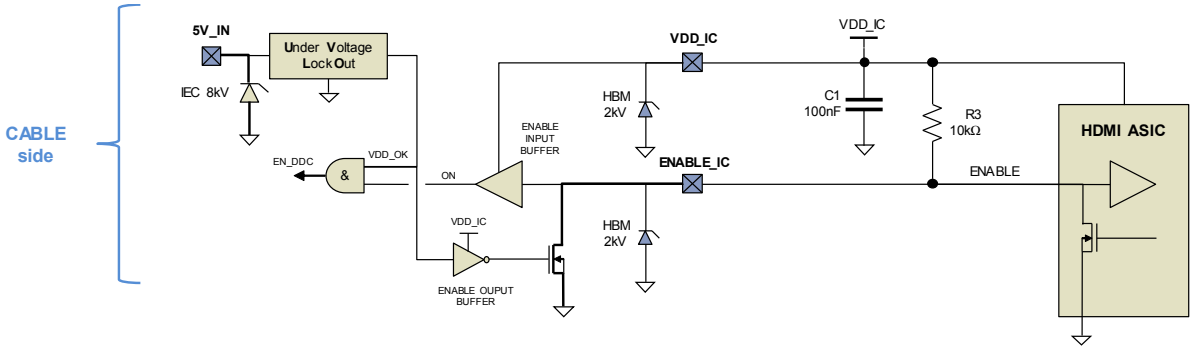
ENABLE_IC function is available to sense 5 V power supply presence from HDMI connector.

On top of 5 V sensing, Enable_IC can be used to switch off our device even if 5_{V_IN} is present.

Following conditions are required:

- The Enable function senses the 5V_IN power supply and provides a logic flag on the ENABLE_IC pin:
  - ENABLE_IC = "1" (V_{DD_IC}) : V_{5V_IN} > $V_{DD\_5V\_ON}$ ($V_{DD\_5V\_ON}$ = 3.8 V (see Table 3))
  - ENABLE_IC = "0": V_{5V_IN} > $V_{DD\_5V\_ON}$
- The ENABLE_IC pin is also an enables / disables input:
  - ENABLE_IC = "1" (V_{DD_IC}) : V_{5V_IN} > $V_{DD\_5V\_ON}$ and the circuit is enabled
  - ENABLE_IC = forced at "0": The circuit is disabled (low quiescent) whatever V_{5V_IN}

Figure 5. Enable function: Block diagram



2.3 Backdrive protection

Thanks to the innovative switch architecture, when the ENABLE_IC input is set at a low level, backdrive current is blocked when backdrive current is coming from DDC lines.

2.4 Application block diagrams

The Figure 6. Application block diagram shows an application block diagram proposal, with all possible options implemented. Thanks to ENABLE_IC signal control, the designer has then the tools to optimize the power consumption of the global application with a stand-by mode.

Figure 6. Application block diagram

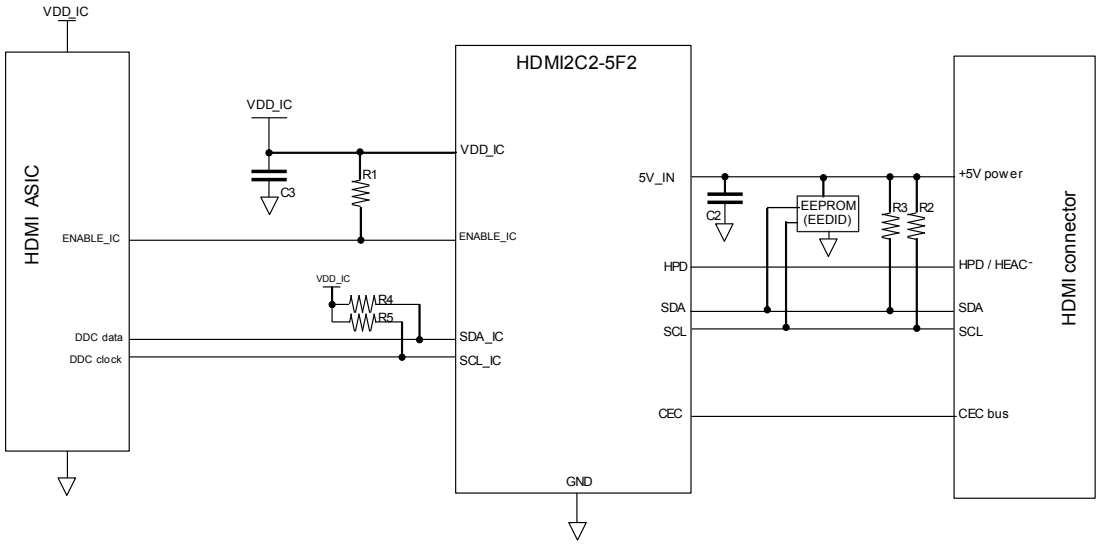


Table 1. External component recommendations

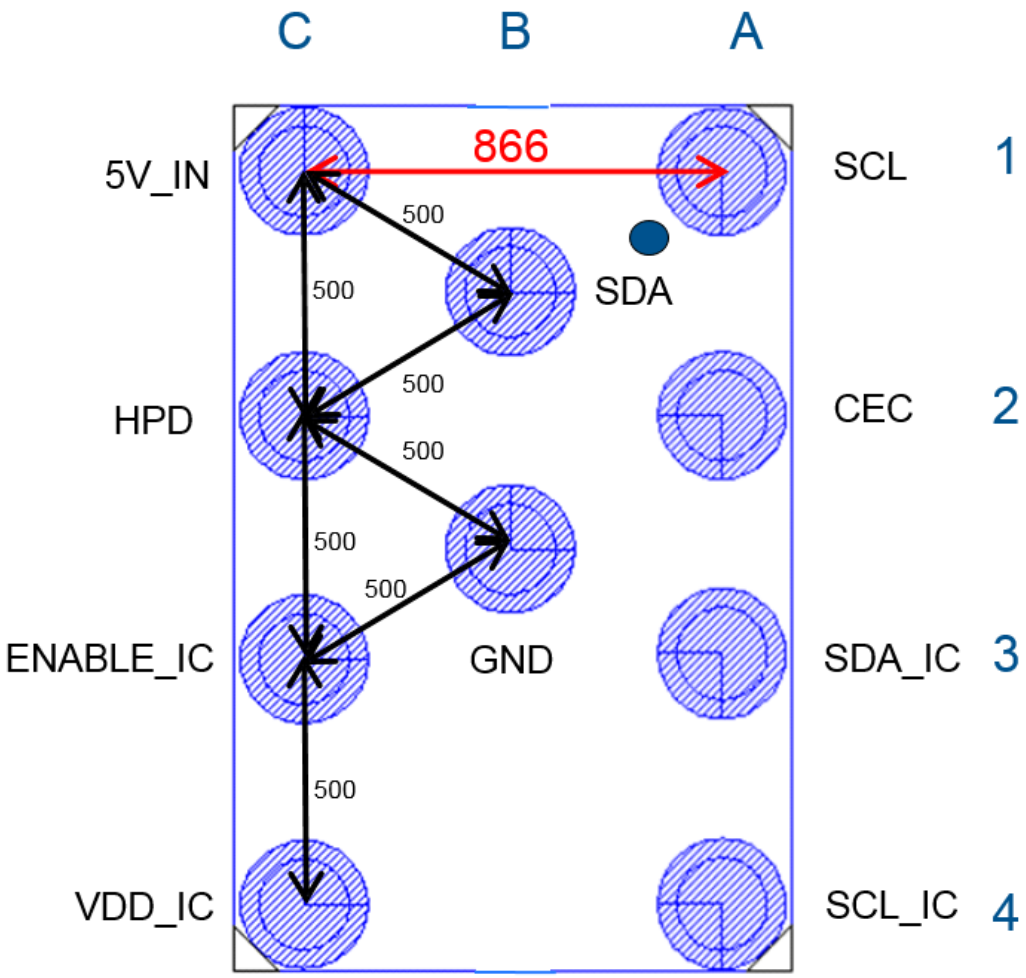
Ref.	Typical value	Comment
R1, R4 and R5	10 kΩ	Pull-up resistance on DDC bus, ASIC side, value selected to be compliant with I2C levels.
C3	100 nF	Decoupling capacitance on power supplies.
R2 and R3	47 kΩ	Pull-up resistances on DDC bus, specified by the HDMI standard.
C2	1 µF	ESD decoupling capacitance.

Note: SCL_IC, SDA_IC have to be driven with an ASIC working with open drain outputs.

Table 2. Pin description

Pin	Name	Direction	Description
A1	SCL	BI	DDC output HDMI cable side
B1	SDA	BI	DDC output HDMI cable side
C1	5V_IN	PWR	+5 V power supply HDMI cable side
A2	CEC	BI	CEC output HDMI cable side
B2	GND	PWR	Ground
C2	HDP	BI	HPD input HDMI cable side
A3	SDA_IC	BI	DDC input ASIC side
C3	ENABLE_IC	BI	Sensing of +5 V main power supply
A4	SCL_IC	BI	DDC input ASIC side
C4	VDD_IC	PWR	HDMI ASIC power supply

Figure 7. Pin numbering (bump side)



3 Electrical characteristics

Table 3. Absolute maximum ratings (limiting values)

Symbol	Parameter	Test conditions	Value	Unit
V_{PP_BUS}	ESD discharge on HDMI cable side (pins A1, B1,C1, A2 and C2) IEC 61000-4-2 level 4	Contact discharge	±8(1)	kV
		Air discharge	±15	
V_{PP_IC}	ESD discharge (all pins) HBM -JESD22-A114D, level 2	Contact discharge	±2	kV
		Air discharge	±2	
T_{STG}	Storage temperature range		-55 to +150	°C
T_{OP}	Operating temperature range		-40 to +85	°C
T_L	Maximum lead temperature		260	°C
V_{5V_IN}, V_{DD_IC}	Supply voltages		6	V
Inputs	Logical input min / max voltage range		-0.3 to 6	V

1. *With a 1 µF low ESR capacitor connected to the 5V_IN pin*

Table 4. Power supply characteristics (T_{amb} = 25 °C)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{DD_IC}	Low-voltage supply voltage		1.62		3.63	V
V_{5V_IN}	5 V supply voltage range		4.7	5.0	5.3	V
$V_{DD\_5V\_ON}$(1)	+5 V power on reset		3.5	3.8	4.1	V
$I_{QS\_5V\_IN}$	Quiescent currents on V_{5V_IN}, V_{DD_IC}	V_{DD_IC} = 1.8 V, V_{5V_IN} = 5 V, idle-state on DDC links, ENABLE_IC = 1.8 V		340	450	µA
I_{QS_IC}				41	65	µA

1. *In order to activate the DDC lines, the V_{DD_5V} has to reach the V_{5V_IN} threshold. The inputs and outputs of the bidirectional level shifters must be set to a high level after the power-on.*

Table 5. Enable electrical characteristics (T_{amb} = 25 °C, V_{DD_5V} = 5 V and $_{DD\_IC}$ = 1.8 V, unless otherwise specified)

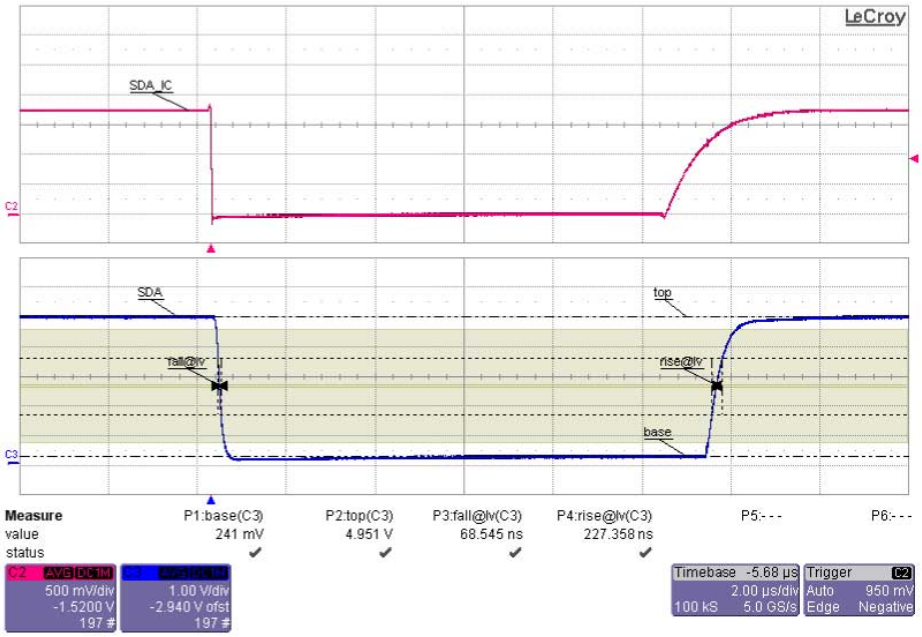
Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
I_{LEAK}	Backdrive current for SDA, SCL	ENABLE_IC=0 V_{5_IN} = 0 V, V_{DD_IC} = 0 V, Tested pin = 5 V			1	µA
$I_{QS\_5V\_OFF}$	Quiescent currents on V_{5V_IN}, V_{DD_IC}	SCL_IC, SDA_IC = V_{DD_IC}, SDA and SCL = V_{5V_IN} and ENABLE_IC = 0 V		54	70	µA
$I_{QS\_IC\_OFF}$				4	8	µA
V_{TH_EN} / V_{DD_IC}	Enable input threshold level		30	50	70	%
$V_{OL\_EN\_IC}$	Output low-level on Enable_IC PIN	Current sunk by ENABLE_IC pins is 1 mA, V_{5V_IN} < $V_{DD\_5V\_ON}$			10	%V_{DD_IC}

Table 6. DDC bus (SDA and SCL lines) line electrical characteristics (T_{amb} = 25 °C, V_{5V_IN} = 5 V, V_{DD_IC} = 1.8 V, unless otherwise specified)

Symbol	Parameter	Test conditions	Value			Unit
			Min.	Typ.	Max.	
V_{Tup_BUS}	Upward input voltage threshold on bus side				3.5	V
V_{Tdown_BUS}	Downward input voltage threshold on bus side		1.5			V
V_{HYST_BUS}	Input hysteresis on bus side		1.0		1.3	V
V_{OL_BUS}	Output low level	Current sunk by SDA and SCL pin is 3 mA			0.35	V
T_{RISE_BUS}	Output rise-time (30%-70%)	C_{BUS} = 750 pF(1), R_{UP} = 2 kΩ // 47 kΩ + 10 % (2)			500	ns
T_{FALL_BUS}	Output fall-time (70%-30%)				200	ns
V_{Tup_IC}	Upward input voltage threshold on IC side		55	60	65	$\%V_{DD\_IC}$
V_{Tdown_IC}	Downward input voltage threshold on IC side		35	40	45	$\%V_{DD\_IC}$
V_{OL_IC}	Output low-level on IC side	Current sunk by S_{DA_IC} or SCL_IC pins is 3 mA			20	$\%V_{DD\_IC}$
C_{IN_DDC}	Input capacitance on DDC link	V_{DD_5V} = 0 V, V_{DD_IC} = 0 V, f = 1 MHz, V_{OSC} = 30 mV		25	30(3)	pF

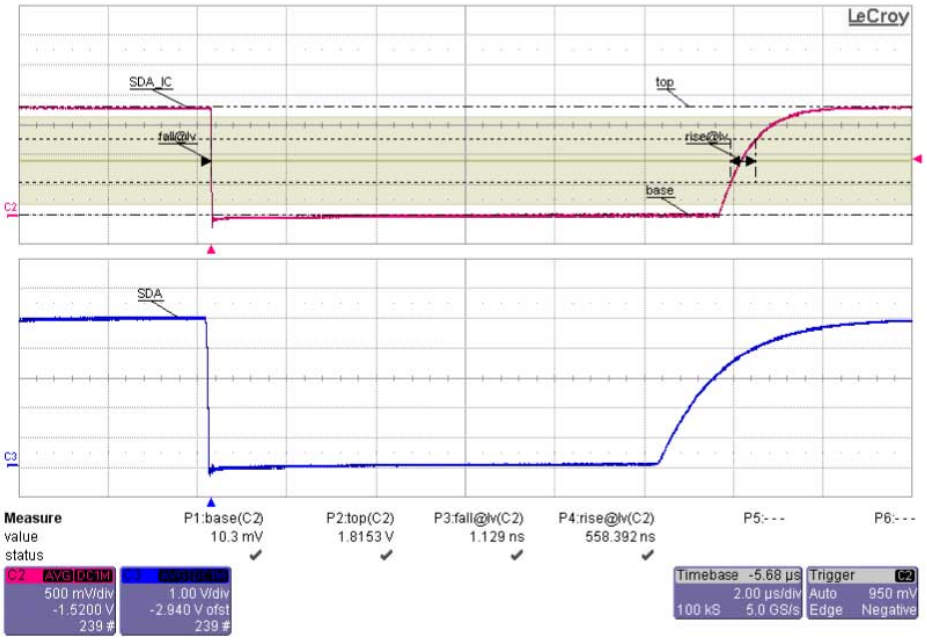
1. *Maximum load capacitance allowed on I2C entire link (cable plus connector) is 750 pF in HDMI 1.4 specification.*
2. *Two pull-up resistors in parallel (sink+source). For typical value is 47 kΩ and maximum value is 47 kΩ +10% in HDMI 1.4 specification.*
3. *Maximum capacitance allowed at connector output is 50 pF in HDMI 1.4 specification.*

Figure 8. DDC typical waveforms – communication from sink to source



Note: Measurements performed with 750 pF load, V_{DD_IC} = 1.8 V

Figure 9. DDC typical waveforms - communication from source to sink



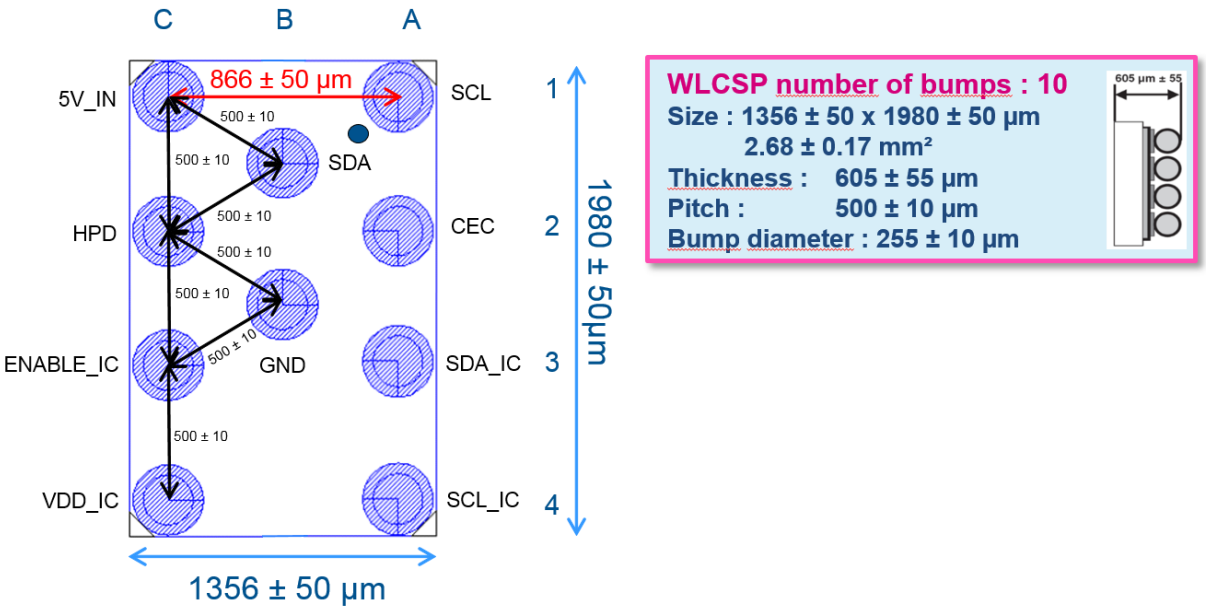
Note: Measurements performed with 750 pF load, V_{DD_IC}=1.8 V

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

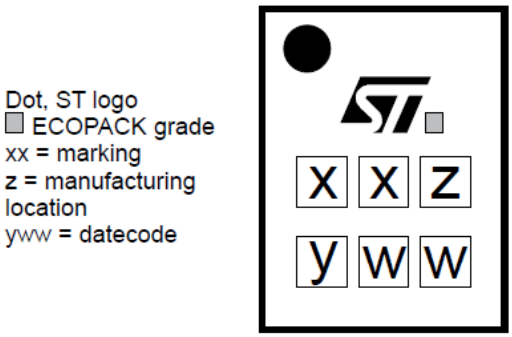
4.1 WLCSP 10 bumps package information

Figure 10. WLCSP 10 bumps package outline



4.2 WLCSP 10 bumps packing information

Figure 11. **Marking**



Note: More packing information is available in the application note:

- *AN2348 Flip-Chip: "Package description and recommendations for use"*

Figure 12. **Footprint**

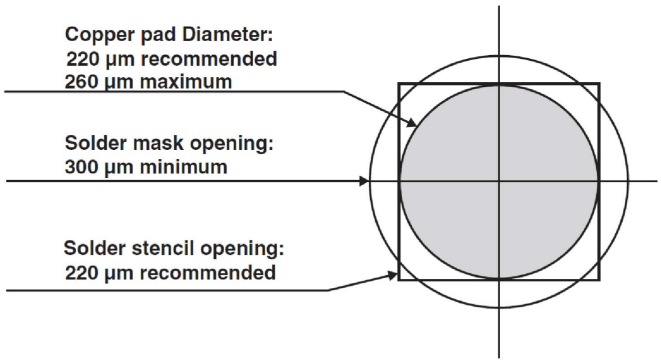
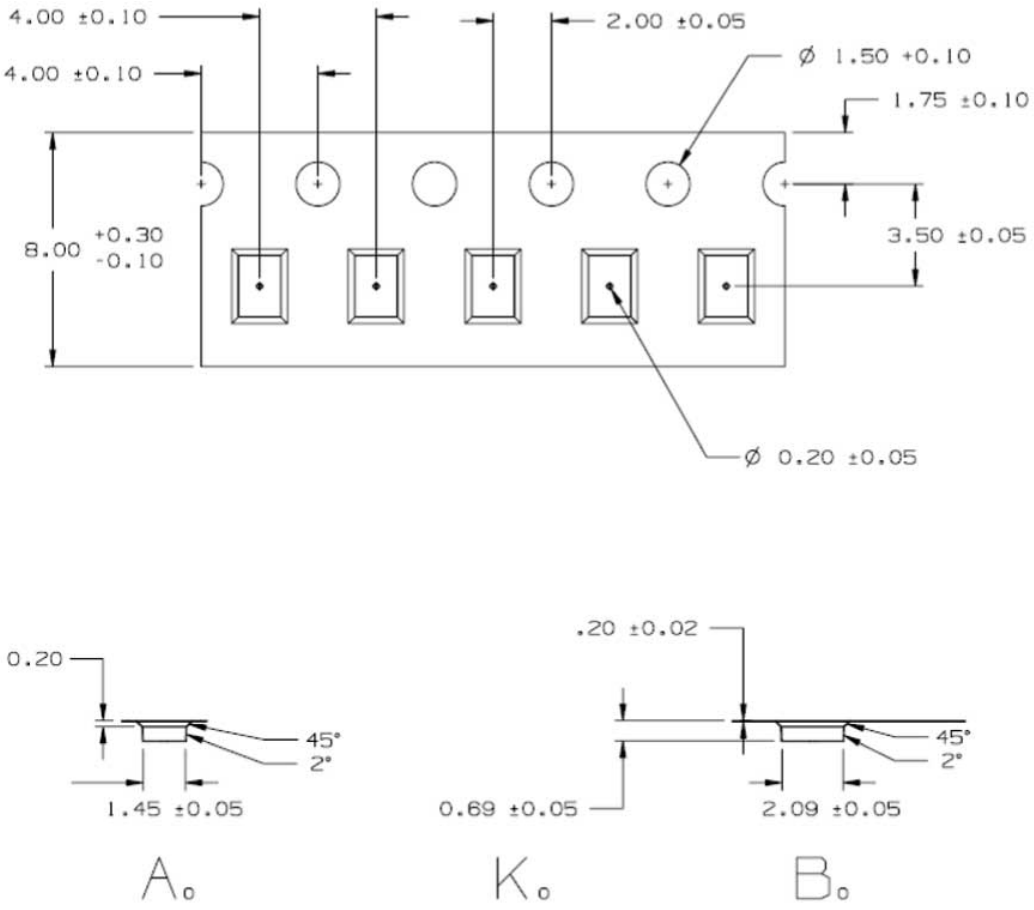


Figure 13. **WLCSP 10 bumps tape and reel specification (all dimensions in mm)**



5 Ordering information

Figure 14. **Ordering information scheme**

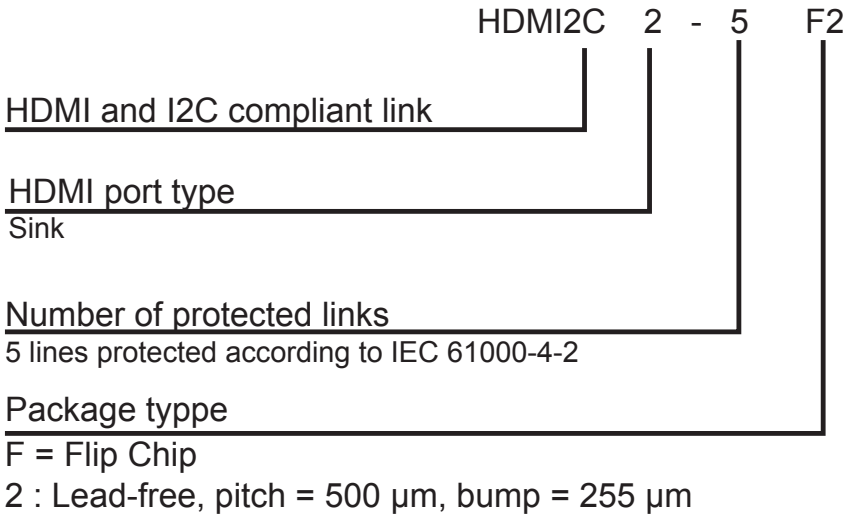


Table 7. **Ordering information**

Order code	Marking	Package	Weight	Base qty.	Delivery mode
HDMI2C2-5F2	PW	WLCSP	3.2 mg	5000	Tape and reel

Note: More information is available in AN2348 application note :

- *STMicroelectronics 400 micro-meter Flip Chip: package description and recommendation for use*

Revision history

Table 8. **Document revision history**

Date	Revision	Changes
10-Aug-2018	1	Initial release.
07-May-2019	2	Updated Section Applications.