HEF4014B-Q100

8-bit static shift register

Rev. 3 — 24 November 2021

Product data sheet

1. General description

The HEF4014B-Q100 is an 8-bit shift register with synchronous parallel enable. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{DD}.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
 - Specified from -40 °C to +85 °C
- Wide supply voltage range from 3.0 V to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Tolerant of slow clock rise and fall times
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
 - MIL-STD-833, method 3015 exceeds 2000 V
 - HBM JESD22-A114F exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0 Ω)

3. Applications

- Parallel-to-serial converter
- Serial data queueing
- General-purpose register

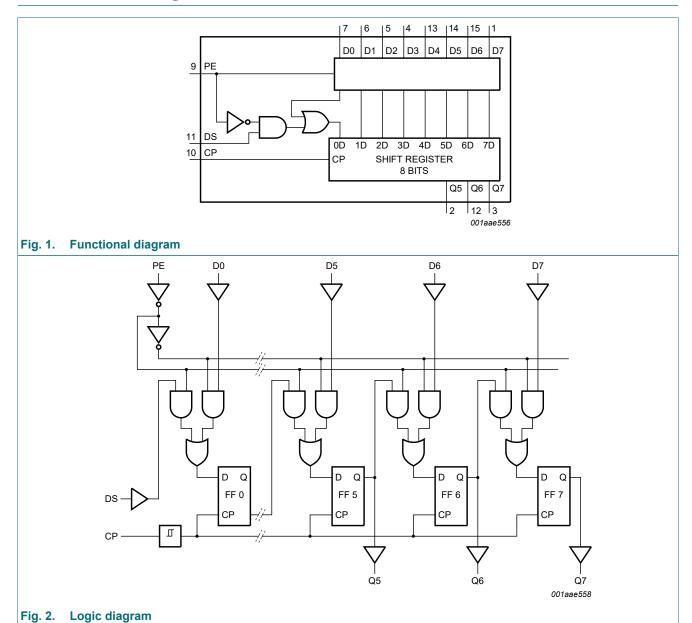
4. Ordering information

Table 1. Ordering information

Type number Package									
	Temperature range	Name	Description	Version					
HEF4014BT-Q100	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1					

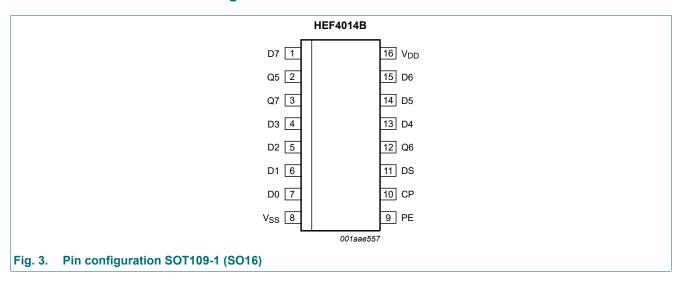


5. Functional diagram



6. Pinning information

6.1. Pinning



6.2. Pin description

Table 2. Pin description

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Symbol	Pin	Description								
Q5 to Q7	2, 12, 3	output								
D0 to D7	7, 6, 5, 4, 13, 14, 15, 1	parallel data input								
V _{SS}	8	ground supply voltage								
PE	9	parallel enable input								
СР	10	clock input (LOW-to-HIGH edge-triggered)								
DS	11	serial data input								
V_{DD}	16	supply voltage								

3 / 12

7. Functional description

Table 3. Function table

 $H = HIGH \ voltage \ level; \ L = LOW \ voltage \ level; \ X = don't \ care; \ nD = HIGH \ or \ LOW;$

 \uparrow = LOW-to-HIGH clock transition; \downarrow = HIGH-to-LOW clock transition.

Number of clock	Inputs			Outputs				
transitions	СР	DS	PE	Q5	Q6	Q7		
Serial operation								
1	1	1D	L	X	X	X		
2	↑	2D	L	X	X	Х		
3	1	3D	L	X	X	Х		
6	1	X	L	1D	X	Х		
7	1	X	L	2D	1D	X		
8	1	X	L	3D	2D	1D		
	\downarrow	X	Х	no change	no change	no change		
Parallel operation	<u> </u>	'		•		'		
1	↑	Х	Н	D5	D6	D7		
	\downarrow	X	Х	no change	no change	no change		

8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		-0.5	+18	V
I _{IK}	input clamping current	$V_{I} < -0.5 \text{ V or } V_{I} > V_{DD} + 0.5 \text{ V}$	-	±10	mΑ
VI	input voltage		-0.5	V _{DD} + 0.5	V
I _{OK}	output clamping current	V_{O} < -0.5 V or V_{O} > V_{DD} + 0.5 V	-	±10	mA
I _{I/O}	input/output current		-	±10	mΑ
I _{DD}	supply current		-	50	mΑ
T _{stg}	storage temperature		-65	+150	°C
T _{amb}	ambient temperature		-40	+85	°C
P _{tot}	total power dissipation	T_{amb} = -40 °C to +85 °C	-	500	mW
Р	power dissipation	per output	-	100	mW

9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V_{DD}	supply voltage		3	-	15	V
VI	input voltage		0	-	V_{DD}	V
T _{amb}	ambient temperature	in free air	-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{DD} = 5 V	-	-	3.75	μs/V
		V _{DD} = 10 V	-	-	0.5	µs/V
		V _{DD} = 15 V	-	-	0.08	µs/V

10. Static characteristics

Table 6. Static characteristics

 $V_{SS} = 0 \ V$; $V_I = V_{SS}$ or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T _{amb} =	-40 °C	T _{amb} =	+25 °C	T _{amb} = +85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V _{IH}	HIGH-level input voltage	I _O < 1 μA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V _{IL}	LOW-level input voltage	I _O < 1 μA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V _{OH}	HIGH-level output voltage	I _O < 1 μA	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V _{OL} LOW-level of	LOW-level output voltage	I _O < 1 μA	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I _{OH}	HIGH-level output current	V _O = 2.5 V	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		V _O = 4.6 V	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		V _O = 9.5 V	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		V _O = 13.5 V	15 V	-	-3.6	-	-3.0	-	-2.4	mA
I _{OL}	LOW-level output current	V _O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V _O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V _O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
l _l	input leakage current		15 V	-	±0.3	-	±0.3	-	±1.0	μA
I _{DD}	supply current	I _O = 0 A	5 V	-	20	-	20	-	150	μA
			10 V	-	40	-	40	-	300	μΑ
			15 V	-	80	-	80	-	600	μΑ
Cı	input capacitance		-	-	-	-	7.5	-	-	pF

11. Dynamic characteristics

Table 7. Dynamic characteristics

 T_{amb} = 25 °C; V_{SS} = 0 V.

Symbol	Parameter	Conditions	V_{DD}	Extrapolation formula [1]	Min	Тур	Max	Unit
t _{PHL}	HIGH to LOW	CP to Qn;	5 V	103 ns + (0.55 ns/pF)C _L	-	130	260	ns
	propagation delay	see Fig. 4	10 V	44 ns + (0.23 ns/pF)C _L	-	55	110	ns
			15 V	32 ns + (0.16 ns/pF)C _L	-	40	80	ns
t _{PLH}	LOW to HIGH	CP to Qn;	5 V	88 ns + (0.55 ns/pF)C _L	-	115	230	ns
	propagation delay	see Fig. 4	10 V	39 ns + (0.23 ns/pF)C _L	-	50	100	ns
			15 V	32 ns + (0.16 ns/pF)C _L	-	40	80	ns
t _t	transition time	Qn output;	5 V [2]	10 ns + (1.00 ns/pF)C _L	-	60	120	ns
		see Fig. 4	10 V	9 ns + (0.42 ns/pF)C _L	-	30	60	ns
			15 V	6 ns + (0.28 ns/pF)C _L	-	20	40	ns
t _W	pulse width		5 V		70	35	-	ns
		minimum width; see Fig. 5	10 V		30	15	-	ns
		see <u>rig. s</u>	15 V		24	12	-	ns
t _{su}	set-up time	PE to CP;	5 V		40	10	-	ns
		see Fig. 5	10 V		25	5	-	ns
			15 V		15	0	-	ns
		DS to CP;	5 V		+35	-5	-	ns
		see Fig. 5	10 V		+25	-5	-	ns
			15 V		25	0	-	ns
		Dn to CP; see Fig. 5	5 V		+35	-5	-	ns
			10 V		+25	-5	-	ns
			15 V		25	0	-	ns
t _h	hold time	PE to CP;	5 V		+25	-5	-	ns
		see Fig. 5	10 V		20	0	-	ns
			15 V		15	0	-	ns
		DS to CP;	5 V		30	15	-	ns
		see Fig. 5	10 V		20	10	-	ns
			15 V		15	7	-	ns
		Dn to CP;	5 V		30	15	-	ns
		see Fig. 5	10 V		20	10	-	ns
			15 V		15	7	-	ns
f _{clk(max)}	maximum clock	see Fig. 5	5 V		6	13	-	MHz
	frequency		10 V		15	30	-	MHz
			15 V		20	40	-	MHz

^[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

^[2] t_t is the same as t_{THL} and t_{TLH} .

Table 8. Dynamic power dissipation P_D

 P_D can be calculated from the formulas shown. V_{SS} = 0 V; t_r = t_f ≤ 20 ns; T_{amb} = 25 °C.

Symbol	Parameter	V_{DD}	Typical formula for P _D (μW)	Where:
P_{D}	dynamic power	5 V	() _ ,	f _i = input frequency in MHz;
	dissipation	10 V	Pn = 4300 x 1; + > 0, x 0, 1 x vnn	f _o = output frequency in MHz; C _L = output load capacitance in pF;
		15 V	D 40000 (E/(0 \)/ /	V_{DD} = supply voltage in V; $\sum (C_L \times f_0)$ = sum of the outputs.

11.1. Waveforms and test circuit

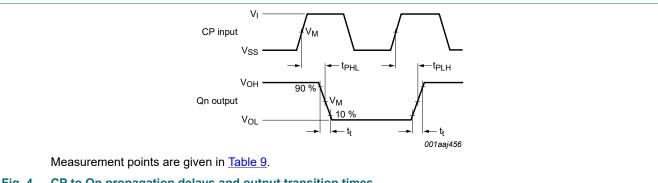
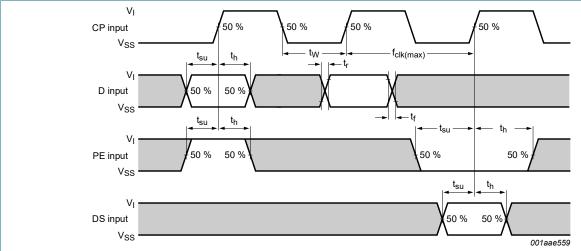


Fig. 4. CP to Qn propagation delays and output transition times

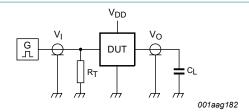


The shaded areas indicate where change is permitted for predictable output performance. Set-up and hold times are shown as positive values but may be specified as negative values. Measurement points are given in Table 9.

Minimum clock pulse width, and set-up and hold times for PE to CP, DS to CP, and D to CP Fig. 5.

Table 9. Measurement points

Supply voltage	Input	Output		
V_{DD}	V _M	V _M		
5 V to 15 V	0.5V _{DD}	0.5V _{DD}		



Test data is given in Table 10.

Definitions for test circuit:

 C_L = load capacitance including jig and probe capacitance.

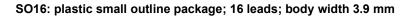
 R_T = termination resistance should be equal to the output impedance Z_o of the pulse generator.

Fig. 6. Test circuit for measuring switching times

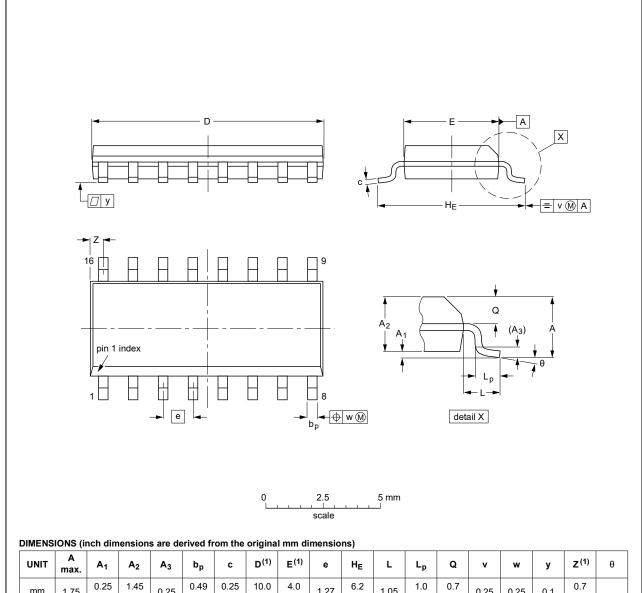
Table 10. Test data

Supply voltage	Input	Load	
V _{DD}	V _I	t _r , t _f	C _L
5 V to 15 V	V _{SS} or V _{DD}	≤ 20 ns	50 pF

12. Package outline



SOT109-1



UNIT	A max.	A ₁	A ₂	A ₃	bp	С	D ⁽¹⁾	E ⁽¹⁾	е	HE	L	Lp	Q	v	w	у	Z ⁽¹⁾	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069	0.010 0.004	0.057 0.049	0.01		0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	0°

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION		REFER	EUROPEAN	ISSUE DATE	
	IEC	JEDEC	JEITA	PROJECTION	ISSUE DATE
SOT109-1	076E07	MS-012			99-12-27 03-02-19

Fig. 7. Package outline SOT109-1 (SO16)

13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
НВМ	Human Body Model
MIL	Military
MM	Machine Model

14. Revision history

Table 12. Revision history

Table 12. Nevision instory					
Document ID	Release date	Data sheet status	Change notice	Supersedes	
HEF4014B_Q100 v.3	20211124	Product data sheet	-	HEF4014B_Q100 v.2	
Modifications:	<u>Section 1</u> and <u>Section 2</u> updated.				
HEF4014B_Q100 v.2	20181017	Product data sheet	-	HEF4014B_Q100 v.1	
Modifications:	 The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 				
HEF4014B_Q100 v.1	20130227	Product data sheet	-	-	

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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