

# HEF4043B

## Quad R/S latch with 3-state outputs

Rev. 13 — 8 December 2021

Product data sheet

### 1. General description

The HEF4043B is a quad R/S latch with 3-state outputs and common output enable input (OE). Each latch has set (nS), and reset (nR) inputs and a 3-state output (nQ). When OE is LOW, the latch outputs are in the high impedance OFF-state. OE does not affect the state of the latch. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of  $V_{DD}$ .

### 2. Features and benefits

- Wide supply voltage range from 3.0 to 15.0 V
- CMOS low power dissipation
- High noise immunity
- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Complies with JEDEC standard JESD 13-B
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V (C = 200 pF, R = 0  $\Omega$ )
- Specified from -40 °C to +85 °C

### 3. Applications

- Four-bit storage with output enable

### 4. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
HEF4043BT	-40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

## 5. Functional diagram

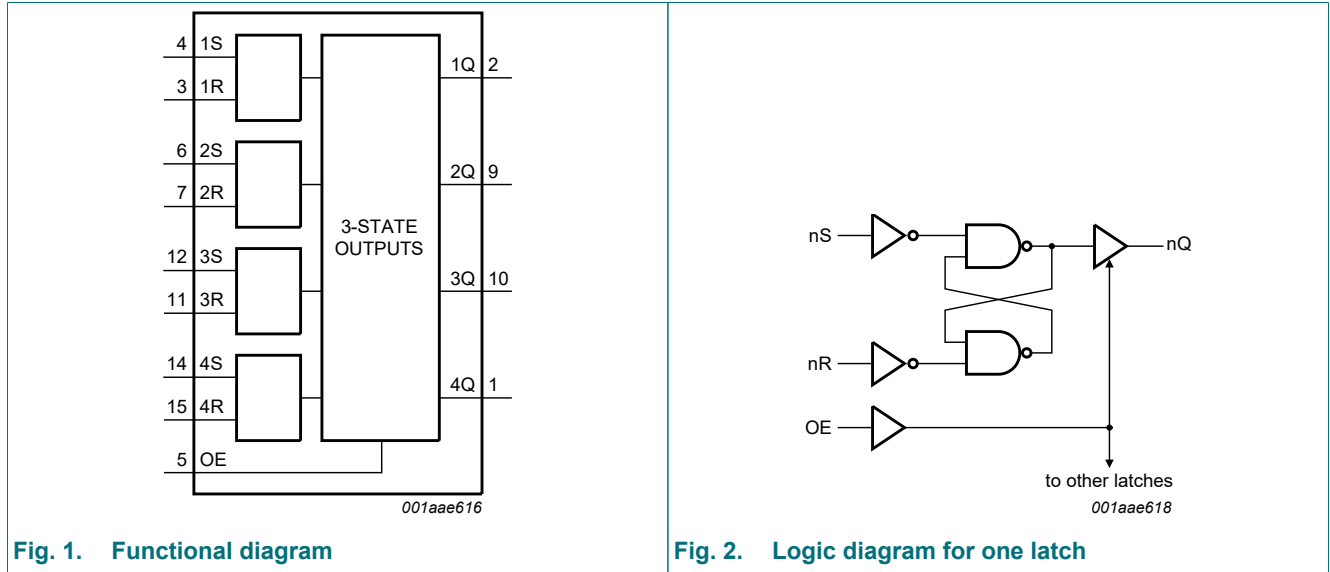


Fig. 1. Functional diagram

Fig. 2. Logic diagram for one latch

## 6. Pinning information

### 6.1. Pinning

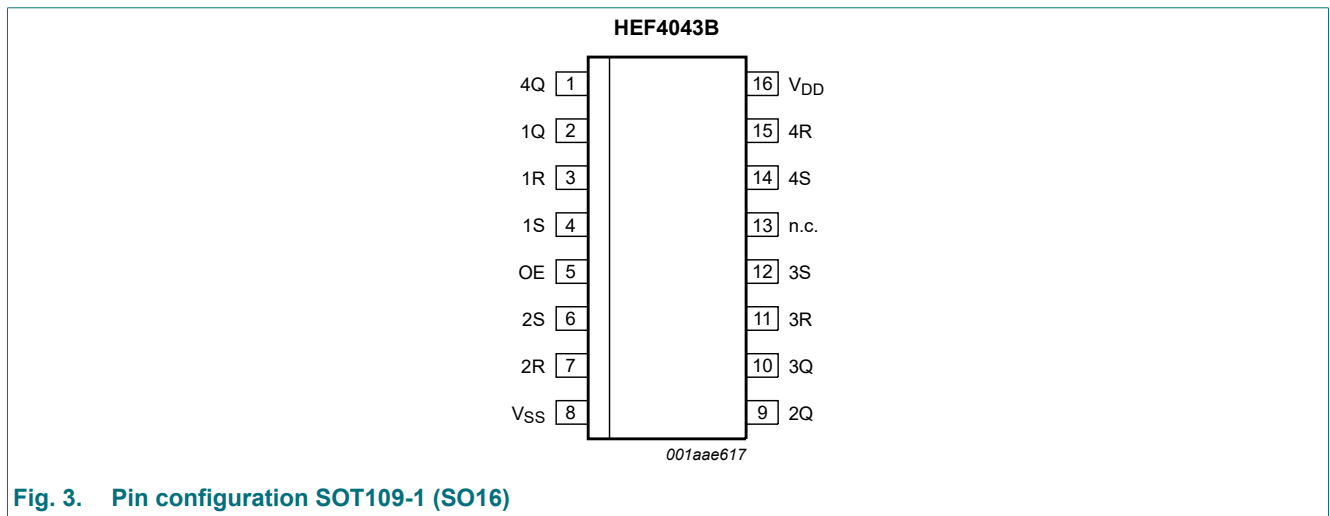


Fig. 3. Pin configuration SOT109-1 (SO16)

## 6.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1Q, 2Q, 3Q, 4Q	2, 9, 10, 1	3-state buffered latch output
1R, 2R, 3R, 4R	3, 7, 11, 15	reset input (active HIGH)
1S, 2S, 3S, 4S	4, 6, 12, 14	set input (active HIGH)
OE	5	common output enable input
V <sub>SS</sub>	8	ground supply voltage
n.c.	13	not connected
V <sub>DD</sub>	16	supply voltage

## 7. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high impedance state.

Inputs			Output
OE	nS	nR	nQ
L	X	X	Z
H	L	H	L
H	H	X	H
H	L	L	latched

## 8. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V <sub>DD</sub>	supply voltage		-0.5	+18	V
I <sub>IK</sub>	input clamping current	V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA
V <sub>I</sub>	input voltage		-0.5	V <sub>DD</sub> + 0.5	V
I <sub>OK</sub>	output clamping current	V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>DD</sub> + 0.5 V	-	±10	mA
I <sub>I/O</sub>	input/output current		-	±10	mA
I <sub>DD</sub>	supply current		-	50	mA
T <sub>stg</sub>	storage temperature		-65	+150	°C
T <sub>amb</sub>	ambient temperature		-40	+85	°C
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> -40 °C to +85 °C	-	500	mW
P	power dissipation	per output	-	100	mW

## 9. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DD}$	supply voltage		3	-	15	V
$V_I$	input voltage		0	-	$V_{DD}$	V
$T_{amb}$	ambient temperature	in free air	-40	-	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{DD} = 5\text{ V}$	-	-	3.75	$\mu\text{s/V}$
		$V_{DD} = 10\text{ V}$	-	-	0.5	$\mu\text{s/V}$
		$V_{DD} = 15\text{ V}$	-	-	0.08	$\mu\text{s/V}$

## 10. Static characteristics

Table 6. Static characteristics

$V_{SS} = 0\text{ V}$ ;  $V_I = V_{SS}$  or  $V_{DD}$  unless otherwise specified.

Symbol	Parameter	Conditions	$V_{DD}$	$T_{amb} = -40\text{ °C}$		$T_{amb} = +25\text{ °C}$		$T_{amb} = +85\text{ °C}$		Unit
				Min	Max	Min	Max	Min	Max	
$V_{IH}$	HIGH-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
$V_{IL}$	LOW-level input voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
$V_{OH}$	HIGH-level output voltage	$ I_O  < 1\ \mu\text{A}$	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
$V_{OL}$	LOW-level output voltage	$ I_O  < 1\ \mu\text{A}$	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
$I_{OH}$	HIGH-level output current	$V_O = 2.5\text{ V}$	5 V	-	-1.7	-	-1.4	-	-1.1	mA
		$V_O = 4.6\text{ V}$	5 V	-	-0.52	-	-0.44	-	-0.36	mA
		$V_O = 9.5\text{ V}$	10 V	-	-1.3	-	-1.1	-	-0.9	mA
		$V_O = 13.5\text{ V}$	15 V	-	-3.6	-	-3.0	-	-2.4	mA
$I_{OL}$	LOW-level output current	$V_O = 0.4\text{ V}$	5 V	0.52	-	0.44	-	0.36	-	mA
		$V_O = 0.5\text{ V}$	10 V	1.3	-	1.1	-	0.9	-	mA
		$V_O = 1.5\text{ V}$	15 V	3.6	-	3.0	-	2.4	-	mA
$I_I$	input leakage current		15 V	-	$\pm 0.3$	-	$\pm 0.3$	-	$\pm 1.0$	$\mu\text{A}$
$I_{OZ}$	OFF-state output current	nQ output HIGH; returned to $V_{DD}$	15 V	-	1.6	-	1.6	-	12.0	$\mu\text{A}$
		nQ output LOW; returned to $V_{SS}$	15 V	-	1.6	-	1.6	-	12.0	$\mu\text{A}$
$I_{DD}$	supply current	$I_O = 0\text{ A}$	5 V	-	20	-	20	-	150	$\mu\text{A}$
			10 V	-	40	-	40	-	300	$\mu\text{A}$
			15 V	-	80	-	80	-	600	$\mu\text{A}$
$C_I$	input capacitance			-	-	-	7.5	-	-	pF

## 11. Dynamic characteristics

**Table 7. Dynamic characteristics**

$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ °C}$  unless otherwise specified; for waveforms and test circuit see [Section 11.1](#).

Symbol	Parameter	Conditions	$V_{DD}$	Extrapolation formula [1]	Min	Typ	Max	Unit
$t_{PHL}$	HIGH to LOW propagation delay	nR → nQ; see <a href="#">Fig. 4</a>	5 V	$63\text{ ns} + (0.55\text{ ns/pF})C_L$	-	90	180	ns
			10 V	$24\text{ ns} + (0.23\text{ ns/pF})C_L$	-	35	70	ns
			15 V	$17\text{ ns} + (0.16\text{ ns/pF})C_L$	-	25	50	ns
$t_{PLH}$	LOW to HIGH propagation delay	nS → nQ; see <a href="#">Fig. 4</a>	5 V	$38\text{ ns} + (0.55\text{ ns/pF})C_L$	-	65	135	ns
			10 V	$14\text{ ns} + (0.23\text{ ns/pF})C_L$	-	25	50	ns
			15 V	$7\text{ ns} + (0.16\text{ ns/pF})C_L$	-	15	35	ns
$t_t$	transition time	nQ output; see <a href="#">Fig. 4</a>	5 V [2]	$10\text{ ns} + (1.00\text{ ns/pF})C_L$	-	60	120	ns
			10 V	$9\text{ ns} + (0.42\text{ ns/pF})C_L$	-	30	60	ns
			15 V	$6\text{ ns} + (0.28\text{ ns/pF})C_L$	-	20	40	ns
$t_{PHZ}$	HIGH to OFF-state propagation delay	OE → nQ; see <a href="#">Fig. 5</a>	5 V		-	45	90	ns
			10 V		-	20	35	ns
			15 V		-	10	25	ns
$t_{PLZ}$	LOW to OFF-state propagation delay	OE → nQ; see <a href="#">Fig. 5</a>	5 V		-	50	100	ns
			10 V		-	20	40	ns
			15 V		-	10	25	ns
$t_{PZH}$	OFF-state to HIGH propagation delay	OE → nQ; see <a href="#">Fig. 5</a>	5 V		-	25	50	ns
			10 V		-	15	30	ns
			15 V		-	10	25	ns
$t_{PZL}$	OFF-state to LOW propagation delay	OE → nQ; see <a href="#">Fig. 5</a>	5 V		-	40	80	ns
			10 V		-	20	45	ns
			15 V		-	15	35	ns
$t_w$	pulse width	nS input HIGH; minimum width; see <a href="#">Fig. 4</a>	5 V		30	15	-	ns
			10 V		20	10	-	ns
			15 V		16	8	-	ns
		nR input HIGH; minimum width; see <a href="#">Fig. 4</a>	5 V		30	15	-	ns
			10 V		20	10	-	ns
			15 V		16	8	-	ns

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown ( $C_L$  in pF).

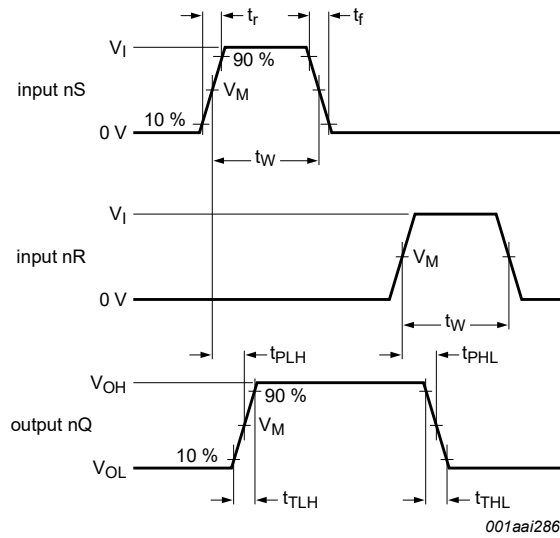
[2]  $t_t$  is the same as  $t_{THL}$  and  $t_{TLH}$ .

**Table 8. Dynamic power dissipation  $P_D$**

$P_D$  can be calculated from the formulas shown.  $V_{SS} = 0\text{ V}$ ;  $t_r = t_f \leq 20\text{ ns}$ ;  $T_{amb} = 25\text{ °C}$ .

Symbol	Parameter	$V_{DD}$	Typical formula for $P_D$ ( $\mu\text{W}$ )	where:
$P_D$	dynamic power dissipation	5 V	$P_D = 1100 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	$f_i$ = input frequency in MHz; $f_o$ = output frequency in MHz; $C_L$ = output load capacitance in pF; $V_{DD}$ = supply voltage in V; $\Sigma(f_o \times C_L)$ = sum of the outputs.
		10 V	$P_D = 4400 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	
		15 V	$P_D = 11400 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	

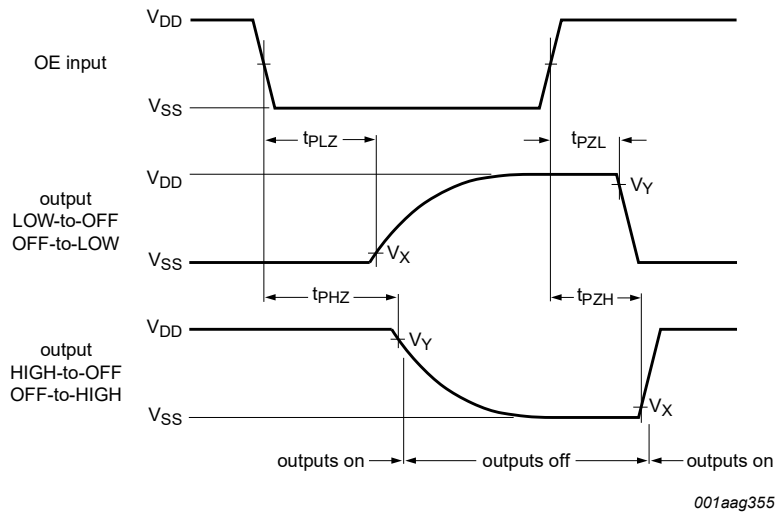
11.1. Waveforms and test circuit



Measurement points are given in Table 9.

Logic levels:  $V_{OL}$  and  $V_{OH}$  are typical output voltage levels that occur with the output load.

Fig. 4. Input minimum set (nS) and reset (nR) pulse widths, inputs nS or nR to latch output (nQ) propagation delay and nQ transition time

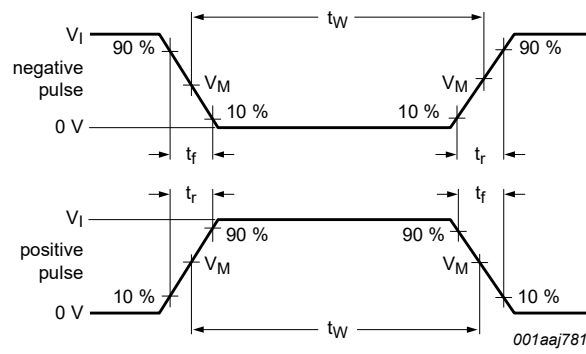


Measurement points are given in Table 9.

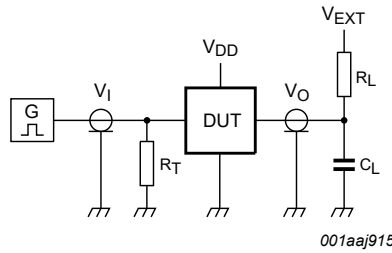
Fig. 5. Output enable (OE) to latch output (nQ) enable time ( $t_{PZH}$  and  $t_{PZH}$ ) and disable time ( $t_{PLZ}$  and  $t_{PLZ}$ )

Table 9. Measurement points

Supply voltage	Input		Output		
$V_{DD}$	$V_i$	$V_M$	$V_M$	$V_X$	$V_Y$
5 V to 15 V	$V_{DD}$ or 0 V	$0.5V_{DD}$	$0.5V_{DD}$	$0.1V_{DD}$	$0.9V_{DD}$



a. Input waveform



b. Test circuit

Test and measurement data is given in [Table 10](#).

Definitions for test circuit:

$R_L$  = Load resistance;

$C_L$  = Load capacitance including jig and probe capacitance;

$R_T$  = Termination resistance should be equal to output impedance  $Z_o$  of the pulse generator;

$V_{EXT}$  = External voltage for measuring switching times.

**Fig. 6. Test circuit for measuring switching times**

**Table 10. Test data**

Supply voltage	Input		Load		$V_{EXT}$		
$V_{DD}$	$V_I$	$t_r, t_f$	$C_L$	$R_L$	$t_{PLH}, t_{PHL}$	$t_{PLZ}, t_{PZL}$	$t_{PHZ}, t_{PZH}$
5 V to 15 V	$V_{DD}$	$\leq 20$ ns	50 pF	1 k $\Omega$	open	$V_{DD}$	GND

## 12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

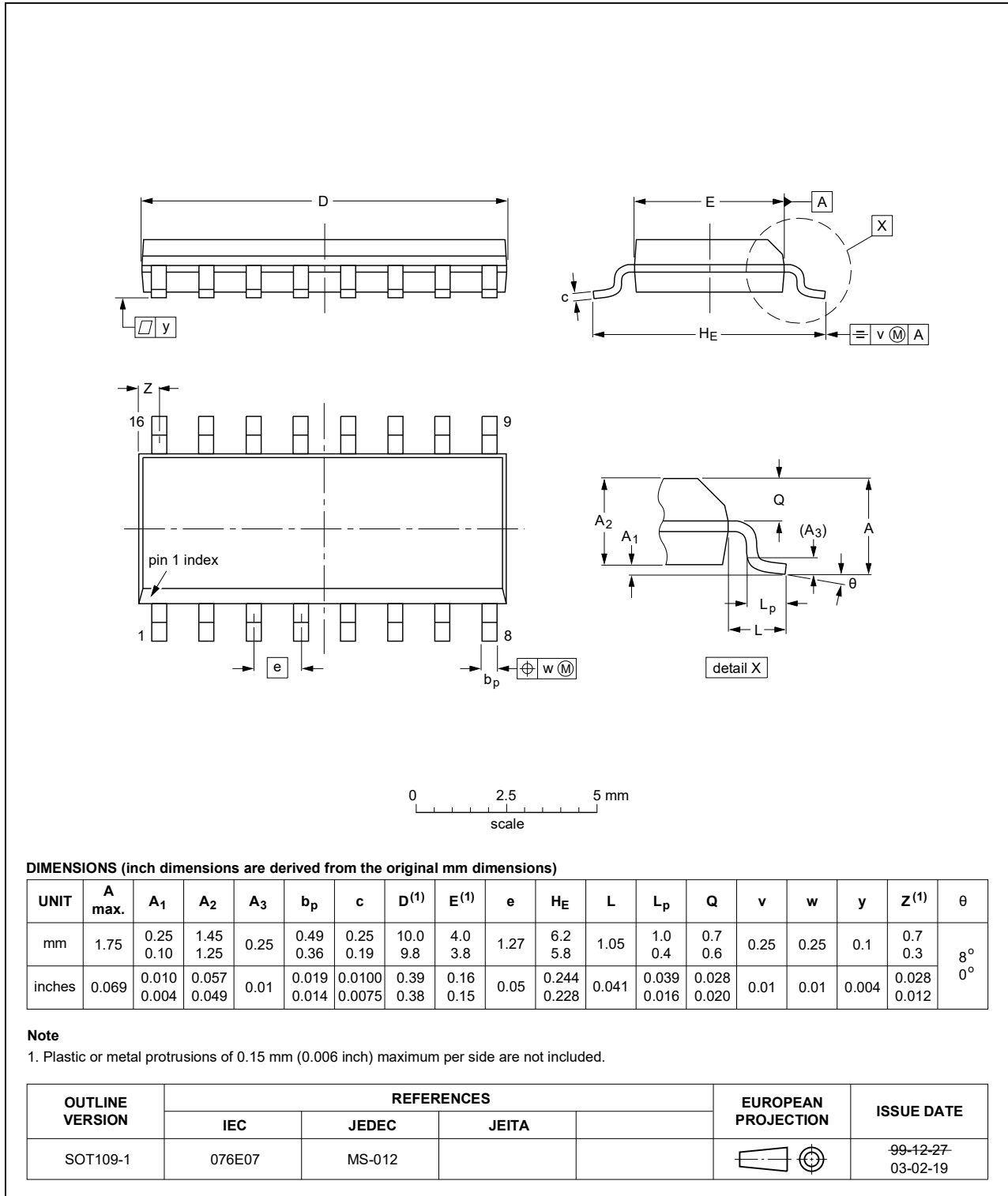


Fig. 7. Package outline SOT109-1 (SO16)



## 13. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model

## 14. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4043B v.13	20211208	Product data sheet	-	HEF4043B v.12
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Section 1</a> and <a href="#">Section 14</a> updated.</li> <li>• <a href="#">Section 13</a> added.</li> </ul>			
HEF4043B v.12	20200130	Product data sheet	-	HEF4043B v.11
Modifications:	<ul style="list-style-type: none"> <li>• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.</li> <li>• Legal texts have been adapted to the new company name where appropriate.</li> <li>• <a href="#">Fig. 2</a>: Typo corrected.</li> </ul>			
HEF4043B v.11	20160324	Product data sheet	-	HEF4043B v.10
Modifications:	<ul style="list-style-type: none"> <li>• Type number HEF4043BP (SOT38-4) removed.</li> </ul>			
HEF4043B v.10	20111118	Product data sheet	-	HEF4043B v.9
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 6</a>: <math>I_{OH}</math> minimum values changed to maximum</li> </ul>			
HEF4043B v.9	20091216	Product data sheet	-	HEF4043B v.8
HEF4043B v.8	20091127	Product data sheet	-	HEF4043B v.7
HEF4043B v.7	20090710	Product data sheet	-	HEF4043B v.6
HEF4043B v.6	20081111	Product data sheet	-	HEF4043B v.5
HEF4043B v.5	20080729	Product data sheet	-	HEF4043B v.4
HEF4043B v.4	20080710	Product data sheet	-	HEF4043B_CNV v.3
HEF4043B_CNV v.3	19950101	Product specification	-	HEF4043B_CNV v.2
HEF4043B_CNV v.2	19950101	Product specification	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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