HIP2103_4DEMO2Z

Evaluation Board

AN9853
Rev 0.00
Jul 1999

Description

The HI5x60EVAL1 evaluation board provides a quick and easy method for evaluating the HI5860/5960 (12- or 14-bit), 125MSPS high speed DACs. The board is configured so that the converter outputs differential current into a transformer circuit to form an output voltage. The amount of current out of the DAC is determined by an external resistor and either an internal or external reference voltage. The CMOS digital inputs have optional external termination resistors. The evaluation board includes a VME digital interface that is compatible with all previous Intersil D/A evaluation boards.

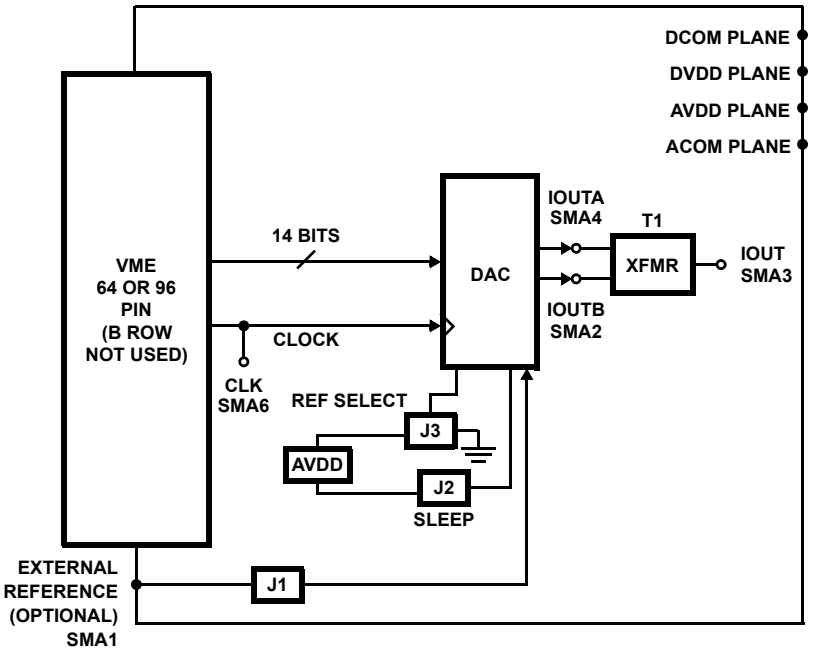
Features

- 125MSPS 12- or 14-Bit CMOS DAC
- Also Can Be Used to Evaluate the 8- and 10-Bit Versions, the HI5660 and HI5760
- Transformer-Coupled or Single-Ended SMA Outputs
- Easily Selectable Internal or External Reference

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	NUMBER OF BITS	CLOCK SPEED
HI5860SOICEVAL1	25	SOIC	12	125MHz
HI5960SOICEVAL1	25	SOIC	14	125MHz

Functional Block Diagram



Functional Descriptions

Voltage Reference

The HI5860/5960 has an internal 1.2V voltage reference with a ±40ppm/°C drift coefficient over the industrial temperature range. The REFLO pin (16) selects the reference. Access to pin 16 is provided through the center pin of Jumper J3. This jumper is labeled INT and EXT for internal or external reference. The REFIO pin (17) provides access to the internal voltage reference, or can be overdriven if the user wishes to use an external source for the reference. The internal reference was not designed to drive an external load. Notice that a 0.1µF capacitor is placed as close as possible to the REFIO pin. This capacitor is necessary for ensuring a noise free reference voltage. If the user wishes to use an external reference voltage, jumper J1 must be in place and an external voltage reference provided via SMA1, labeled 'EXT REF'. The recommended limits of the external reference are between 15mV and 1.2V. Performance of the converter can be expected to decline as the reference voltage is reduced due to the reduction in LSB current size. If the user wishes to amplitude modulate the DAC, the REFIO pin can be overdriven with a waveform. The input multiplying bandwidth of the REFIO input is approximately 1.4MHz when driving a 100mV signal into the REFIO pin, biased at $0.6V_{DC}$. The 3dB BW reduces as this amplitude is increased. It is necessary that the multiplying signal be DC offset so that the minimum and maximum peaks are positive and below 1.2V. For the external reference option, Jumper J3 must be changed so that pin 16 of the DAC is tied to the supply voltage, which is the EXT side of J3. The output current of the converter, IOUTA and IOUTB, is a function of the voltage reference used and the value of R_{SET} (or R2) on the schematic.

Output Current

The output current of the device is set by choosing R_{SET} and V_{FSADJ} such that the resultant of the following equation is less than 20mA:

$$I_{OUT} = 32 \times V_{FSADJ}/R_{SET}.$$

REFIO (PIN 17) and FSADJ (PIN 18) of the DAC are the inputs to an operational amplifier. The voltage at the FSADJ pin (V_{FSADJ}) will be approximately equal to the voltage at the REFIO pin, which will either be the value of the internal or external reference. For example, using the internal reference of (nominal) 1.2V and an R_{SET} value of 1.91kΩ results in an I_{OUT} of approximately 20mA (maximum allowed). Choose the output loading so that the Output Voltage Compliance Range is not violated (-0.3 to 1.25V). If an external reference is chosen, it should not exceed +1.2V.

The output can be configured to drive a load resistor, a transformer, an operational amplifier, or any other type of output configuration so long as the output voltage compliance range and the maximum output current are not violated.

Transformer Output

The evaluation board is configured with a transformer output configuration, shown in Figure 1. This configuration was chosen because it provides: even harmonic performance improvement due to the differential signaling; ~12.5Ω R_{EQ} loading to each output of the DAC; drive impedance of 50Ω for matching with a spectrum analyzer; and 2x voltage gain. The output of this configuration will be biased at zero volts and have an amplitude of ~500mV (V_{OUT}) when the DAC is configured to drive I_{OUTFS} of 20mA.

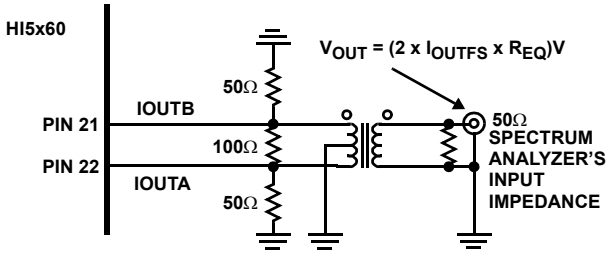


FIGURE 1.

Sleep

The converter can be put into 'sleep' mode by connecting pin 15 of the DAC to either of the converter's supply voltages. The sleep pin has an active pulldown current, so the pin can be left disconnected or be grounded for normal (awake) operation. On the evaluation board, jumper J2 is provided for controlling the sleep pin. Remove the jumper from J2 for normal operation and replace it for sleep mode.

Power Supply(ies) and Ground(s)

The user can operate from either a single supply or from dual supplies. The supplies can be at different voltages. It is important to note that the digital inputs cannot switch more than 0.3V above the digital supply voltage. The evaluation board contains two power supply connections, (analog) AV_{DD1} and (digital) DV_{DD1}, each with their own ground wire. Dual ground and power planes is the recommended configuration, with the ground planes connected at a single point near the DAC.

Digital Inputs

The DAC is designed to accept CMOS inputs. The switching voltage is approximately 1/2 of the digital power supply voltage, so reducing the power supply can make the DAC compatible to smaller levels. The digital inputs (data and clock) cannot go +0.3V higher than the digital supply voltage, else diode ESD protection can begin to turn on and performance could be degraded. The clock source can be a sine wave, with some degradation in performance. The recommended clock is a square wave.

The timing between the clock and the data will affect spectral performance and functionality. Minimum setup and hold times are specified in the datasheet to represent the point at which the DAC begins to lose bits. Optimal setup and hold times vary with the clock rate to output frequency ratio. A general rule is

that the lower the F_{CLK}/F_{OUT} ratio is, the higher the setup time should be to achieve optimum spectral behavior.

Getting Started

A summary of the external supplies, equipment, and signal sources needed to operate the board is given below:

1. +5V to +3V supply for HI5x60 DAC.
2. Pattern Generator.
3. Square wave clock source (usually part of the Pattern Generator).
4. Spectrum Analyzer or Oscilloscope for viewing the output of the converter.

Attach the evaluation board to the power supply(s). Connect the bits from the data generator to the evaluation board, preferably by using a male, 64 or 96-pin VME (Versa Module Eurocard) connector that mates with the evaluation board. Connect the clock source to the evaluation board, also preferably through the VME connector. Failure to make clean and short connections to the data input lines and clock source will result in a decrease in spectral performance.

Using a coaxial cable with the proper SMA connector, attach the output of the converter, I_{OUT}, to the measurement equipment that will be evaluating the converter's performance. Make sure that the jumpers are in their proper placement. Consult the 'Voltage Reference' section and the 'Sleep' section of this document for a definition of the jumpers' functionality.

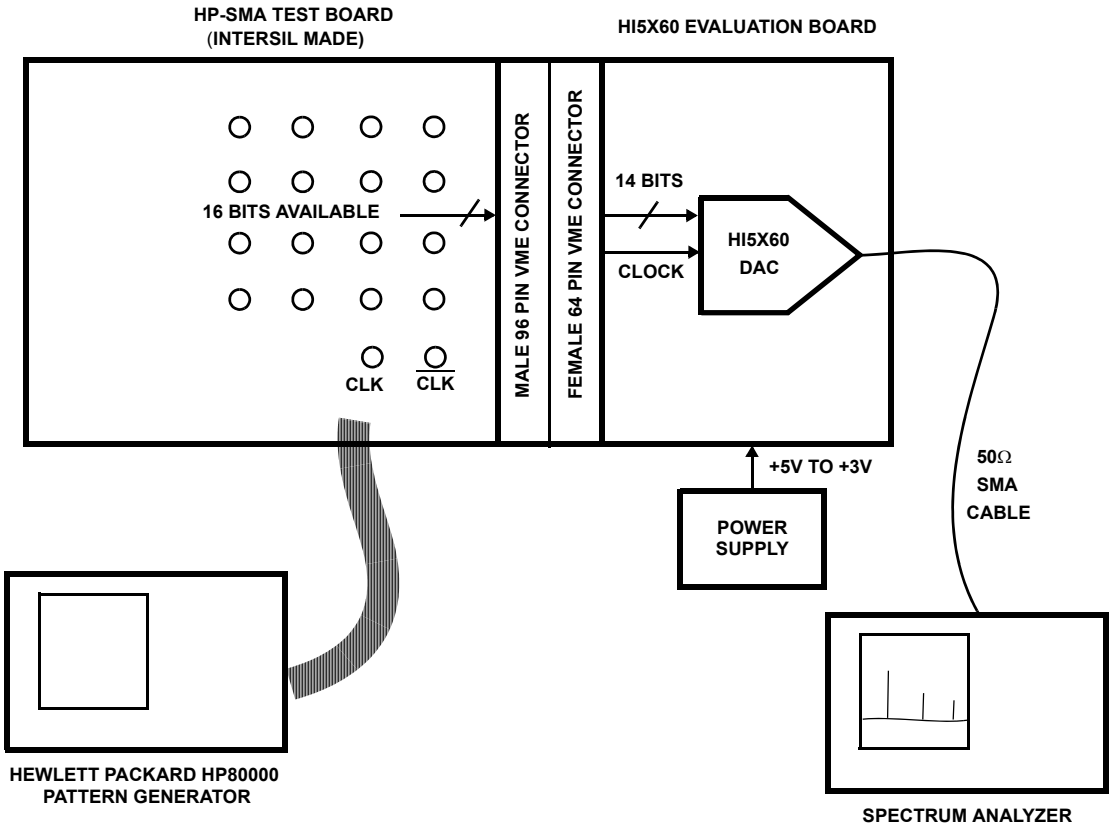


FIGURE 2. INTERSIL HI5x60 EVALUATION SYSTEM SETUP BLOCK DIAGRAM

Appendix A Description of Architecture

The segmented current source architecture has the ability to improve the converter's performance by reducing the amount of current that is switching at any one time. In traditional architectures, major transition points required the converter to switch on or off large amounts of current. In a traditional 10-bit R/2R ladder design, for example, the midscale transition required approximately equal amounts of currents switching on and off. In a segmented current source arrangement, transitions such as midscale become one in which you simply have an additional intermediate current source turning on and several minor ones turning off. In the case of the HI5760, there are 31 intermediate current segments that represent the 5 MSBs and five, binary-weighted current sources representing each of the five LSBs. See the Functional Block Diagram in the datasheet for a visual representation. To relate the midscale transition example to the HI5760, consider the following: The code 0111111111 would be represented by 15 intermediate current segments and each of the 5 LSB current sources all turned on. To transition to code 1000000000 would simply require turning off the 5 LSB current sources and turning on the next intermediate current segment, bringing the total amount of current switching at this 'major' code transition equal to the same amount switching at 30 other code transition points in the code ramp from 0 to 1023, so that the total glitch energy is distributed more evenly.

Appendix B Pin Descriptions

PIN NO.	PIN NAME	PIN DESCRIPTION
1-14	D13 (MSB) Through D0 (LSB)	For the 14-bit, HI5960, these are digital data bit-13 (most significant bit), through digital data bit-0 (least significant bit). Pins 13 and 14 are NC for the 12-bit, HI5860.
15	SLEEP	Control Pin for Power-Down Mode. Sleep mode is active high; Connect to ground for normal mode. Sleep pin has internal 20µA active pull-down current.
16	REFLO	Connect to analog ground to enable internal 1.2V reference or connect to AV_{DD} to disable internal reference.
17	REFIO	Reference voltage input if internal reference is disabled. Reference voltage output if internal reference is enabled. Use 0.1µF cap to ground unless overdriving with a waveform.
18	FSADJ	Full Scale Current Adjust. Use a resistor to ground to adjust full scale output current. Full scale output current (I_{OUTFS}) = 32 x V_{FSADJ}/R_{SET} (maximum I_{OUTFS} = 20mA).
19	COMP1	For use in reducing noise. Recommended: Connect 0.1µF from COMP1 to AV_{DD}.
20, 25	ACOM	Analog Ground.
21	IOUTB	The complementary current output of the device. Full scale output current is achieved when all input bits are set to binary 0.
22	IOUTA	Current output of the device. Full scale output current is achieved when all input bits are set to binary 1.
23	COMP2	Connect to ACOM through a 0.1µF capacitor.
24	AV_{DD}	Analog supply (+3V to +5V).
26	DCOM	Digital ground.
27	DV_{DD}	Digital supply (+3V to +5V).
28	CLK	Input for clock. Positive edge of clock latches data.

Appendix C Circuit Board Layout

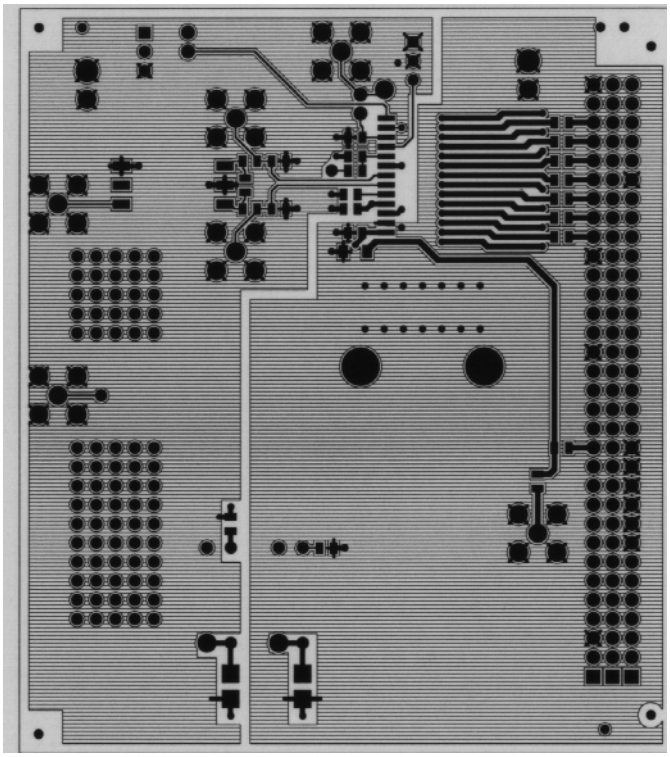


FIGURE 3. BOTTOM (LAYER 4, VIEWED FROM BOTTOM)

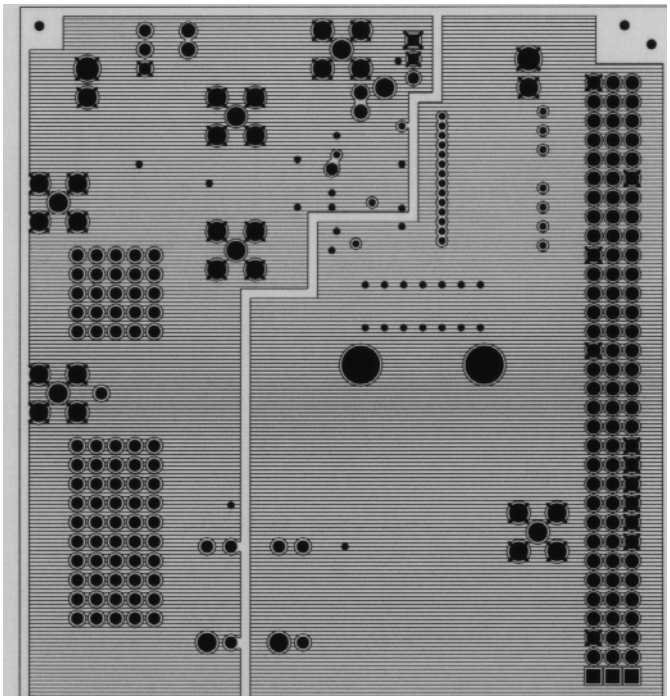


FIGURE 4. GROUND (LAYER 3, VIEWED FROM BOTTOM)

Appendix C Circuit Board Layout (Continued)

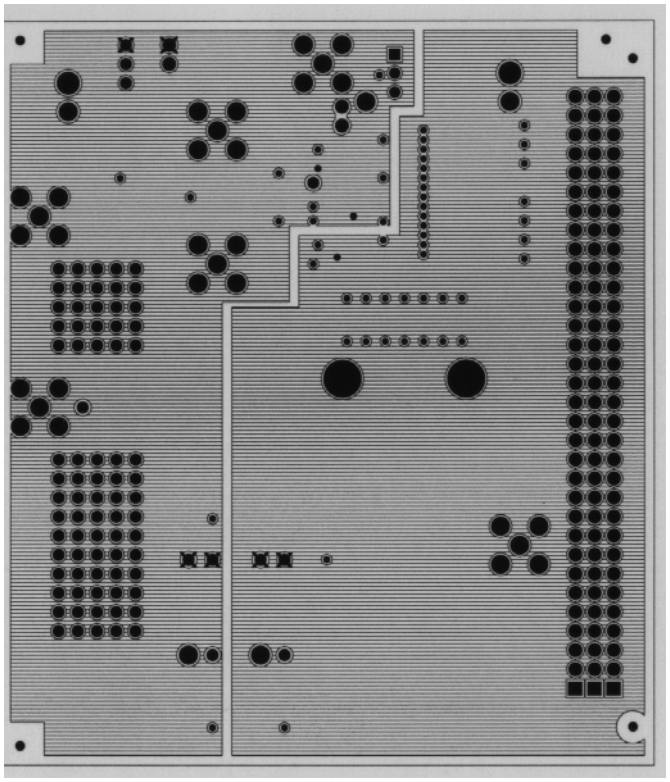


FIGURE 5. POWER (LAYER 2, VIEWED FROM BOTTOM)

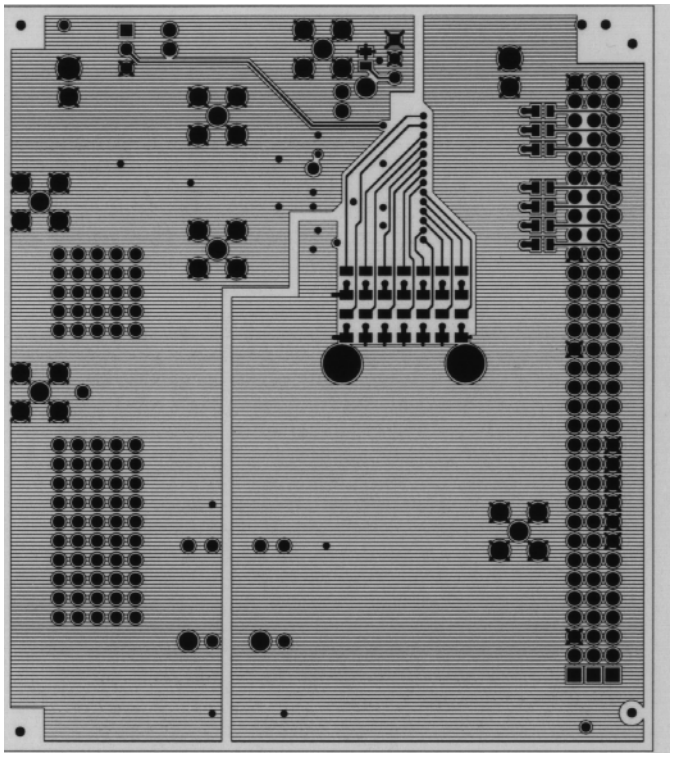


FIGURE 6. TOP SIDE (LAYER 1, VIEWED FROM BOTTOM)

Appendix D Schematic