User's Manual

HIP2211EVAL3Z

User's Manual: Evaluation Board

Industrial Analog and Power

Renesas Electronics Corporation
www.renesas.com

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HIP2211EVAL3Z

Evaluation Board

The HIP2211EVAL3Z evaluation board is designed to provide a quick and comprehensive method for evaluating the HIP2211 100V 3A source, 4A sink high-frequency half-bridge driver for driving the gates of two N-channel MOSFETs in a half-bridge configuration. Two N-channel MOSFETs (with dual footprint supporting multiple packages such as TO220 and DPAK) and an inductor-capacitor LC filter are included on the evaluation board to allow for the evaluation of a half-bridge driven load such as a synchronous buck switching regulator.

The HIP2211 half-bridge driver is offered in an 8 Ld SOIC, 8 Ld DFN, or 10 Ld DFN package (with enhanced thermal EPAD). The HIP2211EVAL3Z evaluation board is designed for the 10 Ld DFN package. The 8 Ld DFN package can fit on this board as well. It operates from a supply voltage of 6V to 18V DC with the capability of driving both the high-side and the low-side MOSFETs in a 100V half-bridge configuration.

Key Features

- 3A source and 4A sink NMOS gate drivers
- Internal level shifter and bootstrap diode for gate driver on high-side NFET
- Up to 100V high-side bootstrap reference
- 6V to 18V bias supply operation
- Fast 15ns typical propagation delay and 2ns typical propagation delay match supports up to 1MHz operation

Specifications

This board is optimized for the following operating conditions:

- V_{DD} supply: 12V nominal
- V_{BRIDGE} supply input: 0V to 60V
- PWM switching frequency: 100kHz
- Peak gate drive current: 3A source and 4A sink

Ordering Information

Part Number	Description
HIP2211EVAL3Z	HIP2211 10 Ld DFN evaluation board

Related Literature

For a full list of related documents, visit our website:

- HIP2210, HIP2211 device pages

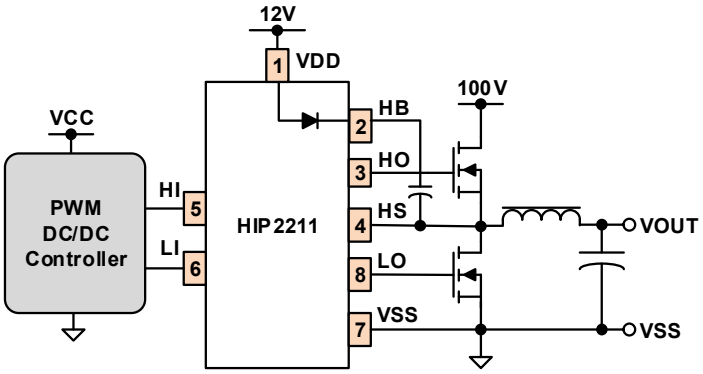

Figure 1. HIP2211 Typical Application Block Diagram

1. Functional Description

The HIP2211EVAL3Z is designed to provide a comprehensive and versatile platform for you to evaluate the functionality and prototype an application of the HIP2211 N-channel MOSFET half-bridge drivers. This evaluation board includes the MOSFETs (with dual footprint supporting for TO220 and DPAK) and an inductor-capacitor output filter for evaluating an open loop type synchronous buck DC/DC converter where the output voltage is controlled through the duty cycle of the signals into the HI/LI pins.

1.1 Operating Range

The HIP2211EVAL3Z evaluation board is designed for 60V half-bridge applications with 12V supply to bias the VDD of the HIP2211 IC. While the HIP2211 voltage ratings for the bootstrap reference and VDD supply are much higher, you should monitor the transient voltages at the switching nodes for applications exceeding 60V on the half-bridge or 12V on the driver bias to ensure they do not violate the absolute maximum ratings of the HIP2211 driver.

The inductance and capacitance value of the output LC filter is chosen for a 100kHz switching operation. You can replace these components with different values if a different switching frequency is required.

1.2 Recommended Equipment

- A power supply that can deliver 12V or higher with at least 2A source current capability
- A power supply that can deliver up to 60V to bias the half bridge
- A pulse generator with 0V to 5V logic level output and 100kHz capability
- Optional: Pulse generator with two synchronizable 0V to 5V logic level outputs and 100kHz capability
- Minimum 4-channel oscilloscope to monitor LI, HI, LO, HO, and HS signals
- Optional: A DC electronic load to draw current out of the LC filter output

1.3 Driver Logic Input

The HIP2211EVAL3Z evaluation board provides two options for the logic input of the driver (HI/LI or PWM) in an effort to relax the pulse generator requirement for evaluating the board.

If a pulse generator is used with only one square wave output available, connect it to the PWM terminal J1 on the board. This single PWM signal is converted into a HI signal and a LI signal with added RC delays.

Note: The HIP2211 HI and LI inputs do not have logic input lockout protection, so it is critical to provide adequate dead time between the two square wave inputs.

Before bringing up the HIP2211, adjust the RC delays (R3 and C30 for the HI signal, R2 and C29 for the LI signal) and verify on the oscilloscope that the required duty cycle and dead time are achieved. As an example, with a value of 3k for R2, 4k for R3, and 100pFfor C29 and C30, a 100kHz PWM input with a 30% duty cycle is converted into the HI and LI signals with an approximately 25% duty cycle and 300ns - 350ns dead time.

If two square wave outputs from a pulse generator are available, simply connect them to the HI (J9) and LI (J13) terminals. Ensure that there are no jumpers on JP1, JP2, and JP3 because the PWM to HI/LI conversion circuit on the board is not required in this case. Adequate dead time is required between the two square wave inputs.

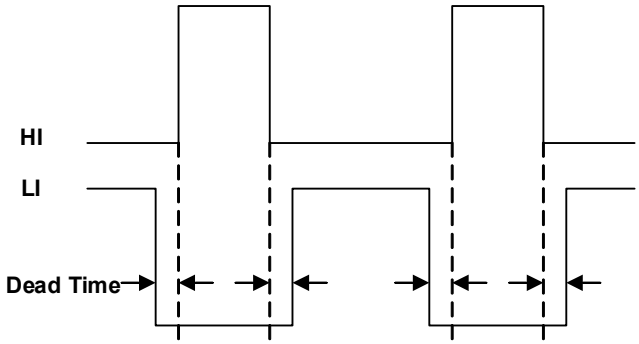

Figure 2. Dead Time

1.4 Quick Start Guide

1. Connect a 6V to 18V supply to VDD terminals on board {J2 (+) and J3 (-)}.
2. If a pulse generator with only one square wave output is used, connect it to the PWM BNC connector J1.
   Note: There is a 50Ω pull-down resistor on this terminal; therefore, the output impedance of the signal generator should be set to 50Ω to match the pull-down resistor.
   a. Place a jumper on JP3 and remove any jumpers on JP1 and JP2 before turning on the VDD power supply.
   b. Place oscilloscope probes on the converted HI and LI signals (the output of U2 and U3, respectively).
   c. Turn on the pulse generator and the VDD power supply. Adjust the RC delays (R3 and C29 for HI, R2 and C30 for LI) until the required dead time and duty cycle are achieved.
   d. Turn off the VDD power supply and the pulse generator output. Place a jumper on JP1 and JP2 and keep the jumper on JP3.
3. If a pulse generator with two square wave outputs is used, connect them to the HI (J9) and LI (J13) BNC connectors. Ensure that adequate dead time is set up between the two signals from the pulse generator. Ensure there are no jumpers on JP1, JP2 and JP3.
4. Connect a power supply capable of 60V or higher and 10A to V_BRIDGE terminals {J18(+) and J17(-)}.
5. Turn on the VDD power supply to 12V.
6. Turn on the bridge voltage supply V_BRIDGE to the required voltage (such as 48V).
7. Turn on the PWM or the HI and LI signals. Verify HO and LO outputs are switching. LO switches between GND and VDD (12V for this example) in phase with LI. HO switches between GND and VHB + V_BDRIDGE in phase with HI.

2. PCB Layout Guidelines

For best thermal performance, connect the driver EPAD to a low thermal impedance ground plane. Use as many vias as possible to connect the top layer PCB thermal land to ground planes on other PCB layers. For best electrical performance, connect the VSS and AGND pins through the EPAD to maintain a low impedance connection between the two pins.

When adjustable dead time is used, connect the resistor to the RDT pin and GND plane close to the IC to minimize ground noise from disrupting the timing performance.

Place the VDD decoupling capacitors and bootstrap capacitors close to the VDD-VSS and HB-HS pins, respectively. Use decoupling capacitors to reduce the influence of parasitic inductors. To be effective, these capacitors must also have the shortest possible lead lengths. If vias are used, connect several paralleled vias to reduce the inductance.

In addition:

- Keep power loops as short as possible by paralleling the source and return traces.
- Adding resistance might be necessary to dampen resonating parasitic circuits. In PCB designs with long leads on the LO and HO outputs, add series gate resistors on the bridge FETs to dampen the oscillations.
- Large power components (such as power FETs, electrolytic capacitors, and power resistors) have internal parasitic inductance, which cannot be eliminated. This must be accounted for in the PCB layout and circuit design.
- If you simulate your circuits, consider including parasitic components.

2.1 HIP2211EVAL3Z Evaluation Board

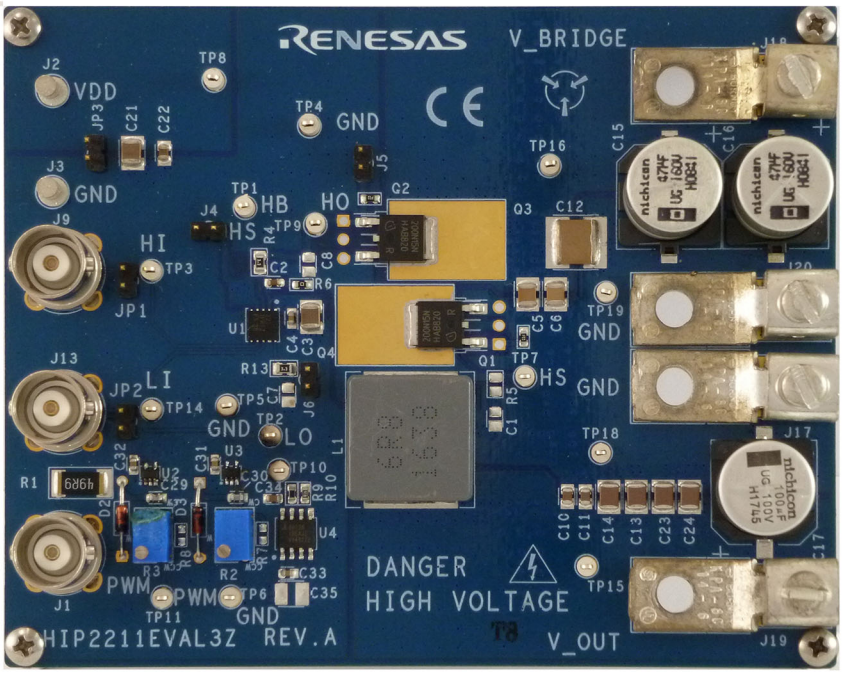

Figure 3. HIP2211EVAL3Z Evaluation Board (Top)

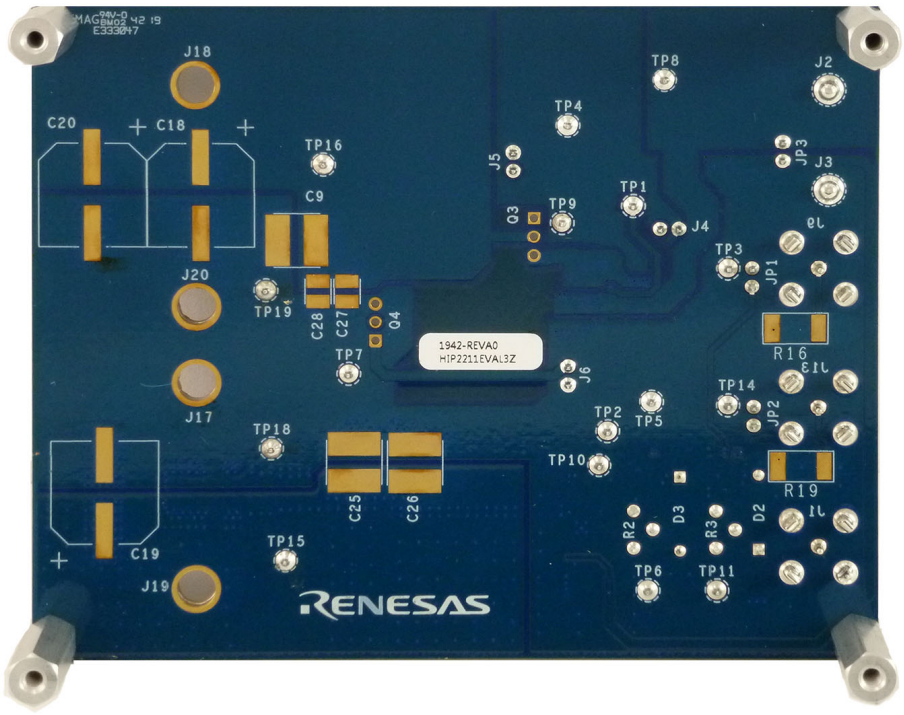

Figure 4. HIP2211EVAL3Z Evaluation Board (Bottom)

2.2 HIP2211EVAL3Z Circuit Schematic

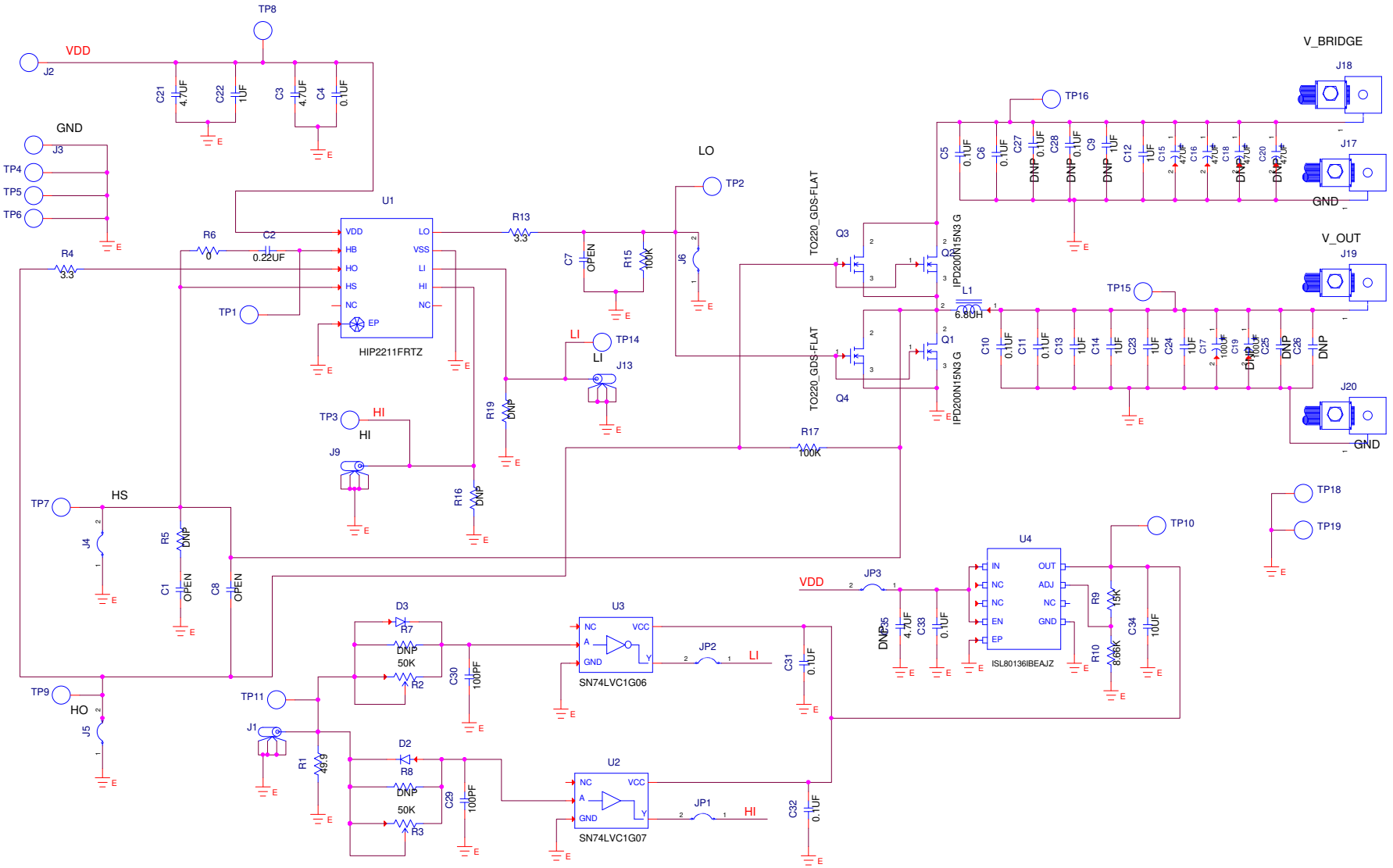

Figure 5. HIP2211EVAL3Z Schematic

2.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PWB-PCB, HIP2211EVAL2Z, REVA, ROHS	IMAGINEERING INC	HIP2211EVAL2ZREVAPCB
2	C5, C6	CAP, SMD, 1210, 0.1µF, 200V, 20%, X7R, ROHS	KEMET	C1210C104K2RAC
1	C12	CAP, SMD, 2225, 1.0µF, 200V, 10%, X7R, ROHS	KEMET	C2225C105K2RAC7800
1	C34	CAP, SMD, 0603, 10µF, 10V, 20%, X7R, ROHS	MURATA	GRM188Z71A106MA73D
1	C22	CAP, SMD, 0805, 1.0µF, 50V, 10%, X7R, ROHS	MURATA	GRM21BR71H105KA12L
2	C29, C30	CAP, SMD, 0603, 100pF, 50V, 5%, C0G, ROHS	PANASONIC	ECJ-1VC1H101J
4	C4, C31, C32, C33	CAP, SMD, 0603, 0.1µF, 50V, 10%, X7R, ROHS	AVX	06035C104KAT2A
1	C2	CAP, SMD, 0603, 0.22µF, 50V, 10%, X7R, ROHS	MURATA	GCM188R71H224KA64D (AEC-Q200)
2	C10, C11	CAP, SMD, 0805, 0.1µF, 100V, 10%, X7R, ROHS	TDK	C2012X7R2A104K
4	C13, C14, C23, C24	CAP, SMD, 1210, 1.0µF, 100V, 10%, X7R, ROHS	VENKEL	C1210X7R101-105KNE
2	C3, C21	CAP, SMD, 1210, 4.7µF, 50V, 10%, X7R, ROHS	MURATA	GRM32ER71H475KA88L
2	J2, J3	CONN-TURRET, TERMINAL POST, TH, ROHS	KEYSTONE	1514-2
3	J1, J9, J13	CONN-BNC, RECEPTACLE, TH, 4 POST, 50Ω, SILVERCONTACT, ROHS	AMPHENOL	31-5329-51RFX
16	TP1-TP11, TP14, TP15, TP16, TP18, TP19	CONN-MINI TEST POINT, VERTICAL, WHITE, ROHS	KEYSTONE	5002
6	J4, J5, J6, JP1, JP2, JP3	CONN-HEADER, 1x2, RETENTIVE, 2.54mm, 0.230x 0.120, ROHS	BERG/FCI	69190-202HLF
2	D2, D3	DIODE-SWITCHING, AXIAL, DO-35, 100V, 0.2A, 500mW, ROHS	FAIRCHILD	1N4148
1	L1	COIL-INDUCTOR, AEC-Q200, SMD, 16.9mm, 6.8µH, 20%, 19A, ROHS	BOURNS	SRP1770TA-6R8M
1	U1	IC-100V, 4A HI/LI HALF BRIDGE DRIVER, 10P, DFN, ROHS	RENESAS ELECTRONICS AMERICA	HIP2211FRTZ
1	U4	IC-40V LDO ADJ. LINEAR REGULATOR, 8P, EPSOIC, ROHS	RENESAS ELECTRONICS AMERICA	ISL80136IBEAJZ
1	U3	IC-INVERTER, 1CHANNEL, SCHMITT TRIGGER, SMD, 5P, SC-70-5, ROHS	TEXAS INSTRUMENTS	SN74LVC1G14DCKT

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	U2	IC-BUFFER, NON-INVERTING, SCHMITT TRIGGER, SMD, 5P, SC-70-5, ROHS	TEXAS INSTRUMENTS	SN74LVC1G17DCKR
2	Q1, Q2	TRANSIST-MOS, N-CHANNEL, SMD, 3P, TO-252-3, 150V, 50A, ROHS	INFINEON TECHNOLOGY	IPD200N15N3GATMA1
2	R2, R3	POT-TRIM, TH, 3P, 50k, 1/4W, 10%, 12TURN, TOPADJUST, ROHS	BOURNS	3262W-1-503LF
1	R6	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	VENKEL	CR0603-10W-000T
2	R15, R17	RES, SMD, 0603, 100k, 1/10W, 1%, TF, ROHS	VENKEL	CR0603-10W-1003FT
1	R7	RES, SMD, 0603, 15k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF1502V
1	R8	RES, SMD, 0603, 8.66k, 1/10W, 1%, TF, ROHS	PANASONIC	ERJ-3EKF8661V
2	R4, R13	RES, SMD, 0805, 3.3Ω, 1/8W, 1%, TF, ROHS	PANASONIC	ERJ-6RQF3R3V
1	R1	RES, SMD, 2512, 49.9Ω, 1W, 1%, TF, ROHS	VISHAY	CRCW251249R9FKEG(PbFREE)
4	J17, J18, J19, J20	HDWARE, MTG, CABLE TERMINAL, 6-14AWG, LUG&SCREW, ROHS	BERG/FCI	KPA8CTP
1	C17	CAP, SMD, 12.5x16, 100µF, 100V, 20%, ALUM.ELEC., ROHS	NICHICON	UUG2A101MNQ1MS
2	C15, C16	CAP, SMD, 13.6mm, 47µF, 160V, 20%, ALUM.ELEC., ROHS	NICHICON	UUG2C470MNL1MS

2.4 Board Layout

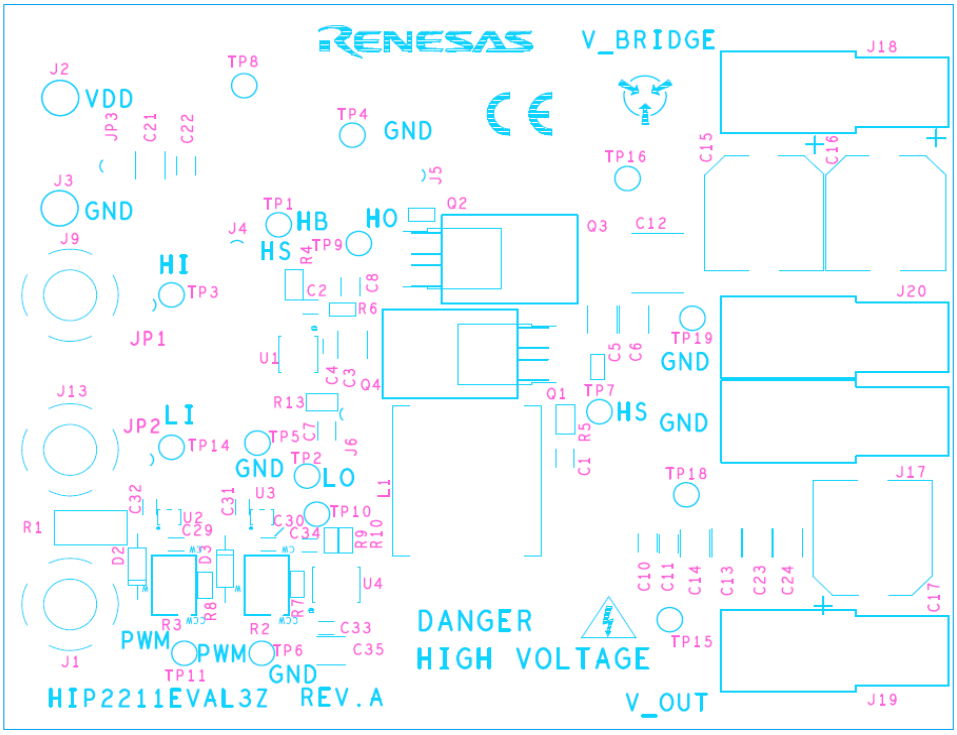

Figure 6. Silkscreen Top Layer

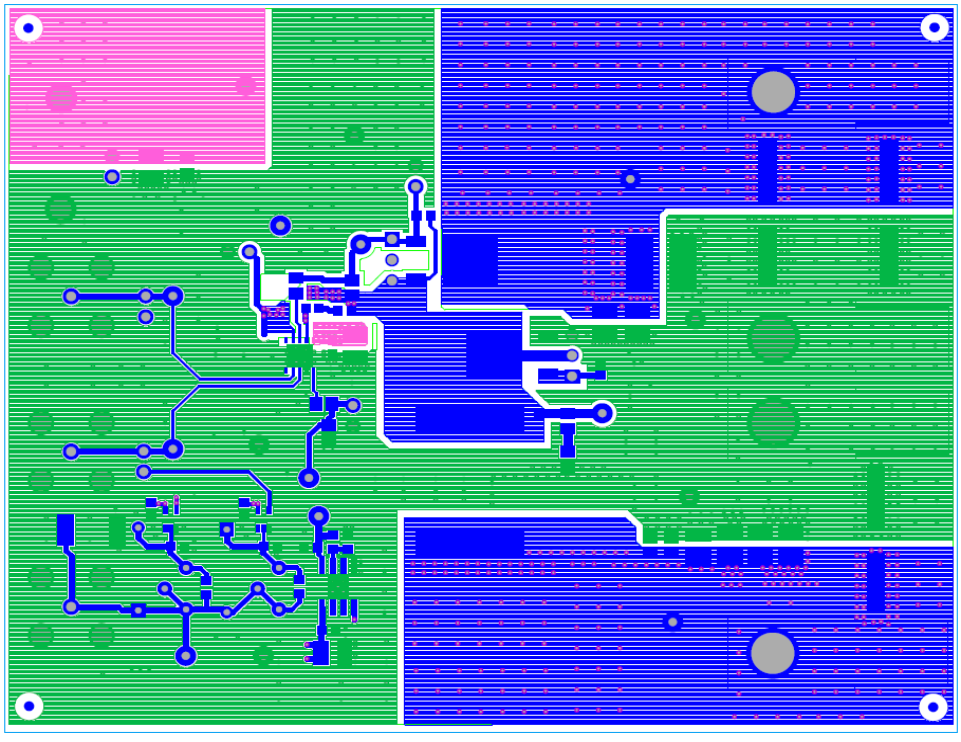

Figure 7. Layer 1

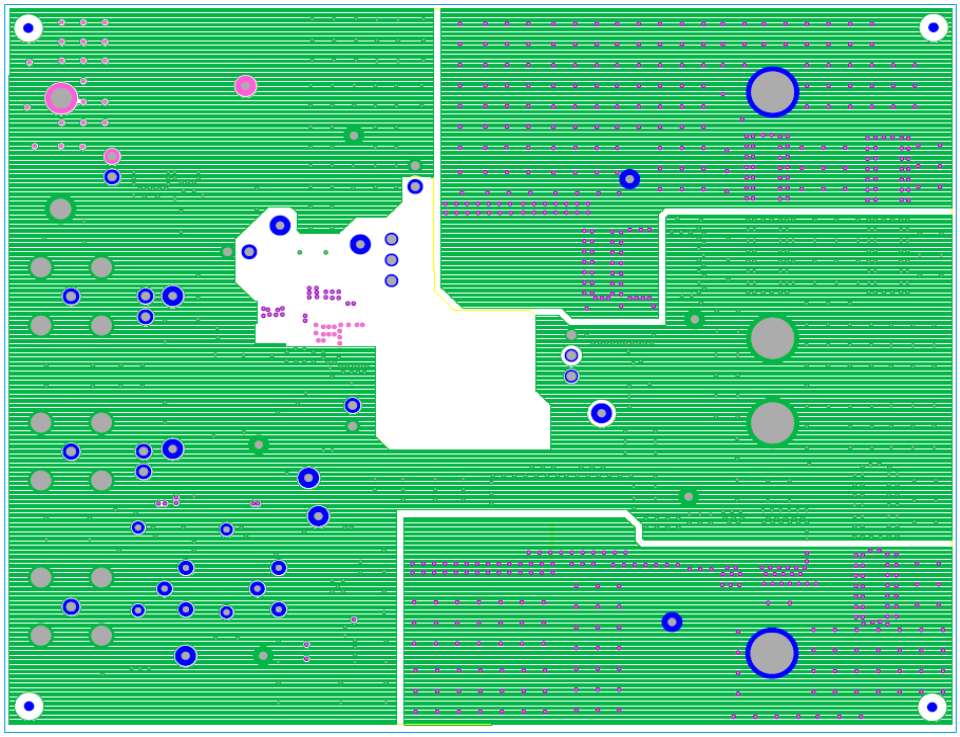

Figure 8. Layer 2

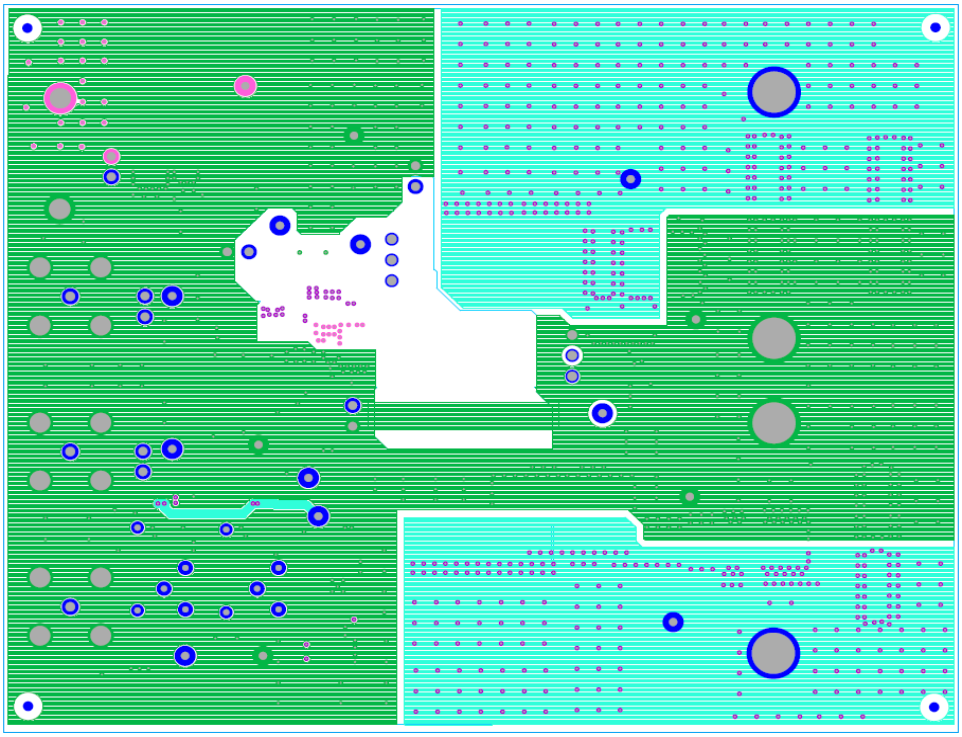

Figure 9. Layer 3

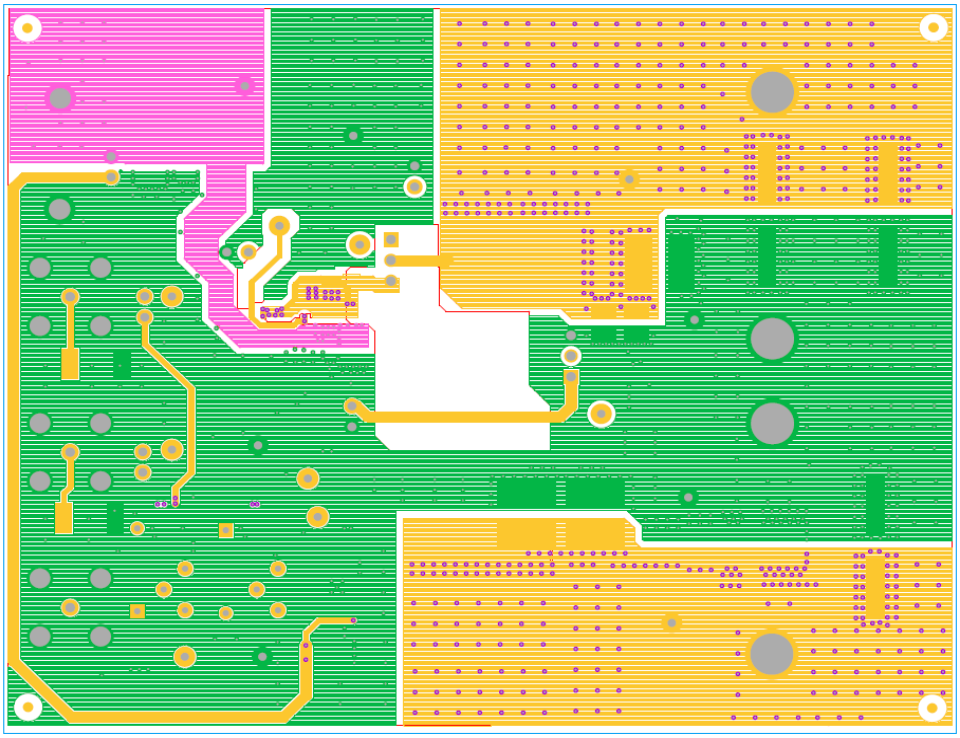

Figure 10. Layer 4

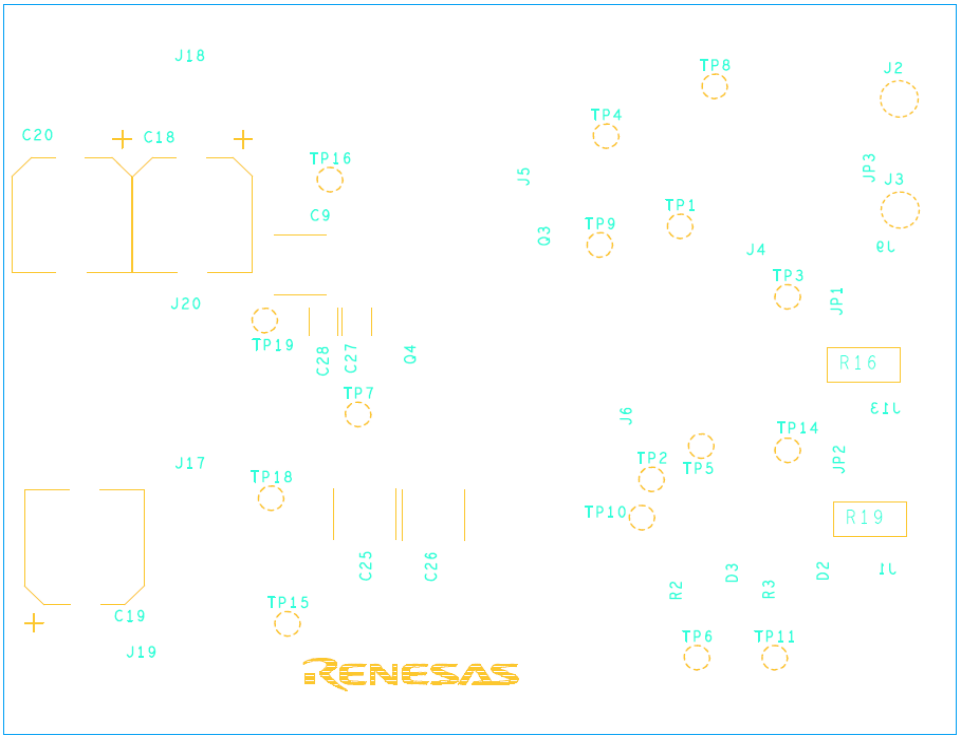

Figure 11. Silkscreen Bottom Layer

3. Typical Performance Curves

V_{DD} = 12V, V_{BRIDGE} = 48V, PWM = 100kHz square wave, 0V to 5V, 35% duty cycle, R_2 = 3.68k, R_3 = 6.1k, C29 = C30 = 100pF, T_A = +25°C

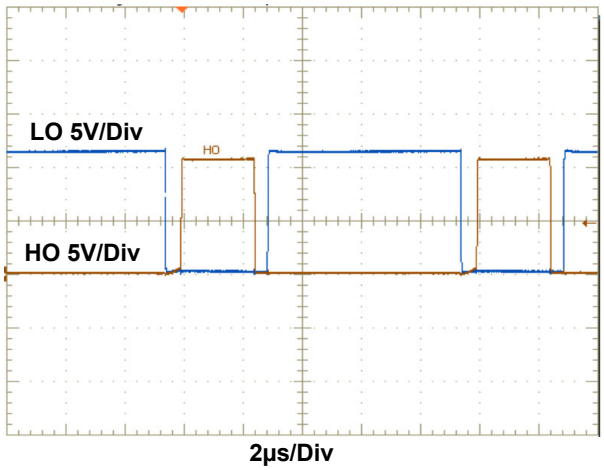

Figure 12. LO and HO when V_BRIDGE is Off

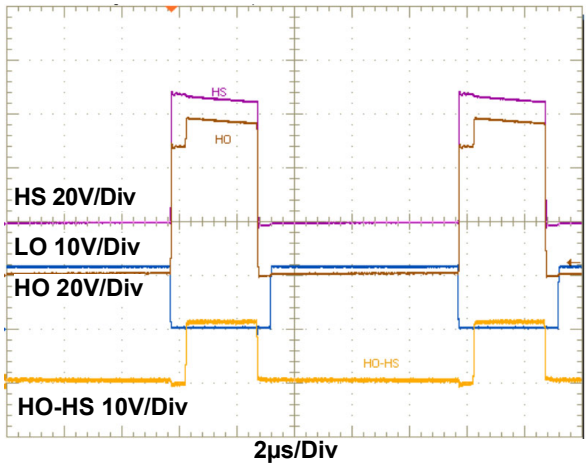

Figure 13. Driving Half Bridge at 48V

4. Revision History

Rev.	Date	Description
1.00	Jan.27.20	Initial release

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