0.5 GHz to 80 GHz, GaAs, HEMT, MMIC, Low Noise Wideband Amplifier

Data Sheet **HMC-AUH312**

FEATURES

Small signal gain: >8 dB
80 GHz distributed amplifier
Configurable with or without bias tees for V_{DD} and $V_{GG}1$ bias
Low power dissipation
- **300 mW with bias tee at V_{DD} = 5 V**
- **360 mW without bias tee at V_{DD} = 6 V**
- **480 mW without bias tee at V_{DD} = 8 V**

Die size: 1.2 mm × 1.0 mm × 0.1 mm

APPLICATIONS

Fiber optic modulator drivers
Fiber optic photoreceiver postamplifiers
Low noise amplifier for test and measurement equipment
Point to point and point to multipoint radios
Wideband communication and surveillance systems
Radar warning receivers

FUNCTIONAL BLOCK DIAGRAM

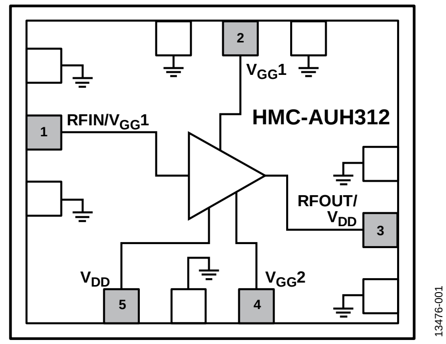

Figure 1.

GENERAL DESCRIPTION

The HMC-AUH312 is a gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), HEMT, low noise, wideband amplifier die that operates between 500 MHz and 80 GHz, providing a typical 3 dB bandwidth of 80 GHz. The amplifier provides 10 dB of small signal gain and a maximum output amplitude of 2.5 V p-p, which makes it ideal for use in broadband wireless, fiber optic communications, and test equipment applications.

The amplifier die occupies 1.2 mm × 1.0 mm, facilitating easy integration into a multichip module (MCM). The HMC-AUH312 can be used with or without a bias tee, and requires off-chip blocking components and bypass capacitors for the dc supply lines. Adjustable gate voltages allow for gain adjustment.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700

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REVISION HISTORY

11/2019—Rev. E to Rev. F

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11/2015—v04.0615 to Rev. E

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

Updated Format ... Universal
Changes to Title of Data Sheet ... Page 1
Change Vg1 to $V_{GG}1$, Vg2 to $V_{GG}2$, Vd to V_{DD}, RFIN to RFIN/$V_{GG}1$, and RFOUT to RFOUT/V_{DD} ... Throughout
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SPECIFICATIONS

T_A = 25°C, V_{DD} = 8 V, $V_{GG}2$ = 1.8 V, I_{DD} = 60 mA, unless otherwise noted.

0.5 GHz to 60 GHz FREQUENCY RANGE

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		0.5		60	GHz	
GAIN		8	10		dB	
RETURN LOSS						
Input			15		dB	
Output			17		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB		13.5		dBm	
Saturated Output Power	P_{SAT}		16		dBm	
Output Third-Order Intercept	IP3		23		dBm	
NOISE FIGURE			5		dB	
SUPPLY CURRENT	I_{DD}		60		mA	V_{DD} = 8 V, adjust $V_{GG}1$ between −2 V and 0 V to achieve I_{DD} = 60 mA typical

60 GHz TO 80 GHz FREQUENCY RANGE

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE		60		80	GHz	
GAIN			9		dB	
RETURN LOSS						
Input			10		dB	
Output			15		dB	
OUTPUT						
Output Power for 1 dB Compression	P1dB		13		dBm	
Saturated Output Power	P_{SAT}		15		dBm	
Output Third-Order Intercept	IP3		22		dBm	
NOISE FIGURE					dB	
SUPPLY CURRENT	I_{DD}		60		mA	V_{DD} = 8 V, adjust $V_{GG}1$ between −2 V and 0 V to achieve I_{DD} = 60 mA typical

RECOMMENDED OPERATING CONDITIONS

Table 3. Recommended Operating Conditions with Bias Tee

Parameter	Symbol	Min	Typ	Max	Unit
POSITIVE SUPPLY					
Voltage		3	5	6	V
Current			60	80	mA
GATE VOLTAGE					
Gate Voltage 1	$V_{GG}1$	−1		+0.3	V
Gate Voltage 2	$V_{GG}2$		1.8		V
POWER DISSIPATION			300		mW
RF INPUT POWER				4	dBm
OPERATING TEMPERATURE		−55	+25	+85	°C

Table 4. Recommended Operating Conditions Without Bias Tee

Parameter	Symbol	Min	Typ	Max	Unit
POSITIVE SUPPLY					
Voltage		6	8	8.25	V
Current			60	65	mA
GATE VOLTAGE					
Gate Voltage 1	$V_{GG}1$	−1		+0.5	V
Gate Voltage 2	$V_{GG}2$	1	1.8		V
POWER DISSIPATION					
V_{DD} = 6 V			360		mW
V_{DD} = 8 V			480		mW
RF INPUT POWER				4	dBm
OPERATING TEMPERATURE		−55	+25	+85	°C

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Drain Bias Voltage with Bias Tee (V_{DD})	7 V dc
Drain Bias Voltage Without Bias Tee (V_{DD})	8.25 V dc
Gain Bias Voltage ($V_{GG}1$)	0.5 V
Gain Bias Voltage ($V_{GG}2$)	2 V
RF Input Power	10 dBm
Channel Temperature	180°C
Storage Temperature Range	−40°C to +85°C
Operating Temperature Range	−55°C to +85°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

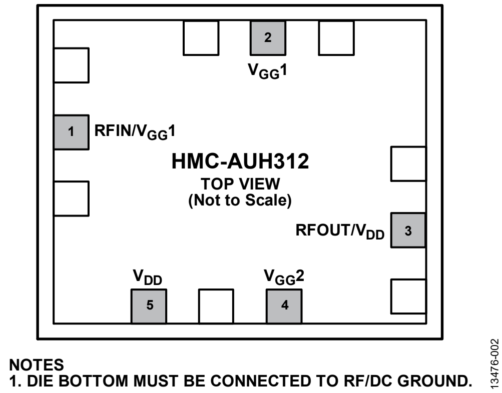

Figure 2. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$RFIN/V_{GG}1$	RF Input/Gate Bias for Alternate Circuit for the Input Stage. This is a multifunction pin where the $V_{GG}1$ function is used in the alternate circuit only for biasing (see Figure 23 and Figure 25 for the alternate applications circuit and alternate assembly drawings, respectively). This pin is dc-coupled and requires a dc block. See Figure 3 for the interface schematic.
2, 4	$V_{GG}1$, $V_{GG}2$	Gate Control for Amplifier. For more information about assembly and required assembly components, see Figure 24. See Figure 4 for the interface schematic.
3	$RFOUT/V_{DD}$	RF Output/DC Bias for Alternate Application Circuit for the Output Stage. This is a multifunction pin where the V_{DD} function is used in the alternate application circuit only for biasing (see Figure 23 and Figure 25 for the alternate applications circuit and alternate assembly diagram, respectively). This pin is dc-coupled and requires a dc block. See Figure 5 for the interface schematic.
5	V_{DD}	Supply Voltage for Application Circuit. See Figure 22 and Figure 24 for the external components. See Figure 6 for the interface schematic.
	GND	Die Bottom (Ground). The die bottom must be connected to RF/dc ground. See Figure 7 for the interface schematic.

INTERFACE SCHEMATICS

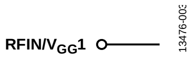

Figure 3. RFIN/V_{GG}1 Interface

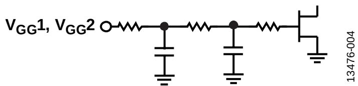

Figure 4. V_{GG}1 and V_{GG}2 Interface

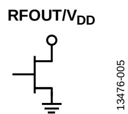

Figure 5. RFOUT/V_{DD} Interface

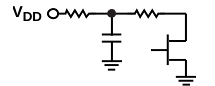

Figure 6. V_{DD} Interface

Figure 7. GND Interface

TYPICAL PERFORMANCE CHARACTERISTICS

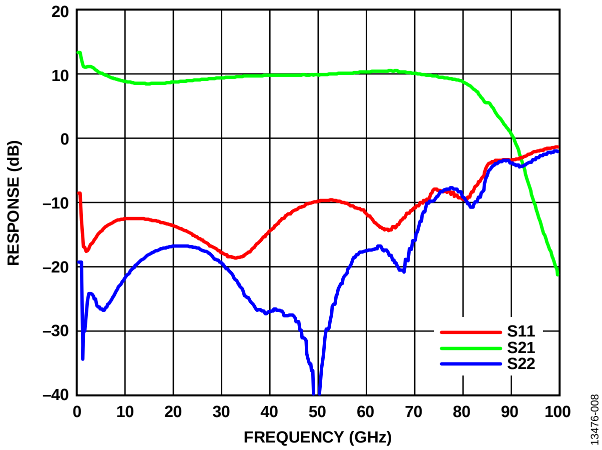

Figure 8. Gain and Return Loss

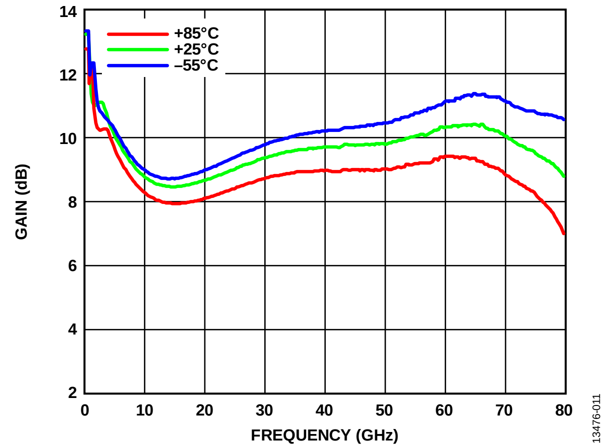

Figure 11. Gain vs. Frequency at Various Temperatures

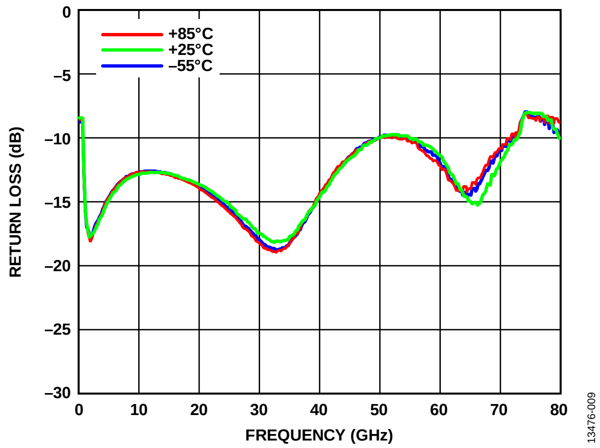

Figure 9. Input Return Loss at Various Temperatures

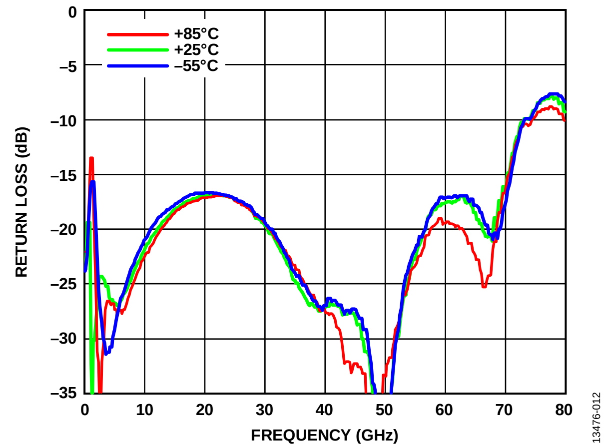

Figure 12. Output Return Loss at Various Temperatures

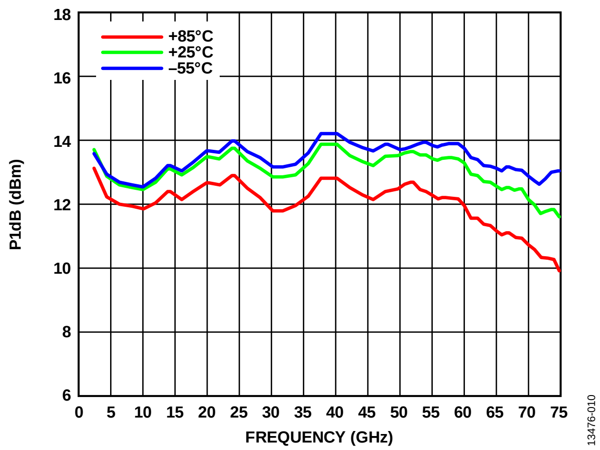

Figure 10. P1dB vs. Frequency at Various Temperatures

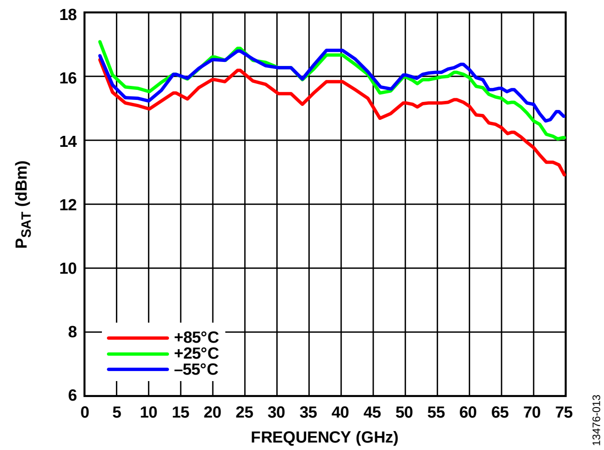

Figure 13. P_{SAT} vs. Frequency at Various Temperatures

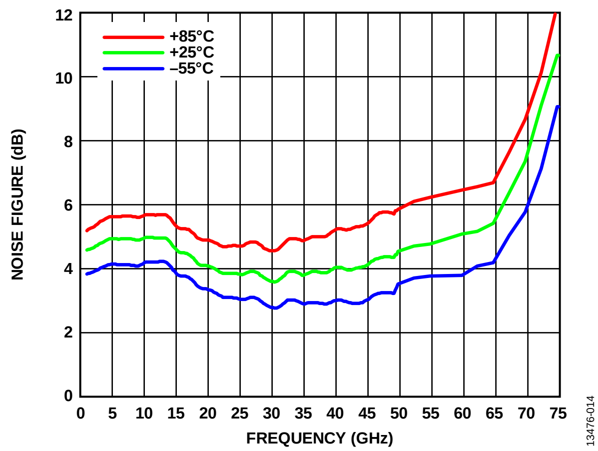

Figure 14. Noise Figure

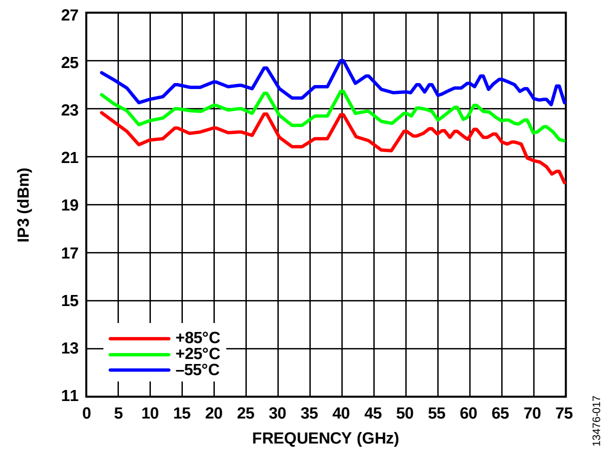

Figure 17. Output IP3 vs. Frequency at Various Temperatures, P_{OUT} = 0 dBm per Tone

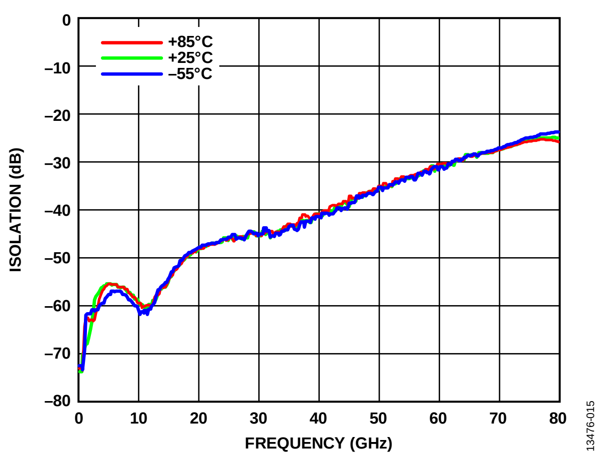

Figure 15. Reverse Isolation vs. Frequency at Various Temperatures

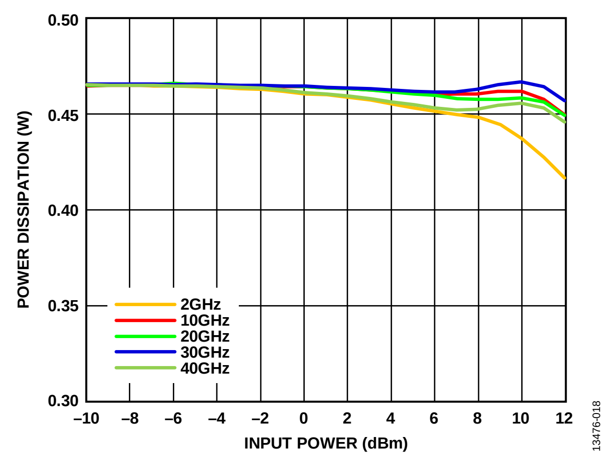

Figure 18. Power Dissipation at 85°C

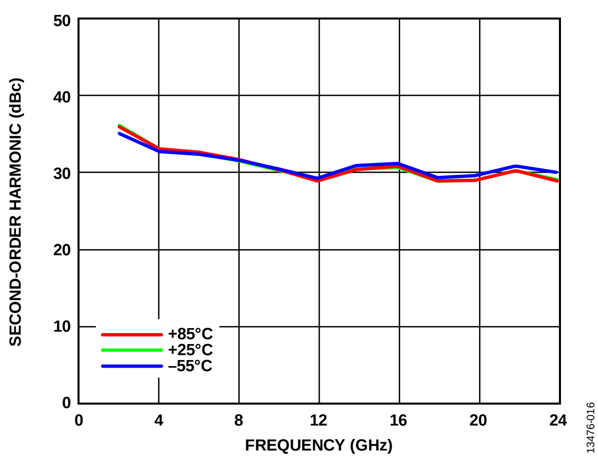

Figure 16. Second-Order Harmonic vs. vs. Frequency at Various Temperatures, P_{OUT} = 2 dBm

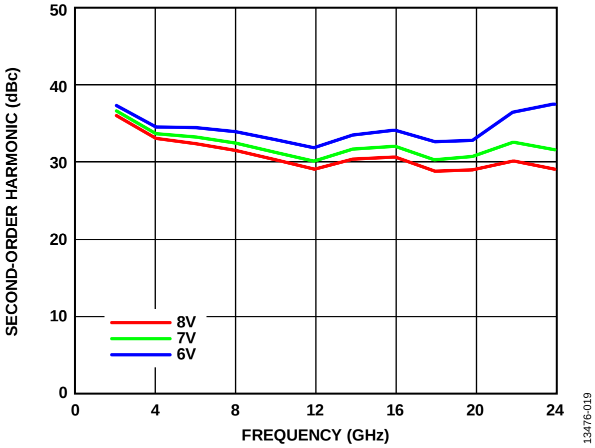

Figure 19. Second-Order Harmonic vs. Frequency at Various Supplies (V_{DD}), P_{OUT} = 2 dBm

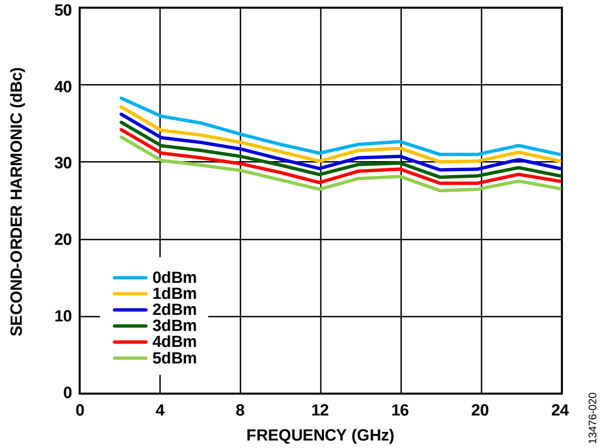

Figure 20. Second-Order Harmonic vs. Frequency at Various P_{OUT} Levels

THEORY OF OPERATION

HMC-AUH312 is a GaAs MMIC HEMT cascode distributed, low noise, wideband amplifier. The cascode distributed amplifier uses a fundamental cell of two field effect transistors (FETs) in series, source to drain. This fundamental cell then duplicates a number of times.

The major benefit of this architecture is an increase in the operation bandwidth. The basic schematic for a fundamental cell is shown in Figure 21, which shows the RFIN and RFOUT functions of the RFIN/$V_{GG}1$ and RFOUT/V_{DD} pins.

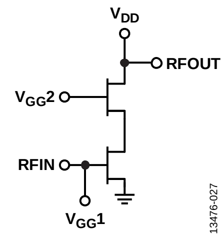

Figure 21. Fundamental Cell Schematic

To obtain the best performance from the HMC-AUH312 and not damage the device, follow the recommended biasing sequence outlined in the Device Operation section.

APPLICATIONS INFORMATION

APPLICATIONS OVERVIEW

The HMC-AUH312 has single-ended input and output ports whose impedances are nominally equal to 50 Ω over the frequency range 0.5 GHz to 80 GHz. Consequently, it can be directly inserted into a 50 Ω system with no impedance matching circuitry required. This means that multiple numbers of HMC-AUH312 amplifiers can be cascaded back to back without the need for external matching circuitry.

Because the input and output impedances are sufficiently stable vs. variations in temperature and supply voltage, no impedance matching compensation is required.

It is critical to supply very low inductance ground connections to the ground pins as well as to the die bottom. These connections ensure stable operation.

The HMC-AUH312 is a wideband amplifier with a positive gain slope with increasing frequency, which helps users to compensate for the typical higher frequency loss introduced by several system components.

There are two methods for biasing the device. The typical biasing technique is shown by the circuit diagram in Figure 22 and the assembly diagram shown in Figure 24. This technique uses only the RFIN and RFOUT functions of the RFIN/$V_{GG}1$ and RFOUT/V_{DD} pins.

The alternate biasing technique is represented by the circuit shown in Figure 23 and the assembly shown in Figure 25, which include the use of the $V_{GG}1$ and V_{DD} functions of the RFIN/$V_{GG}1$ and RFOUT/V_{DD} pins.

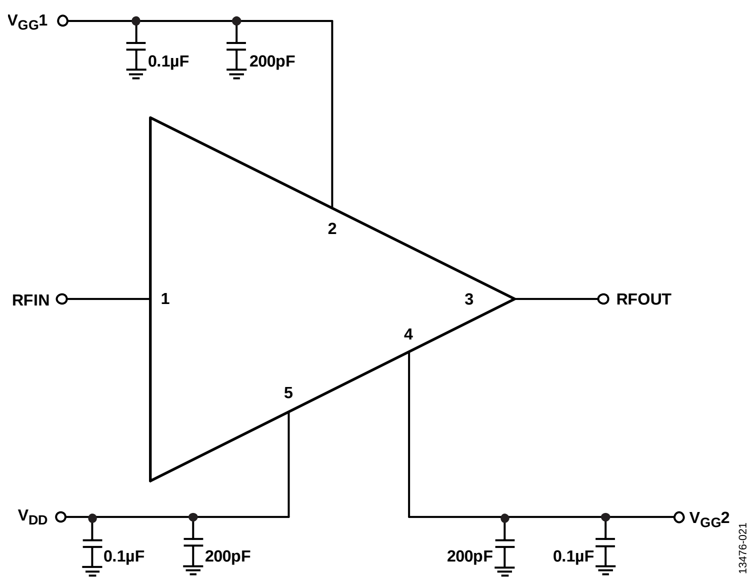

Figure 22. Applications Circuit

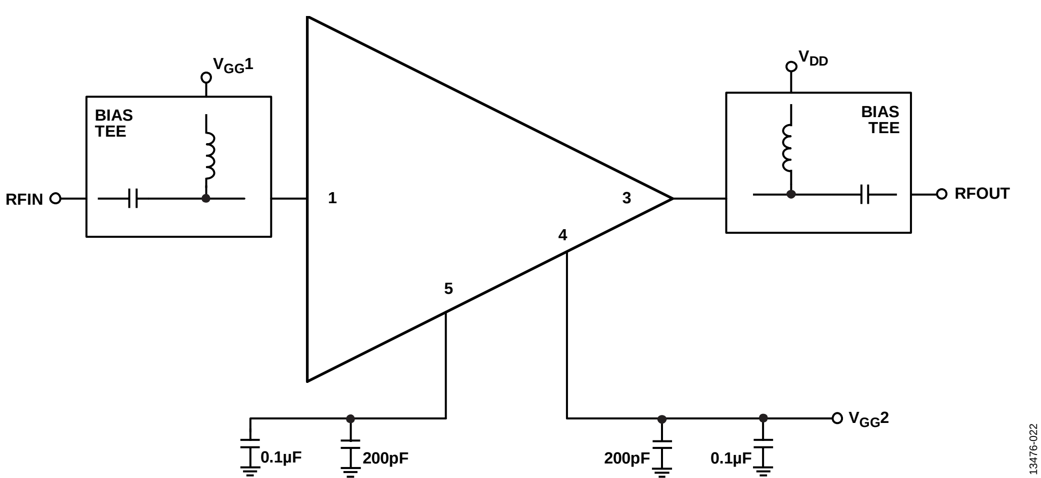

Figure 23. Suggested Alternate Applications Circuit

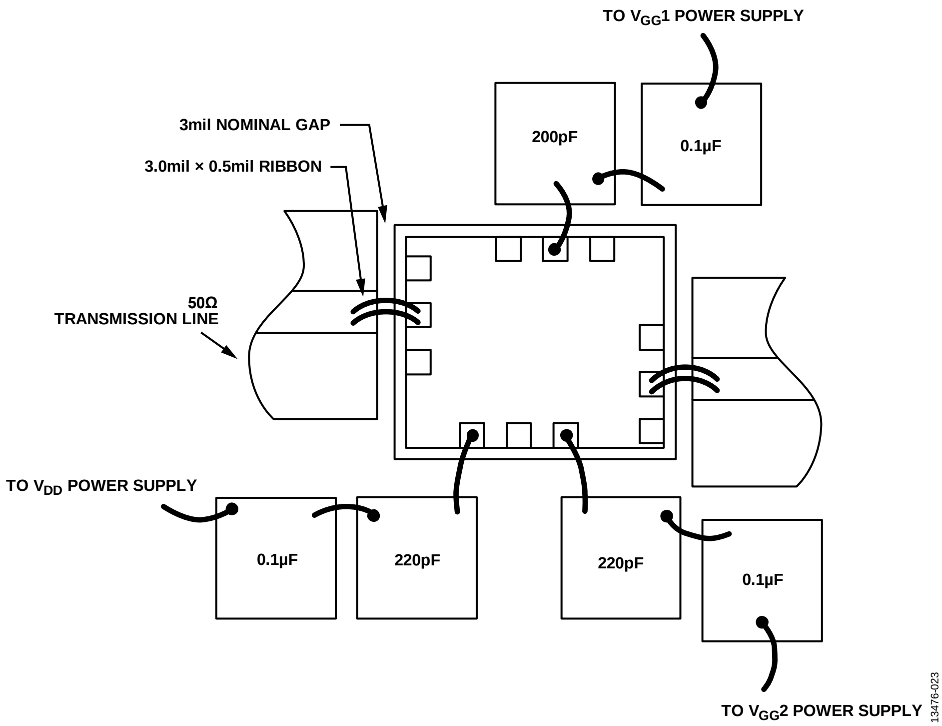

Figure 24. Assembly Diagram

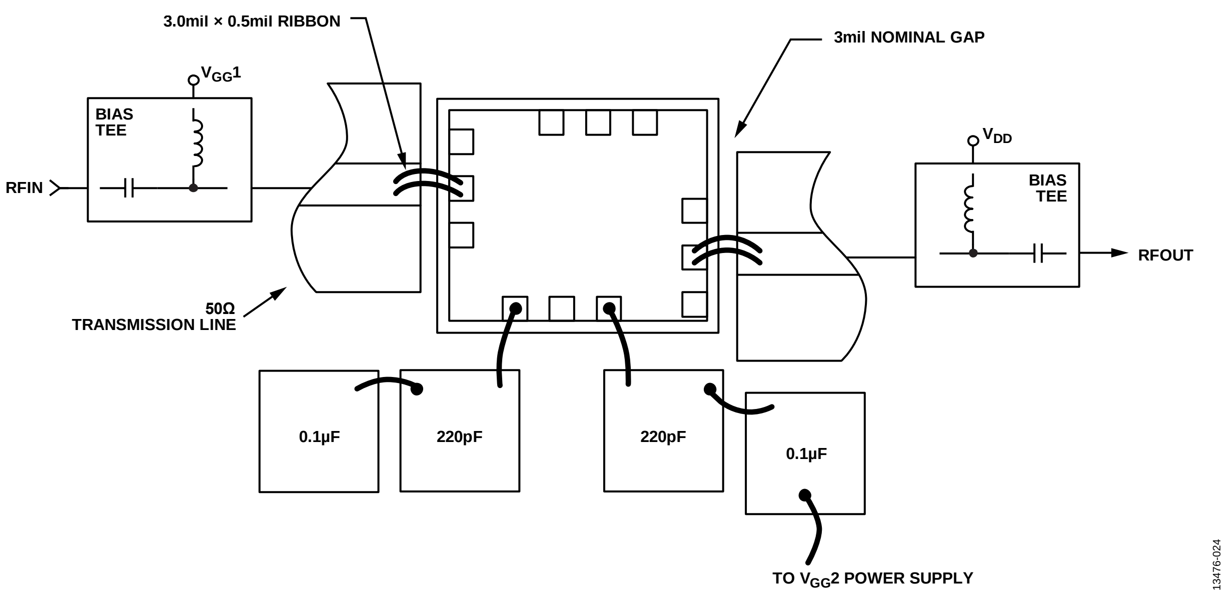

Figure 25. Suggested Alternate Assembly Diagram

DEVICE MOUNTING

The following are best practice layout practices:

- 1 mil wire bonds are used on the $V_{GG}1$ and $V_{GG}2$ connections to the capacitors.
- 0.5 mil × 3 mil round wire bonds are used on all other connections.
- Capacitors on $V_{GG}1$ and $V_{GG}2$ are used to filter the low frequency, <800 MHz, RF noise.
- For best gain flatness and group delay variation, place the capacitors from V_{DD}, $V_{GG}1$, and $V_{GG}2$ as close to the die as possible to minimize bond wire parasitics. V_{DD} is especially sensitive to bond parasitics.
- Silver-filled conductive epoxy is used for die attachment. (Ground the backside of the die and connect the GND pads to the backside metal through vias.)

DEVICE OPERATION

These devices are susceptible to damage from electrostatic discharge. Observe proper precautions during handling, assembly, and test. In addition, dc block the input and output to this device.

Device Power-Up Instructions

Use the following steps to power up the device:

1. Ground the device.
2. Bring $V_{GG}1$ to −2 V to pinch off the drain current.
3. Turn on V_{DD} to 0 V. Bring V_{DD} to 8 V; 6 V is the minimum recommended V_{DD} (5 V if a bias tee is used for V_D bias).
4. Turn on $V_{GG}2$ to 1.8 V (no drain current).
5. Adjust $V_{GG}1$ to achieve a target bias of 60 mA.
6. Apply the RF signal.

Device Power-Down Instructions

To power down the device, reverse the sequence identified in Step 1 through Step 6 in the Device Power-Up Instructions.

Bias conditions provided in the Device Power-Up Instructions are the operating points recommended to optimize the overall performance.

Unless otherwise noted, the data shown in the Specifications section were taken using the recommended bias conditions (see Table 4). Operation of the HMC-AUH312 at different bias conditions may result in performance that differs from that shown in the Specifications section (Table 1 through Table 3) and the Typical Performance Characteristics section (Figure 8 through Figure 20). Typically, output power levels and linearity can be improved at the expense of power consumption.

MOUNTING AND BONDING TECHNIQUES FOR MILLIMETERWAVE GaAs MMICS

HANDLING GUIDELINES FOR ESD PROTECTION OF GaAs MMICS

All electrical components are sensitive to some degree to electrostatic discharge (ESD), and GaAs MMICs are no exception. Many digital semiconductions have some level of protection circuitry designed into the input and output pins. However, GaAs MMIC designs rarely include built-in protection circuitry because of RF performance issues. Specifically, protection circuits add reactive parasitics that limit high frequency performance.

Circuitry on GaAS MMICs can be damaged by ESD at voltages below 250 V. In some cases, this classifies these devices as Class 0, meaning that stringent levels of ESD protection must be observed.

Electrostatic charges are created by the contact and separation of two objects. The magnitude of this charge buildup varies within different materials. Conductive and static dissipative materials release this charge quite easily to a grounded surface. Insulators retain the charge for a longer period of time.

To protect static sensitive devices from an electrostatic discharge, the devices must be completely enclosed with protective conductive packaging. This shielding protects the devices inside by causing any static discharge to follow the shortest conductive path to ground. Prior to opening the protective packaging, the device must be placed on a conductive workbench to dissipate any charge that has built up on the outside of the package.

When the device is removed from its protective package, it must be handled only at a grounded workstation by an operator grounded through a conductive wrist strap. Equipment used in the manufacture, assembly, and test of GaAs MMIC devices must also be properly grounded.

Antistatic or dissipative tubes and pink poly bags provide no ESD protection to the device. The antistatic or dissipative name only implies that it does not create an ESD hazard.

The only proper protection is to completely enclose the device in a conductive static shield; that is, a silver colored bag, black conductive tote box, and/or conductive carrier tape.

For additional information on proper ESD handling, consult the Electrostatic Discharge Association Advisory ESD-ADV-2.0-1994 or MIL-STD-1686. Information contained in this section of the data sheet was obtained from the ESD Association Advisory (Reference) AS-9100.

HANDLING PRECAUTIONS

Take the following precautions to avoid permanent damage to the device.

Opening the Protective Packaging

Prior to opening the protective packaging, the device must be placed on a conductive workbench to dissipate any charge that has built up on the outside of the package.

Storage

All bare die are placed in either waffle or gel-based ESD protective containers and sealed in an ESD protective bag for shipment. Immediately upon opening the sealed ESD protective bag, store all die in a dry nitrogen environment.

Cleanliness

Handle the chips in a clean environment. Do not attempt to clean the chip using liquid cleaning systems.

Static Sensitivity

Follow ESD precautions to protect against ESD strikes. Handle the device at a grounded workstation only by an operator that is also grounded through a conductive wrist strap. Equipment used in the manufacture, assembly, and test of GaAs MMIC devices must also be properly grounded.

Transients

Suppress instrument and bias supply transients during bias application. To minimize inductive pickup, use shielded signal and bias cables.

General Handling

Handle the chip on the edges only using a vacuum collet or a sharp pair of bent tweezers. Because the surface of the chip may have fragile air bridges, do not touch the chip surface with a vacuum collet, tweezers, or fingers.

MOUNTING TECHNIQUES

Attach the die directly to the ground plane eutectically or with conductive epoxy.

Using 50 Ω microstrip transmission lines on 0.127 mm (5 mil) thick alumina thin film substrates is recommended for bringing the RF to and from the chip (see Figure 26). If 0.254 mm (10 mil) thick alumina thin film substrates must be used, raise the die 0.150 mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.100 mm (4 mil) thick die to a 0.150 mm (6 mil) thick molybdenum heat spreader (moly tab), which is then attached to the ground plane (see Figure 27).

To minimize bond wire length, place microstrip substrates as close to the die as possible. Typical die to substrate spacing is 0.076 mm to 0.152 mm (3 mil to 6 mil).

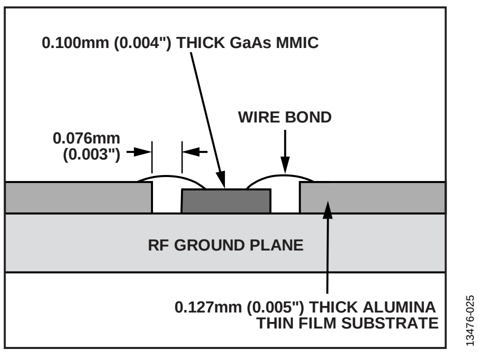

Figure 26. Routing RF Signals

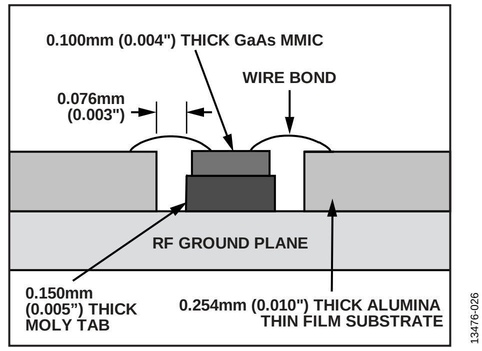

Figure 27. Routing RF Signals Using Molly Tab

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. Ensure that the mounting surface is clean and flat.

Eutectic Die Attach

An 80% gold/20% tin preform is recommended with a work surface temperature of 255°C and a tool temperature of 265°C. When hot 90% nitrogen/10% hydrogen gas is applied, make sure that the tool tip temperature is 290°C. Do not expose the chip to a temperature greater than 320°C for more than 20 sec. No more than 3 sec of scrubbing is required for attachment.

Epoxy Die Attach

Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip when it is placed into position. Cure the epoxy per the schedule provided by the manufacturer.

WIRE BONDING

RF bonds made with two 1 mil wires are recommended. These bonds must be thermosonically bonded with a force of 40 g to 60 g. Use of dc bonds of 0.001 inch (0.025 mm) diameter, thermosonically bonded, are recommended. Create ball bonds with a force of 40 g to 50 g and wedge bonds at 18 g to 22 g.

Create all bonds with a nominal stage temperature of 150°C. Apply a minimum amount of ultrasonic energy to achieve reliable bonds. Keep all bonds as short as possible, less than 12 mil (0.31 mm).