GaAs, pHEMT, Low Noise Amplifier, 400 MHz to 52 GHz

FEATURES

- Gain: 12 dB typical at 10 GHz to 26 GHz
- Input return loss: 14 dB typical at 10 GHz to 26 GHz
- Output return loss: 16 dB typical at 10 GHz to 40 GHz
- OP1dB: 17.5 dB typical at 10 GHz to 26 GHz
- P_{SAT}: 21 dBm typical at 10 GHz to 26 GHz
- OIP3: 28.5 dBm typical at 10 GHz to 26 GHz
- Noise figure: 3.5 dB typical at 10 GHz to 26 GHz
- 5 V supply voltage at 85 mA
- 50 Ω matched input and output
- No external passive components required
- 5.00 mm × 5.00 mm, 24-terminal LGA_CAV package

APPLICATIONS

- Test instrumentation
- Military and space

FUNCTIONAL BLOCK DIAGRAM

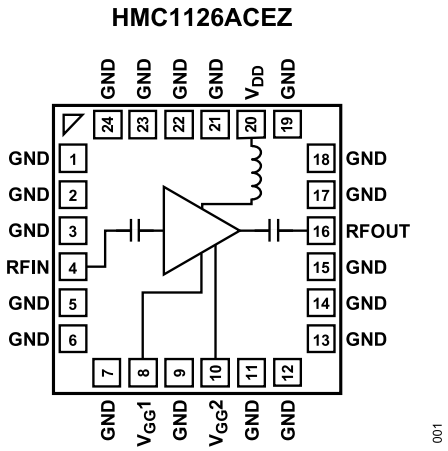

Figure 1.

GENERAL DESCRIPTION

The HMC1126ACEZ is a gallium arsenide (GaAs), pseudomorphic high electron mobility transfer (pHEMT), low noise amplifier that operates from 400 MHz to 52 GHz. The HMC1126ACEZ provides 12 dB of typical gain, 28.5 dBm typical output third-order intercept (OIP3), 17.5 dBm typical output power at 1 dB gain compression (OP1dB), and a 3.5 dB typical noise figure at 10 GHz to 26 GHz. The HMC1126ACEZ requires 85 mA from a 5 V supply. All of the typically required external passive components for operation (ac coupling capacitors and power supply decoupling capacitors) are integrated, which facilitates a small and compact printed circuit board (PCB) footprint.

The HMC1126ACEZ is housed in a 5.00 mm × 5.00 mm, 24-terminal chip array small outline no lead cavity (LGA_CAV) package.

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REVISION HISTORY

2/2023—Rev. 0 to Rev. A

Changes to Table 5..... 5

11/2021—Revision 0: Initial Version

ELECTRICAL SPECIFICATIONS

400 MHZ TO 10 GHZ FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, $V_{GG}2$ = 1 V, and supply current (I_{DQ}) = 85 mA, unless otherwise stated. Adjust $V_{GG}1$ between −2 V and 0 V to achieve I_{DQ} = 85 mA typical.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	0.4		10	GHz	
GAIN	10.5	12.5		dB	
Gain Variation over Temperature		0.003		dB/°C	
RETURN LOSS					
Input		11.5		dB	
Output		13		dB	
OUTPUT					
OP1dB	15	17.5		dBm	
Saturated Output Power (P_{SAT})		20		dBm	
OIP3		29		dBm	Output power (P_{OUT}) per tone = 0 dBm with 1 MHz tone spacing
Second-Order Intercept (OIP2)		31		dBm	P_{OUT} per tone = 0 dBm with 1 MHz tone spacing
NOISE FIGURE		4.0		dB	
SUPPLY					
I_{DQ}		85		mA	Adjust $V_{GG}1$ to achieve I_{DQ} = 85 mA typical
V_{DD}	3.3	5		V	

10 GHZ TO 26 GHZ FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, $V_{GG}2$ = 1 V, and I_{DQ} = 85 mA, unless otherwise stated. Adjust $V_{GG}1$ between −2 V and 0 V to achieve I_{DQ} = 85 mA typical.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	10		26	GHz	
GAIN	10	12		dB	
Gain Variation over Temperature		0.006		dB/°C	
RETURN LOSS					
Input		14		dB	
Output		16		dB	
OUTPUT					
OP1dB		17.5		dBm	
P_{SAT}		21		dBm	
OIP3		28.5		dBm	P_{OUT} per tone = 0 dBm with 1 MHz tone spacing
OIP2		28		dBm	P_{OUT} per tone = 0 dBm with 1 MHz tone spacing
NOISE FIGURE		3.5		dB	
SUPPLY					
I_{DQ}		85		mA	Adjust $V_{GG}1$ to achieve I_{DQ} = 85 mA typical
V_{DD}	3.3	5		V	

ELECTRICAL SPECIFICATIONS

26 GHZ TO 40 GHZ FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, $V_{GG}2$ = 1 V, and I_{DQ} = 85 mA, unless otherwise stated. Adjust $V_{GG}1$ between −2 V and 0 V to achieve I_{DQ} = 85 mA typical.

Table 3.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	26		40	GHz	
GAIN	10.5	12.5		dB	
Gain Variation over Temperature		0.007		dB/°C	
RETURN LOSS					
Input		13.5		dB	
Output		16		dB	
OUTPUT					
OP1dB		16		dBm	
P_{SAT}		20		dBm	
OIP3		27		dBm	P_{OUT} per tone = 0 dBm with 1 MHz tone spacing
NOISE FIGURE		4.5		dB	
SUPPLY					
I_{DQ}		85		mA	Adjust $V_{GG}1$ to achieve I_{DQ} = 85 mA typical
V_{DD}	3.3	5		V	

40 GHZ TO 52 GHZ FREQUENCY RANGE

T_A = 25°C, V_{DD} = 5 V, $V_{GG}2$ = 1 V, and I_{DQ} = 85 mA, unless otherwise stated. Adjust $V_{GG}1$ between −2 V and 0 V to achieve I_{DQ} = 85 mA typical.

Table 4.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
FREQUENCY RANGE	40		52	GHz	
GAIN		12		dB	
Gain Variation over Temperature		0.01		dB/°C	
RETURN LOSS					
Input		7.5		dB	
Output		15		dB	
OUTPUT					
OP1dB		12.5		dBm	
P_{SAT}		17.5		dBm	
OIP3		23.5		dBm	P_{OUT} per tone = 0 dBm with 1 MHz tone spacing
NOISE FIGURE		6		dB	
SUPPLY					
I_{DQ}		85		mA	Adjust $V_{GG}1$ to achieve I_{DQ} = 85 mA typical
V_{DD}	3.3	5		V	

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
V_{DD}	6 V
Gate Bias Voltage	
$V_{GG}1$	−3 V to 0 V
$V_{GG}2$	
For V_{DD} = 3.3 V	0.5 V to 2.5 V
For V_{DD} = 4 V	0.5 V to 3 V
For V_{DD} = 5 V	1.0 V to 4 V
RFIN Power	22 dBm
Continuous Power Dissipation (P_{DISS}), T_A = 85°C (Derate 18.4 mW/°C Above 85°C)	1.66 W
Temperature	
Channel	175°C
Peak Reflow (Moisture Sensitivity Level (MSL) 3)[1]	260°C
Storage Range	−55°C to +150°C
Operating Range	−40°C to +85°C
Maximum Channel Temperature	175°C
Nominal Channel Temperature (T_A = 85°C, V_{DD} = 5 V, I_{DQ} = 85 mA)	108°C

[1] See the Ordering Guide for more information.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to system design and operating environment. Careful attention to the PCB thermal design is required.

θ_{JC} is the channel to case thermal resistance, channel to bottom of die using die attach epoxy.

Table 6. Thermal Resistance

Package Type	θ_{JC}	Unit
CE-24-2 [1]	54.3	°C/W

[1] θ_{JC} was determined by simulation under the following conditions: the heat transfer is due solely to thermal conduction from the channel, through the ground paddle, to the PCB, and the ground pad is held constant at the operating temperature of 85°C.

ELECTROSTATIC DISCHARGE (ESD) RATINGS

The following ESD information is provided for handling of ESD-sensitive devices in an ESD protected area only.

Human body model (HBM) per ANSI/ESDA/JEDDEC JS-001.

Table 7. HMC1126ACEZ, 24-Terminal LGA_CAV

ESD Model	Withstand Threshold (V)	Class
HBM	±250	1A

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

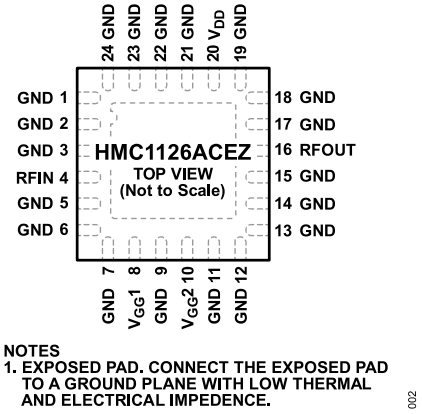

Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 2, 3, 5, 6, 7, 9, 11 to 15, 17, 18, 19, 21 to 24	GND	Ground. All the ground pins must be connected to a low impedance ground plane. See Figure 7 for the interface schematic.
4	RFIN	RF Input. RFIN is ac-coupled and matched to 50 Ω. See Figure 3 for the interface schematic.
8	$V_{GG}1$	Gate Control 1 for the Amplifier. Adjust $V_{GG}1$ to achieve I_{DQ} = 85 mA. See Figure 6 for the interface schematic.
10	$V_{GG}2$	Gate Control 2 for the Amplifier. For nominal operation, apply 1 V to $V_{GG}2$. See Figure 5 for the interface schematic.
16	RFOUT	RF Output. RFOUT is ac-coupled and matched to 50 Ω. See Figure 4 for the interface schematic.
20	V_{DD}	Drain Supply Voltage with Integrated RF Choke. Connect the dc bias to V_{DD} to provide I_{DQ}. See Figure 4 for the interface schematic.
	EPAD	Exposed Pad. Connect the exposed pad to a ground plane with low thermal and electrical impedance.

INTERFACE SCHEMATICS

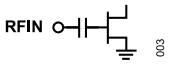

Figure 3. RFIN Interface Schematic

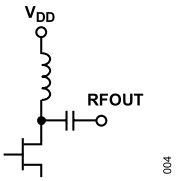

Figure 4. V_{DD} and RFOUT Interface Schematic

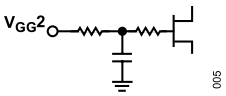

Figure 5. $V_{GG}2$ Interface Schematic

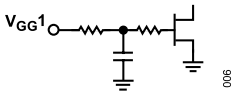

Figure 6. $V_{GG}1$ Interface Schematic

Figure 7. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

I_{DQ} is the drain current without the RF signal applied, and I_{DD} is the drain current with the RF signal applied.

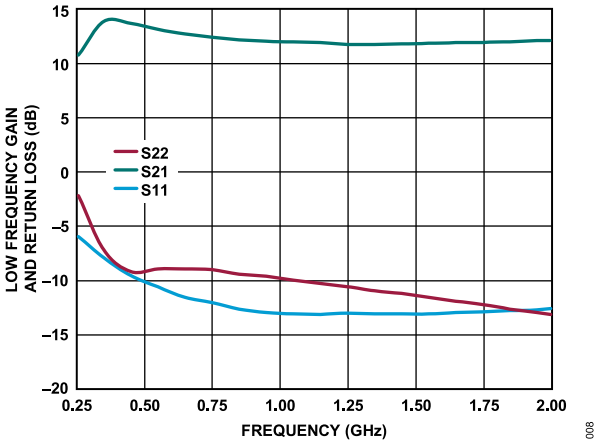

Figure 8. Low Frequency Gain and Return Loss vs. Frequency, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V (S22 Is the Output Return Loss, S21 Is the Gain, and S11 Is the Input Return Loss)

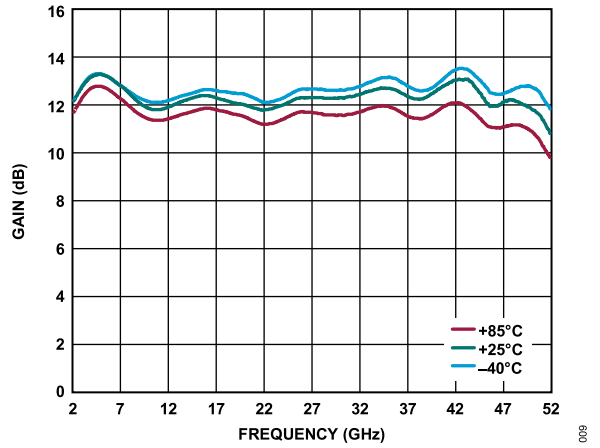

Figure 9. Gain vs. Frequency at Various Temperatures, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

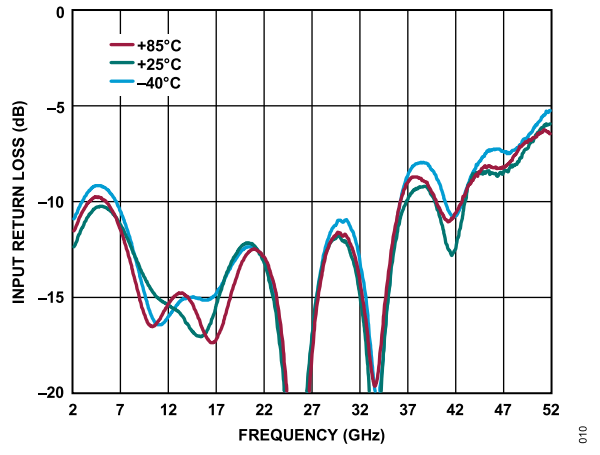

Figure 10. Input Return Loss vs. Frequency at Various Temperatures, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

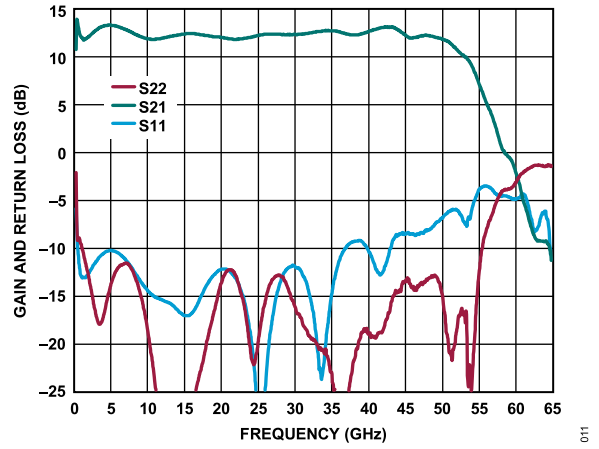

Figure 11. Gain and Return Loss vs. Frequency, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

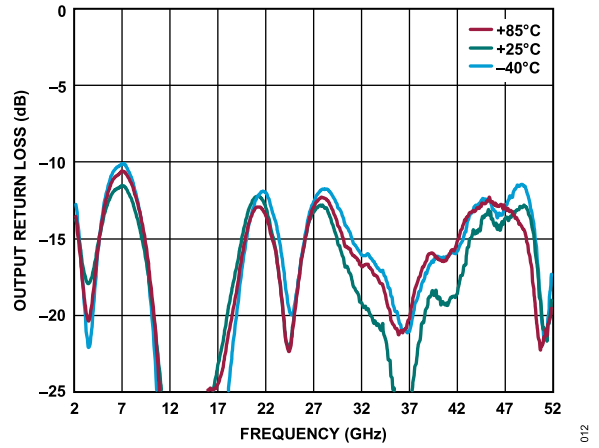

Figure 12. Output Return Loss vs. Frequency at Various Temperatures, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

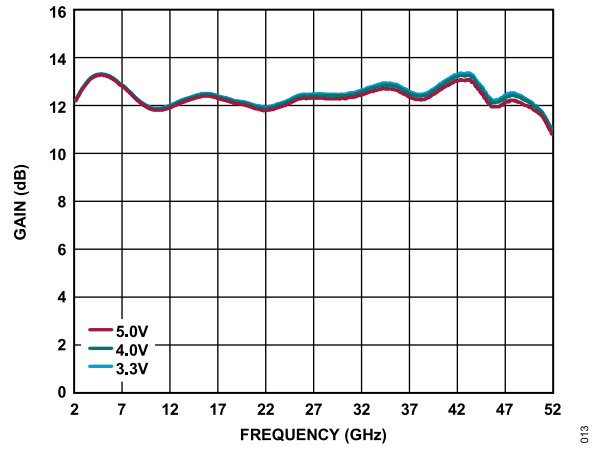

Figure 13. Gain vs. Frequency at Various V_{DD} Voltages, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

TYPICAL PERFORMANCE CHARACTERISTICS

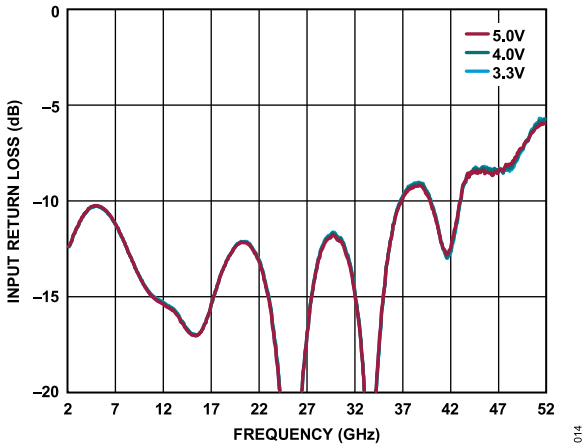

Figure 14. Input Return Loss vs. Frequency at Various V_{DD} Voltages, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

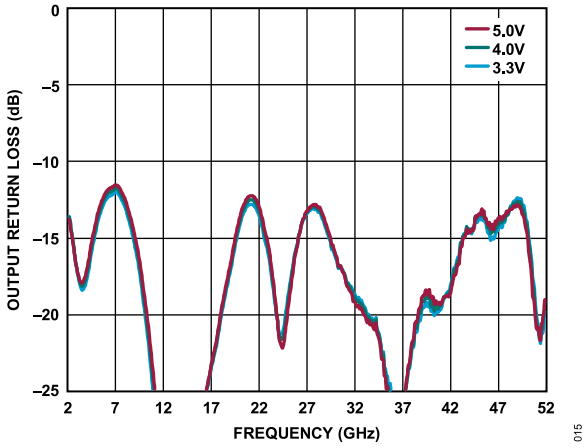

Figure 15. Output Return Loss vs. Frequency at Various V_{DD} Voltages, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

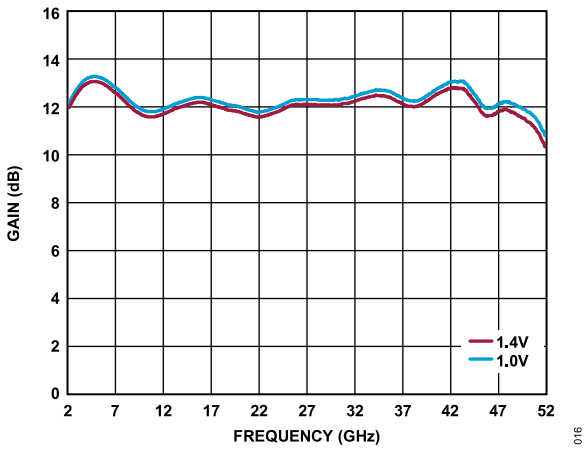

Figure 16. Gain vs. Frequency at Various $V_{GG}2$ Voltages, V_{DD} = 5 V, I_{DQ} = 85 mA

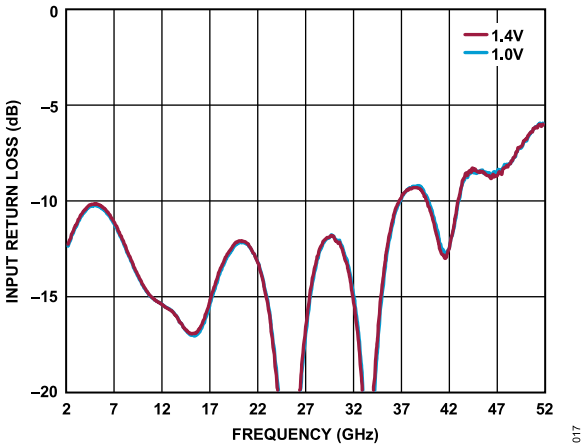

Figure 17. Input Return Loss vs. Frequency at Various $V_{GG}2$ Voltages, V_{DD} = 5 V, I_{DQ} = 85 mA

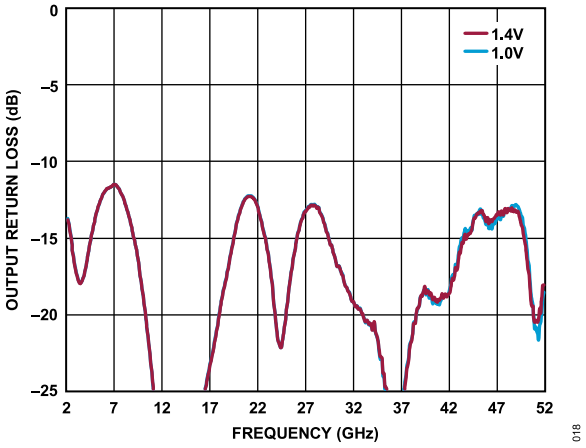

Figure 18. Output Return Loss vs. Frequency at Various $V_{GG}2$ Voltages, V_{DD} = 5 V, I_{DQ} = 85 mA

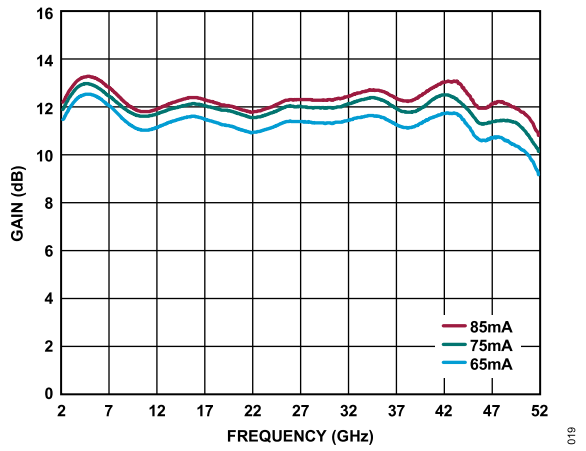

Figure 19. Gain vs. Frequency at Various I_{DQ} Currents, V_{DD} = 5 V, $V_{GG}2$ = 1 V

TYPICAL PERFORMANCE CHARACTERISTICS

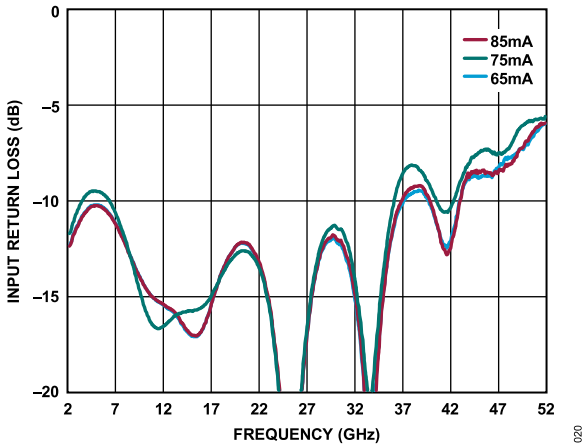

Figure 20. Input Return Loss vs. Frequency at Various I_{DQ} Currents, V_{DD} = 5 V, $V_{GG}2$ = 1 V

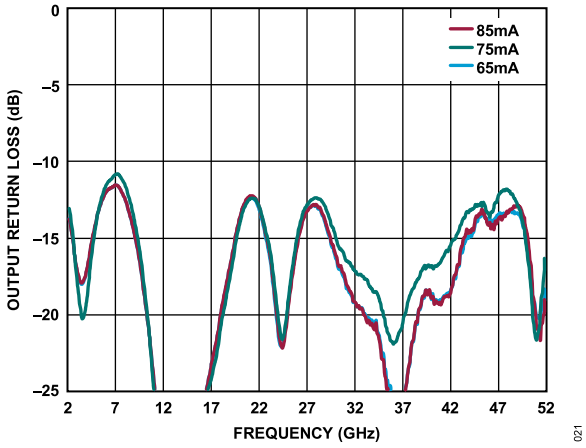

Figure 21. Output Return Loss vs. Frequency at Various I_{DQ} Currents, V_{DD} = 5 V, $V_{GG}2$ = 1 V

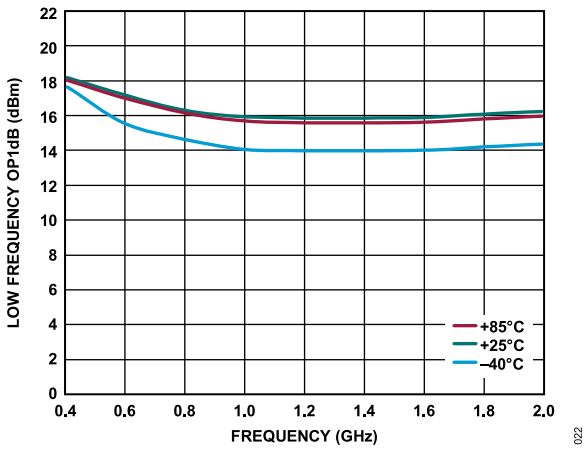

Figure 22. Low Frequency OP1dB vs. Frequency at Various Temperatures, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

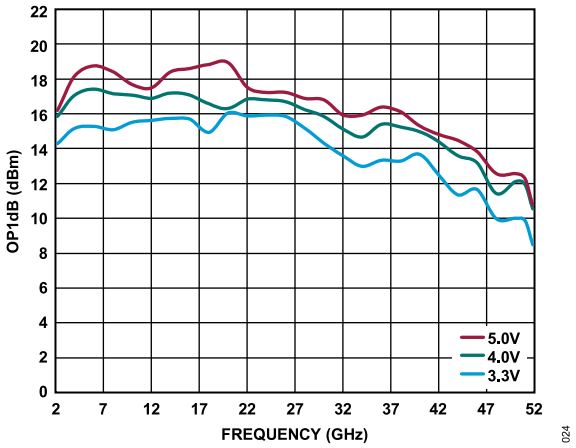

Figure 23. OP1dB vs. Frequency at Various V_{DD} Voltages, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

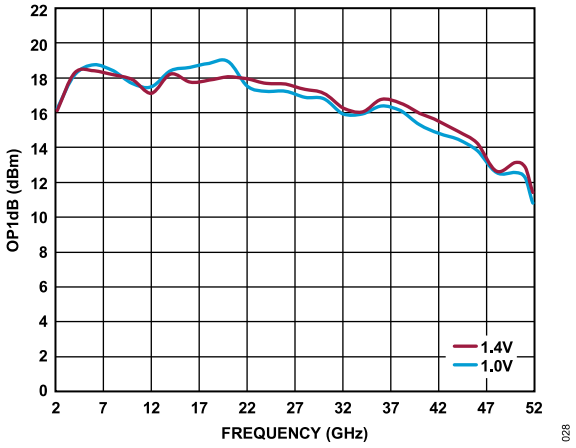

Figure 24. OP1dB vs. Frequency at Various $V_{GG}2$ Voltages, V_{DD} = 5 V, I_{DQ} = 85 mA

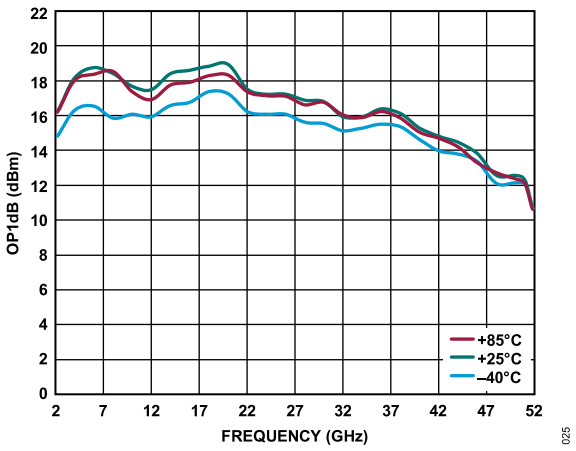

Figure 25. OP1dB vs. Frequency at Various Temperatures, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

TYPICAL PERFORMANCE CHARACTERISTICS

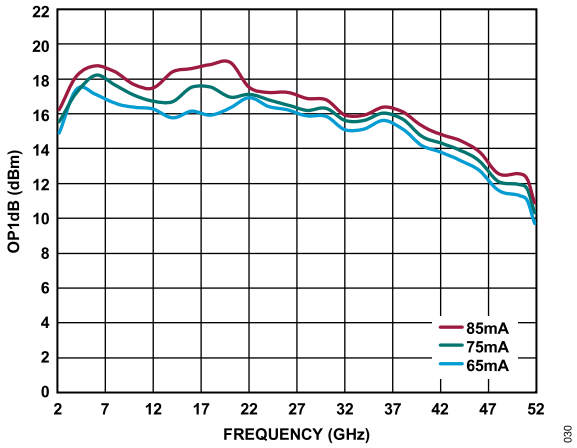

Figure 26. OP1dB vs. Frequency at Various I_{DQ} Currents, V_{DD} = 5 V, $V_{GG}2$ = 1 V

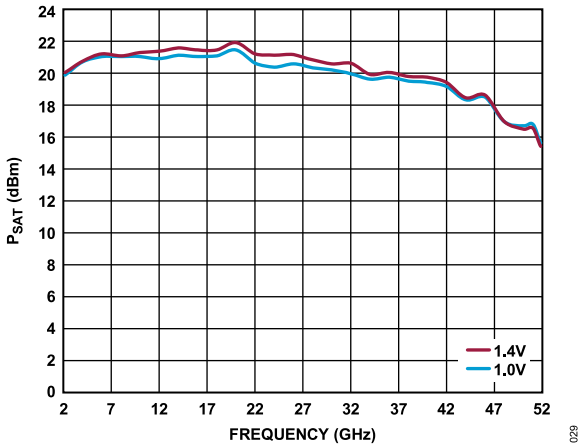

Figure 29. P_{SAT} vs. Frequency at Various $V_{GG}2$ Voltages, V_{DD} = 5 V, I_{DQ} = 85 mA

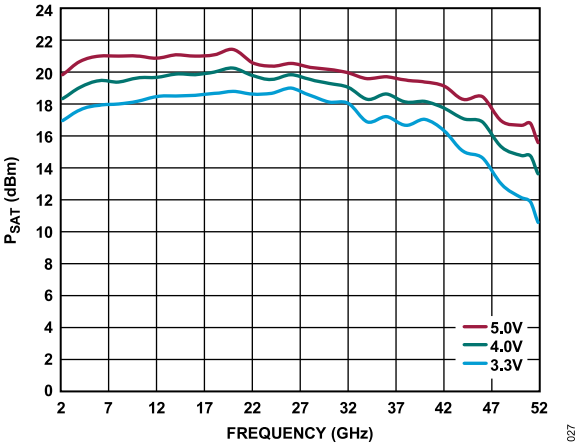

Figure 27. P_{SAT} vs. Frequency at Various V_{DD} Voltages, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

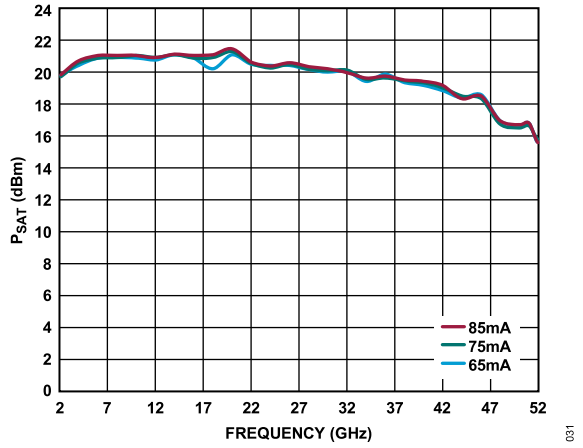

Figure 30. P_{SAT} vs. Frequency at Various I_{DQ} Currents, V_{DD} = 5 V, $V_{GG}2$ = 1 V

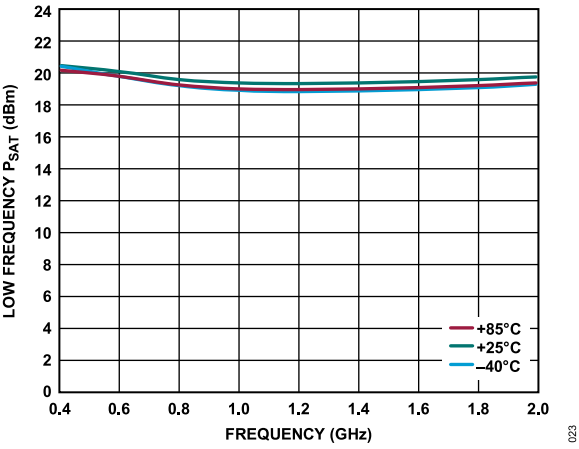

Figure 28. Low Frequency P_{SAT} vs. Frequency at Various Temperatures, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

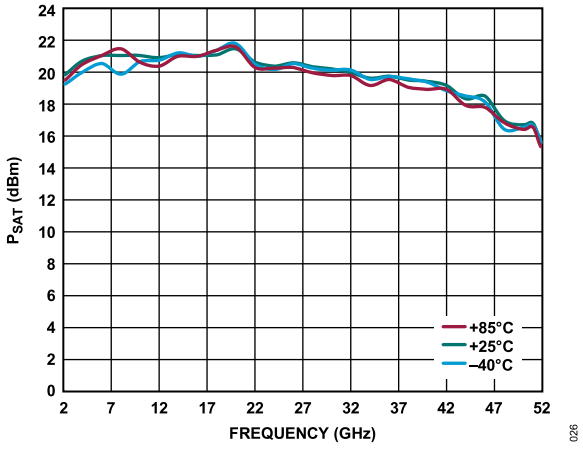

Figure 31. P_{SAT} vs. Frequency at Various Temperatures, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

TYPICAL PERFORMANCE CHARACTERISTICS

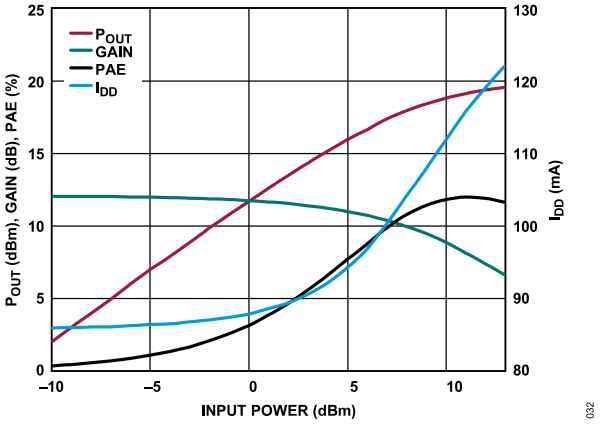

Figure 32. P_{OUT}, Gain, Power Added Efficiency (PAE), and I_{DD} vs. Input Power at 2 GHz, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

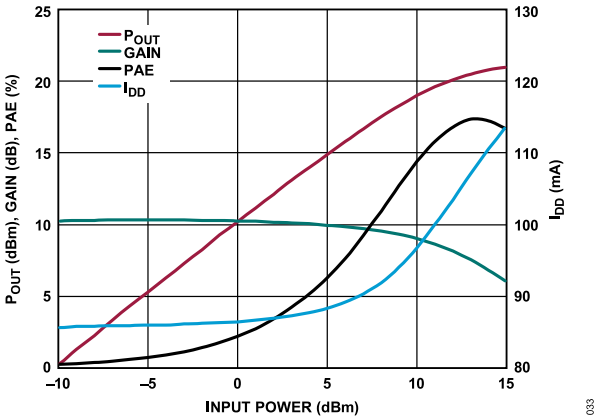

Figure 33. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at 26 GHz, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

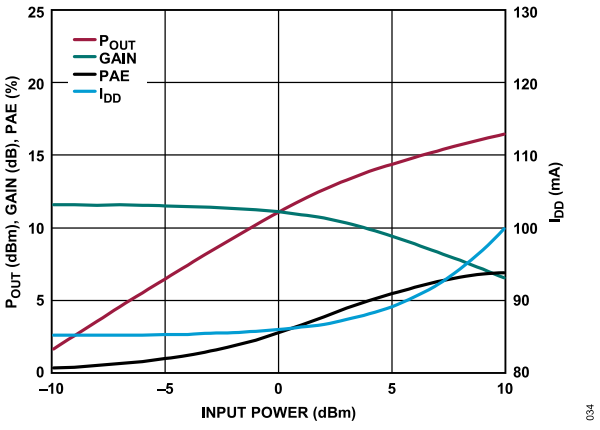

Figure 34. P_{OUT}, Gain, PAE, and I_{DD} vs. Input Power at 50 GHz, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

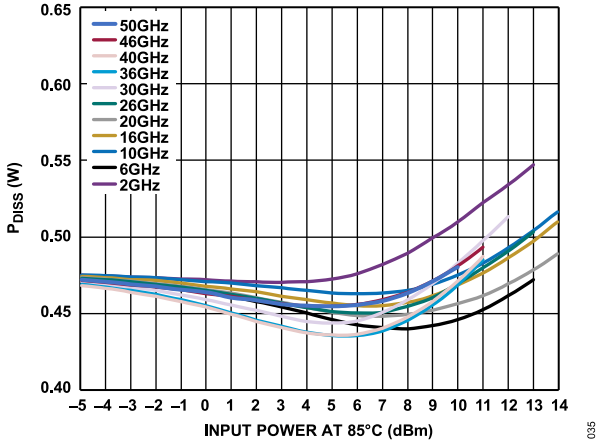

Figure 35. P_{DISS} vs. Input Power at 85°C for Various Frequencies, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

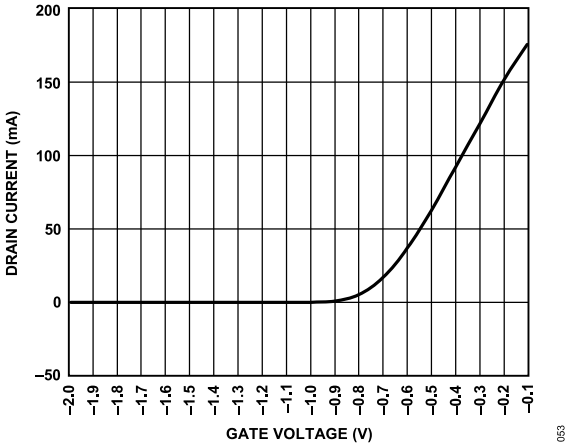

Figure 36. Drain Current vs. Gate Voltage, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

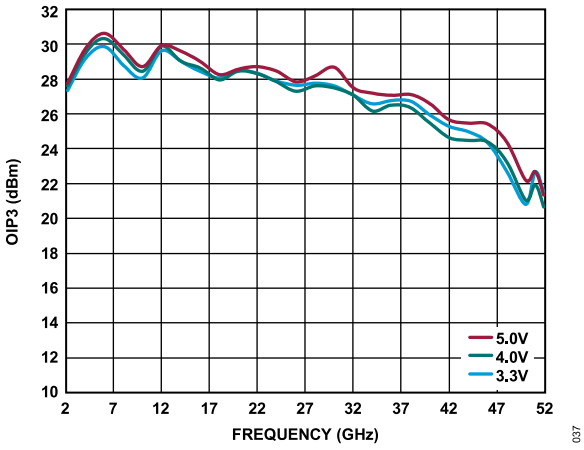

Figure 37. OIP3 vs. Frequency at Various V_{DD} Voltages, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

TYPICAL PERFORMANCE CHARACTERISTICS

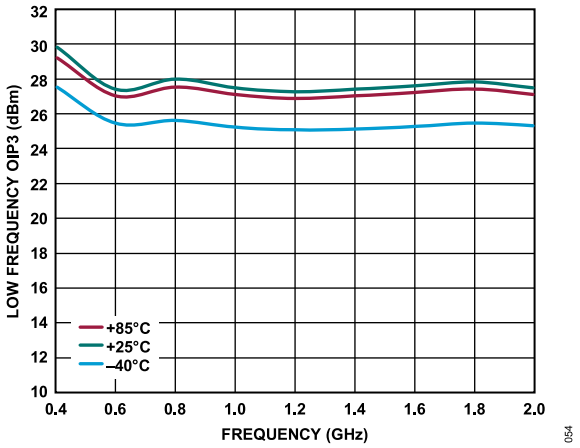

Figure 38. Low Frequency OIP3 vs. Frequency at Various Temperatures, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

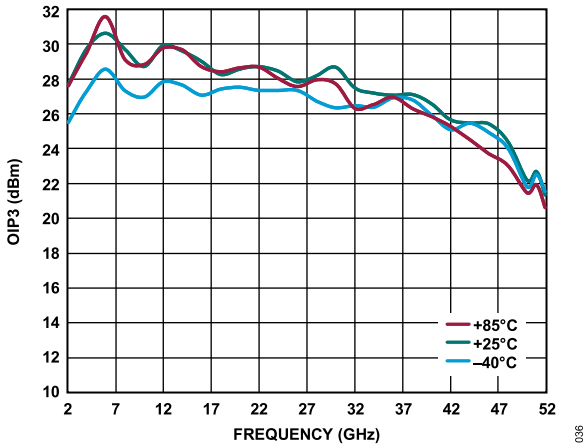

Figure 41. OIP3 vs. Frequency at Various Temperatures, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

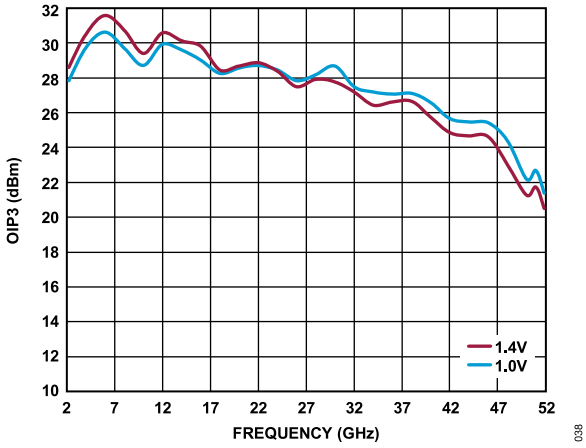

Figure 39. OIP3 vs. Frequency at Various $V_{GG}2$ Voltages, V_{DD} = 5 V, I_{DQ} = 85 mA

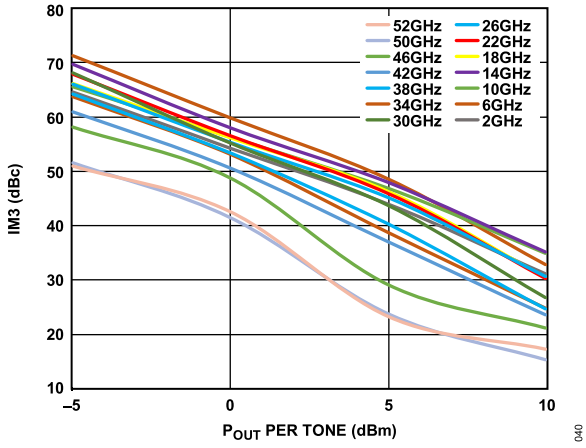

Figure 42. Third-Order Intermodulation (IM3) vs. P_{OUT} per Tone at Various Frequencies, V_{DD} = 3.3 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

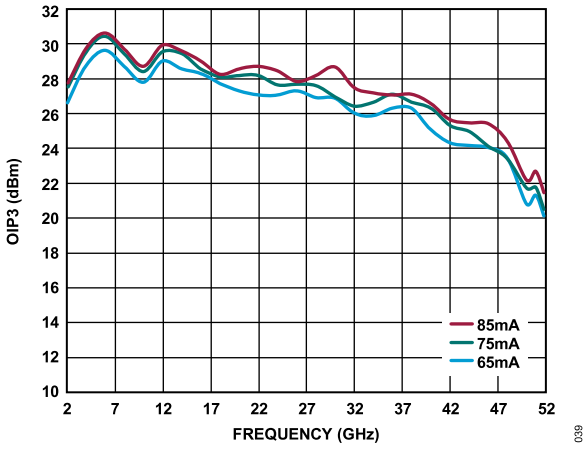

Figure 40. OIP3 vs. Frequency at Various I_{DQ} Currents, V_{DD} = 5 V, $V_{GG}2$ = 1 V

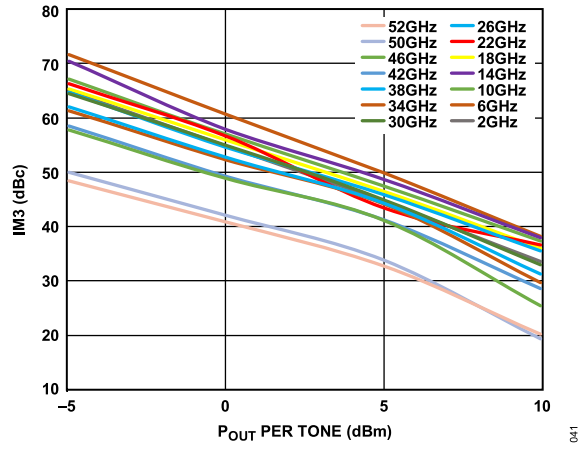

Figure 43. IM3 vs. P_{OUT} per Tone at Various Frequencies, V_{DD} = 4 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

TYPICAL PERFORMANCE CHARACTERISTICS

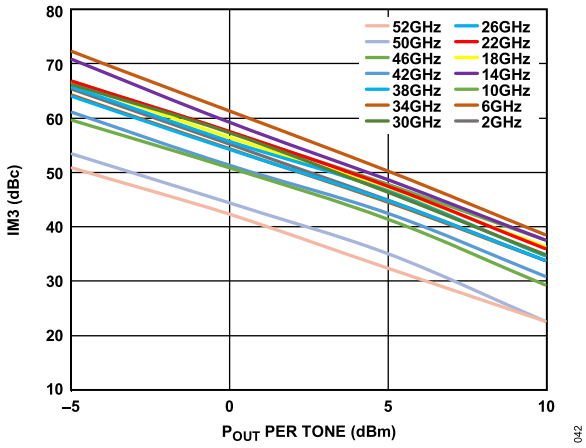

Figure 44. IM3 vs. P_{OUT} per Tone at Various Frequencies, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

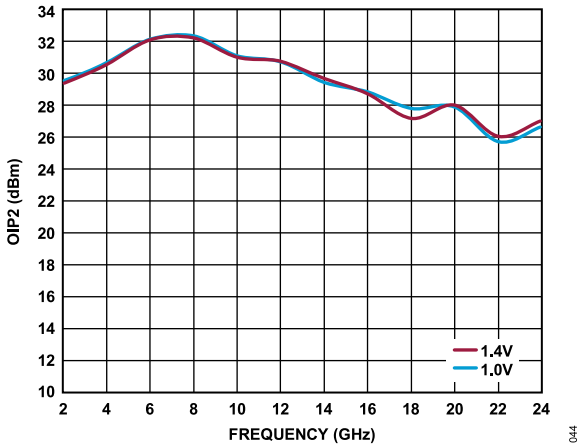

Figure 47. OIP2 vs. Frequency at Various $V_{GG}2$ Voltages, V_{DD} = 5 V, I_{DQ} = 85 mA

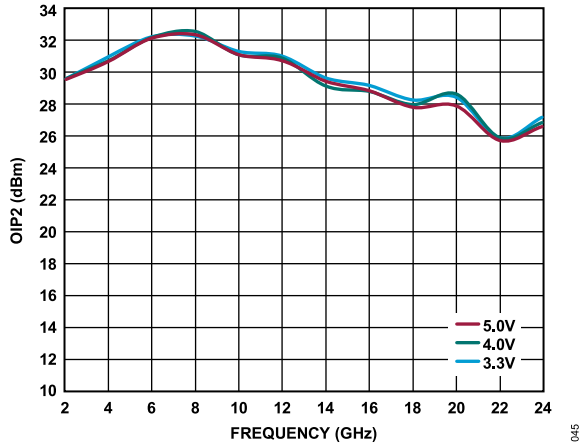

Figure 45. OIP2 vs. Frequency at Various V_{DD} Voltages, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

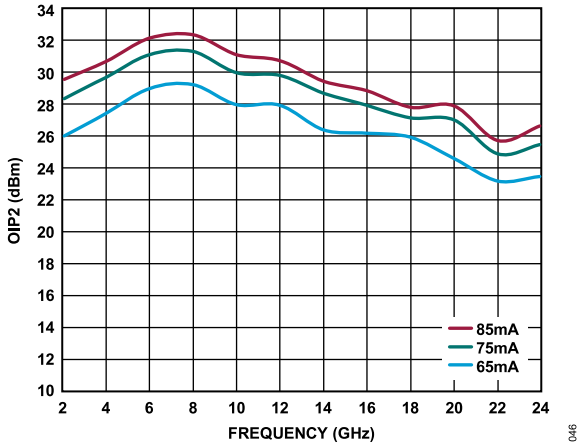

Figure 48. OIP2 vs. Frequency at Various I_{DQ} Currents, V_{DD} = 5 V, $V_{GG}2$ = 1 V

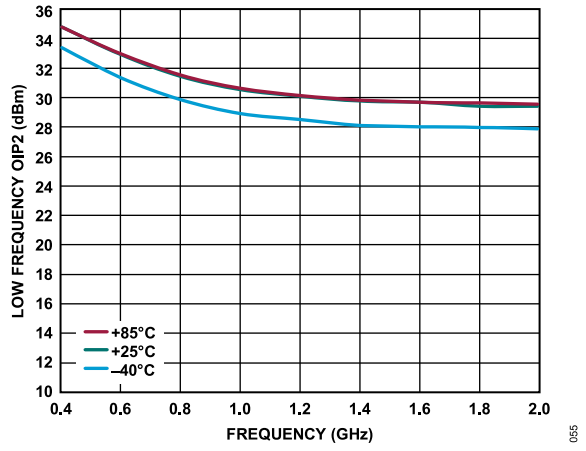

Figure 46. Low Frequency OIP2 vs. Frequency at Various Temperatures, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

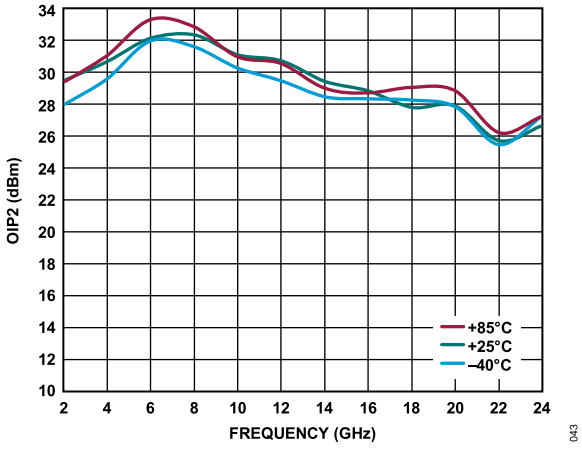

Figure 49. OIP2 vs. Frequency at Various Temperatures, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

TYPICAL PERFORMANCE CHARACTERISTICS

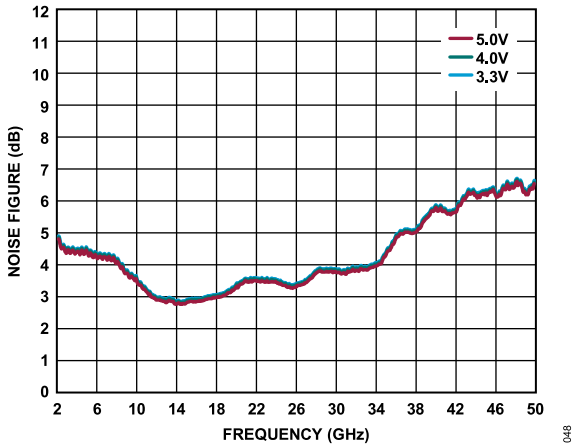

Figure 50. Noise Figure vs. Frequency at Various V_{DD} Voltages, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

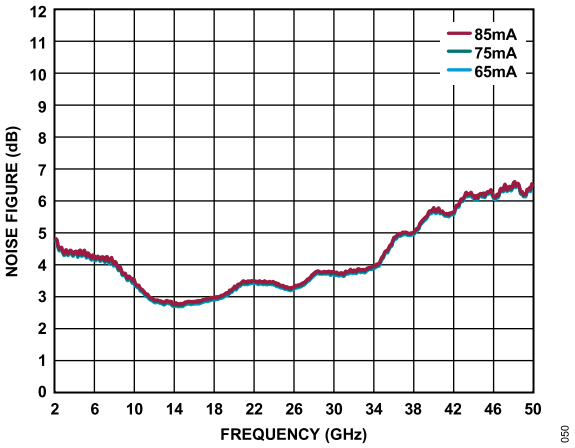

Figure 53. Noise Figure vs. Frequency at Various I_{DQ} Currents, V_{DD} = 5 V, $V_{GG}2$ = 1 V

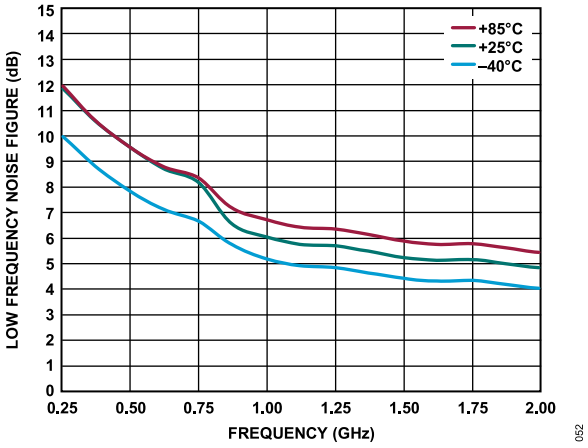

Figure 51. Low Frequency Noise Figure vs. Frequency at Various Temperatures, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

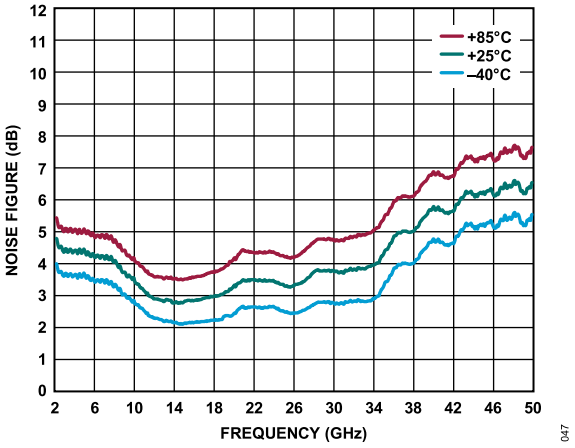

Figure 54. Noise Figure vs. Frequency at Various Temperatures, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

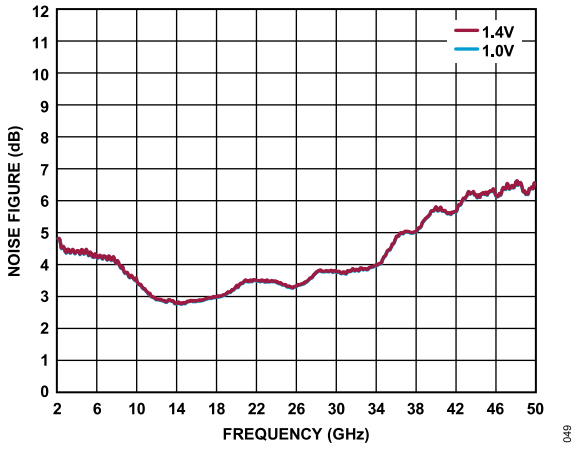

Figure 52. Noise Figure vs. Frequency at $V_{GG}2$ Voltages, V_{DD} = 5 V, I_{DQ} = 85 mA

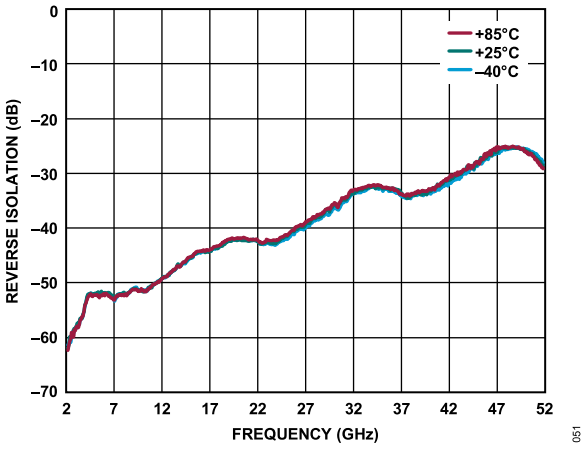

Figure 55. Reverse Isolation vs. Frequency at Various Temperatures, V_{DD} = 5 V, I_{DQ} = 85 mA, $V_{GG}2$ = 1 V

THEORY OF OPERATION

The HMC1126ACEZ is a GaAs, pHEMT, low noise amplifier.

The low noise amplifier uses a fundamental cell of two field effect transistors (FETs), as shown in Figure 56. This fundamental cell is duplicated a number of times, thereby increasing the operational bandwidth.

The negative $V_{GG}1$ sets the supply current, and the voltage on $V_{GG}2$ ensures that there are approximately equal dc voltages across the top and bottom FETs. The RFIN and RFOUT pins are ac-coupled and matched to 50 Ω. V_{DD} is applied through an integrated choke. The 0.1 µF and 100 pF decoupling capacitors are integrated. As a result, no external passive components are required for operation.

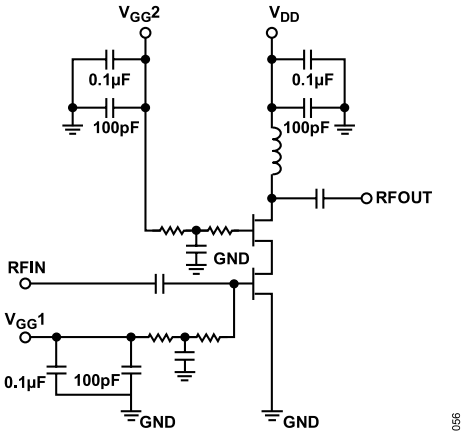

Figure 56. Simplified Block Diagram

APPLICATIONS INFORMATION

Figure 57 shows the basic connections for operating the HMC1126ACEZ. Because the RFIN and RFOUT pins are internally ac-coupled, no external ac coupling is required. Because V_{DD}, $V_{GG}1$, and $V_{GG}2$ are internally decoupled, no external components are required on these pins. Figure 57 shows the configuration used to characterize and qualify the device.

See the HMC1126-EVALZ user guide for information on using the evaluation board.

POWER-UP AND POWER-DOWN SEQUENCING

To avoid damaging the device, careful attention must be paid to the power-up and power-down sequencing of the RF input, the gate bias voltages, and the drain bias voltage.

Power-Up

The following power-up sequencing is recommended:

1. Connect GND to ground.
2. Set $V_{GG}1$ to −2 V.
3. Set V_{DD} to 5 V.
4. Set $V_{GG}2$ to 1 V.
5. Increase $V_{GG}1$ to achieve an I_{DQ} = 85 mA.
6. Apply the RF signal.

Power-Down

The following power-down sequencing is recommended:

1. Turn off the RF signal.
2. Decrease $V_{GG}1$ to −2 V to achieve an I_{DQ} = 0 mA.
3. Decrease $V_{GG}2$ to 0 V.
4. Decrease V_{DD} to 0 V.
5. Increase $V_{GG}1$ to 0 V.

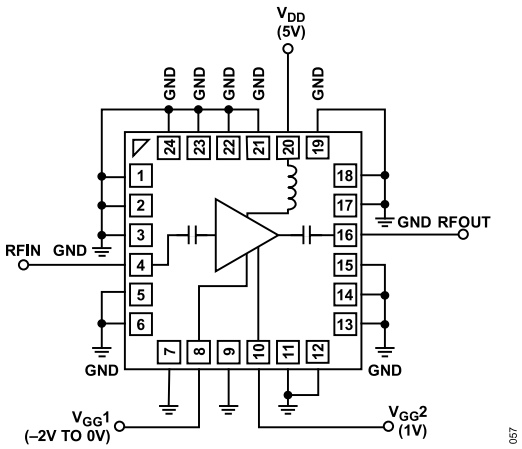

Figure 57. Basic Connections

APPLICATIONS INFORMATION

BIASING THE HMC1126ACEZ WITH THE HMC920LP5E

The HMC920LP5E (see Figure 58) is designed to provide active bias control for enhancement mode and depletion mode amplifiers, such as the HMC1126ACEZ. The HMC920LP5E measures and regulates drain current to compensate for temperature changes and part to part variations.

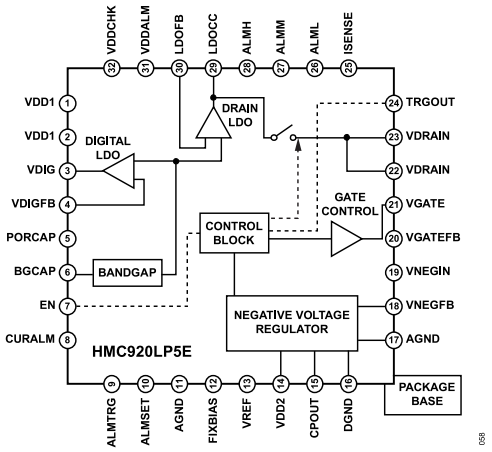

Figure 58. Functional Diagram of the HMC920LP5E

Additionally, the HMC920LP5E properly sequences gate and drain voltages to ensure safe on and off operation and offers circuit self protection in the event of a short circuit. The active bias controller contains an internal charge pump that generates the negative voltage needed to drive the $V_{GG}1$ pin on the HMC1126ACEZ. Alternatively, an external negative voltage can be provided.

For more information regarding the use of the HMC920LP5E, refer to the HMC920LP5E data sheet and the AN-1363 Application Note.

Application Circuit Setup

Figure 58 shows the application circuit for bias control of the HMC1126ACEZ using the HMC920LP5E. The current through the HMC920LP5E is measured, and the VGATE output voltage serves until the setpoint drain current is achieved. The various external components around the HMC920LP5E are set as follows in this section.

The target drain current must first be determined and set. This current must be set based on the maximum drain current required during operation, including when the device is generating the maximum expected output power. In this case, a target drain current of 120 mA was chosen. Set the target value by attaching a 2.05 kΩ ground referenced resistor to the ISENSE pin (Pin 25) on the HMC920LP5E.

To ensure adequate headroom, the supply voltage for the HMC920LP5E must be set higher than the target drain voltage to the HMC1126ACEZ (5 V). Accordingly, VDD1 and VDD2 on the HMC920LP5E are set to 5.3 V.

The voltage on the LDOCC pin (Pin 29) on the HMC920LP5E drives the VDRAIN pins which in turn drive the V_{DD} pin of the HMC1126ACEZ. Because the LDOCC output is connected to the VDRAIN output through an internal metal-oxide semiconductor field effect transistor (MOSFET) switch with an on resistance of 0.5 Ω, the LDOCC voltage (V_{LDOCC}) must be set slightly higher than the target drain voltage to the HMC1126ACEZ. To determine the required LDOCC voltage, use the following equation:

$$V_{LDOCC} = VDRAIN + IDRAIN \times 0.5$$

Therefore, V_{LDOCC} = 5 V+ (0.12 × 0.5) = 5.06 V.

To set V_{LDOCC} to 5.06 V, use the following equation with R5 set to 10 kΩ:

$$R10 = (R5/2) \times (V_{LDOCC} - 2)$$

Therefore, $R10$ = (10000/2) × (5.06 – 2) = 15.3 kΩ.

Setting $V_{GG}1$ and $V_{GG}2$

The $V_{GG}2$ fixed bias voltage is set to 1 V using a resistor divider that is derived from VDD1 and VDD2 on the HMC920LP5E. Because the current into the $V_{GG}2$ pin is low (<1 mA), large resistor values in the kΩ range can be used to set the $V_{GG}2$ voltage and save on overall current usage.

The recommended minimum voltage for $V_{GG}1$ into the HMC1126ACEZ is −2 V, which is also the default value for the VNEGIN pin on the HMC920LP5E. As a result, there is no need to adjust the VNEGIN and VGATE voltages.

Refer to the HMC920LP5E data sheet for the detailed schematic.

APPLICATIONS INFORMATION

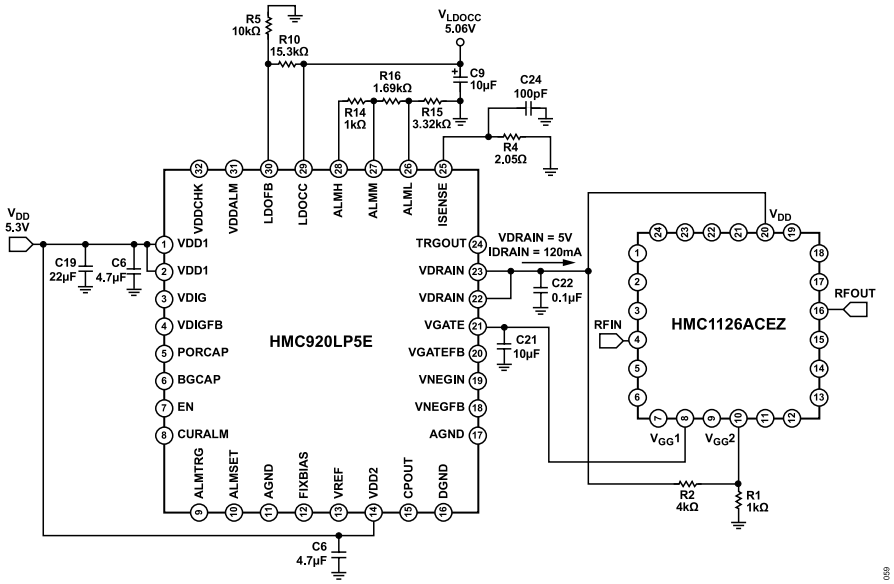

Figure 59. Application Circuit Using the HMC920LP5E with the HMC1126ACEZ (Additional Circuitry Omitted for Clarity)

HMC920LP5E Bias Sequence

When the HMC920LP5E bias control circuit is set up, the HMC1126ACEZ bias can be toggled on and off by applying 3.5 V (high) or 0 V (low) to the EN pin of the HMC920LP5E. If EN is left floating, the pin floats high. When EN is set to 3.5 V, VGATE initially drops to −2 V, and VDRAIN rises to 5 V. Then, VGATE and $V_{GG}1$ increase until IDRAIN equals 120 mA. The closed control loop then regulates IDRAIN to 120 mA. When the EN pin goes low, VGATE and $V_{GG}1$ drop back to −2 V and VDRAIN drops to 0 V.

APPLICATIONS INFORMATION

CONSTANT DRAIN CURRENT BIASING VS. CONSTANT GATE VOLTAGE BIASING

Voltage Biasing

The HMC920LP5E uses closed loop feedback to continuously adjust VGATE to maintain a constant drain current bias over the dc supply variation, temperature, and part to part variations. Constant drain current bias is an ideal method for reducing time in calibration procedures and maintaining consistent performance over time.

In comparison to a constant gate voltage bias, where the current increases dynamically when the RF power is applied, a constant drain current bias results in constant power consumption.

The OP1dB performance for the constant drain current bias can be varied by varying the bias setpoint. By increasing the bias current, OP1dB increases, as shown in Figure 66. The trade-off with a constant drain current is that this higher drain current is present for all RF input and output power levels.

The current and temperature limit of I_{DD} under the constant current operation is usually set by the thermal limitations detailed in the Absolute Maximum Ratings section (see the continuous power dissipation specification in Table 5). Increasing I_{DD} does not indefinitely increase OP1dB. Therefore, consider the trade-off between the power dissipation and OP1dB performance when using a constant drain current bias.

The performance of the constant drain current circuit is summarized in Figure 60 to Figure 67. These figures include comparisons with a constant gate voltage bias. Note that Figure 60 indicates a current consumption of 140 mA, which includes the complete current consumption of the circuit, that is, 120 mA drain current for the HMC1126ACEZ and an additional 20 mA of quiescent current in the HMC920LP5E. Using 140 mA as the current consumption also results in lower PAE compared to a constant gate voltage bias.

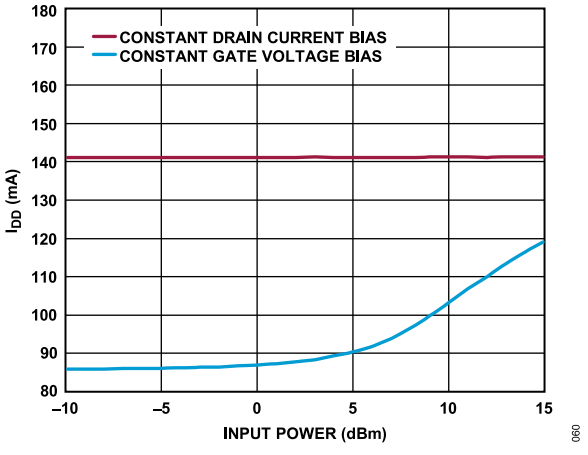

Figure 60. I_{DD} vs. Input Power, V_{DD} = 5 V, Frequency = 26 GHz, Constant Drain Current Bias (I_{DD} = 140 mA) and Constant Gate Voltage Bias

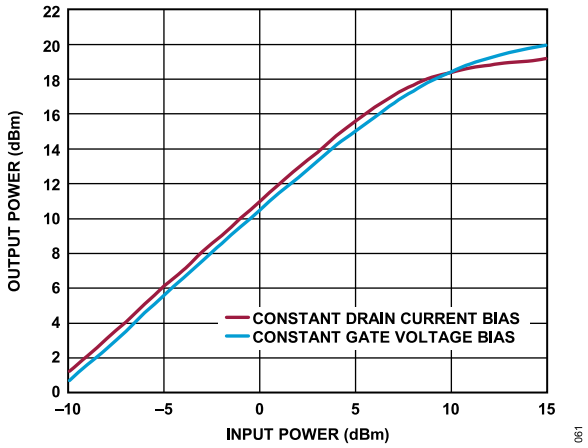

Figure 61. Output Power vs. Input Power, V_{DD} = 5 V, Frequency = 26 GHz, Constant Drain Current Bias (I_{DD} = 140 mA) and Constant Gate Voltage Bias

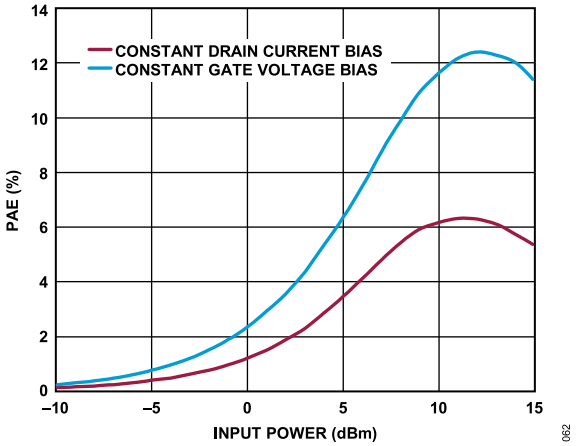

Figure 62. PAE vs. Input Power, V_{DD} = 5 V, Frequency = 26 GHz,Constant Drain Current Bias (I_{DD} = 140 mA) and Constant Gate Voltage Bias

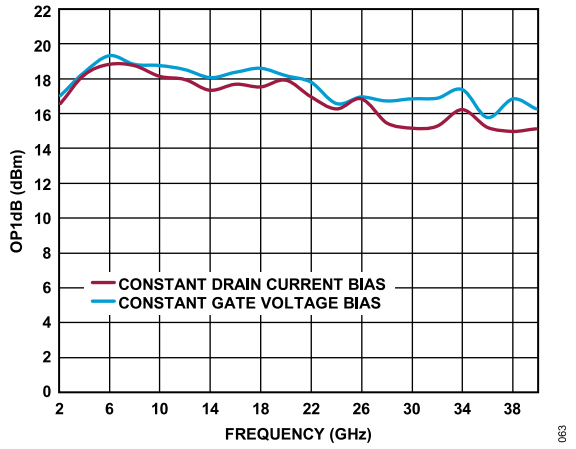

Figure 63. OP1dB vs. Frequency, V_{DD} =5 V, Constant Drain Current Bias (I_{DD} = 140 mA) and Constant Gate Voltage Bias

APPLICATIONS INFORMATION

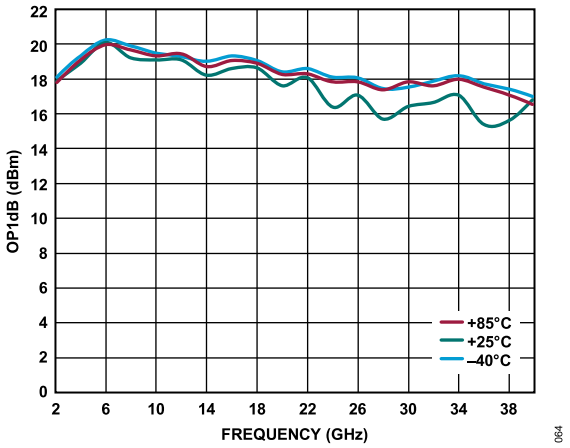

Figure 64. OP1dB vs. Frequency for Various Temperatures, Data Measured with Constant Drain Current

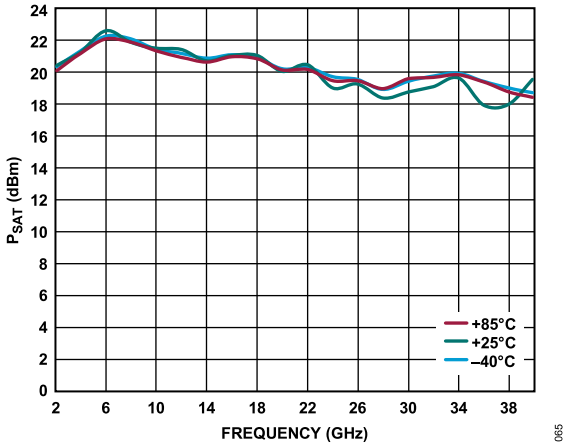

Figure 65. P_{SAT} vs. Frequency for Various Temperatures,Data Measured with Constant Drain Current

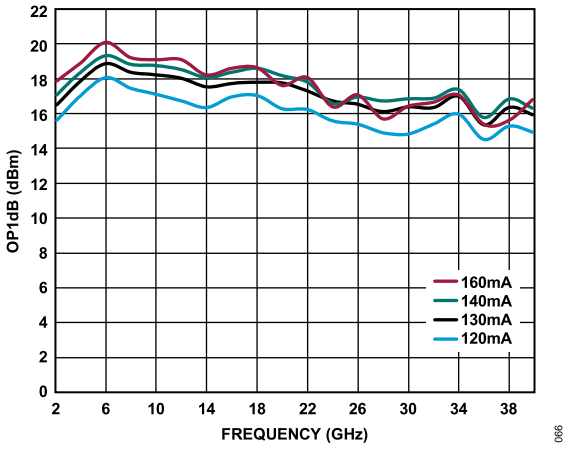

Figure 66. OP1dB vs. Frequency for Various Drain Currents, Data Measured with Constant Drain Current Bias

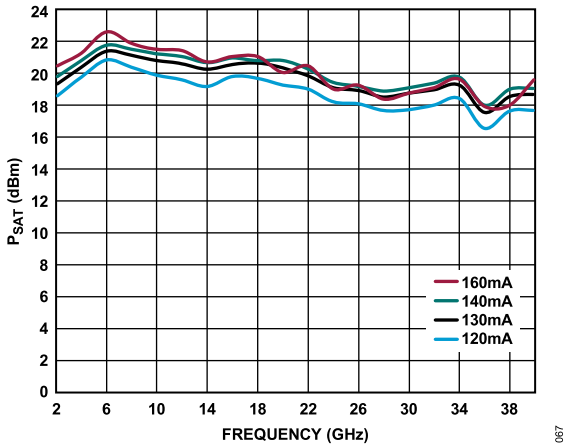

Figure 67. P_{SAT} vs. Frequency for Various Drain Currents,Data Measured with Constant Drain Current Bias