HMC374SC70E

v01.0814

GaAs pHEMT LOW NOISE AMPLIFIER 0.3 - 3.0 GHz

Typical Applications

The HMC374SC70E is ideal for:

- Cellular/PCS/3G
- WCS, MMDS & ISM
- Fixed Wireless & WLAN
- Private Land Mobile Radio

Features

Single Supply: Vdd = +3.0 to +3.6V

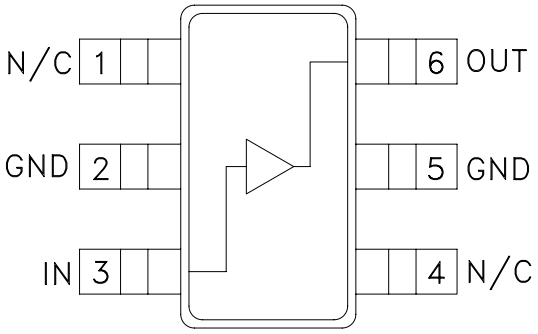
Broadband Performance

Low Noise Figure: 1.6 dB

High Output IP3: +35 dBm

High Gain: 15 dB @ 0.6 GHz

Functional Diagram



General Description

The HMC374SC70E is a general purpose broadband Low Noise Amplifier (LNA) for use in the 0.3 - 3 GHz frequency range. The LNA provides 15 dB of gain and a 1.6 dB noise figure from a single positive supply of +3.0 to +3.6V. The low noise figure coupled with a high P1dB (17 dBm) and high OIP3 (35 dBm) make this part ideal for cellular applications. The compact LNA is designed for repeatable gain and noise figure performance. To minimize board area the design is offered in a low cost SC70E package that occupies only 0.089" x 0.053".

Electrical Specifications, Vdd= +3.3V

Parameter	Min. [2]	Typ.[1]	Max. [2]	Min. [2]	Typ. [1]	Max. [2]	Min. [2]	Typ. [1]	Max. [2]	Units
Frequency		0.6			1.0			3.0		GHz
Gain	14	15		13	14.5		6	8.5		dB
Gain Variation Over Temperature (-40°C to +25°C)		0.005			0.008			0.012		dB/°C
Gain Variation Over Temperature (+25 °C to +85 °C)		0.004			0.005			0.008		
Noise Figure		2	2.6		1.6	2.3		1.8	2.2	dB
Input Return Loss	4.5	5.5		6	7.5		8	9		
Output Return Loss	5.5	7.5		8	10		13	15		
Output 1 dB Compression (P1dB)	15.5	16.5		16	17		16.5	18		dBm
Saturated Output Power (Psat)	17.5	18.5		17.5	18.5		18	19		
Output Third Order Intercept (OIP3)		34			33.5			36		
Supply Current (Idd) (Vdd = +3.3V)		75			75			75		mA
Supply Voltage (Vdd)	3.0	3.3	3.6	3.0	3.3	3.6	3.0	3.3	3.6	V

[1] Typical values are determined at T_A=+25°C

[2] Minimum and maximum values are determined from T_A=-40°C to T_A=+85°C

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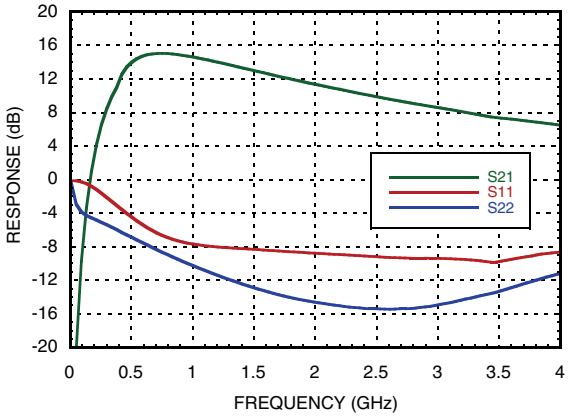
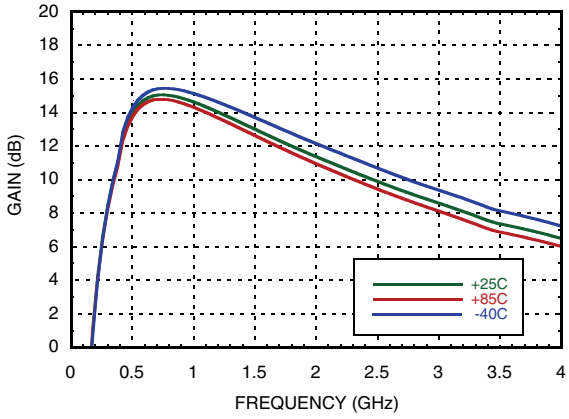
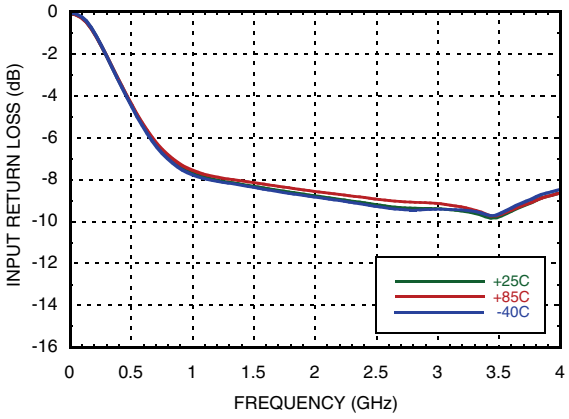
Broadband Gain & Return Loss



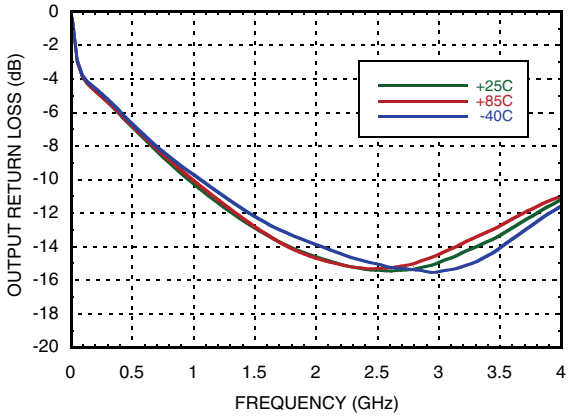
Gain vs. Temperature



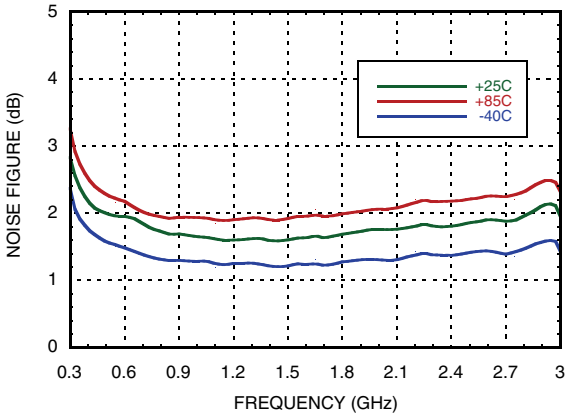
Input Return Loss vs. Temperature



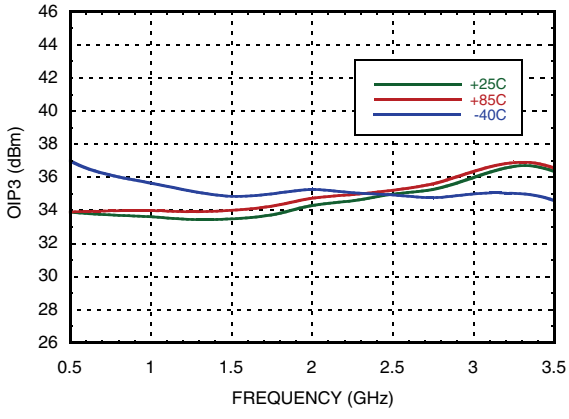
Output Return Loss vs. Temperature



Noise Figure vs. Temperature



Output IP3 vs. Temperature [1]



[1] OIP3 measurements were taken for Pout = 0 dBm

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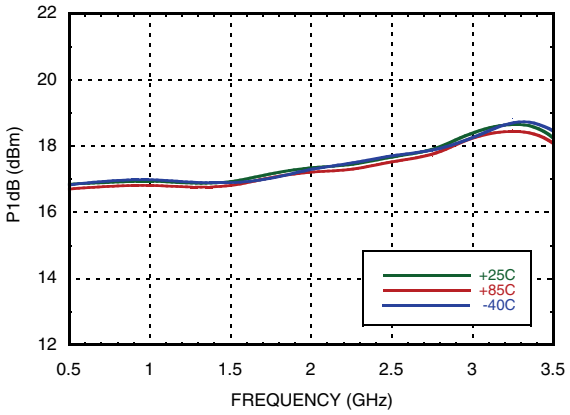
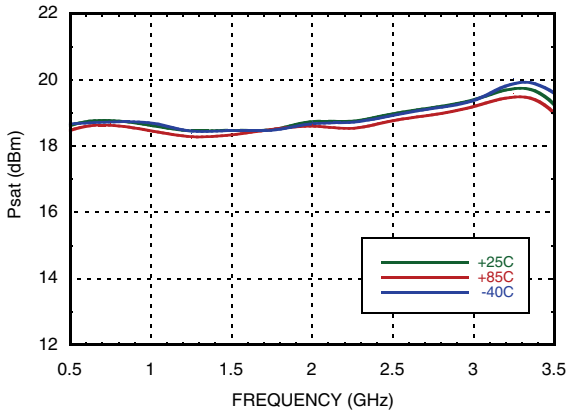
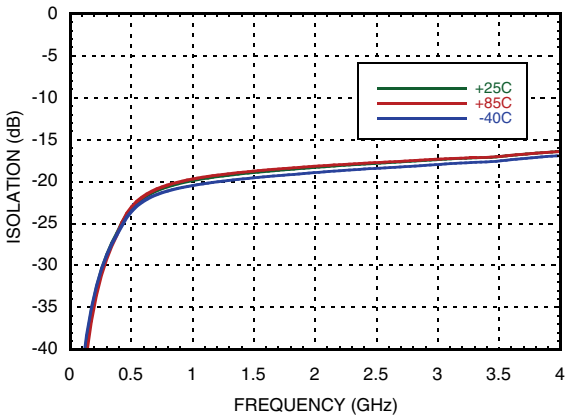
Output P1dB vs. Temperature



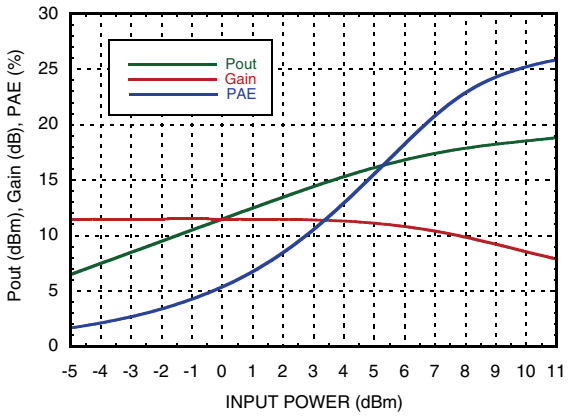
Output Psat vs. Temperature



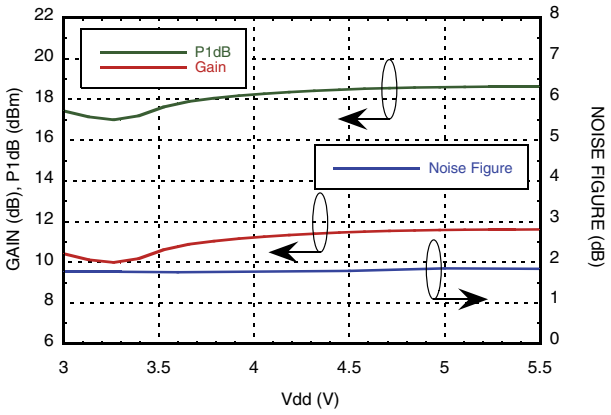
Reverse Isolation vs. Temperature



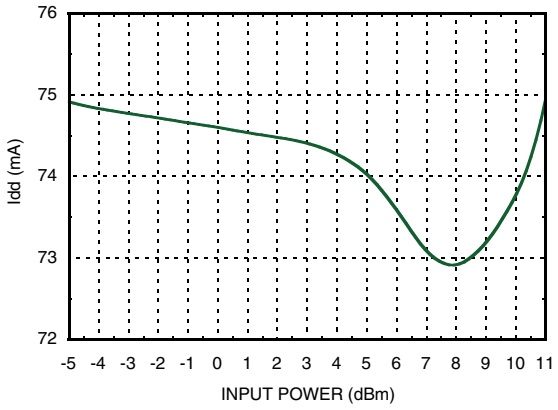
Pout, Gain & PAE @ 2 GHz



Gain, Noise Figure & P1dB vs. Supply Voltage @ 2 GHz



Supply Current vs. Input Power @ 2 GHz



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Absolute Maximum Ratings

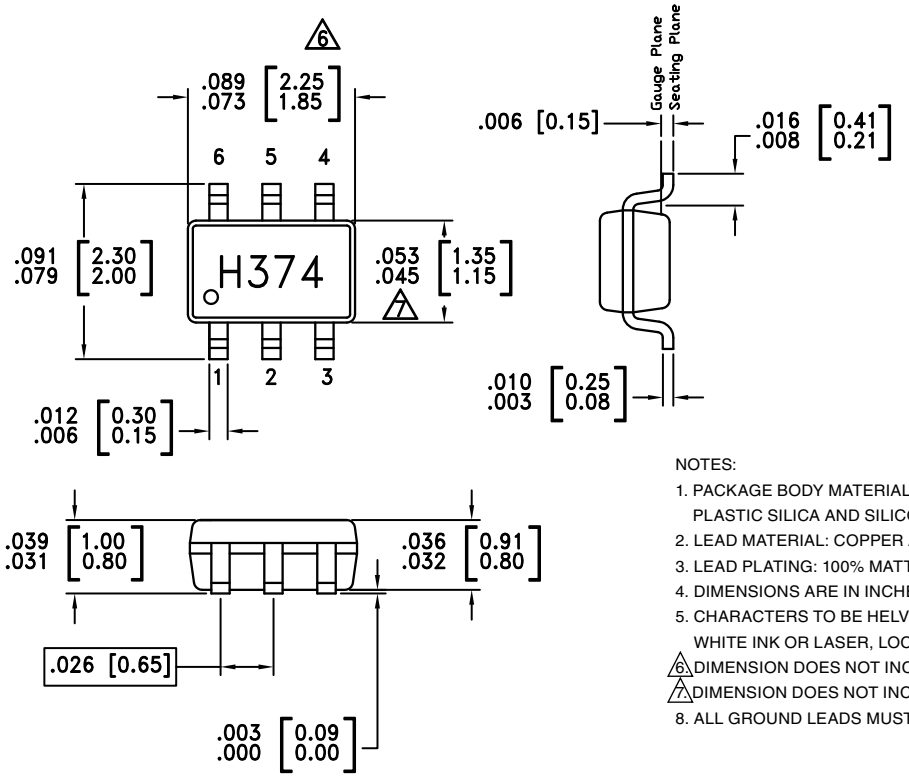
Drain Bias Voltage (Vdd)	+7.0 Vdc
RF Input Power (RFIN)(Vdd = +5.0 Vdc)	15 dBm
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 4.88 mW/°C above 85 °C)	0.32 W
Thermal Resistance (channel to lead)	205 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 0

Typical Supply Current vs. Vdd

Vdd (V)	Idd (mA)
3	75
3.3	75
3.6	75

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD MATERIAL: COPPER ALLOY
3. LEAD PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS]
5. CHARACTERS TO BE HELVETICA MEDIUM, .015 HIGH, WHITE INK OR LASER, LOCATED APPROXIMATELY AS SHOWN.
6. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.15mm PER SIDE.
7. DIMENSION DOES NOT INCLUDE MOLDFLASH OF 0.25mm PER SIDE.
8. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC374SC70E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H374E XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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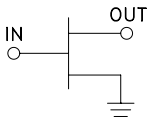
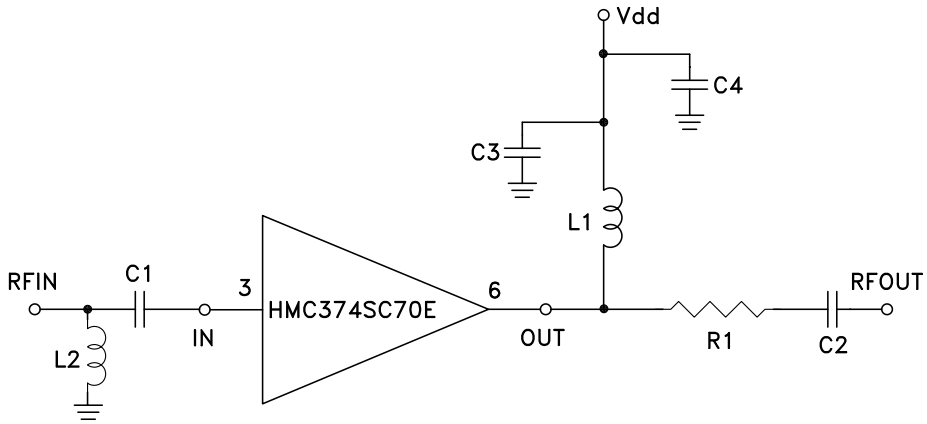
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1,4	N/C	These pins may be connected to RF/DC ground. Performance will not be affected.	
2, 5	GND	These pins must be connected to RF/DC ground.	
3	IN	RF input pin is DC coupled. An off-chip DC blocking capacitor is required.	
6	OUT	RF output and DC Bias for the output stage. See application circuit for off-chip components.	

Application Circuit



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