0.2 GHz to 8 GHz, GaAs, HBT MMIC, Divide by 8 Prescaler

Enhanced Product

HMC434-EP

FEATURES

Ultralow SSB phase noise: −150 dBc/Hz typical
Single-ended input/outputs
RF output power: −2 dBm typical
Single-supply operation: 3 V
Ultrasmall, surface-mount, 2.90 mm × 2.80 mm, 6-lead SOT-23 package

ENHANCED PRODUCT FEATURES

Supports defense and aerospace applications (AQEC standard)
Extended industrial temperature range: −55°C to +105°C
Controlled manufacturing baseline
1 assembly/test site
1 fabrication site
Product change notification
Qualification data available upon request

APPLICATIONS

DC to C band PLL prescalers
Very small aperture terminal (VSAT) radios
Unlicensed national information infrastructure (UNII) and point to point radios
IEEE 802.11a and high performance radio local area network (HiperLAN) WLAN
Fiber optics
Cellular/3G infrastructure

FUNCTIONAL BLOCK DIAGRAM

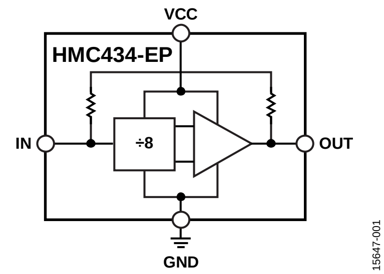

Figure 1.

GENERAL DESCRIPTION

The HMC434-EP is a low noise, static, divide by 8 prescaler monolithic microwave integrated circuit (MMIC) utilizing indium gallium phosphide/gallium arsenide (InGaP/GaAs) heterojunction bipolar transistor (HBT) technology in an ultrasmall surface-mount 6-lead SOT-23 package.

The HMC434-EP operates from near dc (square wave) or 0.2 GHz (sine wave) to 8 GHz input frequency with a single 3 V dc supply.

The HMC434-EP features single-ended inputs and outputs for reduced component count and cost. The low additive single sideband (SSB) phase noise of −150 dBc/Hz at 100 kHz offset helps the user maintain optimal system noise performance.

Additional application and technical information can be found in the HMC434 data sheet.

Rev. B **Document Feedback**

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REVISION HISTORY

3/2019—Rev. A to Rev. B

Changes to Figure 11 6

8/2017—Rev. 0 to Rev. A

Changes to Features Section and General Description Section 1
Added Endnote 2 to Table 1 3

3/2017—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = 3 V, T_A = 25°C, 50 Ω system, unless otherwise noted. P_{IN} is input power.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions / Comments
RADIO FREQUENCY (RF) INPUT					
Frequency[1, 2]	0.2		8	GHz	Sine wave input
Power	−10	0	+10	dBm	f_{IN} = 1.0 GHz to 3.0 GHz
	0	0	10	dBm	f_{IN} = 3.0 GHz to 8.0 GHz
RF OUTPUT					
SSB Phase Noise		−150		dBc/Hz	100 kHz offset, P_{IN} = 0 dBm, f_{IN} = 4.0 GHz
Power	−5	−2		dBm	f_{IN} = 1.0 GHz to 8.0 GHz
REVERSE LEAKAGE		−25		dBm	P_{IN} = 0 dBm, f_{IN} = 4.0 GHz , output terminated
SUPPLY					
Voltage (V_{CC})	2.85	3	3.15	V	
Current (I_{CC})		62	83	mA	

[1] Below 200 MHz, a square wave input is required.
[2] For stable operation without an input signal, refer to the AN-1463 Application Note, *Frequency Divider Operation and Compensation with No Input Signal*.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (V_{CC})	−0.3 V to +3.5 V
RF Input Power (V_{CC} = 3 V)	13 dBm
Temperature	
Operating	−55°C to +105°C
Storage	−65°C to +125°C
Junction, T_J	135°C
Nominal (T_A = 105°C)	119°C
Reflow	260°C
ESD Sensitivity	
Human Body Model (HBM)	Class 0

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the natural convection junction to ambient thermal resistance measured in a one cubic foot sealed enclosure. θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JA}[1]	θ_{JC}[2]	Unit
RJ-6	359	70	°C/W

[1] Simulated values per JEDEC JESD51-12 standards.
[2] Junction to GND package pin.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

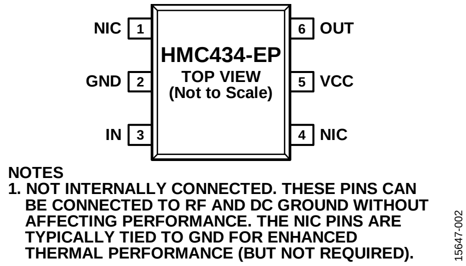

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4	NIC	Not Internally Connected. These pins can be connected to RF and dc ground without affecting performance. The NIC pins are typically tied to GND for enhanced thermal performance (but not required).
2	GND	Ground. This pin must be connected to both RF and dc ground.
3	IN	RF Input. This pin must be dc blocked.
5	VCC	Supply Voltage (3 V).
6	OUT	RF Output. This pin must be dc blocked.

INTERFACE SCHEMATICS

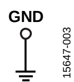

Figure 3. GND Interface Schematic

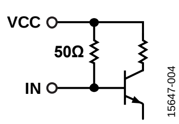

Figure 4. IN Interface Schematic

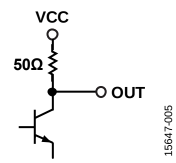

Figure 5. OUT Interface Schematic

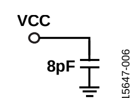

Figure 6. VCC Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

In Figure 9, $P_{FEEDTHROUGH}$ is the power of the output spectrum at the input frequency.

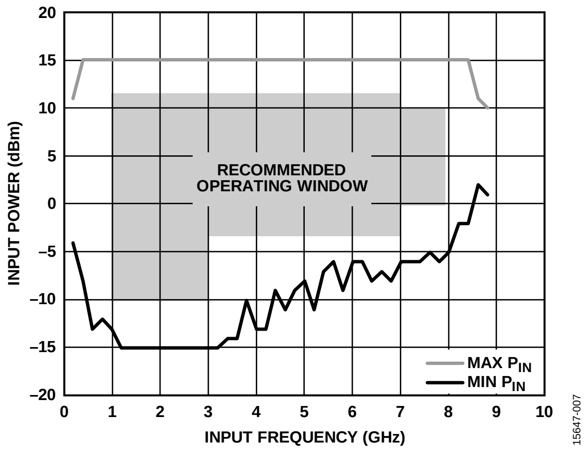

Figure 7. Input Sensitivity Window

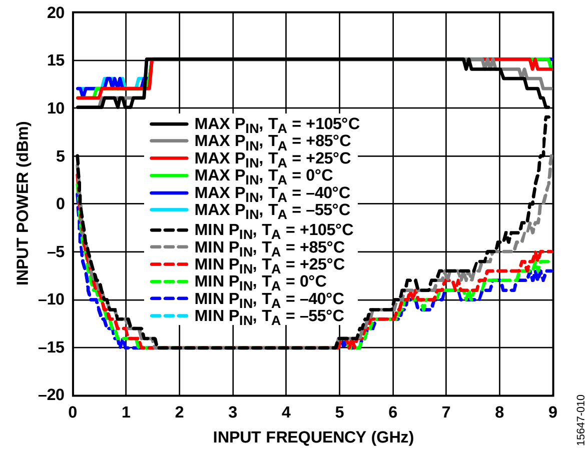

Figure 10. Input Sensitivity Window at Various Temperatures

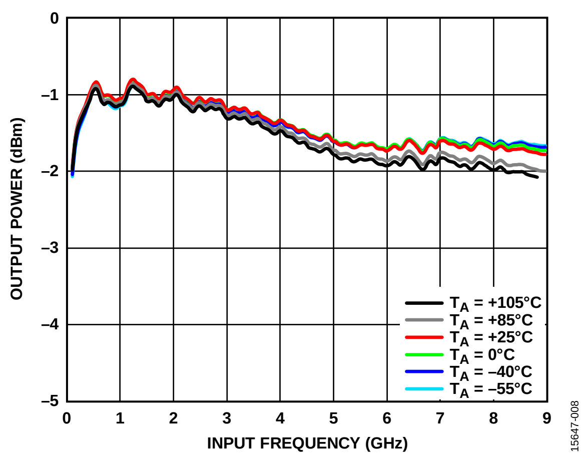

Figure 8. Output Power vs. Frequency at Various Temperatures

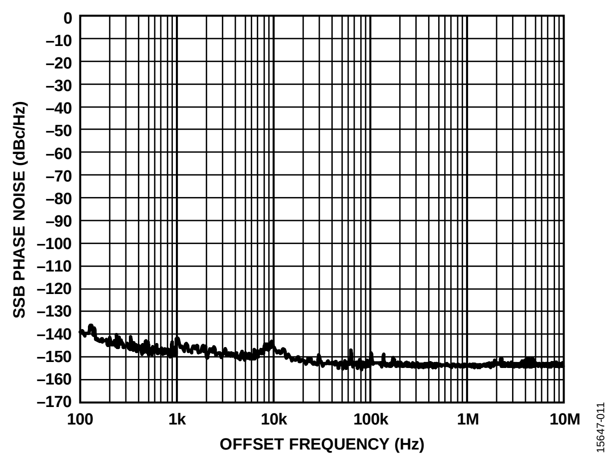

Figure 11. SSB Phase Noise (P_{IN} = 0 dBm)

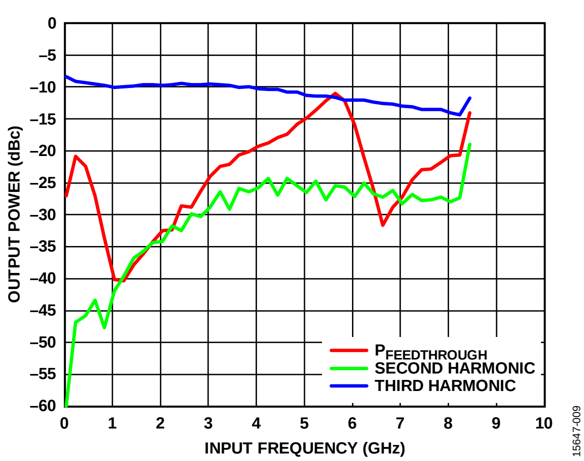

Figure 9. Output Harmonic Content (P_{IN} = 0 dBm)

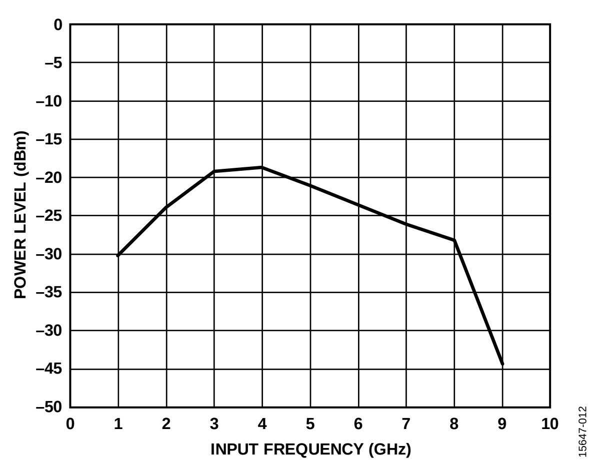

Figure 12. Reverse Leakage (P_{IN} = 0 dBm)