HMC539ALP3/539ALP3E

v01.0416

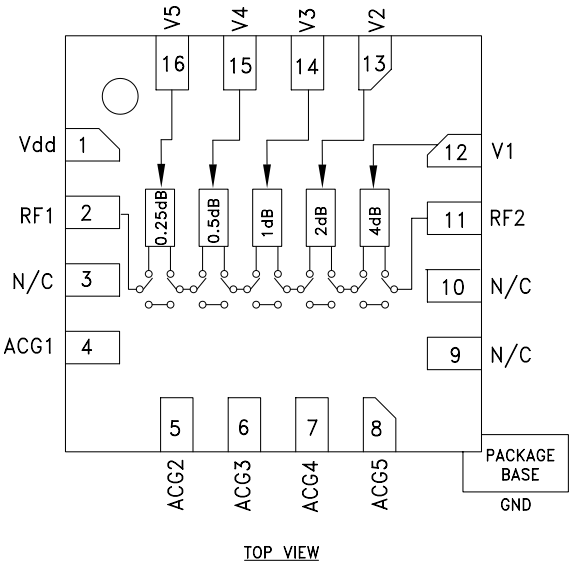
0.25 dB LSB GaAs MMIC 5-BIT DIGITAL POSITIVE CONTROL ATTENUATOR, DC - 4 GHz

Typical Applications

The HMC539ALP3/539ALP3E is ideal for both RF and IF applications:

- Cellular Infrastructure
- ISM, MMDS, WLAN, WiMAX, WiBro
- Microwave Radio & VSAT
- Test Equipment and Sensors

Functional Diagram



Features

0.25 dB LSB Steps to 7.75 dB

± 0.05 dB Typical Step Error

Low Insertion Loss: 0.7 dB

High IP3: +62 dBm

Single Control Line Per Bit

TTL/CMOS Compatible Control

Single +3V to +5V Supply

3x3 mm SMT Package

General Description

The HMC539ALP3/539ALP3E is a broadband 5-bit GaAs IC digital attenuator in a low cost leadless surface mount package. This single positive control line per bit digital attenuator utilizes an off chip AC ground capacitor for near DC operation, making it suitable for a wide variety of RF and IF applications. Covering DC to 4 GHz, the insertion loss is less than 0.7 dB typical. The attenuator bit values are 0.25 (LSB), 0.5, 1, 2, and 4 dB for a total attenuation of 7.75 dB. Attenuation accuracy is excellent at ± 0.05 dB typical step error. The attenuator also features a high IIP3 of +62 dBm. Five TTL/CMOS control inputs are used to select each attenuation state. A single Vdd bias of +3V to +5V is required.

Electrical Specifications, T_A = +25° C, With Vdd = +5V & Vctl = 0/+5V (Unless Otherwise Noted)

Parameter		Frequency (GHz)	Min.	Typ.	Max.	Units
Insertion Loss		DC - 1.5 GHz 1.5 - 3.0 GHz 3.0 - 4.0 GHz		0.7 1.0 1.3	1.0 1.3 1.7	dB dB dB
Attenuation Range		DC - 4 GHz		7.75		dB
Return Loss (RF1 & RF2, All Atten. States)		DC - 3 GHz 3.0 - 4.0 GHz		27 25		dB dB
Attenuation Accuracy: (Referenced to Insertion Loss)	All States	DC - 3 GHz 3.0 - 4.0 GHz	± (0.2 + 2% of Atten. Setting) Max. ± (0.2 + 4% of Atten. Setting) Max.			dB dB
Input Power for 0.1 dB Compression		0.1 - 4.0 GHz		32		dBm
Input Third Order Intercept Point (Two-Tone Input Power= 15 dBm Each Tone)		0.1 - 4.0 GHz		62		dBm
Switching Characteristics tRISE, tFALL (10/90% RF) tON, tOFF (50% CTL to 10/90% RF)		DC - 4 GHz		 45 52		 ns ns

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

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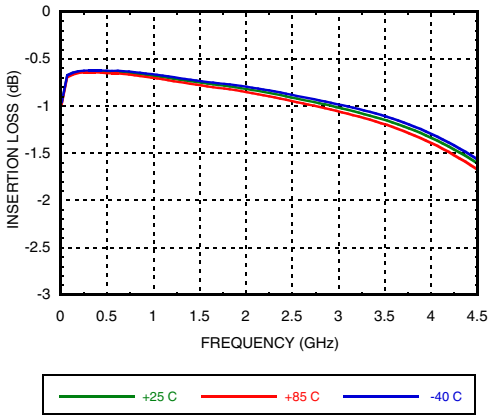
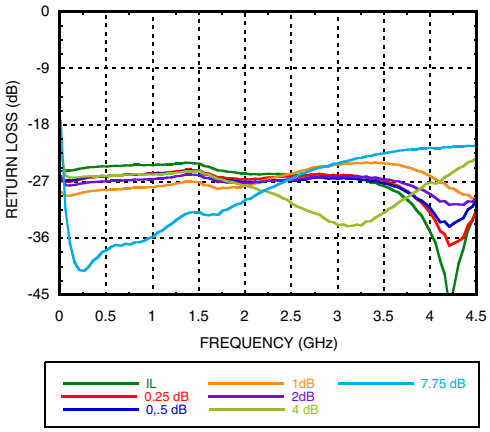
Insertion Loss



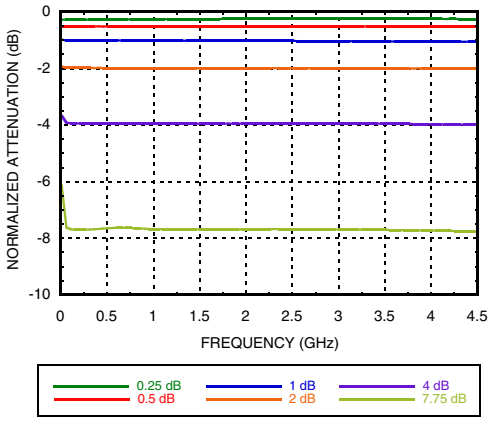
Return Loss RF1, RF2

(Only Major States are Shown)

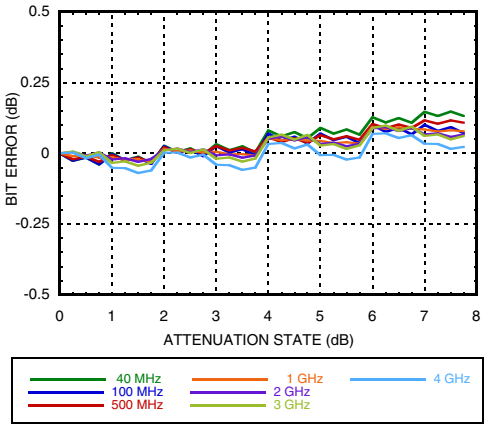


Normalized Attenuation

(Only Major States are Shown)

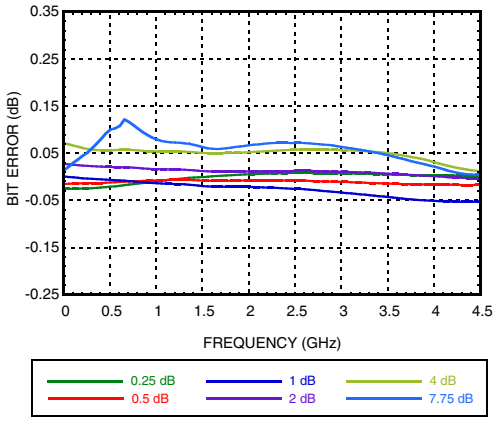


Bit Error vs. Attenuation State



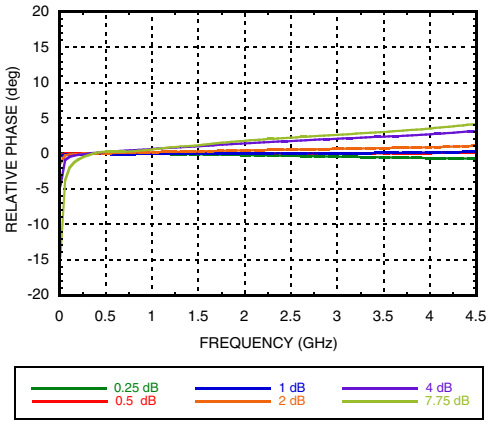
Bit Error vs. Frequency

(Only Major States are Shown)



Relative Phase vs. Frequency

(Only Major States are Shown)



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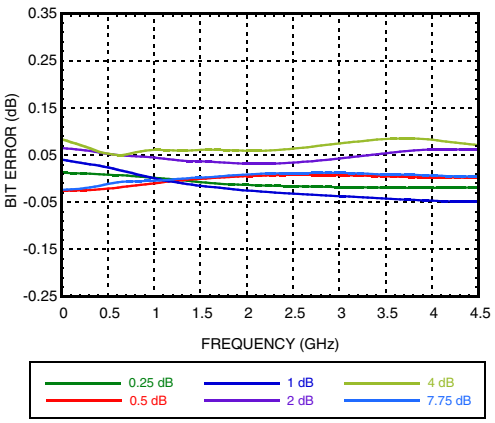
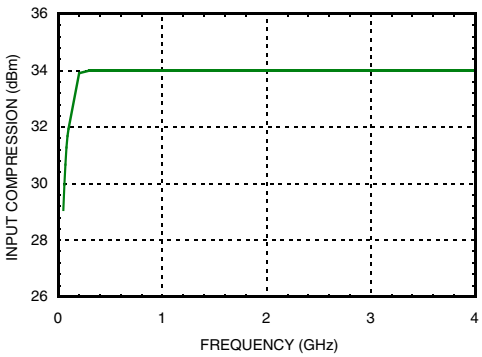
Step Error vs. Frequency

(Only Major States are Shown)



1dB Input Compression Point



Bias Voltage & Current

Vdd = +5.0 Vdc ± 10%	
Vdd (VDC)	Idd (Typ.) (mA)
+3.0	1.6
+5.0	1.7

Control Voltage

State	Vdd = +3V	Vdd = +5V
Low	0 to 0.8V @ <1 uA	0 to +1.1V @ 33uA Typ.
High	1.2 to 3.3V @ <1 uA	1.8V to +5.0V @ 33uA Typ.

Truth Table

Control Voltage Input					Attenuation State RF1 - RF2
V1 4 dB	V2 2 dB	V3 1 dB	V4 0.5 dB	V5 0.25 dB	
High	High	High	High	High	Reference I.L.
High	High	High	High	Low	0.25 dB
High	High	High	Low	High	0.5 dB
High	High	Low	High	High	1 dB
High	Low	High	High	High	2 dB
Low	High	High	High	High	4 dB
Low	Low	Low	Low	Low	7.75 dB
Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.					

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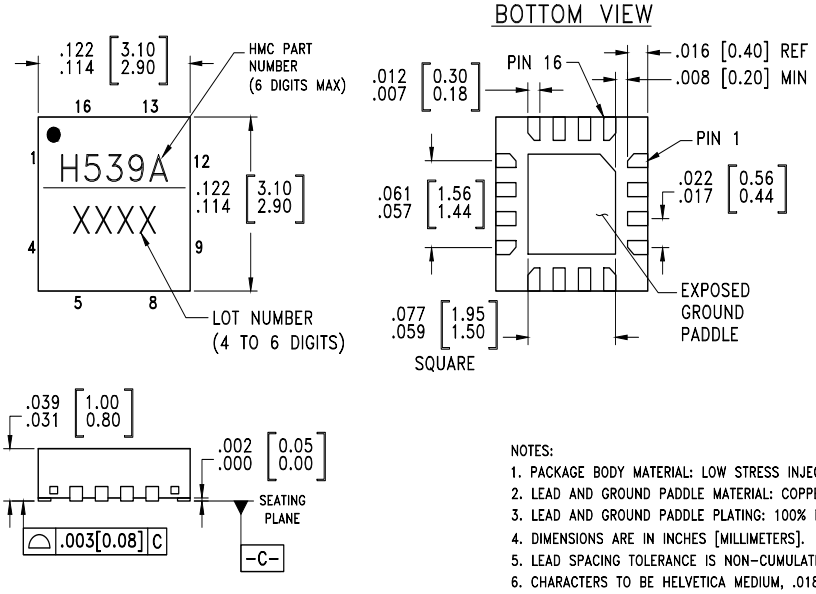
Absolute Maximum Ratings

RF Input Power (DC - 4 GHz)	+29 dBm (T = +85 °C)
Control Voltage Range (V1 to V5)	-1V to Vdd +1V
Bias Voltage (Vdd)	+7.0 Vdc
Channel Temperature	150 °C
Continuous Pdiss (T = 85 °C) (derate 12.0 mW/°C above 85 °C)	0.551 W
Thermal Resistance	118 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. CHARACTERS TO BE HELVETICA MEDIUM, .018 HIGH, WHITE INK, OR LASER MARK LOCATED APPROX. AS SHOWN.
7. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.05mm MAX.
8. PACKAGE WARP SHALL NOT EXCEED 0.05mm
9. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
10. REFER TO ADI APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC539ALP3	Low Stress Injection Molded Plastic	Sn/Pb solder	MSL3 [1]	H539A XXXX
HMC539ALP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL3 [2]	H539A XXXX

[1] Max peak reflow temperature of 235 °C
[2 Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

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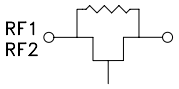
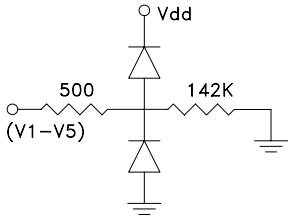
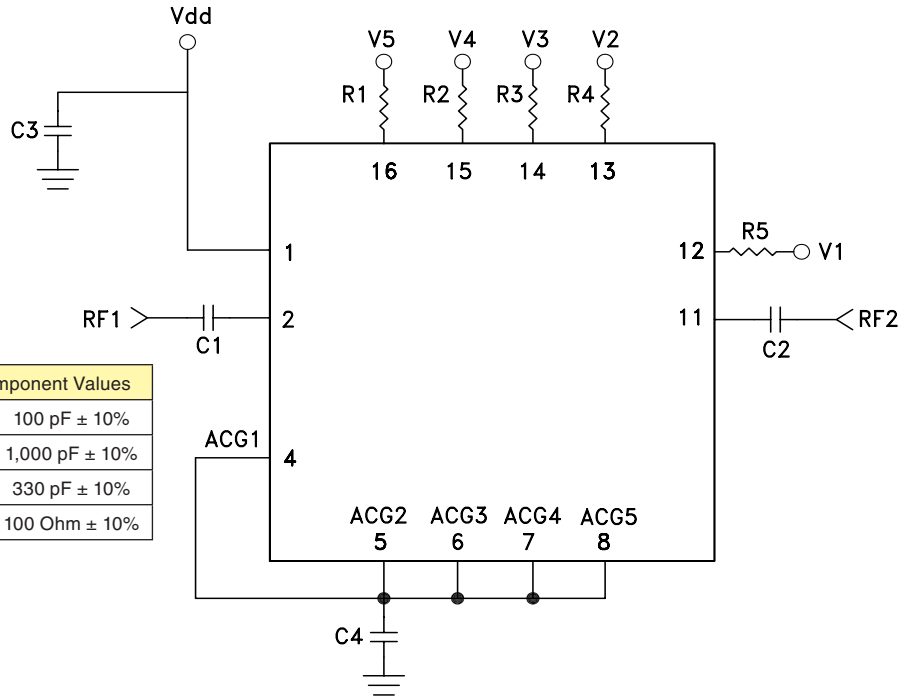
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	Vdd	Supply Voltage.	
2, 11	RF1, RF2	This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required. Select value based on lowest frequency of operation.	
3, 9, 10	N/C	These pins should be connected to PCB RF ground to maximize performance.	
4 - 8	ACG1 - ACG5	External capacitor to ground is required. Select value for lowest frequency of operation. Place capacitor as close to pins as possible.	
12 - 16	V1 - V5	See truth table and control voltage table.	
	GND	Package bottom has an exposed metal paddle that must be connected to RF Ground.	

Application Circuit



Recommended Component Values	
C1, C2	100 pF ± 10%
C3	1,000 pF ± 10%
C4	330 pF ± 10%
R1 - R5	100 Ohm ± 10%