HMC561

v04.0714

GaAs MMIC x2 ACTIVE FREQUENCY MULTIPLIER, 8 - 21 GHz OUTPUT

Typical Applications

The HMC561 is suitable for:

- Clock Generation Applications: SONET OC-192 & SDH STM-64
- Point-to-Point & VSAT Radios
- Test Instrumentation
- Military & Space

Features

High Output Power: +17 dBm

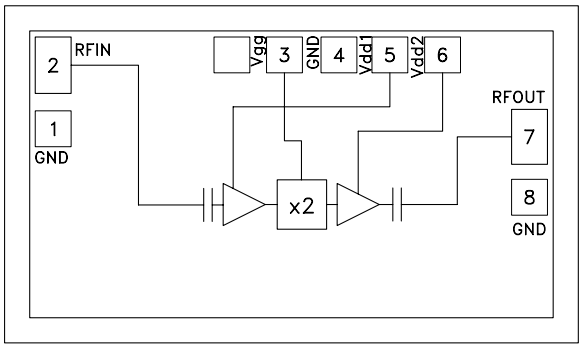
Low Input Power Drive: 0 to +6 dBm

Fo Isolation: 15 dBc @ Fout= 16 GHz

100 KHz SSB Phase Noise: -139 dBc/Hz

Die Size: 1.6 x 0.9 x 0.1 mm

Functional Diagram



General Description

The HMC561 is a x2 active broadband frequency multiplier chip utilizing GaAs PHEMT technology. When driven by a +5 dBm signal, the multiplier provides +17 dBm typical output power from 8 to 21 GHz and the Fo and 3Fo isolations are 15 dBc at 16 GHz. The HMC561 is ideal for use in LO multiplier chains for Pt to Pt & VSAT Radios yielding reduced parts count vs. traditional approaches. The low additive SSB Phase Noise of -139 dBc/Hz at 100 kHz offset helps maintain good system noise performance.

Electrical Specifications, T_A = +25°C, Vdd1 = Vdd2 = +5V, 5 dBm Drive Level [1]

Parameter	Min.	Typ.	Max.	Units
Frequency Range, Input		4 - 10.5		GHz
Frequency Range, Output		8 - 21		GHz
Output Power	14	17		dBm
Fo Isolation (with respect to output level)		15		dBc
3Fo Isolation (with respect to output level)		15		dBc
4Fo Isolation (with respect to output level)		15		dBc
Input Return Loss		15		dB
Output Return Loss		12		dB
SSB Phase Noise (100 kHz Offset)		-139		dBc/Hz
Supply Current (Idd) (Vdd1= Vdd2= +5V, Vgg = -1.7V Typ.)		98	126	mA

[1] Adjust Vgg between -2.0 and -1.2V to achieve Idd1 + Idd2 = 98 mA.

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RoHS✓ EARTH FRIENDLY

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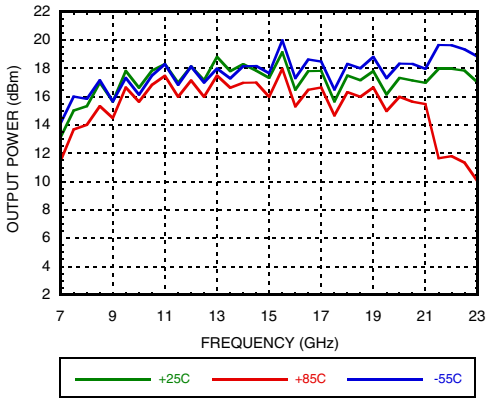
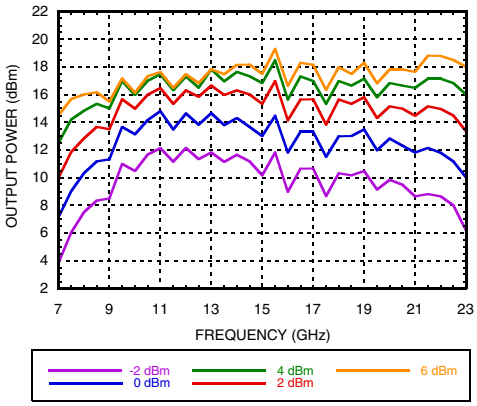
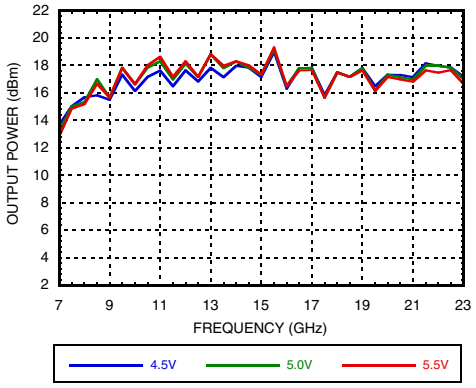
Output Power vs. Temperature @ 5 dBm Drive Level



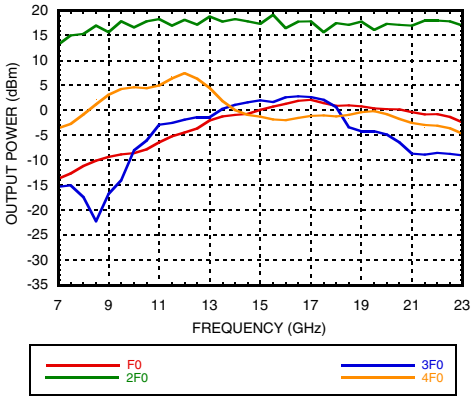
Output Power vs. Drive Level



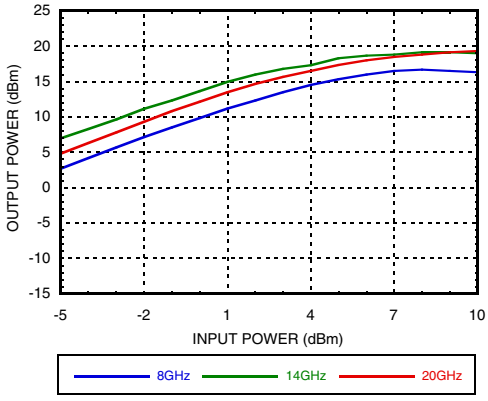
Output Power vs. Supply Voltage @ 5 dBm Drive Level



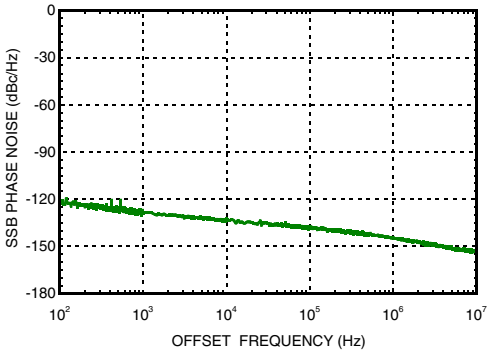
Isolation @ 5 dBm Drive Level



Output Power vs. Input Power



SSB Phase Noise Performance, Fout = 16 GHz, Input Power = +3 dBm



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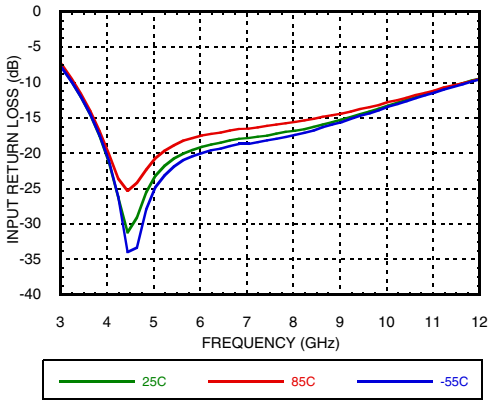
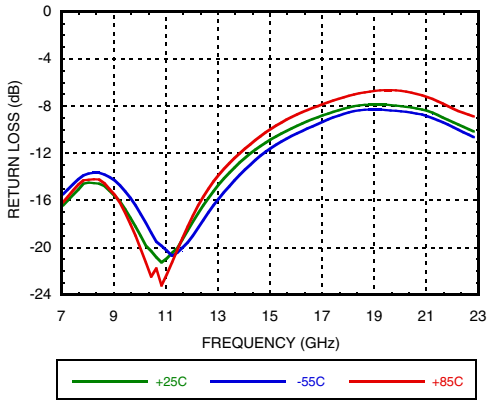
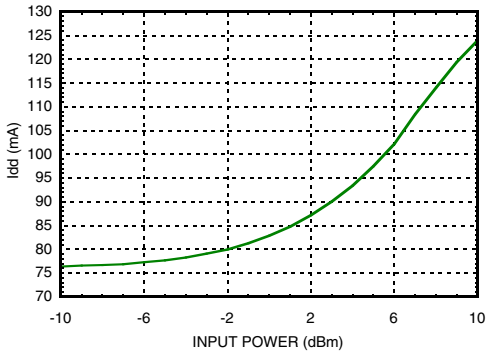
Input Return Loss vs. Temperature



Output Return Loss vs. Temperature



Supply Current vs. Input Power



Absolute Maximum Ratings

RF Input (Vdd1= Vdd2= +5V)	+10 dBm
Supply Voltage (Vdd1, Vdd2)	+5.5 Vdc
Channel Temperature	175 °C
Continuous Pdiss (T= 85 °C) (derate 10.4 mW/°C above 85 °C)	940 mW
Thermal Resistance (channel to die bottom)	95.9 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-55 to +85 °C

Typical Supply Current vs. Vdd1, Vdd2

Vdd1, Vdd2 (Vdc)	Idd1 + Idd2 (mA)
4.5	97
5.0	98
5.5	99

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

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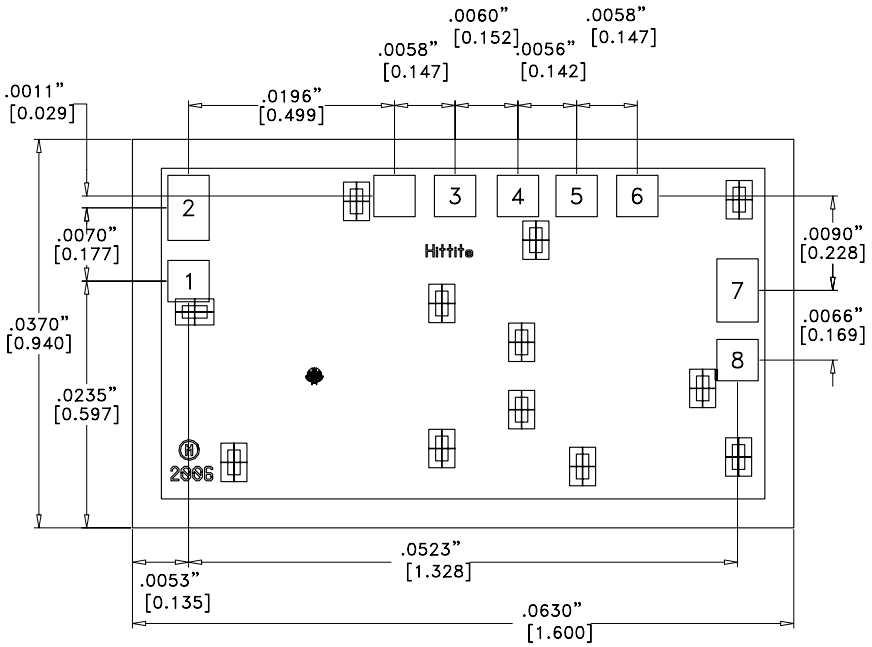
Outline Drawing



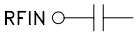
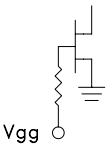
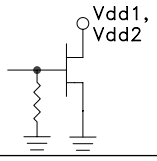
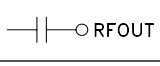
Die Packaging Information [1]

Standard	Alternate [2]
GP-2 (Gel Pack)	—

[1] Refer to the "Packaging Information" section for die packaging dimensions.
[2] Reference this suffix only when ordering alternate die packaging.

NOTES:
1. ALL DIMENSIONS ARE IN INCHES [MILLIMETERS].
2. DIE THICKNESS IS .004"
3. TYPICAL BOND PAD IS .004" SQUARE.
4. TYPICAL BOND SPACING IS .006" CENTER TO CENTER.
5. BOND PAD METALIZATION: GOLD
6. BACKSIDE METALIZATION: GOLD
7. BACKSIDE METAL IS GROUND.
8. NO CONNECTION REQUIRED FOR UNLABELED BOND PADS.

Pad Descriptions

Pad Number	Function	Description	Interface Schematic
1, 4, 8	GND	Die bottom must be connected to RF ground.	
2	RFIN	This pad is AC coupled and matched to 50 Ohms.	
3	Vgg	Gate control for multiplier. Adjust to achieve Idd of 98 mA. Please follow "MMIC Amplifier Biasing Procedure" Application note.	
5, 6	Vdd1, Vdd2	Supply voltage 5V ± 0.5V.	
7	RFOUT	This pad is AC coupled and matched to 50 Ohms.	

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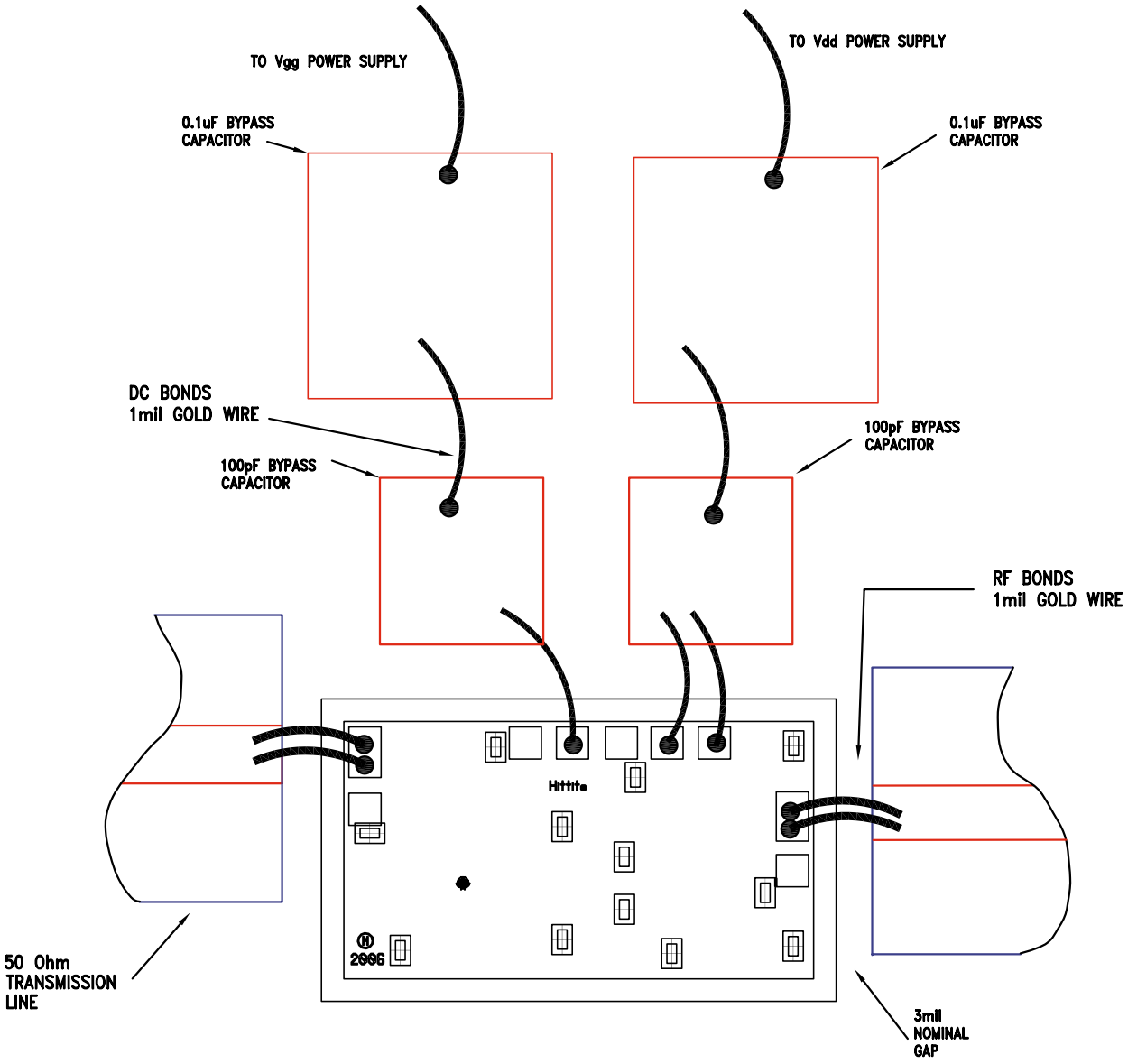
Assembly Diagram



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