

## GaAs MMIC 6-BIT DIGITAL PHASE SHIFTER, 2.5 - 3.1 GHz

### Typical Applications

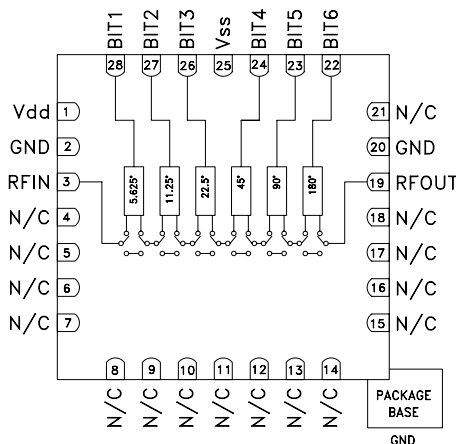
The HMC647ALP6E is ideal for:

- EW Receivers
- Weather & Military Radar
- Satellite Communications
- Beamforming Modules
- Phase Cancellation

### Features

- Low RMS Phase Error: 1.5°
- Low Insertion Loss: 4 dB
- High Linearity: +50 dBm
- Positive Control Logic
- 360° Coverage, LSB = 5.625°
- 28 Lead QFN Leadless SMT Package: 36mm<sup>2</sup>

### Functional Diagram



### General Description

The HMC647ALP6E is a 6-bit digital phase shifter which is rated from 2.5 to 3.1 GHz, providing 360 degrees of phase coverage, with a LSB of 5.625 degrees. The HMC647ALP6E features very low RMS phase error of 1.5 degrees and extremely low insertion loss variation of  $\pm 0.4$  dB across all phase states. This high accuracy phase shifter is controlled with positive control logic of 0/+5V. The HMC647ALP6E is housed in a compact 6x6 mm plastic leadless SMT package and is internally matched to 50 Ohms with no external components.

### Electrical Specifications

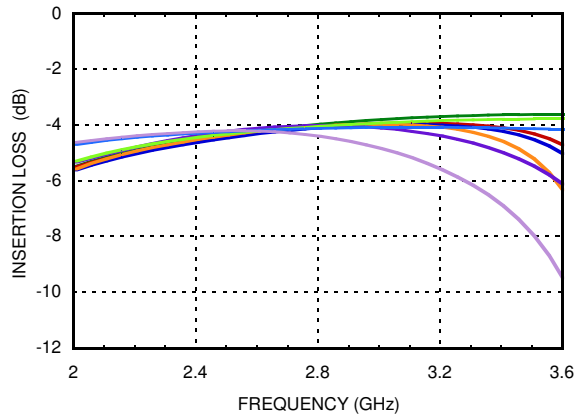
$T_A = +25^\circ\text{C}$ ,  $V_{SS} = -5\text{V}$ ,  $V_{DD} = +5\text{V}$ , control Voltage = 0/ +5V, 50 Ohm System

Parameter	Min.	Typ.	Max.	Units
Frequency Range	2.5		3.1	GHz
Insertion Loss*		4	6.5	dB
Input Return Loss*		16		dB
Output Return Loss*		16		dB
Phase Error*		$\pm 5$	+6 / -15	deg
RMS Phase Error		1.5		deg
Amplitude Settling Time (50% cntl to +/- 0.1dB margin of final RFout)		150		nS
Phase Settling Time (50% cntl to +/- 1 degree margin of final RFout)		125		nS
Insertion Loss Variation*		$\pm 0.4$		dB
Input Power for 1 dB Compression		31		dBm
Input Third Order Intercept		50		dBm
Control Voltage Current		35	250	$\mu\text{A}$
Bias Control Current		5	15	mA

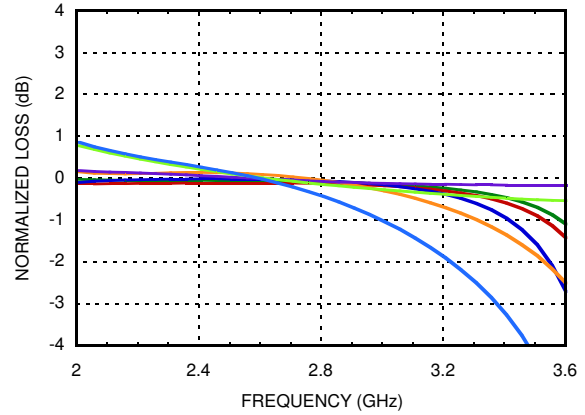
\*Note: Major States Shown

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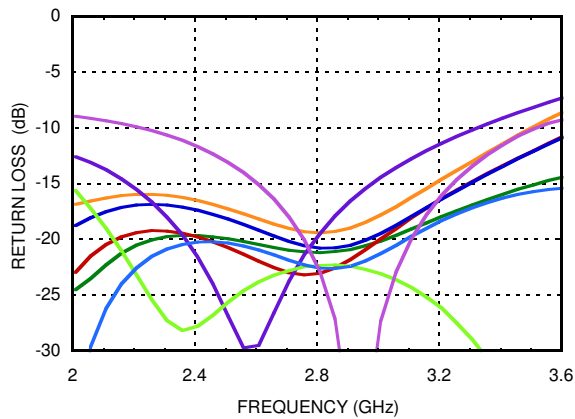
**Insertion Loss, Major States Only**



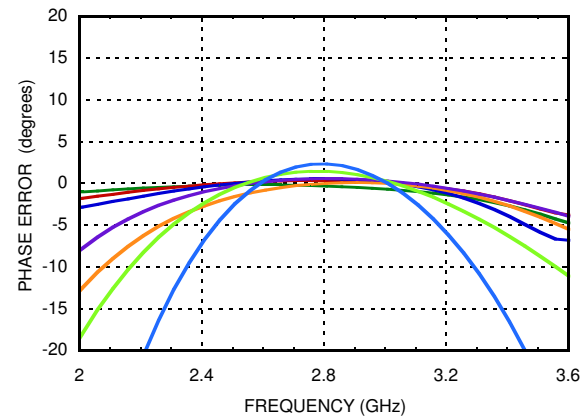
**Normalized Loss, Major States Only**



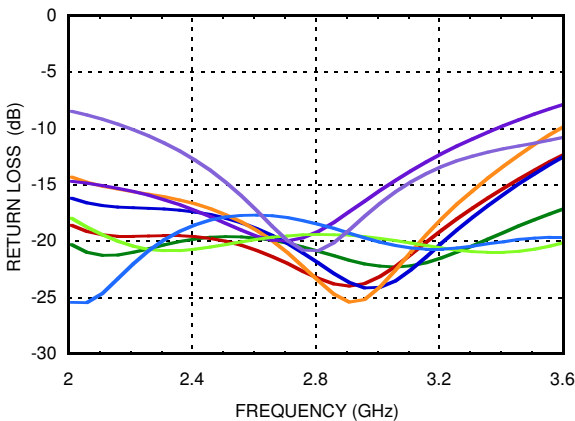
**Input Return Loss, Major States Only**



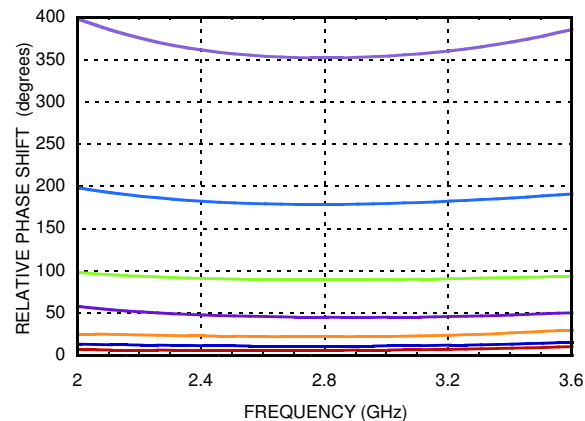
**Phase Error, Major States Only**



**Output Return Loss, Major States Only**

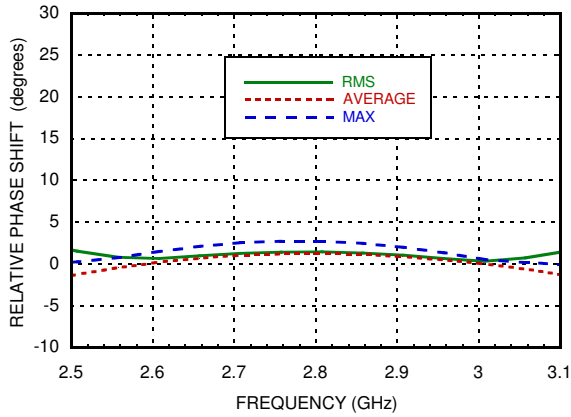


**Relative Phase Shift  
Major States Including All Bits**

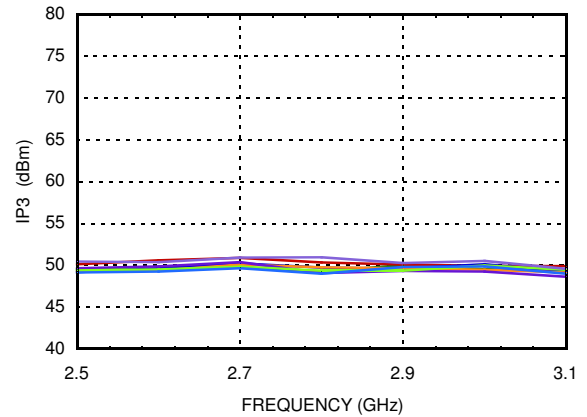


**GaAs MMIC 6-BIT DIGITAL  
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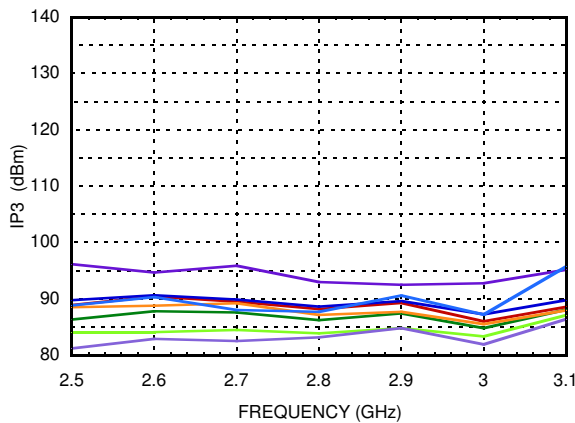
**Relative Phase Shift,  
RMS, Average, Max, All States**



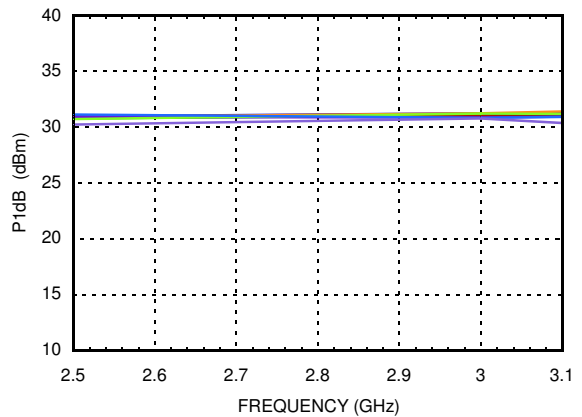
**Input IP3, Major States Only**



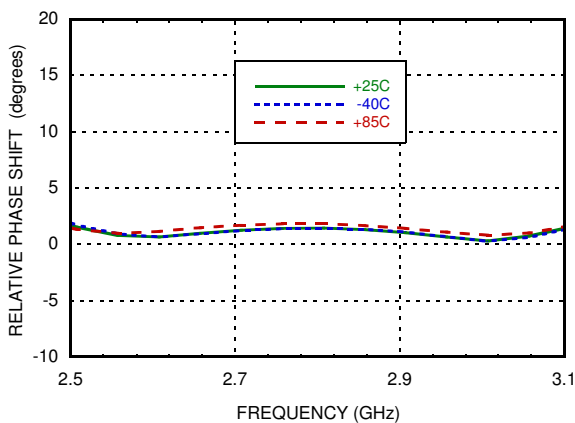
**Input IP2, Major States Only**



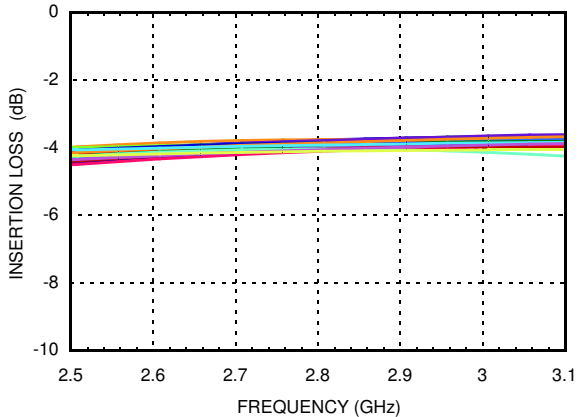
**Input P1dB, Major States Only**



**RMS Phase Error vs. Temperature**

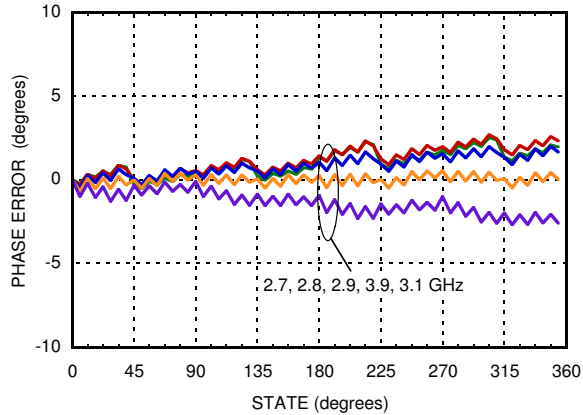


**Insertion Loss vs. Temperature,  
Major States Only**



## GaAs MMIC 6-BIT DIGITAL PHASE SHIFTER, 2.5 - 3.1 GHz

### Phase Error vs. State



### Bias Voltage & Current

Vdd	Idd
5.0	5.3mA
Vss	Iss
-5.0	5.3mA

### Control Voltage

State	Bias Condition
Low (0)	0 to 0.2 Vdc
High (1)	Vdd ±0.2 Vdc @ 35 µA Typ.

### Absolute Maximum Ratings

Input Power (RFIN)	33 dBm (T= +85 °C)
Bias Voltage Range (Vdd)	-0.2 to +12V
Bias Voltage Range (Vss)	+0.2 to -12V
Channel Temperature (Tc)	150 °C
Thermal Resistance (channel to ground paddle)	128 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class1A Passed 250V



ELECTROSTATIC SENSITIVE DEVICE  
OBSERVE HANDLING PRECAUTIONS

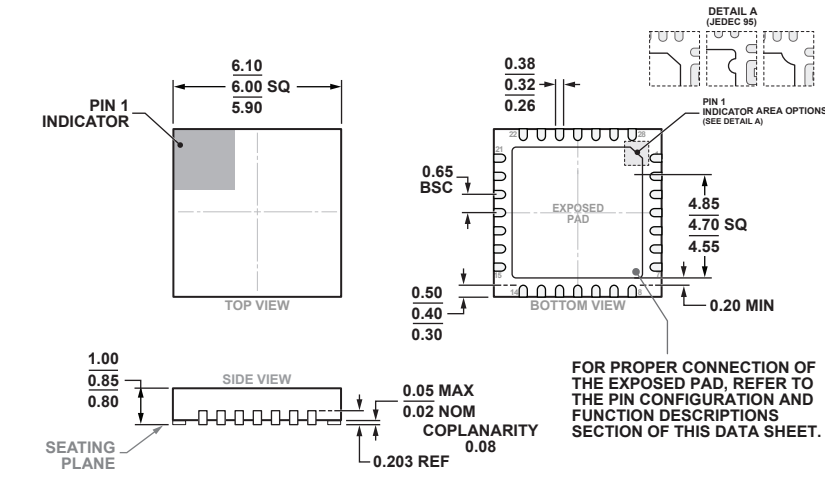
### Truth Table

Control Voltage Input						Phase Shift (Degrees) RFIN - RFOUT
Bit 1	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	
0	0	0	0	0	0	Reference*
1	0	0	0	0	0	5.625
0	1	0	0	0	0	11.25
0	0	1	0	0	0	22.5
0	0	0	1	0	0	45.0
0	0	0	0	1	0	90.0
0	0	0	0	0	1	180.0
1	1	1	1	1	1	354.375

Any combination of the above states will provide a phase shift approximately equal to the sum of the bits selected.  
\*Reference corresponds to monotonic setting

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**Outline Drawing**



COMPLIANT TO JEDEC STANDARDS MO-220-VJJC-3.

28-Lead Lead Frame Chip Scale Package [LFCSP]  
6 mm x 6 mm Body and 0.85 mm Package Height  
(CP-28-13)

Dimensions shown in millimeters

**Package Information**

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking <sup>[2]</sup>
HMC647ALP6E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL3 <sup>[1]</sup>	H647A XXXX

[1] Max peak reflow temperature of 260 °C

[2] 4-Digit lot number XXXX

**Pin Descriptions**

Pin Number	Function	Description	Interface Schematic
1	Vdd	Voltage Supply	
2, 20	GND	These pins and exposed ground paddle must be connected to RF/DC ground.	
3	RFIN	This port is DC coupled and matched to 50 Ohms.	
4 - 18, 21	N/C	No connection required. These pins may be connected to RF/DC ground without affecting performance.	
19	RFOUT	This port is DC coupled and matched to 50 Ohms.	
22 - 24 26 - 28	BIT6, BIT5, BIT4, BIT3, BIT2, BIT1	Control Input. See truth table and control voltage tables.	
25	Vss	Voltage Supply	