HMC659

v02.0217

GaAs PHEMT MMIC POWER AMPLIFIER, DC - 15 GHz

Typical Applications

The HMC659 is ideal for:

- Telecom Infrastructure
- Microwave Radio & VSAT
- Military & Space
- Test Instrumentation
- Fiber Optics

Features

P1dB Output Power: +26.5 dBm

Gain: 19 dB

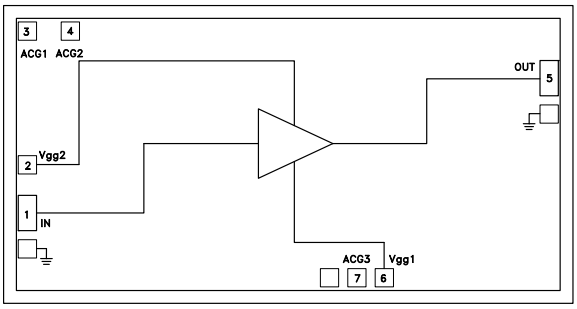
Output IP3: +35 dBm

Supply Voltage: +8V @ 300mA

50 Ohm Matched Input/Output

Die Size: 3.115 x 1.630 x 0.1 mm

Functional Diagram



General Description

The HMC659 is a GaAs MMIC PHEMT Distributed Power Amplifier die which operates between DC and 15 GHz. The amplifier provides 19 dB of gain, +35 dBm output IP3 and +26.5 dBm of output power at 1 dB gain compression while requiring 300mA from a +8V supply. Gain flatness is excellent at ±0.5 dB from DC to 10 GHz making the HMC659 ideal for EW, ECM, Radar and test equipment applications. The HMC659 amplifier I/Os are internally matched to 50 Ohms facilitating integration into Mutli-Chip-Modules (MCMs). All data is taken with the chip connected via two 0.025mm (1 mil) wire bonds of minimal length 0.31 mm (12 mils).

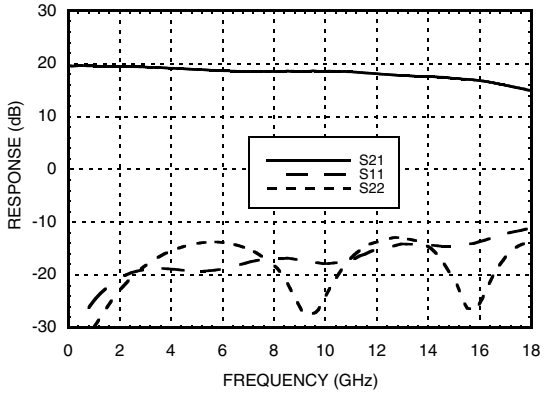
Electrical Specifications, T_A = +25° C, Vdd= +8V, Vgg2= +3V, Idd= 300mA*

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		DC - 6			6 - 11			11 - 15		GHz
Gain	16.1	19.1		15.5	18.5		14.8	17.8		dB
Gain Flatness		±0.5			±0.15			±0.6		dB
Gain Variation Over Temperature		0.013			0.018			0.025		dB/ °C
Input Return Loss		19			17			15		dB
Output Return Loss		18			17			15		dB
Output Power for 1 dB Compression (P1dB)	23	25.5		24	26.5		22.5	25		dBm
Saturated Output Power (Psat)		26			27			27		dBm
Output Third Order Intercept (IP3)		35			32			29		dBm
Noise Figure		2.5			2			3		dBc
Supply Current (Idd) (Vdd= 8V, Vgg1= -0.8V Typ.)		300			300			300		mA

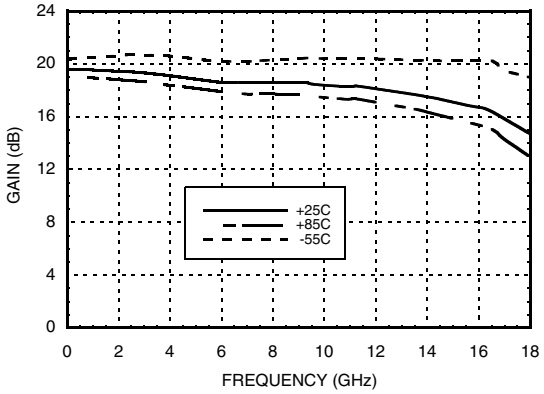
** Adjust Vgg1 between -2 to 0V to achieve Idd= 300mA typical.*

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

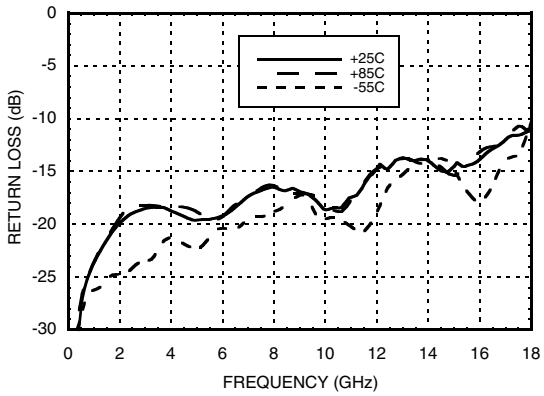
Gain & Return Loss



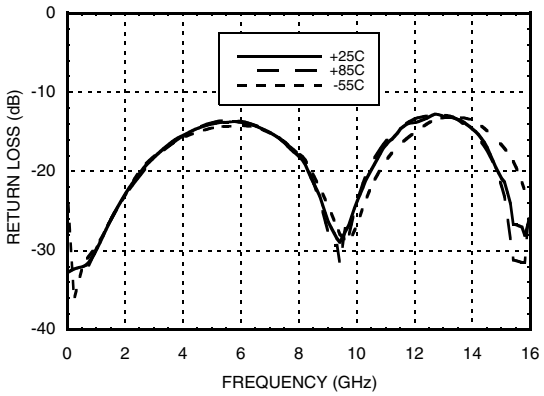
Gain vs. Temperature



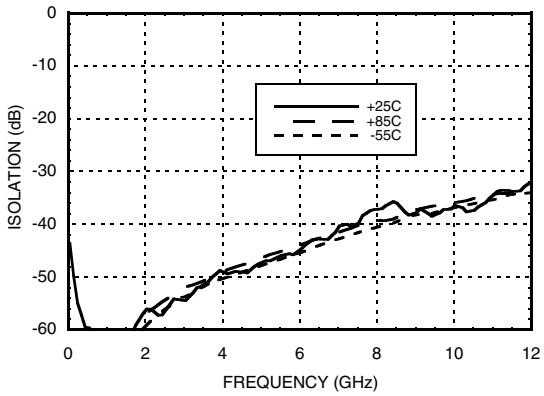
Input Return Loss vs. Temperature



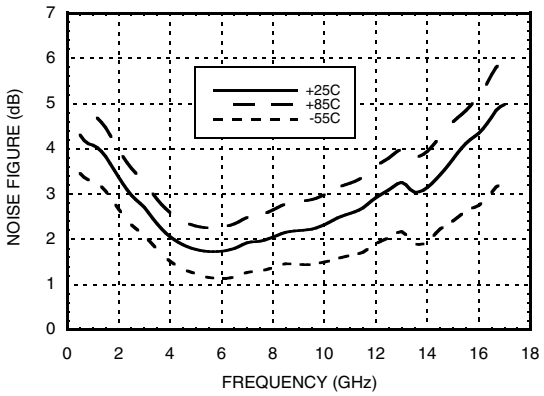
Output Return Loss vs. Temperature



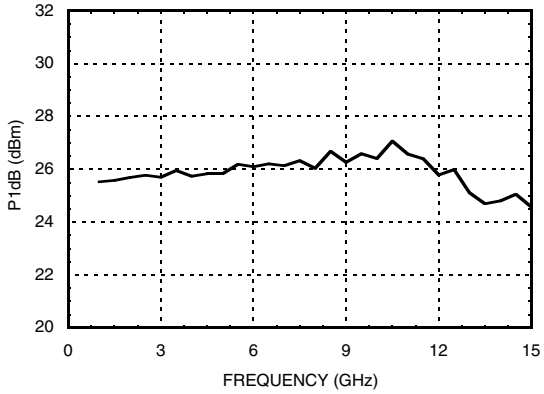
Reverse Isolation vs. Temperature



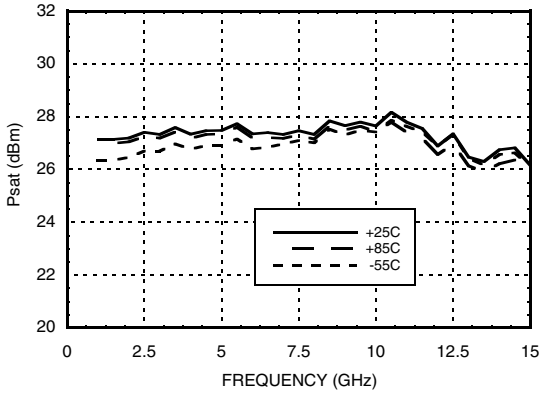
Noise Figure vs. Temperature



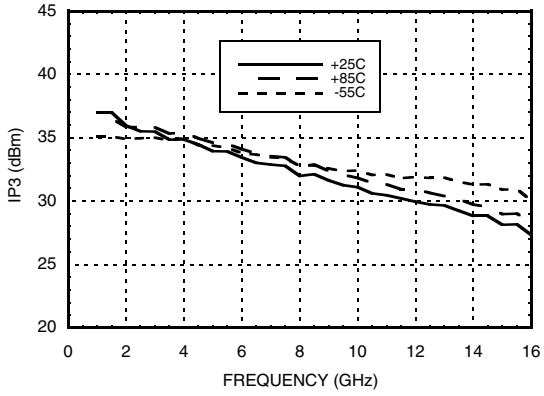
P1dB vs. Frequency



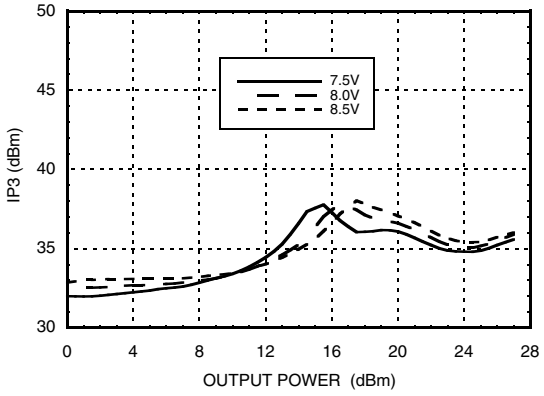
Psat vs. Temperature



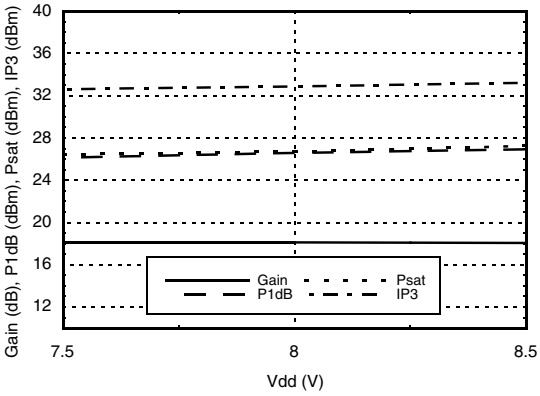
Output IP3 vs. Temperature



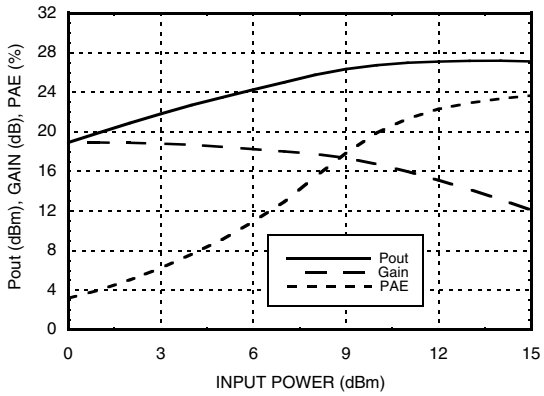
Output IP3 vs. Output Power @ 7GHz



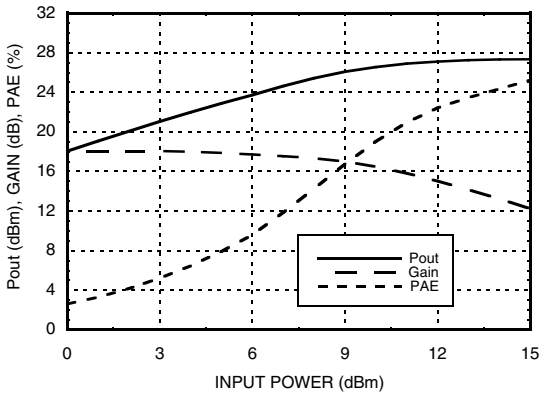
Gain, Power & Output IP3 vs. Supply Voltage @ 10 GHz, Fixed Vgg



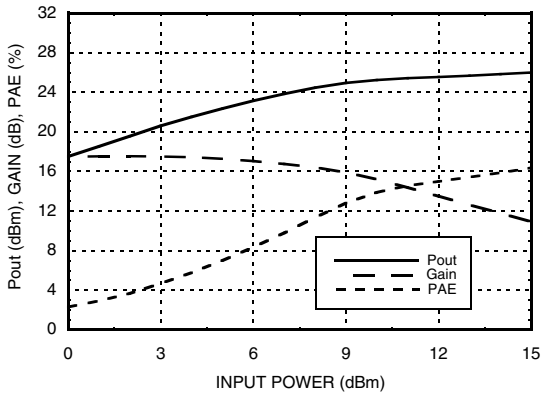
Power Compression @ 2 GHz



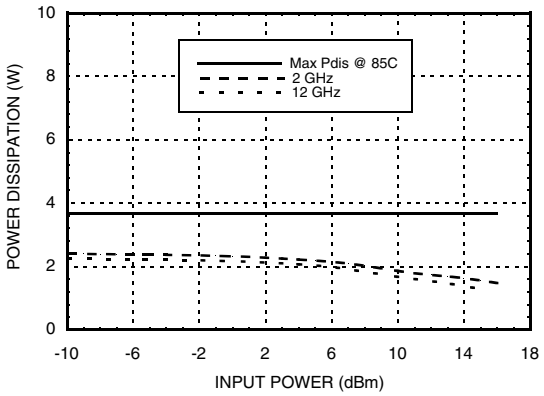
Power Compression @ 7 GHz



Power Compression @ 15 GHz



Power Dissipation



Absolute Maximum Ratings

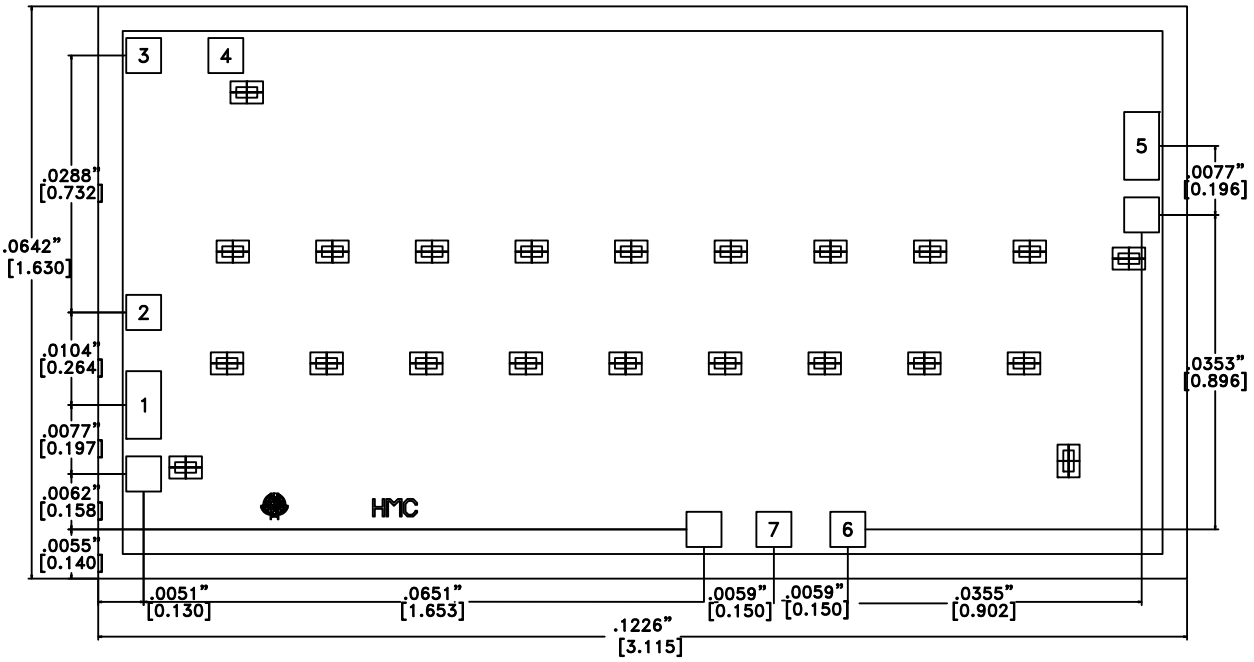
Drain Bias Voltage (Vdd)	+9 Vdc
Gate Bias Voltage (Vgg1)	0 to -2 Vdc
Gate Bias Voltage (Vgg2)	+2V to +4V
RF Input Power (RFIN)(Vdd = +12V)	+20 dBm
Channel Temperature	175 °C
Continuous Pdiss (T= 85 °C) (derate 41 mW/°C above 85 °C)	3.69 W
Thermal Resistance (channel to die bottom)	24.4 °C/W
Storage Temperature	-65 to 150°C
Operating Temperature	-55 to 85 °C
ESD Sensitivity (HBM)	Class1A, Passed 250V

Typical Supply Current vs. Vdd

Vdd (V)	Idd (mA)
+7.5	299
+8.0	300
+8.5	301

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



Die Packaging Information [1]

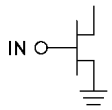
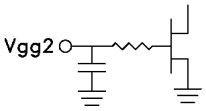
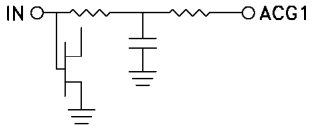
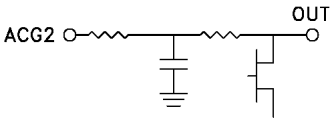
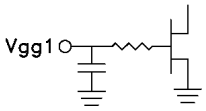
Standard	Alternate
GP-1 (Gel Pack)	[2]

[1] Refer to the "Packaging Information" section for die packaging dimensions.

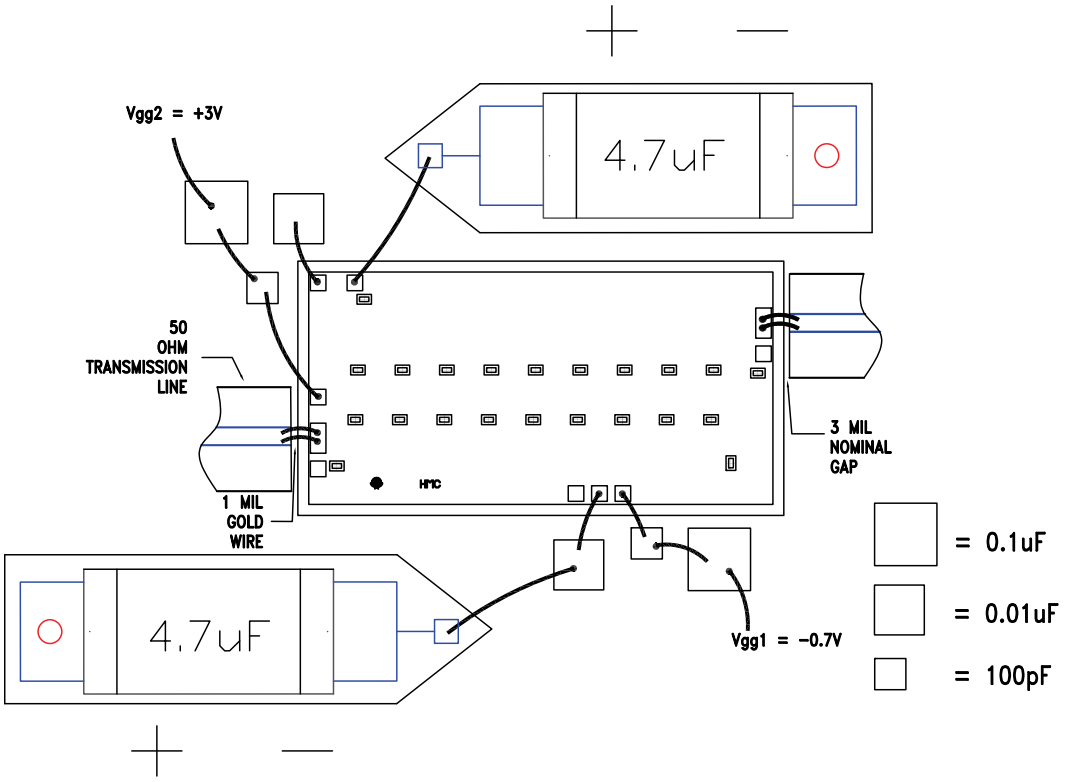
[2] For alternate packaging information contact Hittite Microwave Corporation.

NOTES:
1. ALL DIMENSIONS IN INCHES [MILLIMETERS]
2. DIE THICKNESS IS 0.004 (0.100)
3. TYPICAL BOND PAD IS 0.004 (0.100) SQUARE
4. BOND PAD METALIZATION: GOLD
5. BACKSIDE METALLIZATION: GOLD
6. BACKSIDE METAL IS GROUND
7. NO CONNECTION REQUIRED FOR UNLABELED BOND PADS
8. OVERALL DIE SIZE IS ±.002

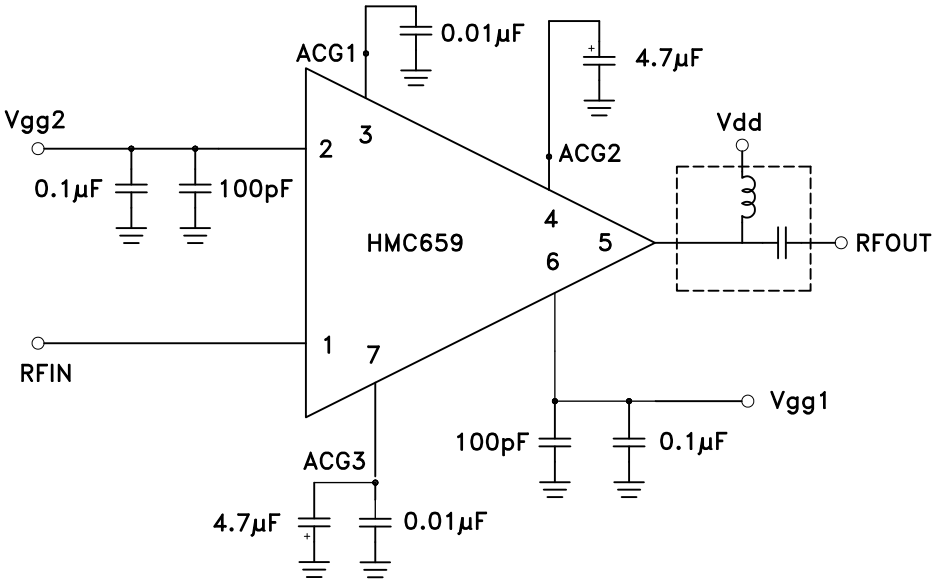
Pad Descriptions

Pad Number	Function	Description	Interface Schematic
1	IN	This pad is DC coupled and matched to 50 Ohms. Blocking capacitor is required.	
2	Vgg2	Gate control 2 for amplifier. Attach bypass capacitor per application circuit herein. For nominal operation +3V should be applied to Vgg2.	
3	ACG1	Low frequency termination. Attach bypass capacitor per application circuit herein.	
4	ACG2	Low frequency termination. Attach bypass capacitor per application circuit herein.	
5	OUT & Vdd	RF output for amplifier. Connect DC bias (Vdd) network to provide drain current (Idd). See application circuit herein.	
7	ACG3	Low frequency termination. Attach bypass capacitor per application circuit herein.	
6	Vgg1	Gate control 1 for amplifier. Attach bypass capacitor per application circuit herein. Please follow “MMIC Amplifier Biasing Procedure” application note.	
Die Bottom	GND	Die bottom must be connected to RF/DC ground.	

Assembly Diagram



Application Circuit



NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee with low series resistance and capable of providing 500mA