0.01 GHz to 10 GHz, MMIC, GaAs, pHEMT RF Gain Block

Data Sheet **HMC788A**

FEATURES

- Gain: 14 dB typical
- Operational frequency range: 0.01 GHz to 10 GHz
- Input/output internally matched to 50 Ω
- High input linearity
  - 1 dB compression (P1dB): 20 dBm typical
  - Output third-order intercept (OIP3): 33 dBm typical
- Supply voltage: 5 V typical
- 2 mm × 2 mm, 6-lead lead frame chip scale package

APPLICATIONS

- Cellular, 3G, LTE, WiMAX, and 4G
- LO driver applications
- Microwave radio
- Test and measurement equipment
- Ultra wideband (UWB) communications

FUNCTIONAL BLOCK DIAGRAM

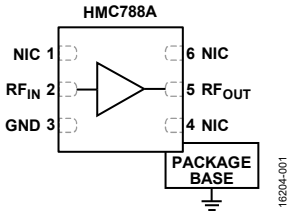

Figure 1.

GENERAL DESCRIPTION

The HMC788A is a 0.01 GHz to 10 GHz, gain block, monolithic microwave integrated circuit (MMIC) amplifier using gallium arsenide (GaAs), pseudomorphic high electron mobility transistor (pHEMT) technology.

This 2 mm × 2 mm LFCSP amplifier can be used as either a cascadable 50 Ω gain stage, or to drive the local oscillator (LO) port of many of the single and double balanced mixers from Analog Devices, Inc. with up to 20 dBm output power.

The HMC788A offers 14 dB of gain and an output IP3 of 33 dBm while requiring only 76 mA from a 5 V supply.

The Darlington feedback pair exhibits reduced sensitivity to normal process variations and yields excellent gain stability over temperature while requiring a minimal number of external bias components.

Rev. D

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9/2018—Rev. B to Rev. C

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11/2017—Rev. A to Rev. B

Changes to Continuous Power Dissipation, P_{DISS} Parameter and Junction (T_J) Temperature Parameter, Table 2 4

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

10/2017—v00.0913 to Rev. A

Changes to Product Title, Features Section, General Description Section, and Figure 1 1
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Added Thermal Resistance Section and Table 3; Renumbered Sequentially 4
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SPECIFICATIONS

ELECTRICAL SPECIFICATIONS

Collector bias voltage (V_{CC}) = 5 V, T_{CASE} = 25°C, 6.35 µH external inductor between V_{CC} and RF_{OUT}, 50 Ω system, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
OVERALL FUNCTION						
Frequency Range		0.01		10	GHz	
Gain		12	14		dB	0.01 GHz to 6.0 GHz
		9	12		dB	6.0 GHz to 10.0 GHz
Gain Variation Over Temperature			0.004		dB/°C	0.01 GHz to 6.0 GHz
			0.007		dB/°C	6.0 GHz to 10.0 GHz
Reverse Isolation			23		dB	0.01 GHz to 6.0 GHz
			20		dB	6.0 GHz to 10 GHz
RADIO FREQUENCY (RF) INPUT INTERFACE						
Input Return Loss			16		dB	0.01 GHz to 6.0 GHz
			9		dB	6.0 GHz to 10.0 GHz
RF OUTPUT INTERFACE						
Output Power for 1 dB Compression	P1dB	18	20		dBm	0.01 GHz to 6.0 GHz
		15	18		dBm	6.0 GHz to 10.0 GHz
Output Return Loss			9		dB	0.01 GHz to 6.0 GHz
			12		dB	6.0 GHz to 10.0 GHz
DISTORTION AND NOISE						
Output Third-Order Intercept	OIP3		33		dBm	0.01 GHz to 6.0 GHz
			30		dBm	6.0 GHz to 10.0 GHz
Noise Figure	NF		6		dB	0.01 GHz to 6.0 GHz
			7		dB	6.0 GHz to 10.0 GHz
POWER INTERFACE						
Supply Voltage		4.5	5	5.5	V	
Supply Current	I_{CC}	60	65		mA	V_{CC} = 4.5 V
			76		mA	V_{CC} = 5 V
			87	90	mA	V_{CC} = 5.5 V

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Collector Bias Voltage (V_{CC})	7 V
RF Input Power (RF_{IN}), V_{CC} = 5 V	20 dBm
Continuous Power Dissipation, P_{DISS} (T_{CASE} = 85°C, Derate 8.5 mW/°C Above 85°C)	0.76 W
Junction (T_J) Temperature	175°C
Operating (T_{OPR}) Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Electrostatic Discharge (ESD) Sensitivity, Human Body Model (HBM)	Class 1A

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JC} is the junction to case thermal resistance.

Table 3. Thermal Resistance

Package Type	θ_{JC}	Unit
CP-6-10[1]	118.0	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P thermal test board with nine thermal vias. See JEDEC JESD51.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

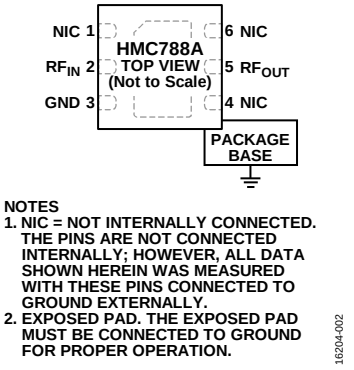

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 4, 6	NIC	Not Internally Connected. The pins are not connected internally; however, all data shown herein was measured with these pins connected to GND externally.
2	RF_{IN}	RF Input. This pin is dc-coupled and ac matched to 50 Ω. An external dc blocking capacitor is required on this pin.
3	GND	Ground. This pin must be connected to ground.
5	RF_{OUT}	RF Output. This pin is ac matched to 50 Ω and supplies dc bias for the output stage.
	EPAD	Exposed Pad. The exposed pad must be connected to GND for proper operation.

INTERFACE SCHEMATICS

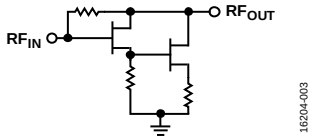

Figure 3. RF_{IN}, RF_{OUT} Interface Schematic

Figure 4. GND Interface Schematic

TYPICAL PERFORMANCE CHARACTERISTICS

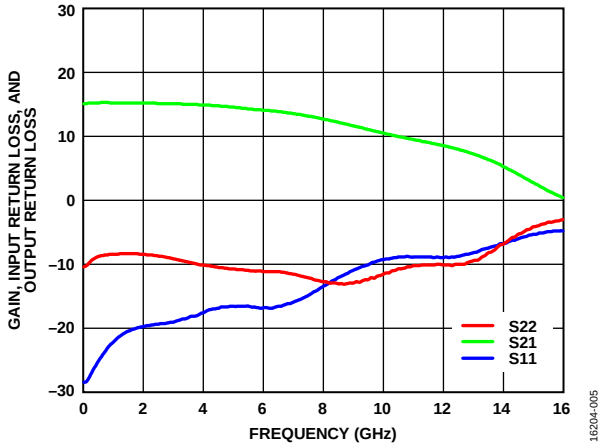

Figure 5. Gain, Input Return Loss, and Output Return Loss vs. Frequency; S21 is Gain, S11 is Input Return Loss, S22 is Output Return Loss

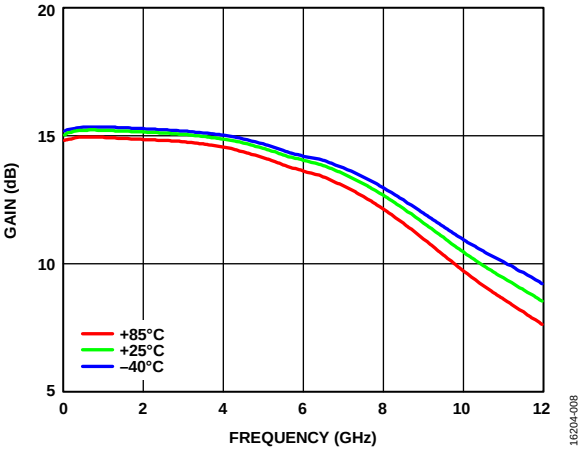

Figure 8. Gain vs. Frequency at Various Temperatures

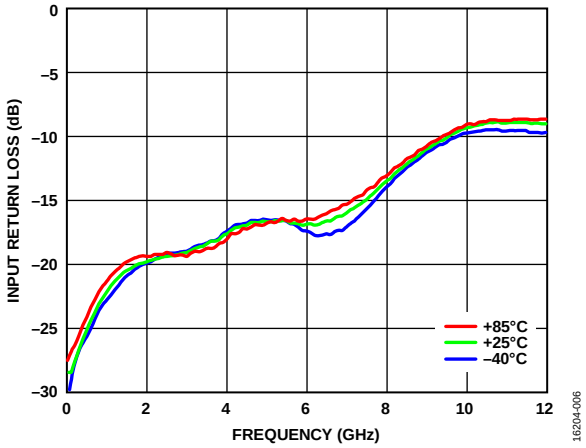

Figure 6. Input Return Loss vs. Frequency at Various Temperatures

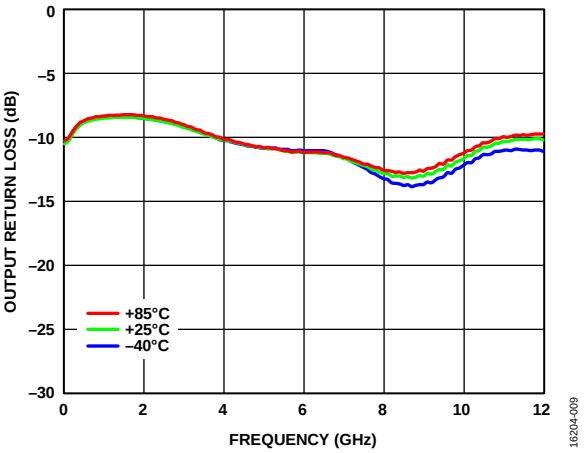

Figure 9. Output Return Loss vs. Frequency at Various Temperatures

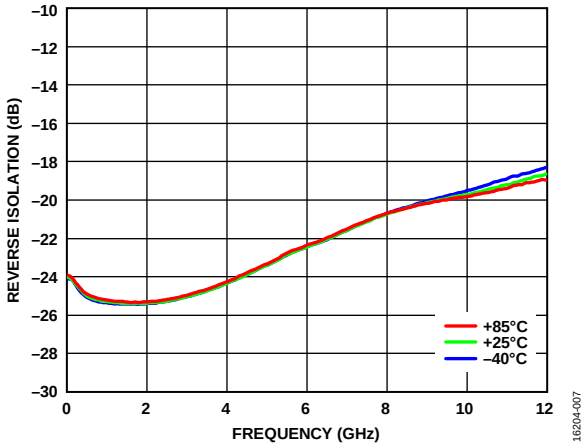

Figure 7. Reverse Isolation vs. Frequency at Various Temperatures

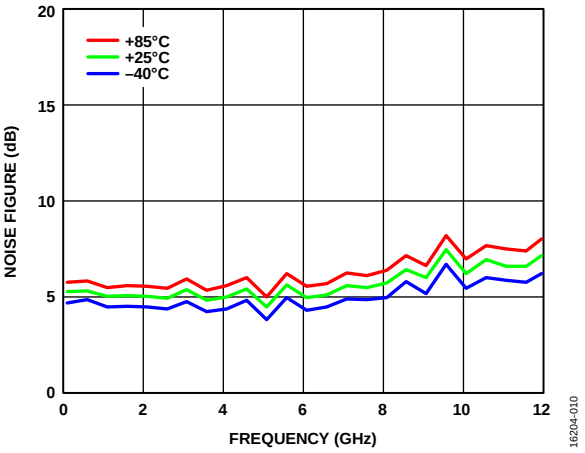

Figure 10. Noise Figure vs. Frequency at Various Temperatures

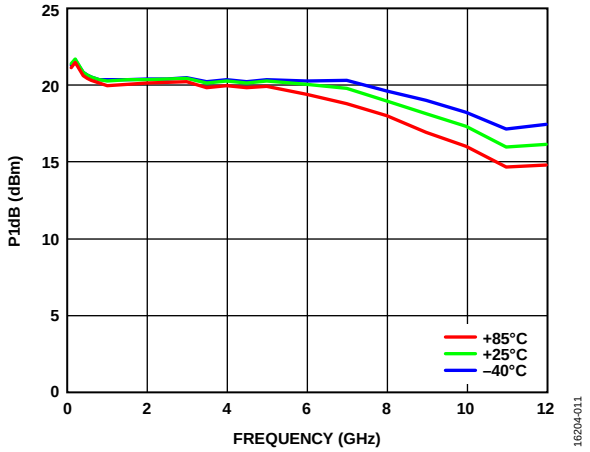

Figure 11. P1dB vs. Frequency at Various Temperatures

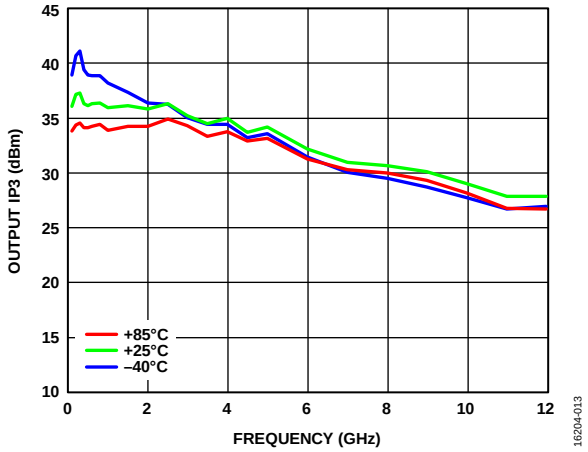

Figure 13. Output IP3 vs. Frequency at Various Temperatures; 5 dBm per Tone Output Power

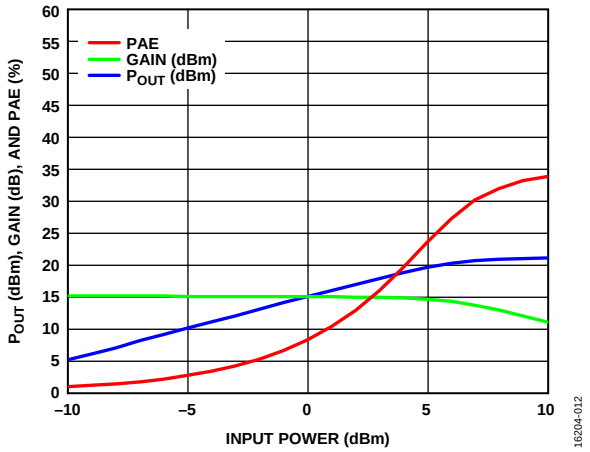

Figure 12. Output Power (P_{OUT}), Gain, and Power Added Efficiency (PAE) vs. Input Power at 1 GHz

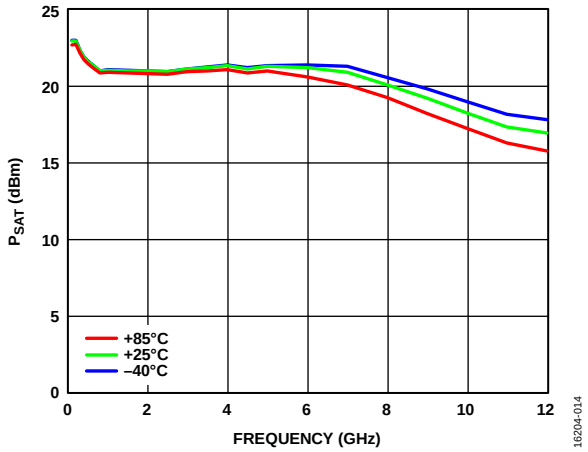

Figure 14. Saturation Power (P_{SAT}) vs. Frequency at Various Temperatures

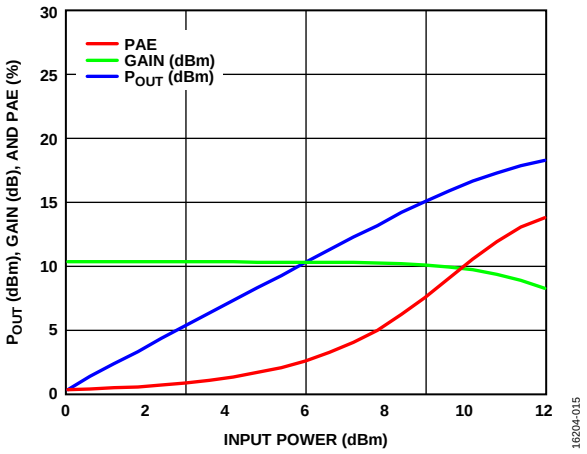

Figure 15. P_{OUT}, Gain, and PAE vs. Input Power at 10 GHz

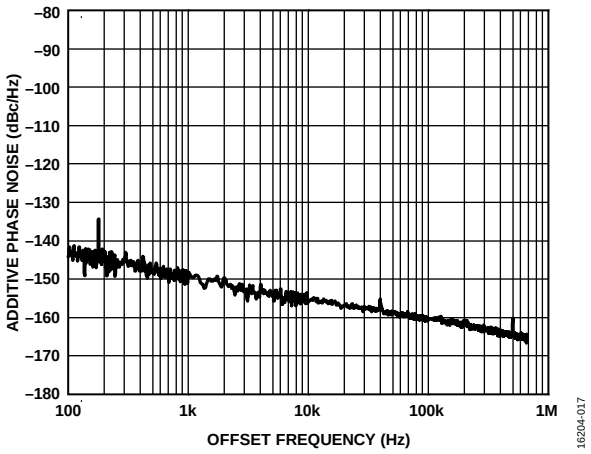

Figure 17. Additive Phase Noise vs. Offset Frequency; RF Frequency = 5 GHz, RF Input Power = 6 dBm (P1dB)

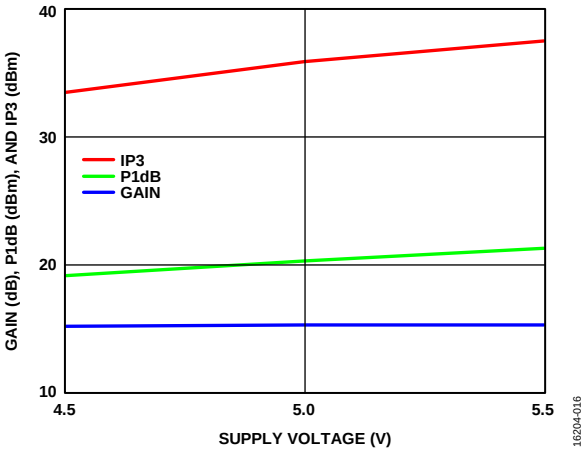

Figure 16. Gain, P1dB, and IP3 vs. Supply Voltage at 1 GHz

THEORY OF OPERATION

The HMC788A is designed with a Darlington feedback pair that exhibits reduced sensitivity to normal process variations and yields excellent gain stability over temperature while requiring minimal external bias components. The amplifier can be operated from a 5 V supply by adding a choke inductor from the amplifier output to V_{CC}.

BASIC CONNECTIONS

The HMC788A RF gain block is a fixed gain amplifier with single-ended input and output ports featuring impedances nominally equal to 50 Ω over the 0.01 GHz to 10 GHz frequency range. The input and output impedances are sufficiently stable across variations in temperature and supply voltage such that the HMC788A can be directly inserted into a 50 Ω system with no impedance matching circuitry required.

The input pin, RF_{IN}, is dc-coupled and ac matched to 50 Ω. A dc blocking capacitor must be connected between the source that drives the HMC788A and the RF_{IN} pin.

It is critical to supply very low inductance ground connections to the GND pin as well as to the backside exposed pad, ensuring stable operation. It is recommended that the NIC pins also be connected to GND.

The HMC788A is designed to operate with a supply voltage of 5 V, which is connected through an external RF choke between the supply voltage and the output pin, RF_{OUT}. The inductance of the RF choke must be approximately 6 µH, and care must be taken to ensure that the lowest series self resonant frequency of this choke is well above the maximum frequency of operation for the HMC788A. Consequently, a dc blocking capacitor must be connected between the bias connection to RF_{OUT} and the output load. The value of this capacitor is not critical, but it is recommended to be 100 pF or larger.

Bypass the bias supply voltage, V_{CC}, using a large value capacitance (approximately 2.2 µF or larger) and a smaller, high frequency bypass capacitor (approximately 100 pF).

The recommended connections and components are shown in the Evaluation PCB section.

APPLICATIONS INFORMATION

EVALUATION PCB

The PCB used in this application must use RF circuit design techniques. Signal lines must have 50 Ω impedance while the package ground leads and exposed pad must be connected directly to the ground plane similar to that shown in Figure 19.

A sufficient number of via holes must be used to connect the top and bottom ground planes. The EV1HMC788ALP2 evaluation board must be mounted to an appropriate heat sink.

Figure 18 shows the schematic of the EV1HMC788ALP2 evaluation board. The board is powered by a single supply between 4.5 V and 5.5 V and is decoupled by a 2.2 µF capacitor and a 100 pF capacitor. DC blocking capacitors are installed at the RF_{IN} and RF_{OUT} ports. Note that inductor L1 is a required component to apply the V_{CC} = 5 V bias to the RF_{OUT} pin.

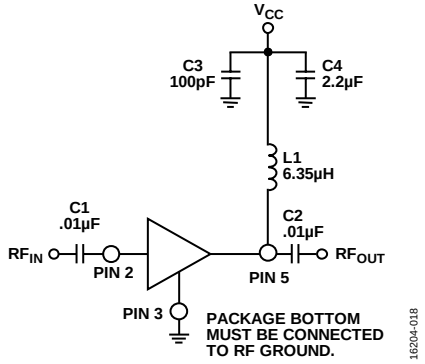

Figure 18. Evaluation Board Schematic

Table 5. List of Materials for the Evaluation PCB EV1HMC788ALP2[1]

Item	Description
J1 to J2	PCB mount Subminiature Version A (SMA) connector
J5, J6	DC pin
C1, C2	0.01 µF capacitor, 0502 package
C3	100 pF capacitor, 0402 package
C4	2.2 µF Case A package
R1	0 Ω resistor, 0402 package
L1	Inductor, conical 6.35 µH, P/N CC75T38K240G5 (Piconics)
U1	HMC788ALP2E
PCB[2]	129549 evaluation PCB

[1] Reference this number when ordering the complete evaluation PCB.
[2] The circuit board material is Rogers 4350.

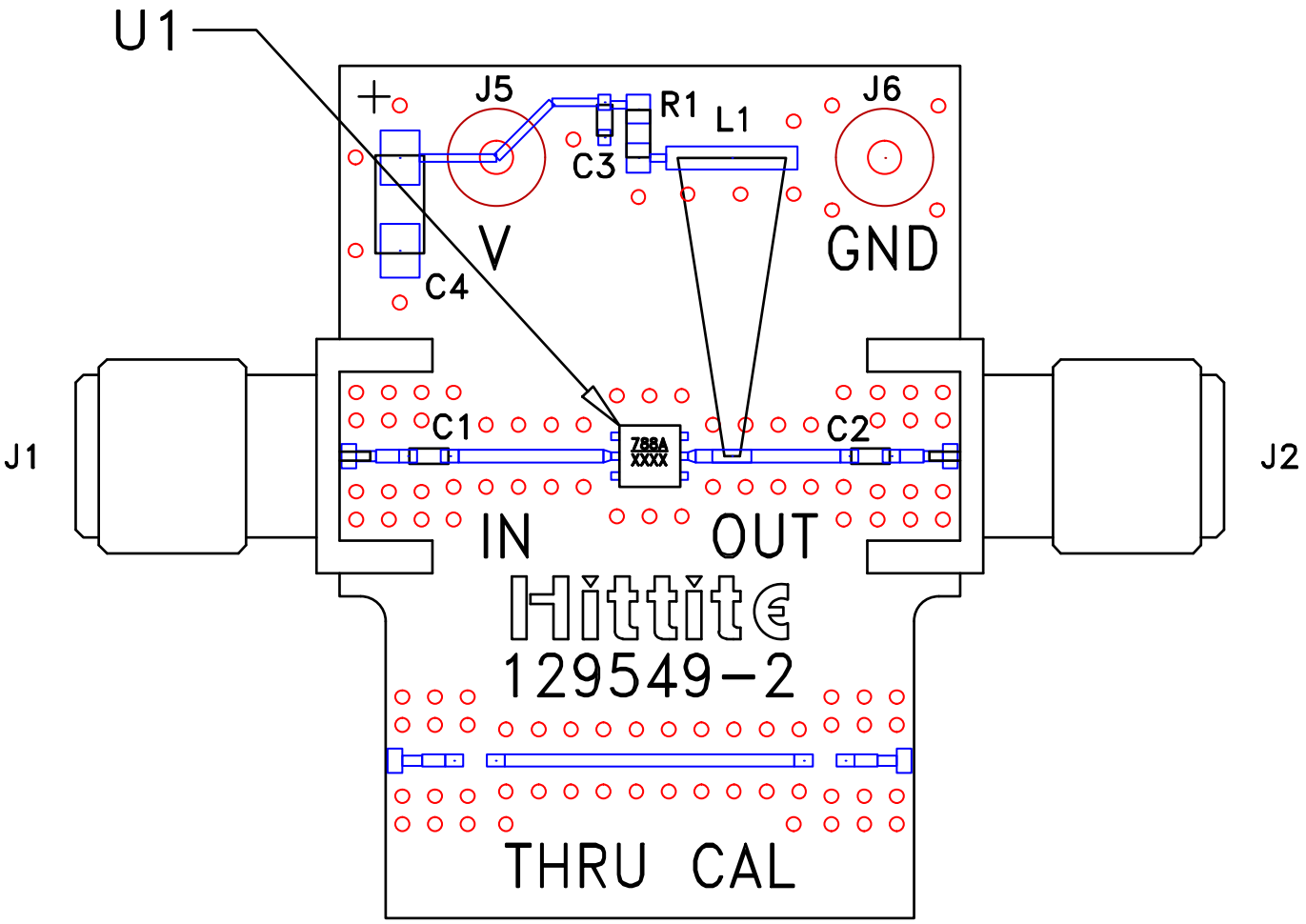

Figure 19. Evaluation Board, Top View