

## FEATURES

- Differential and single-ended operation**
- Supports data rates up to 28 Gbps**
- Fast rise/fall time: 20 ps/18 ps**
- Low power consumption: 610 mW typical**
- Programmable differential**
- Output voltage swing: 500 mV p-p to 1350 mV p-p**
- Single supply: -3.3 V**
- 5 mm × 5 mm, 32-terminal ceramic leadless chip carrier (LCC) package: 25 mm<sup>2</sup>**

## APPLICATIONS

- SONET OC-192**
- High speed serial logic**
- Clock and data recovery**
- Broadband test and measurement equipment**
- Frequency synthesis**
- Matched timing**

## GENERAL DESCRIPTION

The **HMC856** is a wideband time delay device with a 5-bit digital control designed for timing compensation or clock skew management applications. The time delay provides nearly 100 ps (maximum) of delay range with 3 ps resolution and supports 28 Gbps data. The monotonic delay is compensated for stable operation over both power supply and temperature variation.

All differential inputs to the **HMC856** are current mode logic (CML) and terminated on chip with 50 Ω to the positive supply ground, GND, and can be ac or dc-coupled. The differential CML

## FUNCTIONAL BLOCK DIAGRAM

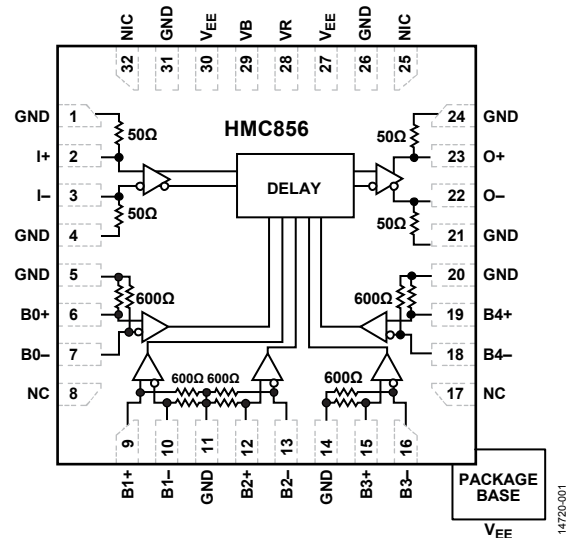


Figure 1.

outputs are source terminated to 50 Ω and can also be ac or dc-coupled. Connect outputs directly to a 50 Ω ground terminated system or drive devices with CML logic input. The control lines, B4 to B0, are differential CML inputs terminated with 600 Ω to the positive rail, which supports lower power control options. The **HMC856** features an output level control pin, VR, that allows loss compensation or signal level optimization. The **HMC856** operates from a single -3.3 V supply and is available in a 5 mm × 5 mm LCC package.

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## REVISION HISTORY

### 6/2018—Rev. C to Rev. D

|   |    |
|---|----|
| Changes to Figure 1 .....                                   | 1  |
| Changes to Resolution Parameter, Table 1 and Figure 2 ..... | 3  |
| Changes to Figure 22 Caption and Figure 23 .....            | 9  |
| Changes to Theory of Operation Section.....                 | 10 |
| Changes to Figure 25.....                                   | 12 |
| Changes to Ordering Guide .....                             | 13 |

This Hittite Microwave Products data sheet has been reformatted to meet the styles and standards of Analog Devices, Inc.

### 12/2016—Rev. 01.0611 to Rev. C

|  |           |
|--|-----------|
| Updated Format.....  | Universal |
| Changes to Features Section, General Description Section, and Figure 1 ..... | 1         |
| Added Power Consumption Parameter, Table 1 .....                             | 3         |
| Changes to Figure 2.....   | 3         |
| Changes to Table 2.....  | 4         |
| Changes to Figure 3 and Table 3.....   | 5         |
| Changes to Typical Performance Characteristics Section.....                  | 7         |
| Added Theory of Operation Section .....                                      | 10        |
| Changes to Table 4 and Figure 24 Caption .....                               | 11        |
| Changes to Figure 25.....  | 12        |
| Updated Outline Dimensions .....   | 13        |
| Changes to Ordering Guide .....  | 13        |

# SPECIFICATIONS

## ELECTRICAL SPECIFICATIONS

T<sub>A</sub> = 25°C, V<sub>EE</sub> = -3.3 V, V<sub>R</sub> = 0 V, unless otherwise noted.

Table 1.

| Parameter                      | Symbol                          | Test Conditions/Comments  | Min  | Typ   | Max  | Unit     |
|--------------------------------|---------------------------------|---|------|-------|------|----------|
| POWER SUPPLY                   |                                 |   |      |       |      |          |
| Voltage                        | V <sub>EE</sub>                 |   | -3.7 | -3.3  | -2.9 | V        |
| Current                        |                                 |   |      | 185   |      | mA       |
| POWER CONSUMPTION              |                                 |   |      | 610   |      | mW       |
| MAXIMUM DATA RATE              |                                 |   |      |       | 28   | Gbps     |
| INPUT VOLTAGE                  |                                 | CML logic input   |      |       |      |          |
| Single-Ended                   |                                 |   | -1.5 |       | +0.5 | V        |
| Differential                   |                                 |   | 0.1  |       | 2.0  | V        |
| OUTPUT                         |                                 |   |      |       |      |          |
| Rise/Fall Time                 | t <sub>R</sub> , t <sub>F</sub> | Differential, 20% to 80%  |      | 20/18 |      | ps       |
| Single-Ended Amplitude         |                                 |   |      | 565   |      | mV p-p   |
| Differential Amplitude         |                                 |   | 500  | 1130  | 1350 | mV p-p   |
| High Voltage                   |                                 |   |      | -20   |      | mV       |
| Low Voltage                    |                                 |   |      | -585  |      | mV       |
| RETURN LOSS                    |                                 | Frequency <12 GHz   |      |       |      |          |
| Input                          |                                 |   |      | 10    |      | dB       |
| Output                         |                                 |   |      | 10    |      | dB       |
| JITTER                         |                                 |   |      |       |      |          |
| Random                         | J <sub>R</sub>                  | RMS   |      | 0.2   |      | ps rms   |
| Deterministic                  | J <sub>D</sub>                  | 2 <sup>15</sup> - 1 pseudo random binary sequence (PRBS)<br>28 Gbps input |      | <2    |      | ps p-p   |
| VR PIN CURRENT                 |                                 | V <sub>R</sub> = 0 V<br>V <sub>R</sub> = 0.4 V                            |      | 3     | 4.25 | mA<br>mA |
| DELAY                          |                                 |   |      |       |      |          |
| Propagation Delay Data to Data | t <sub>PROP</sub>               |   |      | 255   |      | ps       |
| Control Range                  |                                 |   |      | 92    |      | ps       |
| Temperature Variation          |                                 | T <sub>A</sub> = 85°C<br>T <sub>A</sub> = -40°C                           | 9    |       | 12   | ps<br>ps |
| Resolution                     | t <sub>PROG_DELAY</sub>         |   | 4    |       | 8    | ps<br>ps |

## TIMING DIAGRAM

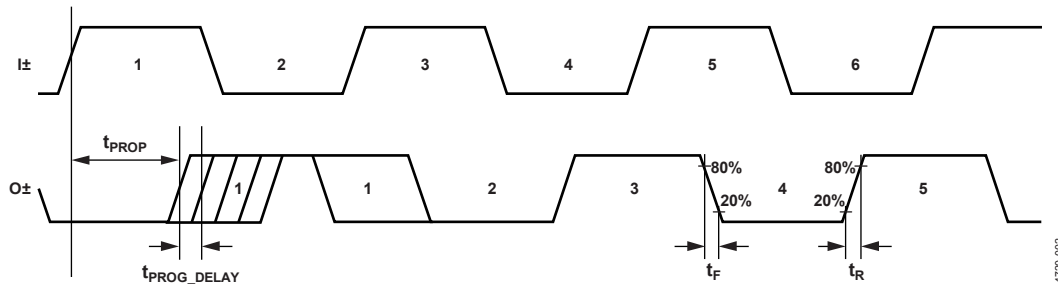


Figure 2. Timing Diagram

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## ABSOLUTE MAXIMUM RATINGS

Table 2.

| Parameter   | Rating            |
|---|-------------------|
| Power Supply Voltage ( $V_{EE}$ )   | -3.75 V to +0.5 V |
| Input Signals   | -2 V to +0.5 V    |
| Output Signals  | -1.5 V to 0.5 V   |
| Maximum Junction Temperature  | 125°C             |
| Continuous Power Dissipation, $P_{DISS}$<br>( $T = 85^{\circ}\text{C}$ , Derate 33 mW/ $^{\circ}\text{C}$ Above 85°C) | 1.33 W            |
| Thermal Resistance, $\theta_{JC}$ (Worst Case Device<br>to Package Exposed Paddle)                                    | 30°C/W            |
| Temperature   |                   |
| Storage   | -65°C to +150°C   |
| Operating   | -40°C to +85°C    |
| Reflow (MSL3 Rating)  | 260°C             |
| ESD Sensitivity Human Body Model (HBM)  | Class 1C          |

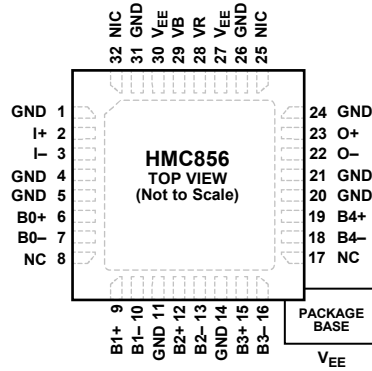
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



- NOTES
1. NC = NO CONNECT.
  2. NIC = NOT INTERNALLY CONNECTED.
  3. EXPOSED PAD. THE EXPOSED PAD MUST BE CONNECTED TO THE NEGATIVE VOLTAGE SUPPLY.

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Figure 3. Pin Configuration

Table 3. Pin Function Descriptions

| Pin Number                          | Mnemonic   | Description   |
|-------------------------------------|--|---|
| 1, 4, 5, 11, 14, 20, 21, 24         | GND  | Signal Ground.  |
| 2, 3                                | I+, I-   | Differential Data Inputs. CML referenced to positive supply.  |
| 6, 7, 9, 10, 12, 13, 15, 16, 18, 19 | B0+, B0-, B1+, B1-, B2+, B2-, B3+, B3-, B4-, B4+ | Differential Digital Control Inputs. CML referenced to positive supply.   |
| 8, 17                               | NC   | No Connect. These pins are internally connected to the device. These pins can be connected to radio frequency (RF)/dc ground without affecting performance. |
| 25, 32                              | NIC  | Not Internally Connected. These pins can be connected to radio frequency (RF)/dc ground without affecting performance.                                      |
| 22, 23                              | O-, O+   | Differential Data Outputs. CML referenced to positive supply, 50 $\Omega$ termination.  |
| 26, 31                              | GND  | Supply Ground.  |
| 27, 30                              | V <sub>EE</sub>                                  | Negative Supply Voltage. These pins and the exposed pad must be connected to the negative voltage supply.   |
| 28                                  | VR   | Output Level Control. Output levels can be increased or decreased by applying voltage to VR, as shown in Figure 12.   |
| 29                                  | VB   | DC Bias Voltage. VB must be connected to ground.  |
|                                     | EPAD (V <sub>EE</sub> )                          | Exposed Pad. The exposed pad must be connected to the negative voltage supply.  |

INTERFACE SCHEMATICS



Figure 4. GND Interface Schematic

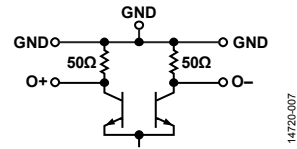


Figure 7. O+, O- Interface Schematic

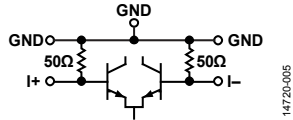


Figure 5. I+, I- Interface Schematic

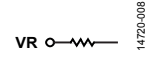


Figure 8. VR Interface Schematic

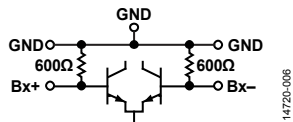


Figure 6. Bx+, Bx- Interface Schematic

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{EE} = -3.3\text{ V}$ ,  $V_R = 0\text{ V}$ ,  $400\text{ mV}$ ,  $28\text{ Gbps}$ , PRBS  $2^{15} - 1$ , input applied, unless otherwise noted.

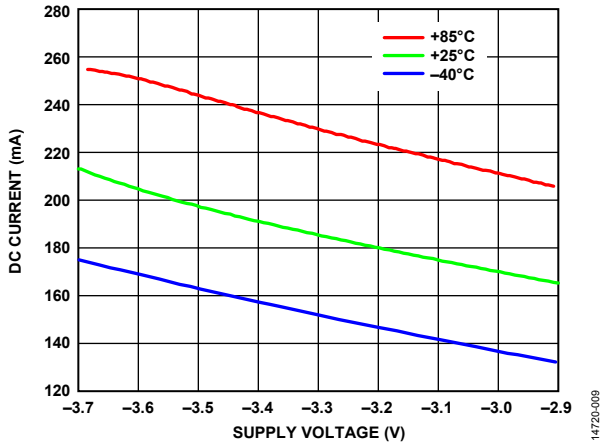


Figure 9. DC Current vs. Supply Voltage,  $V_R = 0\text{ V}$  at Various Temperatures

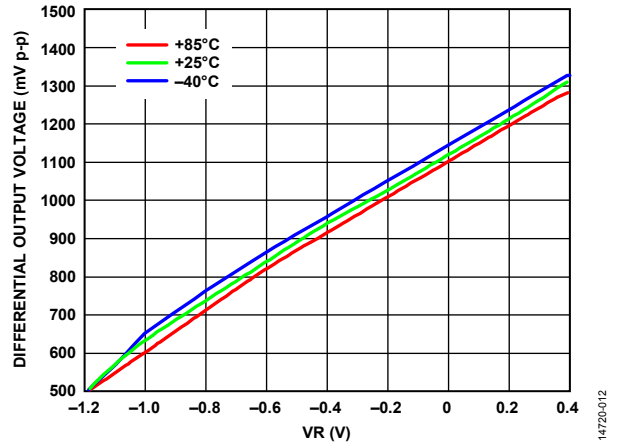


Figure 12. Differential Output Voltage vs.  $V_R$  at Various Temperatures

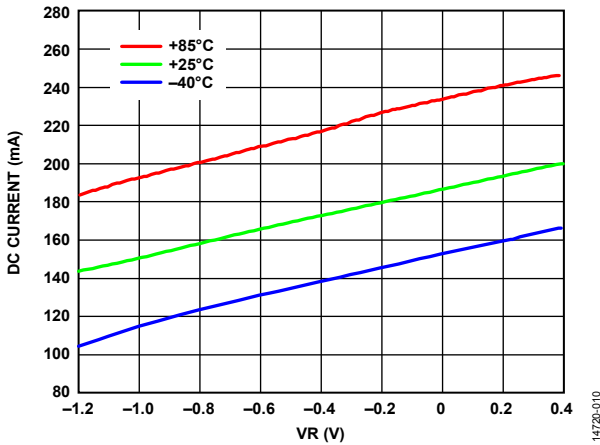


Figure 10. DC Current vs.  $V_R$  at Various Temperatures

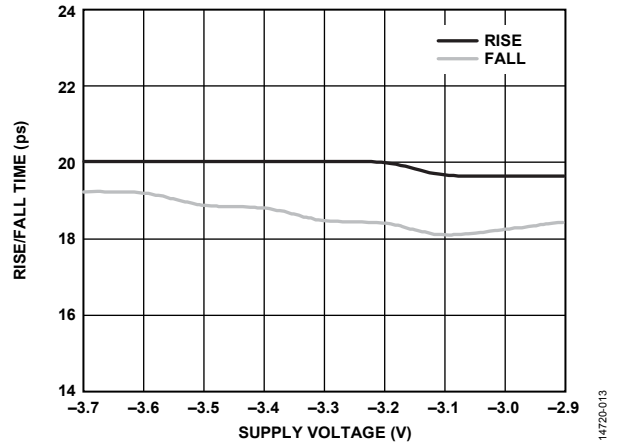


Figure 13. Rise/Fall Time vs. Supply Voltage

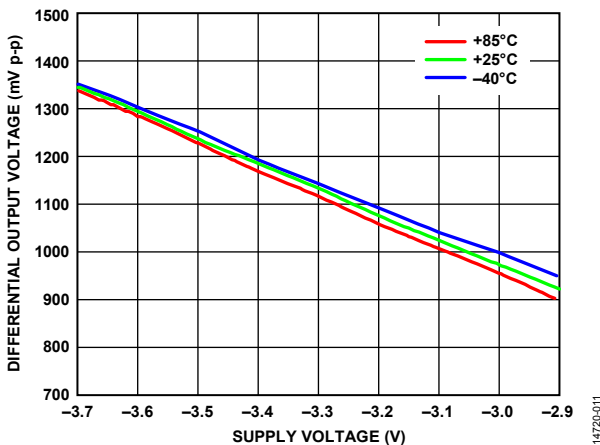


Figure 11. Differential Output Voltage vs. Supply Voltage at Various Temperatures

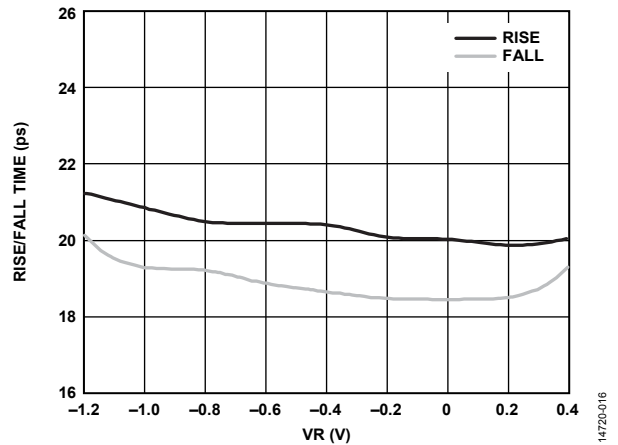


Figure 14. Rise/Fall Time vs.  $V_R$

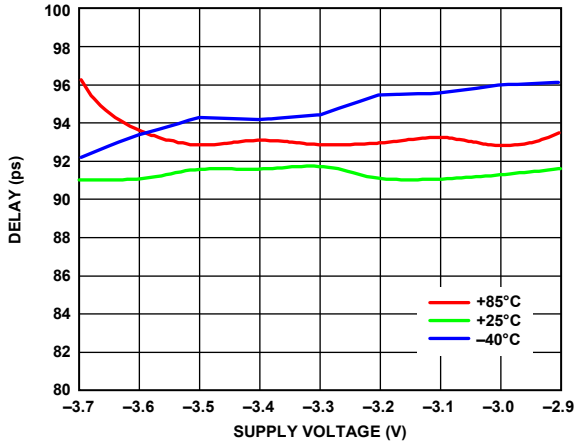


Figure 15. Delay vs. Supply Voltage at Various Temperatures

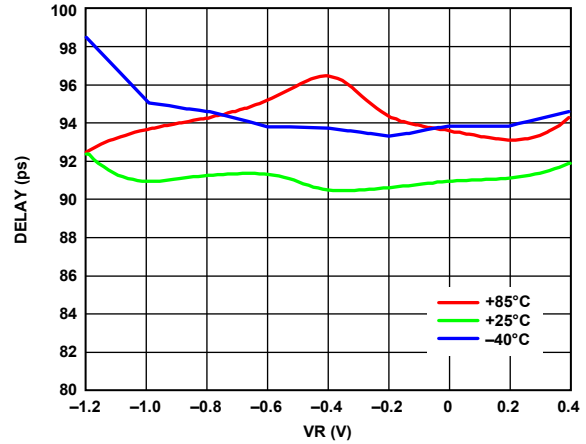


Figure 18. Delay vs. VR at Various Temperatures

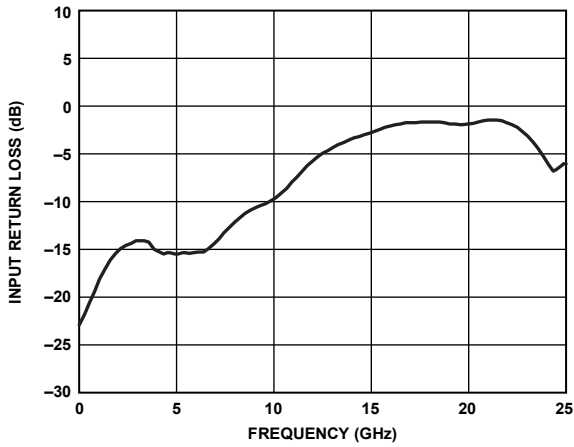


Figure 16. Input Return Loss vs. Frequency (Device Measured on an Evaluation Board with Port Extensions)

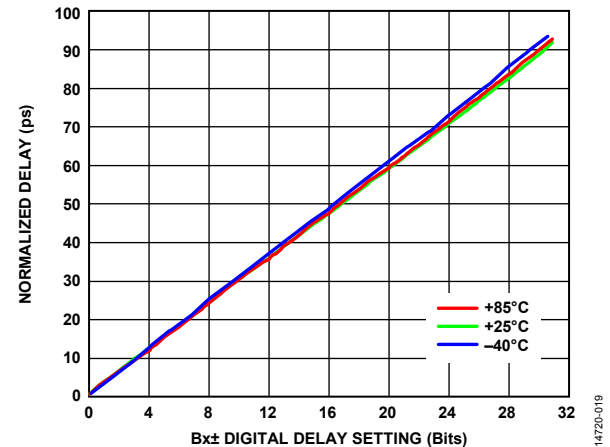


Figure 19. Normalized Delay vs. Bx± Digital Delay Setting (Device Measured on an Evaluation Board with Port Extensions Normalized to Minimum Delay, 0 Setting (B4±:B0± = 00000), at its Respective Temperature)

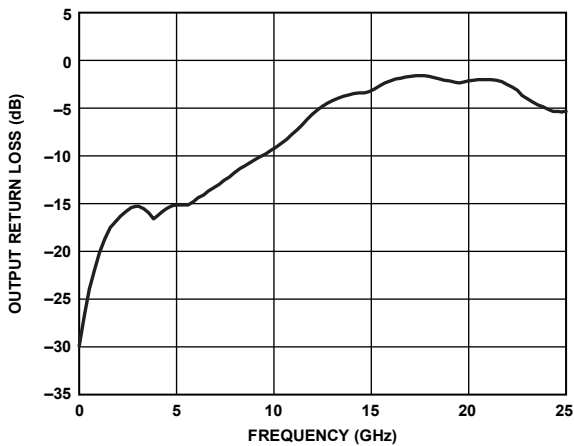


Figure 17. Output Return Loss vs. Frequency (Device Measured on an Evaluation Board with Port Extensions)

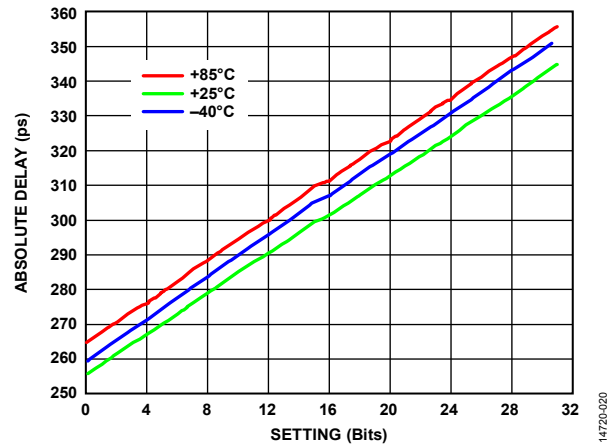


Figure 20. Absolute Delay vs. Setting (Normalized to 0 Setting at its Respective Temperature)



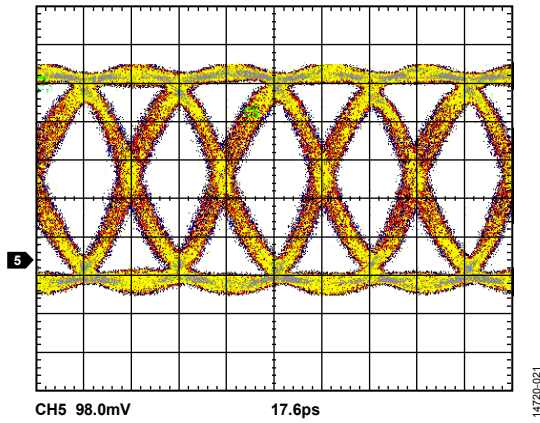


Figure 21. Single-Ended Output Eye Diagram at 28 Gbps, Measured  $V_{OUT} = 550\text{ mV p-p}$

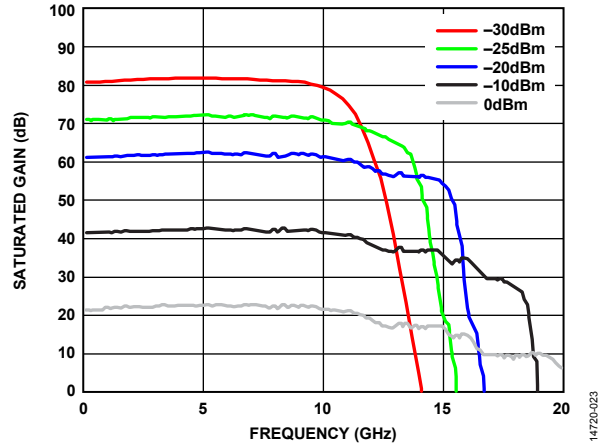


Figure 23. Saturated Gain vs. Frequency at Various Input Powers (Device Measured on an Evaluation Board with Port Extensions), The Output is Saturated, Limiting the Gain for Larger Input Signals, Gain  $\approx$  Saturated Output Power – Input Power

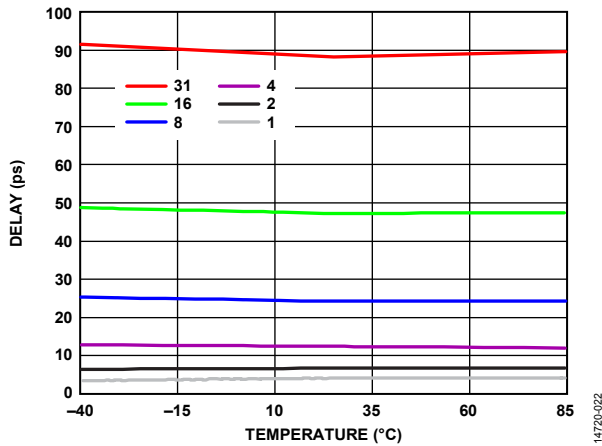


Figure 22. Delay vs. Temperature at Various Bit Settings (Device Measured on an Evaluation Board with Port Extensions)

## THEORY OF OPERATION

The [HMC856](#) is a wideband time delay device with a 5-bit digital control designed for timing compensation or clock skew management applications. The [HMC856](#) operates from a single  $-3.3$  V supply and is available in a  $5\text{ mm} \times 5\text{ mm}$  LCC package.

The [HMC856](#) can support data rates up to 28 Gbps and is able to provide 100 ps variable delay with 3 ps resolution. The total propagation delay of the [HMC856](#) varies between 250 ps and 350 ps. The maximum achievable bandwidth of the [HMC856](#) depends on the power of the input signal. The highest bandwidth of the device is at the larger input power levels, as shown in Figure 23.

The [HMC856](#) uses a CML interface, which uses  $50\ \Omega$  internal terminations to the ground. The input and output pins can be interfaced with either ac or dc coupling. For ac coupling, using a series resistor, which is effectively short circuit, and an ac load of

$50\ \Omega$  is recommended. For dc coupling, inputs and outputs can be directly interfaced with another CML circuit. The control lines, B4 to B0, are also CML, but they are terminated with  $600\ \Omega$  to the positive rail for low power operation.

The [HMC856](#) features an output level control pin, VR, that allows loss compensation or signal level optimization. VR can have a voltage value between  $-1.2$  V and  $0.4$  V, which results in a differential output swing of 500 mV p-p and 1350 mV p-p. Increasing the output swing affects the rise and fall times. As VR becomes higher, the rise and fall times increase. Changing the VR pin also changes the power dissipation because the [HMC856](#) can consume between 140 mA and 200 mA at room temperature depending on the VR pin.

## APPLICATIONS INFORMATION

### EVALUATION PRINTED CIRCUIT BOARD (PCB)

The evaluation PCB of the [HMC856](#) uses RF circuit design techniques. Signal lines must have 50 Ω impedance whereas the package ground leads must connect directly to the ground plane similar to that shown in Figure 25. The exposed metal package base must connect to V<sub>EE</sub>. A sufficient number of via holes must connect the top and bottom ground planes. The evaluation PCB shown in Figure 24 is available from Analog Devices, Inc., upon request. Install a jumper on the JP1 header to short VR to GND for normal operation.

Table 4. Bill of Materials for the Evaluation PCB [127102-HMC856LC5](#)<sup>1</sup>

| Item             | Description                                       |
|------------------|---|
| J1 to J4         | K connectors                                      |
| J5               | 0.1 inch 2 × 5 header                             |
| J7 to J14        | 0.04 inch dc pin                                  |
| JP1              | 0.1 inch 2 position header with shunt             |
| C1, C2           | 4.7 μF capacitor, Case A                          |
| C3 to C5         | 100 pF capacitor, 0402 package                    |
| R1, R8           | 10 Ω resistor, 0603 package                       |
| R2               | 1.2 kΩ resistor, 0603 package                     |
| R3 to R7         | 2.7 kΩ resistor, 0603 package                     |
| U1               | 28 Gbps digital time delay <a href="#">HMC856</a> |
| PCB <sup>2</sup> | 127100 evaluation board PCB                       |

<sup>1</sup> 127100 is the raw bare PCB. Reference [127102-HMC856LC5](#) when ordering the complete evaluation PCB.

<sup>2</sup> Use Arlon 25FR or Rogers 4350 for circuit board material.

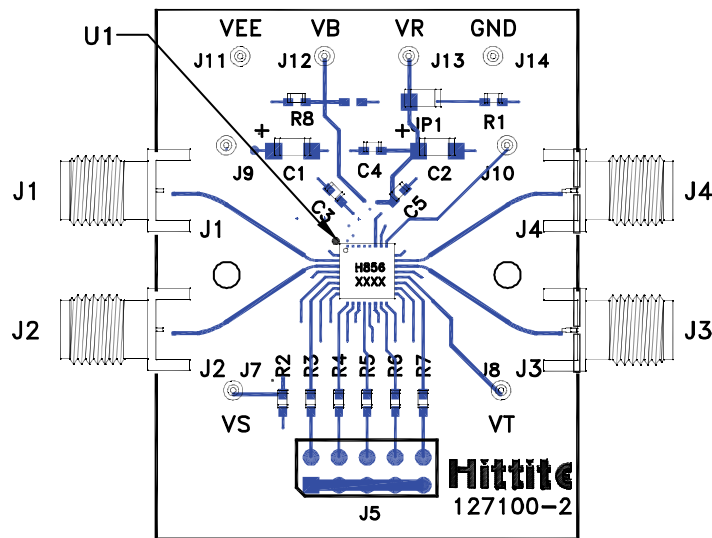


Figure 24. Evaluation Board Layout, Top Side

TYPICAL APPLICATION CIRCUIT

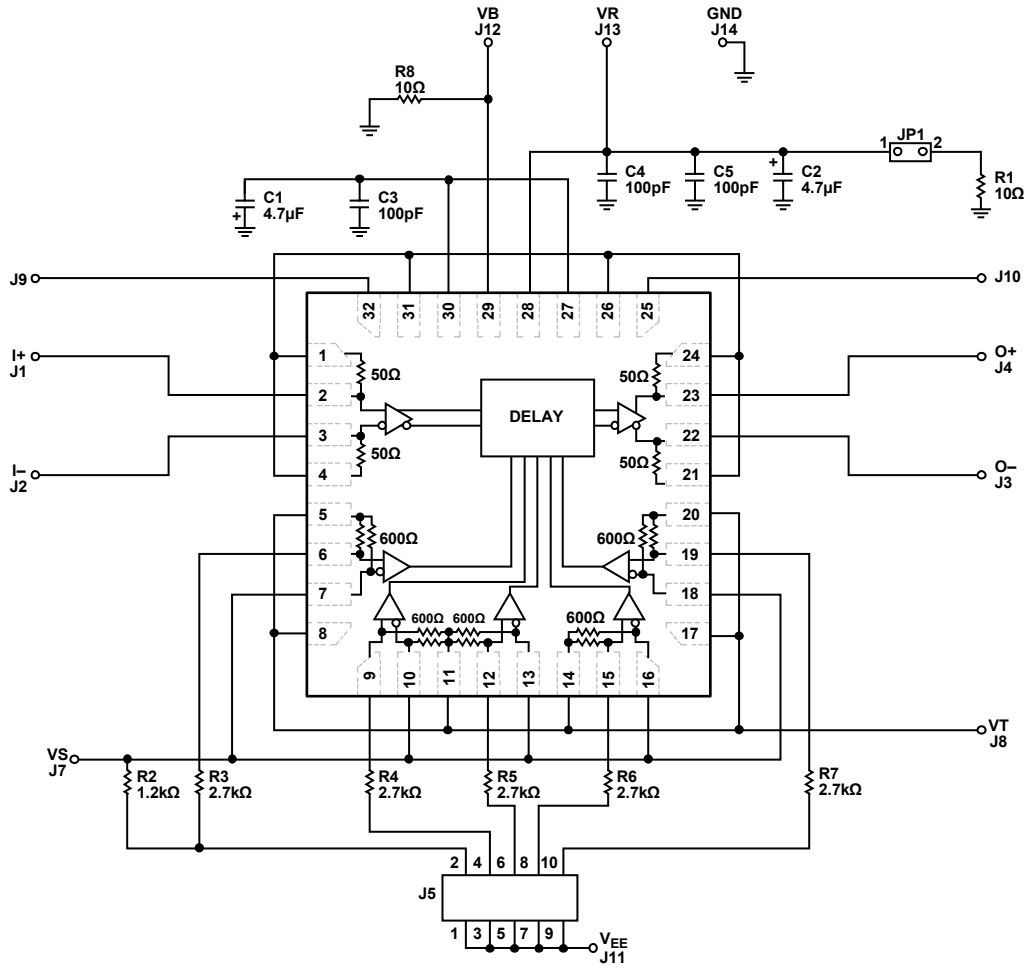


Figure 25. Typical Application Circuit

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