

Low Charge Injection, 8-Channel, High Voltage, Enhanced Analog Switch with Bleed Resistors

Features

- ▶ HVCMOS technology for high performance
- ▶ Integrated bleed resistors on the outputs
- ▶ 8 Channels of high voltage analog switch
- ▶ 3.3 or 5.0V CMOS input logic level
- ▶ 20MHz data shift clock frequency
- ▶ Very low quiescent power dissipation (-10µA)
- ▶ Low parasitic capacitance
- ▶ DC to 50MHz analog signal frequency
- ▶ -60dB typical off-isolation at 5MHz
- ▶ CMOS logic circuitry for low power
- ▶ Excellent noise immunity
- ▶ Cascadable serial data register with latches
- ▶ Flexible operating supply voltages

Applications

- ▶ Medical ultrasound imaging
- ▶ NDT metal flaw detection
- ▶ Piezoelectric transducer drivers
- ▶ Inkjet printer heads
- ▶ Optical MEMS modules

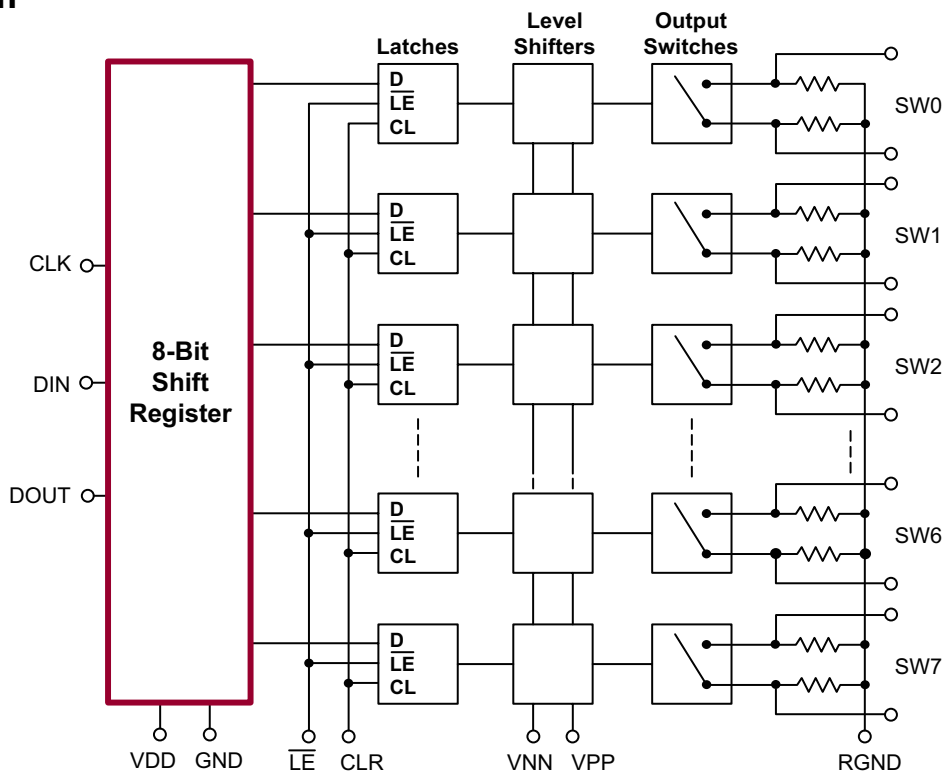
General Description

The Supertex HV2301 is a low charge injection, 8-channel, high voltage analog switch integrated circuit (IC) with bleed resistors. The device can be used in applications requiring high voltage switching, controlled by low voltage control signals, such as medical ultrasound imaging, piezoelectric transducer driver, and printers. The built-in bleed resistors eliminate voltage built up on capacitive loads such as piezoelectric transducers. The HV2301 is an enhanced version of the HV232.

Input data is shifted into an 8-bit shift register that can then be retained in an 8-bit latch. To reduce any possible clock feed-through noise, the latch enable bar should be left high until all bits are clocked in. Data is clocked in during the rising edge of the clock. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN} : +40V/-160V, +100V/-100V, and +160V/-40V.

Block Diagram



Ordering Information

| Device | Package Options | |
|--------|---|---|
| | 48-Lead LQFP 7.00x7.00mm body 1.60mm height (max) 0.50mm pitch | 28-Lead PLCC .453x.453in body .180in height (max) .050in pitch |
| HV2301 | HV2301FG-G | HV2301PJ-G |



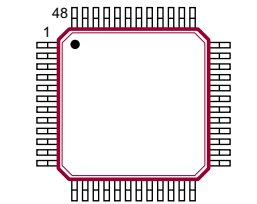
-G indicates the part is RoHS compliant (Green)

Absolute Maximum Ratings

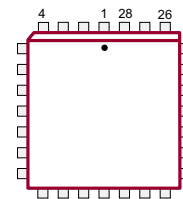
| Parameter | Value |
|---|-------------------------|
| V_{DD} logic supply | -0.5V to +7V |
| V_{PP} - V_{NN} differential supply | 220V |
| V_{PP} positive supply | -0.5V to V_{NN} +200V |
| V_{NN} negative supply | +0.5V to -200V |
| Logic input voltage | -0.5V to V_{DD} +0.3V |
| Analog signal range | V_{NN} to V_{PP} |
| Peak analog signal current/channel | 3.0A |
| Storage temperature | -65°C to 150°C |
| Power dissipation: | |
| 48-Lead LQFP | 1.0W |
| 28-Lead PLCC | 1.2W |

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



48-Lead LQFP (FG)
(top view)



28-Lead PLCC (PJ)
(top view)

Operating Conditions

| Sym | Parameter | Value |
|-----------|------------------------------------|--------------------------------|
| V_{DD} | Logic power supply voltage | 3.0V to 5.5V |
| V_{PP} | Positive high voltage supply | 40V to V_{NN} +200V |
| V_{NN} | Negative high voltage supply | -40V to -160V |
| V_{IH} | High level input voltage | 0.9 V_{DD} to V_{DD} |
| V_{IL} | Low-level input voltage | 0V to 0.1 V_{DD} |
| V_{SIG} | Analog signal voltage peak-to-peak | V_{NN} +10V to V_{PP} -10V |
| T_A | Operating free air temperature | 0°C to 70°C |

Notes:

- Power up/down sequence is arbitrary except GND must be powered-up first and powered down last.
- V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transition.
- Rise and fall times of power supplies V_{DD} , V_{PP} and V_{NN} should not be less than 1.0msec.

Product Marking

Top Marking



YY = Year Sealed
WW = Week Sealed
L = Lot Number

Bottom Marking

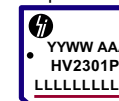


C = Country of Origin*
A = Assembler ID*
— = "Green" Packaging
*May be part of top marking

Package may or may not include the following marks: Si or

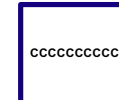
48-Lead LQFP (FG)

Top Marking



YY = Year Sealed
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L = Lot Number
A = Assembler ID

Bottom Marking



C = Country of Origin*
— = "Green" Packaging
*May be part of top marking

Package may or may not include the following marks: Si or

28-Lead PLCC (PJ)

DC Electrical Characteristics

(Over operating conditions unless otherwise specified)

| Sym | Parameter | 0°C | | +25°C | | | +70°C | | Units | Conditions | |
|-------------------|--|------|-----|-------|------|-----|-------|-----|-------|---|--|
| | | Min | Max | Min | Typ | Max | Min | Max | | | |
| R _{ONS} | Small signal switch on-resistance | - | 30 | - | 26 | 38 | - | 48 | Ω | I _{SIG} = 5.0mA | V _{PP} = +40V V _{NN} = -160V |
| | | - | 25 | - | 22 | 27 | - | 32 | | I _{SIG} = 200mA | |
| | | - | 25 | - | 22 | 27 | - | 30 | | I _{SIG} = 5.0mA | V _{PP} = +100V V _{NN} = -100V |
| | | - | 18 | - | 18 | 24 | - | 27 | | I _{SIG} = 200mA | |
| | | - | 23 | - | 20 | 25 | - | 30 | | I _{SIG} = 5.0mA | V _{PP} = +160V V _{NN} = -40V |
| | | - | 22 | - | 16 | 25 | - | 27 | | I _{SIG} = 200mA | |
| ΔR _{ONS} | Small signal switch on-resistance matching | - | 20 | - | 5.0 | 20 | - | 20 | % | I _{SIG} = 5.0mA, V _{PP} = +100V, V _{NN} = -100V | |
| R _{ONL} | Large signal switch on-resistance | - | - | - | 15 | - | - | - | Ω | V _{SIG} = V _{PP} -10V, I _{SIG} = 1.0A | |
| R _{INT} | Value of output bleed resistance | - | - | 20 | 35 | 50 | - | - | KΩ | Output switch to RGND I _{RINT} = 0.5mA | |
| I _{SOL} | Switch off leakage per switch | - | 5.0 | - | 1.0 | 10 | - | 15 | μA | V _{SIG} = V _{PP} -10V, V _{NN} +10V | |
| V _{OS} | DC offset switch off | - | 300 | - | 100 | 300 | - | 300 | mV | No load | |
| | DC offset switch on | - | 500 | - | 100 | 500 | - | 500 | mV | | |
| I _{PPQ} | Quiescent V _{PP} supply current | - | - | - | 10 | 50 | - | - | μA | All switches off | |
| I _{NNQ} | Quiescent V _{NN} supply current | - | - | - | -10 | -50 | - | - | μA | All switches off | |
| I _{PPQ} | Quiescent V _{PP} supply current | - | - | - | 10 | 50 | - | - | μA | All switches on, I _{SW} = 5.0mA | |
| I _{NNQ} | Quiescent V _{NN} supply current | - | - | - | -10 | -50 | - | - | μA | All switches on, I _{SW} = 5.0mA | |
| I _{SW} | Switch output peak current | - | 3.0 | - | 3.0 | 2.0 | - | 2.0 | A | V _{SIG} duty cyclcy < 0.1% | |
| f _{SW} | Output switching frequency | - | - | - | - | 50 | - | - | kHz | Duty cycle = 50% | |
| I _{PP} | Average V _{PP} supply current | - | 4.0 | - | - | 5.0 | - | 5.5 | mA | V _{PP} = +40V V _{NN} = -160V | All output switches are turning on and off at 50kHz with no load |
| | | - | 3.5 | - | - | 3.5 | - | 3.5 | | V _{PP} = +100V V _{NN} = -100V | |
| | | - | 3.5 | - | - | 3.5 | - | 4.0 | | V _{PP} = +160V V _{NN} = -40V | |
| I _{NN} | Average V _{NN} supply curent | - | 4.5 | - | - | 5.0 | - | 5.5 | mA | V _{PP} = +40V V _{NN} = -160V | All output switches are turning on and off at 50kHz with no load |
| | | - | 3.5 | - | - | 3.5 | - | 3.5 | | V _{PP} = +100V V _{NN} = -100V | |
| | | - | 3.5 | - | - | 3.5 | - | 4.0 | | V _{PP} = +160V V _{NN} = -40V | |
| I _{DD} | Average V _{DD} supply current | - | 4.0 | - | - | 4.0 | - | 4.0 | mA | f _{CLK} = 5.0MHZ, V _{DD} = 5.0V | |
| I _{DDQ} | Quiescent V _{DD} supply current | - | 10 | - | - | 10 | - | 10 | μA | All logic inputs are static | |
| I _{SOR} | Data out source current | 0.45 | - | 0.45 | 0.70 | - | 0.40 | - | mA | V _{OUT} = V _{DD} -0.7V | |
| I _{SINK} | Data out sink current | 0.45 | - | 0.45 | 0.70 | - | 0.40 | - | mA | V _{OUT} = 0.7V | |
| C _{IN} | Logic input capacitance | - | 10 | - | - | 10 | - | 10 | pF | --- | |

AC Electrical Characteristics

(Over recommended operating conditions: $V_{DD} = 5.0V$, $t_R = t_F \leq 5ns$, 50% duty cycle, $C_{LOAD} = 20pF$ unless otherwise specified)

| Sym | Parameter | 0°C | | +25°C | | | +70°C | | Units | Conditions |
|---------------|--|-----|-----|-------|-----|-----|-------|-----|---------|---|
| | | Min | Max | Min | Typ | Max | Min | Max | | |
| t_{SD} | Set up time before \overline{LE} rises | 25 | - | 25 | - | - | 25 | - | ns | --- |
| t_{WLE} | Time width of \overline{LE} | 56 | - | - | 56 | - | 56 | - | ns | $V_{DD} = 3.0V$ |
| | | 12 | - | - | 12 | - | 12 | - | | $V_{DD} = 5.0V$ |
| t_{DO} | Clock delay time to data out | - | 120 | - | 95 | 140 | - | 167 | ns | $V_{DD} = 3.0V$ |
| | | - | 58 | - | 40 | 69 | - | 85 | | $V_{DD} = 5.0V$ |
| t_{WCL} | Time width of CL | 55 | - | 55 | 30 | - | 55 | - | ns | --- |
| t_{SU} | Set up time data to clock | 39 | - | 47 | 30 | - | 58 | - | ns | $V_{DD} = 3.0V$ |
| | | 16 | - | 21 | 10 | - | 26 | - | | $V_{DD} = 5.0V$ |
| t_H | Hold time data from clock | 2 | - | 2 | - | - | 2 | - | ns | $V_{DD} = 3.0$ or $5.0V$ |
| f_{CLK} | Clock frequency | - | - | - | - | 8.0 | - | - | MHz | $V_{DD} = 3.0V$ |
| | | - | 20 | - | - | 20 | - | 20 | | $V_{DD} = 5.0V$ |
| t_R, t_F | Clock rise and fall times | - | 50 | - | - | 50 | - | 50 | ns | --- |
| t_{ON} | Turn on time | - | 5.0 | - | - | 5.0 | - | 5.0 | μs | $V_{SIG} = V_{PP} - 10V, R_{LOAD} = 10k\Omega$ |
| t_{OFF} | Turn off time | - | 5.0 | - | - | 5.0 | - | 5.0 | μs | $V_{SIG} = V_{PP} - 10V, R_{LOAD} = 10k\Omega$ |
| dv/dt | Maximun V_{SIG} slew rate | - | 20 | - | - | 20 | - | 20 | V/ns | $V_{PP} = +40V, V_{NN} = -160V$ |
| | | - | 20 | - | - | 20 | - | 20 | | $V_{PP} = +100V, V_{NN} = -100V$ |
| | | - | 20 | - | - | 20 | - | 20 | | $V_{PP} = +160V, V_{NN} = -40V$ |
| K_O | Off isolation | -30 | - | -30 | -33 | - | -30 | - | dB | $f = 5.0MHz, 1k\Omega/15pF$ load |
| | | -58 | - | -58 | - | - | -58 | - | | $f = 5.0MHz, 50\Omega$ load |
| K_{CR} | Switch crosstalk | -60 | - | -60 | -70 | - | -60 | - | dB | $f = 5.0MHz, 50\Omega$ load |
| I_{ID} | Output switch isolation diode current | - | 300 | - | - | 300 | - | 300 | mA | 300ns pulse width, 2.0% duty cycle |
| $C_{SG(OFF)}$ | Off capacitance SW to GND | 5.0 | 17 | 5.0 | 12 | 17 | 5.0 | 17 | pF | 0V, $f = 1.0MHz$ |
| $C_{SG(ON)}$ | On capacitance SW to GND | 25 | 50 | 25 | 38 | 50 | 25 | 50 | pF | 0V, $f = 1.0MHz$ |
| $+V_{SPK}$ | Output voltage spike | - | - | - | - | 150 | - | - | mV | $V_{PP} = +40V, V_{NN} = -160V, R_{LOAD} = 50\Omega$ |
| $-V_{SPK}$ | | - | - | - | - | 150 | - | - | | |
| $+V_{SPK}$ | | - | - | - | - | 150 | - | - | | $V_{PP} = +100V, V_{NN} = -100V, R_{LOAD} = 50\Omega$ |
| $-V_{SPK}$ | | - | - | - | - | 150 | - | - | | |
| $+V_{SPK}$ | | - | - | - | - | 150 | - | - | | $V_{PP} = +160V, V_{NN} = -40V, R_{LOAD} = 50\Omega$ |
| $-V_{SPK}$ | | - | - | - | - | 150 | - | - | | |
| QC | Charge injection | - | - | - | 820 | - | - | - | pC | $V_{PP} = +40V, V_{NN} = -160V, V_{SIG} = 0V$ |
| | | - | - | - | 600 | - | - | - | | $V_{PP} = +100V, V_{NN} = -100V, V_{SIG} = 0V$ |
| | | - | - | - | 350 | - | - | - | | $V_{PP} = +160V, V_{NN} = -40V, V_{SIG} = 0V$ |

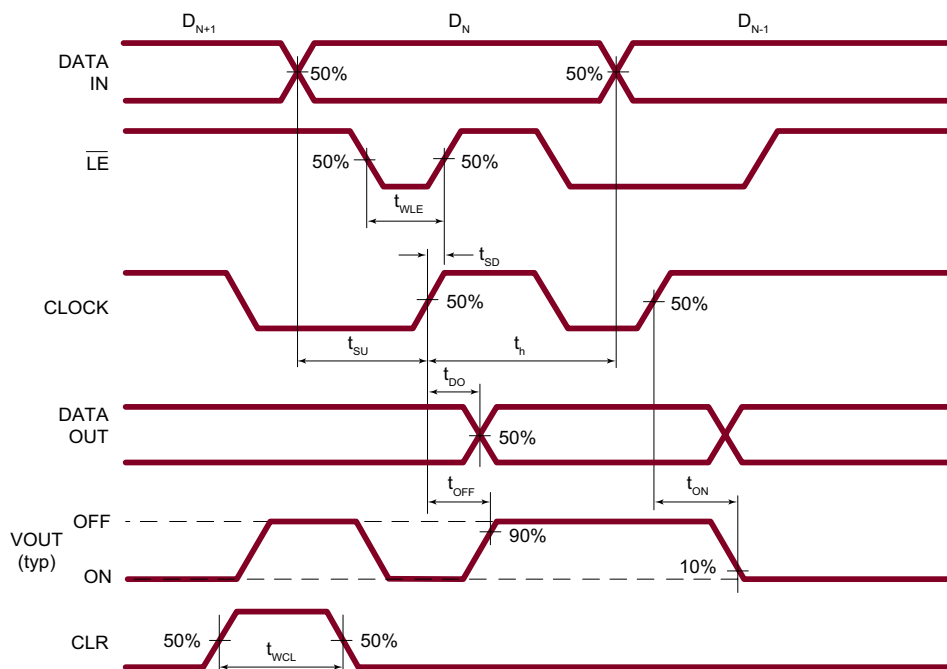
Truth Table

| D0 | D1 | D2 | D3 | D4 | D5 | D6 | D7 | \overline{LE} | CLR | SW0 | SW1 | SW2 | SW3 | SW4 | SW5 | SW6 | SW7 |
|----|----|----|----|----|----|----|----|-----------------|-----|---------------------|-----|-----|-----|-----|-----|-----|-----|
| L | | | | | | | | L | L | Off | | | | | | | |
| H | | | | | | | | L | L | On | | | | | | | |
| | L | | | | | | | L | L | | Off | | | | | | |
| | H | | | | | | | L | L | | On | | | | | | |
| | | L | | | | | | L | L | | | Off | | | | | |
| | | H | | | | | | L | L | | | On | | | | | |
| | | | L | | | | | L | L | | | | Off | | | | |
| | | | H | | | | | L | L | | | | On | | | | |
| | | | | L | | | | L | L | | | | | Off | | | |
| | | | | H | | | | L | L | | | | | On | | | |
| | | | | | L | | | L | L | | | | | | Off | | |
| | | | | | H | | | L | L | | | | | | On | | |
| | | | | | | L | | L | L | | | | | | | | Off |
| | | | | | | H | | L | L | | | | | | | | On |
| | | | | | | | L | L | L | | | | | | | | Off |
| | | | | | | | H | L | L | | | | | | | | On |
| X | X | X | X | X | X | X | X | H | L | Hold Previous State | | | | | | | |
| X | X | X | X | X | X | X | X | X | H | All Switches Off | | | | | | | |

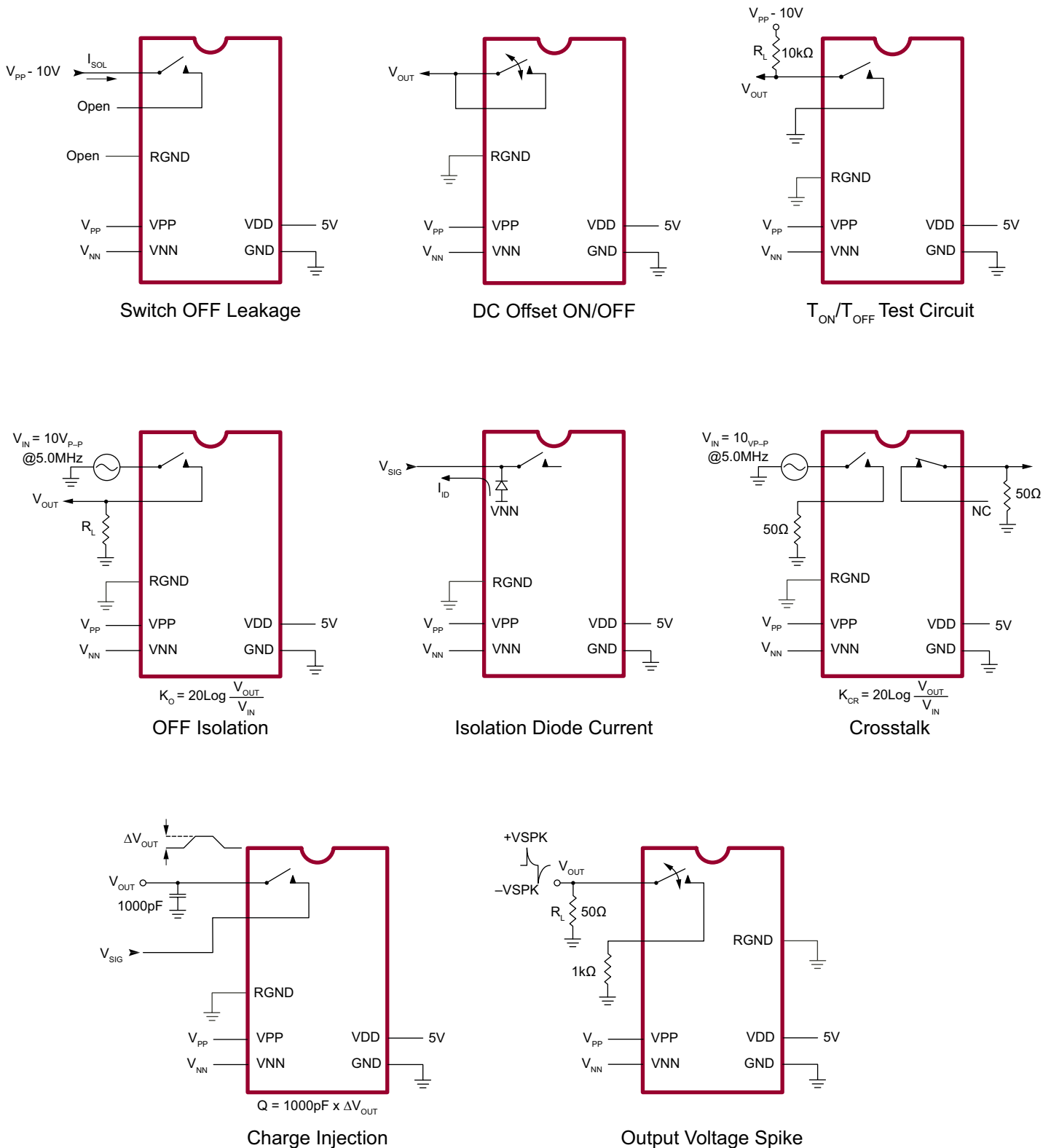
Notes:

1. The eight switches operate independently.
2. Serial data is clocked in on the L to H transition of the CLK.
3. The switches go to a state retaining their present condition at the rising edge of \overline{LE} . When \overline{LE} is low the shift register data flow through the latch.
4. D_{OUT} is high when data in the shift register 7 is high.
5. Shift register clocking has no effect on the switch states if \overline{LE} is high.
6. The CLR clear input overrides all other inputs.

Typical Waveforms



Test Circuits



Pin Configuration 48-Lead LQFP (FG)

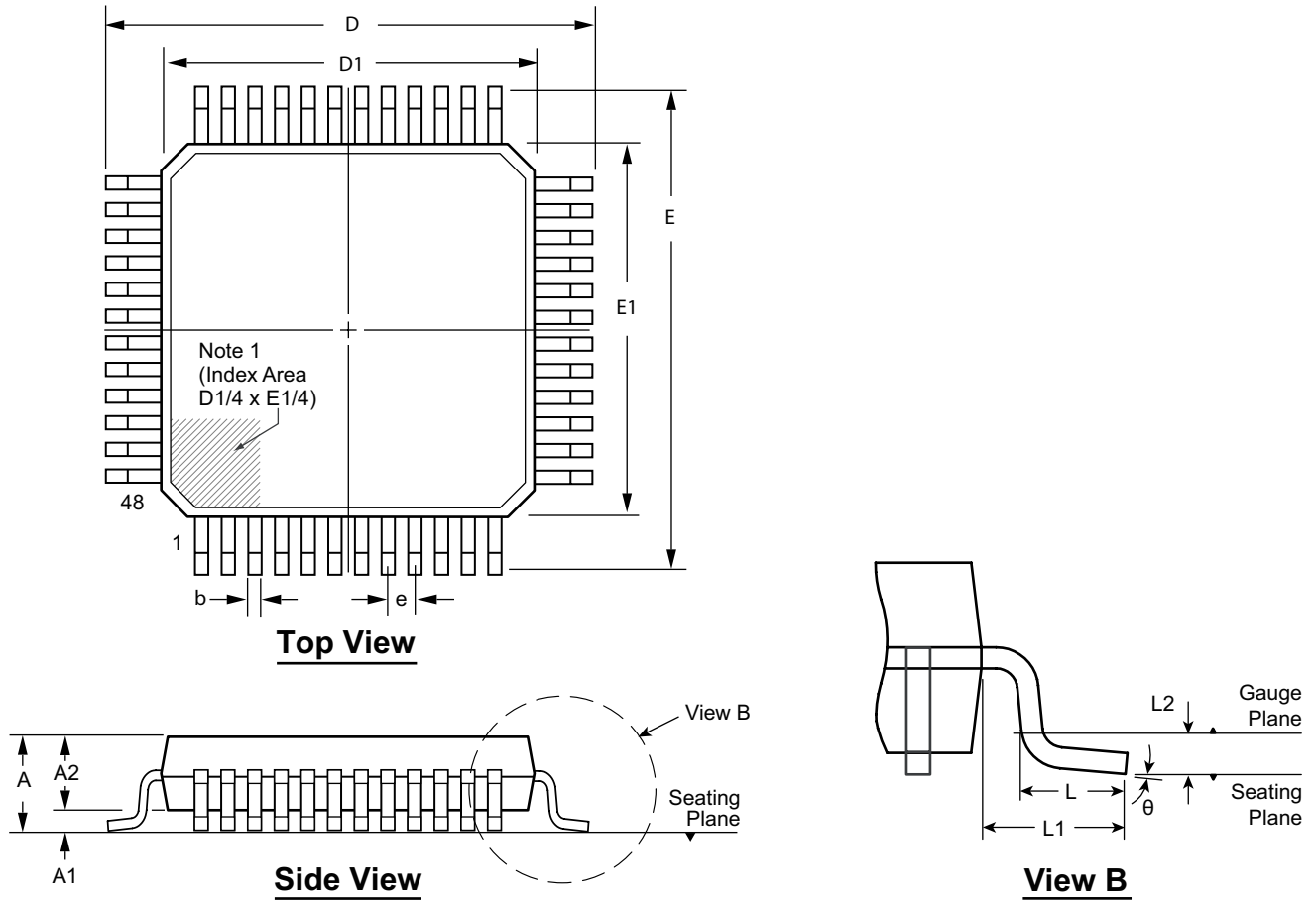
| Pin # | Pin Name | Pin # | Pin Name |
|-------|----------|-------|-----------------|
| 1 | SW5 | 25 | VNN |
| 2 | NC | 26 | NC |
| 3 | SW4 | 27 | RGND |
| 4 | NC | 28 | GND |
| 5 | SW4 | 29 | VDD |
| 6 | NC | 30 | NC |
| 7 | NC | 31 | NC |
| 8 | SW3 | 32 | NC |
| 9 | NC | 33 | DIN |
| 10 | SW3 | 34 | CLK |
| 11 | NC | 35 | \overline{LE} |
| 12 | SW2 | 36 | CLR |
| 13 | NC | 37 | DOUT |
| 14 | SW2 | 38 | NC |
| 15 | NC | 39 | SW7 |
| 16 | SW1 | 40 | NC |
| 17 | NC | 41 | SW7 |
| 18 | SW1 | 42 | NC |
| 19 | NC | 43 | SW6 |
| 20 | SW0 | 44 | NC |
| 21 | NC | 45 | SW6 |
| 22 | SW0 | 46 | NC |
| 23 | NC | 47 | SW5 |
| 24 | VPP | 48 | NC |

Pin Configuration 28-Lead PLCC (PJ)

| Pin # | Pin Name | Pin # | Pin Name |
|-------|----------|-------|-----------------|
| 1 | SW3 | 15 | NC |
| 2 | SW3 | 16 | DIN |
| 3 | SW2 | 17 | CLK |
| 4 | SW2 | 18 | \overline{LE} |
| 5 | SW1 | 19 | CLR |
| 6 | SW1 | 20 | DOUT |
| 7 | SW0 | 21 | SW7 |
| 8 | SW0 | 22 | SW7 |
| 9 | NC | 23 | SW6 |
| 10 | VPP | 24 | SW6 |
| 11 | RGND | 25 | SW5 |
| 12 | VNN | 26 | SW5 |
| 13 | GND | 27 | SW4 |
| 14 | VDD | 28 | SW4 |

48-Lead LQFP Package Outline (FG)

7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Note:
1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

| Symbol | A | A1 | A2 | b | D | D1 | E | E1 | e | L | L1 | L2 | θ | |
|----------------|-----|-------|------|------|------|-------|-------|-------|-------|----------|------|----------|----------|----|
| Dimension (mm) | MIN | 1.40* | 0.05 | 1.35 | 0.17 | 8.80* | 6.80* | 8.80* | 6.80* | 0.50 BSC | 0.45 | 1.00 REF | 0.25 BSC | 0° |
| | NOM | - | - | 1.40 | 0.22 | 9.00 | 7.00 | 9.00 | 7.00 | | 0.60 | | 3.5° | |
| | MAX | 1.60 | 0.15 | 1.45 | 0.27 | 9.20* | 7.20* | 9.20* | 7.20* | | 0.75 | | 7° | |

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.
* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.
Supertex Doc. #: DSPD-48LQFPFG Version, D041309.