HV9921/HV9922/HV9923

3-Pin Switch-Mode LED Lamp Driver ICs

Features

- Constant output current:
  - HV9921 – 20mA
  - HV9922 – 50mA
  - HV9923 – 30mA
- Universal 85 - 264VAC operation
- Fixed off-time buck converter
- Internal 475V power MOSFET

Applications

- Decorative lighting
- Low power lighting fixtures

Description

HV9921/HV9922/HV9923 are pulse-width modulated (PWM), high-efficiency, LED driver control ICs. They allow efficient operation of LED strings from voltage sources ranging up to 400VDC. HV9921/22/23 include an internal high voltage switching MOSFET controlled with fixed off-time (T_{OFF}) of approximately 10µs. The LED string is driven at constant current, thus providing constant light output and enhanced reliability. The output current is internally fixed at 20mA for HV9921, 50mA for HV992, and 30mA for HV9923. The peak current control scheme provides good regulation of the output current throughout the universal AC line voltage range of 85 to 264VAC or DC input voltage of 20 to 400V.

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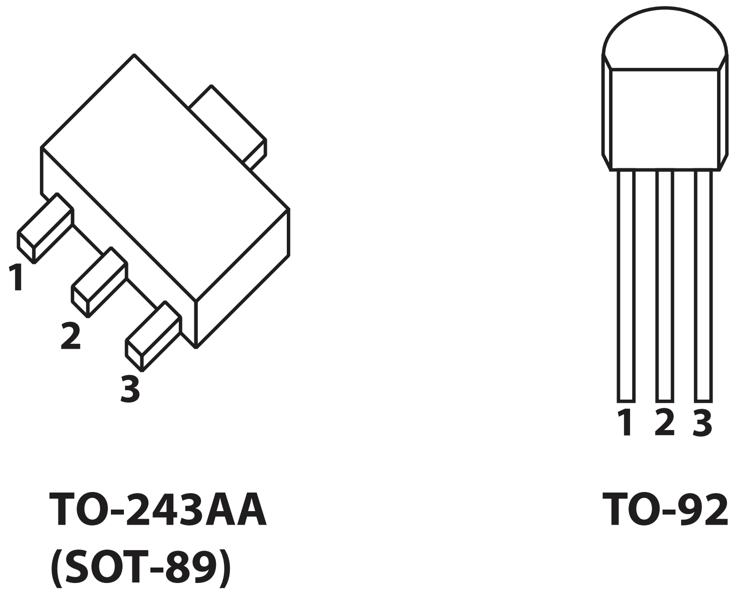
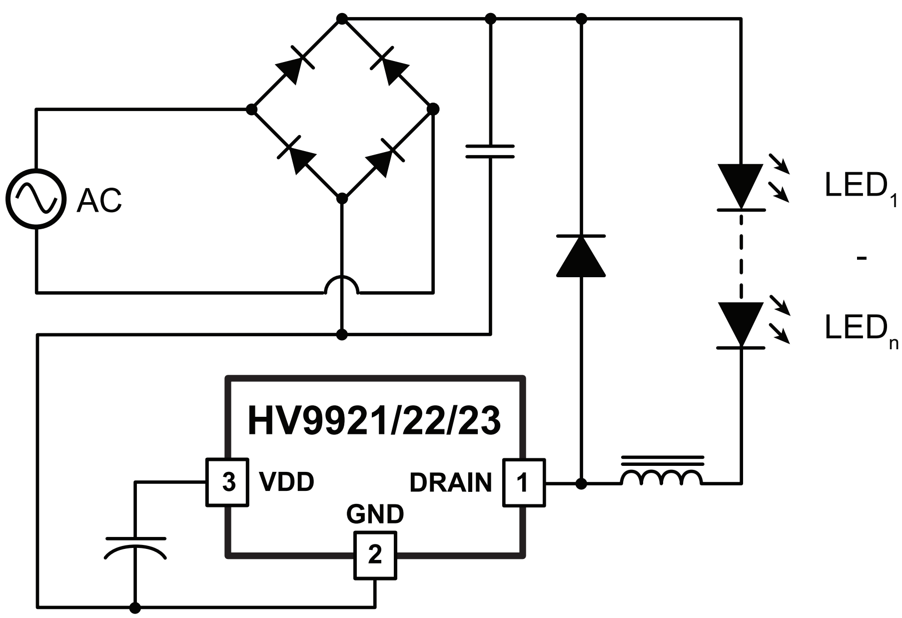
PIN DIAGRAM



See Table 2-1 for Pin information.

TYPICAL APPLICATION CIRCUIT



1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{DD} .... -0.3V to +10V
Supply Current I_{DD} .... +5mA
Operating Ambient temperature .... -40°C to +85°C
Operating Junction Temperature .... -40°C to +125°C
Storage temperature .... -65°C to +150°C
Power dissipation @+25°C for TO-92 .... 740 mW
Power dissipation @+25°C for SOT-89 .... 1600 mW*

* Mounted on FR4 board, 24mmx25mmx1.57mm

Note: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions, above those indicated in the operational listings of this specification, is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

1.1 ELECTRICAL SPECIFICATIONS

TABLE 1-1: ELECTRICAL CHARACTERISTICS[1]

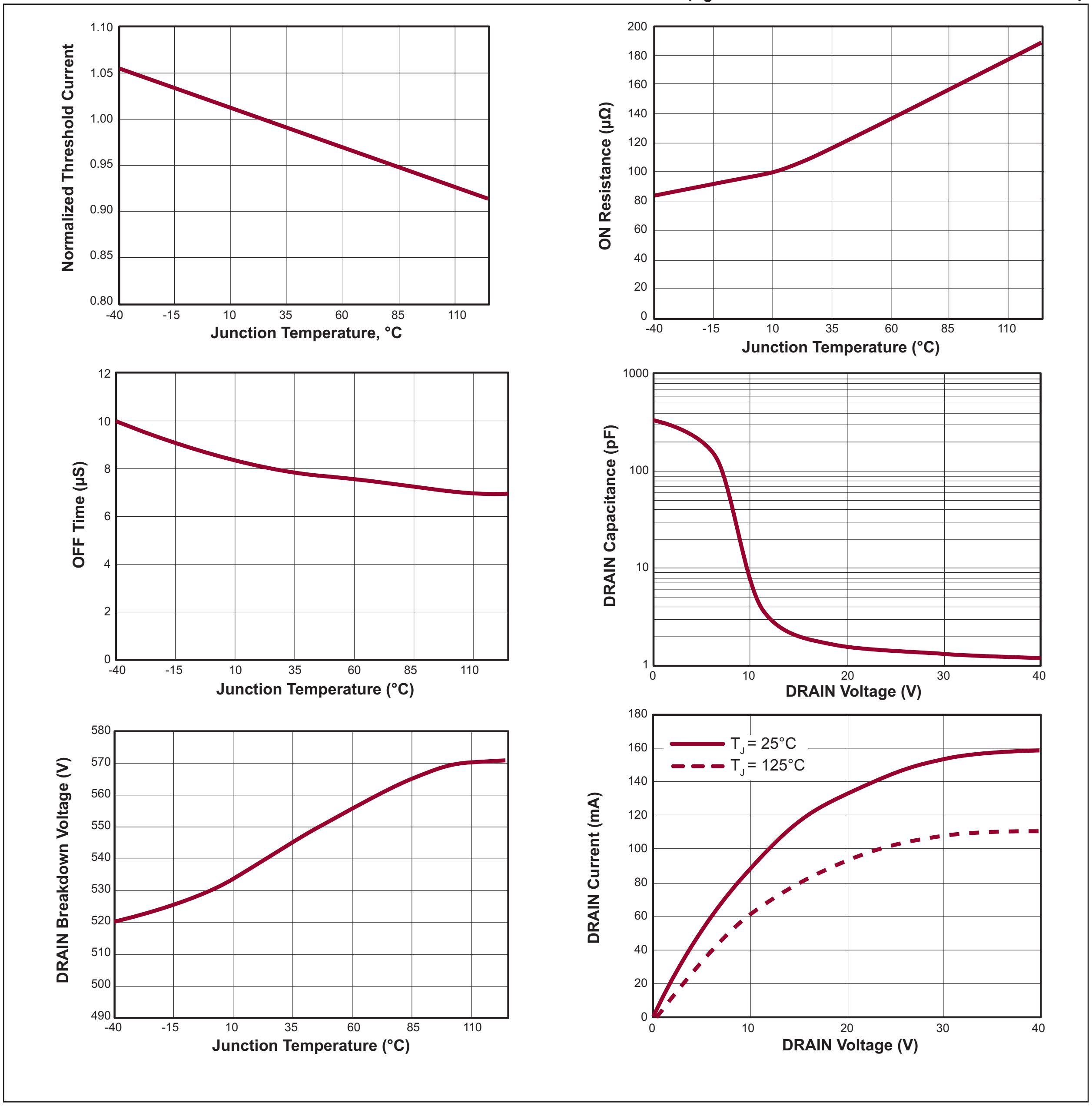
Symbol	Parameter	Notes	Min	Typ	Max	Units	Conditions
Regulator (V_{DD})							
V_{DD}	V_{DD} Regulator Output	-	-	7.5	-	V	
V_{DRAIN}	V_{DRAIN} Supply Voltage	-	20	-	-	V	
V_{UVLO}	V_{DD} Under-voltage Threshold	-	5.0	-	-	V	
ΔV_{UVLO}	V_{DD} Under-voltage Lockout Hysteresis	-	-	200	-	mV	
I_{DD}	Operating Supply Current	-	-	200	350	µA	$V_{DD(EXT)}$ = 8.5V, V_{DRAIN} = 40V
Output (DRAIN)							
V_{BR}	Breakdown Voltage	2	475	-	-	V	
R_{ON}	ON Resistance	-	-	-	210	Ω	I_{DRAIN}= 20mA (HV9921) I_{DRAIN}= 50mA (HV9922) I_{DRAIN}= 30mA (HV9923)
C_{DRAIN}	Output Capacitance	3	-	1	5	pF	V_{DRAIN} = 400V
I_{SAT}	MOSFET Saturation Current	3	100	150	-	mA	
Current Sense Comparator							
I_{THL}	Threshold Current - HV9921	2	18.5	-	25.5	mA	
	Threshold Current - HV9922	2	49	-	63	mA	
	Threshold Current - HV9923	2	28.2	-	38.2	mA	
T_{BLANK}	Leading Edge Blanking Delay	2, 3	200	300	400	ns	
$T_{ON(MIN)}$	Minimum ON Time	-	-	-	650	ns	
OFF-Time Generator							
T_{OFF}	OFF Time	-	8	10.5	13	µS	

1 Specifications are T_A = 25°C, V_{DRAIN} = 50V unless otherwise noted.
2 Applies over the full operating ambient temperature range of -40°C < T_A < +125°C.
3 For design guidance only

THERMAL RESISTANCE

Package	θja
TO-92	132°C/W
TO-243AA(SOT-89)	133°C/W

FIGURE 1-1: TYPICAL PERFORMANCE CHARACTERISTICS (T_J= 25°C UNLESS OTHERWISE NOTED)



2.0 PIN DESCRIPTION

See Pin Diagram on page 3 for the figures.

TABLE 2-1: PIN DESCRIPTION

Pin #	Name	Description
1	Drain	Drain terminal of the output switching MOSFET and a linear regulator input
2	GND	Common connection for all circuits
3	VDD	Power Supply pin for all control circuits. By pass this pin with a 0.1 µF low-impedance capacitor

3.0 FUNCTIONAL DESCRIPTION

The HV9921/22/23 are PWM peak current controllers designed to control a buck converter topology in continuous conduction mode (CCM). The output current is internally preset at 20mA for HV9921, 50mA for HV992, and 30mA for HV9923.

When the input voltage of 20 to 400V appears at the DRAIN pin, the internal high-voltage linear regulator seeks to maintain a voltage of 7.5VDC at the V_{DD} pin. Until this voltage exceeds the internally programmed under-voltage threshold, the output switching MOSFET is non-conductive. When the threshold is exceeded, the MOSFET turns on. The input current begins to flow into the DRAIN pin. Hysteresis is provided in the under-voltage comparator to prevent oscillation.

When the input current exceeds the internal preset level, a current sense comparator resets an RS flip-flop, and the MOSFET turns off. At the same time, a one-shot circuit is activated that determines the duration of the off-state (10.5µs typical). As soon as this time is over, the flip-flop sets again. The new switching cycle begins.

A “blanking” delay of 300ns is provided that prevents false triggering of the current sense comparator due to the leading edge spike caused by circuit parasitics.

4.0 APPLICATION INFORMATION

HV9921/22/23 are low-cost off-line buck converter ICs specifically designed for driving multi-LED strings. They can be operated from either universal AC line range of 85 to 264VAC, or 20 to 400VDC, and drive up to tens of high-brightness LEDs. All LEDs can be run in series, and the HV9921/22/23 regulate at constant current, yielding uniform illumination. HV9921/22/23 are compatible with triac dimmers. The output current is internally fixed at 20mA for HV9921, 50mA for HV9922, and 30mA for HV9923. These parts are available in space saving TO-92 and SOT-89 packages.

4.1 Selecting L1 and D1

There is a certain trade-off to be considered between optimal sizing of the output inductor L1 and the tolerated output current ripple. The required value of L1 is inversely proportional to the ripple current ΔI_O in it.

$$L1 = \frac{V_O \bullet T_{OFF}}{\Delta I_O}$$

V_O is the forward voltage of the LED string. T_{OFF} is the off-time of HV9921/22/23. The output current in the LED string (I_O) is calculated then as:

$$I_O = I_{TH} - \left(\frac{1}{2} \bullet \Delta I_O\right)$$

where I_{TH} is the current sense comparator threshold. The ripple current introduces a peak-to-average error in the output current setting that needs to be accounted for. Due to the constant off-time control technique used in HV9921/22/23, the ripple current is independent of the input AC or DC line voltage variation. Therefore, the output current will remain unaffected by the varying input voltage.

Adding a filter capacitor across the LED string can reduce the output current ripple even further, thus permitting a reduced value of L1. However, keep in mind that the peak-to-average current error is affected by the variation of T_{OFF}. Therefore, the initial output current accuracy might be sacrificed at large ripple current in L1.

Another important aspect of designing an LED driver with the HV9921/22/23 is related to certain parasitic elements of the circuit, including distributed coil capacitance of L1, junction capacitance and reverse recovery of the rectifier diode D1, capacitance of the printed circuit board traces C_{PCB} and output capacitance C_{DRAIN} of the controller itself. These parasitic elements affect the efficiency of the switching converter and could potentially cause false triggering of the current sense comparator if not properly managed. Minimizing these parasitics is essential for efficient and reliable operation of the HV9921/22/23.

Coil capacitance of inductors is typically provided in the manufacturer's data books either directly or in terms of the self-resonant frequency (SRF).

$$SRF = 1/\left(2\pi\sqrt{(L \bullet C_L)}\right)$$

where L is the inductance value, and C_L is the coil capacitance.) Charging and discharging this capacitance every switching cycle causes high-current spikes in the LED string. Therefore, connecting a small capacitor C_O (~10nF) is recommended to bypass these spikes.

Using an ultra-fast rectifier diode for D1 is recommended to achieve high efficiency and reduce the risk of false triggering of the current sense comparator. Using diodes with shorter reverse recovery time, t_{rr}, and lower junction capacitance, C_J, achieves better performance. The reverse voltage rating, V_R, of the diode must be greater than the maximum input voltage of the LED lamp.

The total parasitic capacitance present at the DRAIN pin of the HV9921/22/23 can be calculated as:

$$C_P = C_{DRAIN} + C_{PCB} + C_L + C_J$$

When the switching MOSFET turns on, the capacitance C_P is discharged into the DRAIN pin of the IC. The discharge current is limited to about 150mA typically. However, it may become lower at increased junction temperature. The duration of the leading edge current spike can be estimated as:

$$T_{SPIKE} = \frac{V_{IN} \bullet C_P}{I_{SAT}} + t_{rr}$$

In order to avoid false triggering of the current sense comparator, C_P must be minimized in accordance with the following expression:

$$C_P < \frac{I_{SAT} \bullet (T_{BLANK(MIN)} - t_{rr})}{V_{IN(MAX)}}$$

where $T_{BLANK(MIN)}$ is the minimum blanking time of 200ns, and $V_{IN(MAX)}$ is the maximum instantaneous input voltage.

4.2 Estimating Power Loss

Discharging the parasitic capacitance CP into the DRAIN pin of the HV9921/22/23 is responsible for the bulk of the switching power loss. It can be estimated using the following equation:

$$P_{SWITCH} = \left(\frac{V_{IN}^2 C_P}{2} + V_{IN} \bullet I_{SAT} \bullet t_{rr}\right) \bullet F_S$$

where F_S is the switching frequency, I_{SAT} is the saturated DRAIN current of the HV9921/22/23. The switching loss is the greatest at the maximum input voltage.

The switching frequency is given by the following equation.

$$F_S = \frac{V_{IN} - V_O}{V_{IN} \bullet T_{OFF}}$$

When the HV9921/22/23 LED driver is powered from the full-wave rectified AC input, the switching power loss can be estimated as:

$$P_{SWITCH} \approx \frac{1}{2 \bullet T_{OFF}}(V_{AC} \bullet C_P + 2 \bullet I_{SAT} \bullet t_{rr})(V_{AC} - V_O)$$

V_{AC} is the input AC line voltage.

The switching power loss associated with turn-off transitions of the DRAIN pin can be disregarded. Due to the large amount of parasitic capacitance connected to this switching node, the turn-off transition occurs essentially at zero-voltage.

Conduction power loss in the HV9921/22/23 can be calculated as:

$$P_{COND} = D \bullet I_O^2 \bullet R_{ON} + I_{DD} \bullet V_{IN} \bullet (1 - D)$$

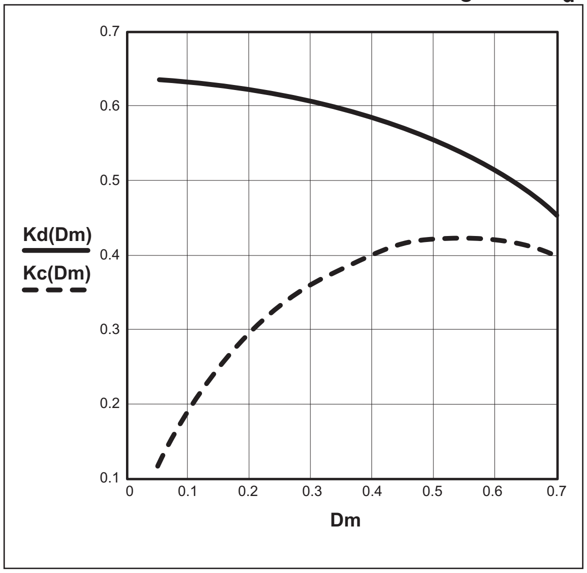
where D = V_O/V_{IN} is the duty ratio, R_{ON} is the on-resistance, I_{DD} is the internal linear regulator current.

When the LED driver is powered from the full-wave rectified AC line input, the exact equation for calculating the conduction loss is more cumbersome. However, it can be estimated using the following equation:

$$P_{COND} = K_C \bullet I_O^2 \bullet R_{ON} + K_d \bullet I_{DD} \bullet V_{AC}$$

where V_{AC} is the input AC line voltage. The coefficients K_C and K_d can be determined from the minimum duty ratio of the HV9921/22/23.

FIGURE 4-1: CONDUCTION LOSS COEFFICIENTS K_C AND K_d



4.3 EMI Filter

As with all off-line converters, selecting an input filter is critical to obtaining good EMI. A switching side capacitor, albeit of small value, is necessary in order to ensure low impedance to the high frequency switching currents of the converter. As a rule of thumb, this capacitor should be approximately 0.1-0.2 µF/W of LED output power. A recommended input filter is shown in Figure 4-2 for the following design example.

4.3.1 DESIGN EXAMPLE

The following example designs a HV9921 LED lamp driver meeting the following specifications:

- **Input:** Universal AC, 85-265VAC
- **Output Current:** 20mA
- **Load:** String of 10 LED (LW541C by OSRAM VF = 4.1V max. each)

4.3.1.1 Step 1. Calculating L1.

The output voltage $V_O = 10 \times V_F \approx 41V$ (max.). Use this equation assuming a 30% peak-to-peak ripple.

$$L1 = \frac{41V \bullet 10.5\mu s}{0.3 \bullet 20mA} = 72mH$$

Select L1 68mH, I = 30mA. Typical SRF = 170KHz. Calculate the coil capacitance.

$$C_L = \frac{1}{L1 \bullet (2\pi \bullet SRF)^2} = \frac{1}{68mH \bullet (2\pi \bullet 170KHz)^2} = 13pF$$

4.3.1.2 Step 2. Selecting D1

Usually, the reverse recovery characteristics of ultra-fast rectifiers at I_F = 20 ~ 50mA are not provided in the manufacturer's data books. The designer may want to experiment with different diodes to achieve the best result.

Select D1 MUR160 with V_R = 600V, $t_{rr} \approx$ 20ns (I_F = 20mA, I_{RR} = 100mA) and $C_J \approx$ 8pF (VF > 50V).

4.3.1.3 Step 3. Calculating total parasitic capacitance

$$C_p = 5pF + 5pF + 13pF + 8pF = 13pF$$

4.3.1.4 Step 4. Calculating the leading edge spike duration

$$T_{SPIKE} = \frac{264V \bullet \sqrt{2} \bullet 31pF}{100mA} + 20ns \approx 136ns < T_{BLANK(MIN)}$$

4.3.1.5 Step 5. Estimating power dissipation in HV9921 at 265VAC

Switching power loss:

$$P_{SWITCH} \approx \frac{1}{2 \bullet 10.5\mu s}(264V \bullet 31pF + 2 \bullet 100mA \bullet 20ns) \bullet (264V - 41V) \approx 131mW$$

Minimum duty ratio:

$$D_M = \frac{41V}{265V \bullet \sqrt{2}} \approx 0.11$$

Conduction power loss:

$$P_{COND} = 0.25 \bullet (20mA)^2 \bullet 210\Omega + 0.63 \bullet 200\mu A \bullet 264V \approx 55mW$$

Total power dissipation in HV9921:

$$P_{TOTAL} = 131mW + 55mW = 186mW$$

4.3.1.6 Step 6. Selecting input capacitor C_{IN}

$$OutputPower = 41V \bullet 20mA = 820mW$$

Select C_{IN} ECQ-E4104KF by Panasonic® (0.1µF, 400V, Metalized Polyester Film).

FIGURE 4-2: UNIVERSAL 85-264VAC LED LAMP DRIVER

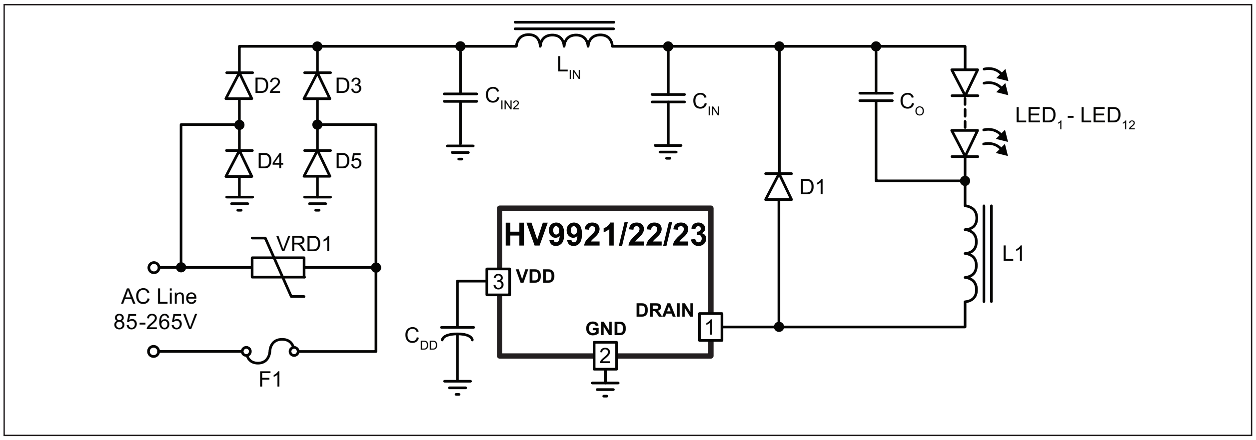


FIGURE 4-3: TYPICAL EFFICIENCY

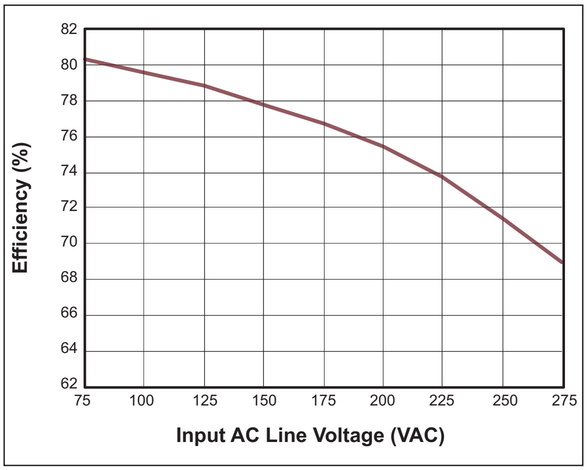


FIGURE 4-4: SWITCH-OFF TRANSITION Ch1:V_{DRAIN}, Ch3: I_{DRAIN}

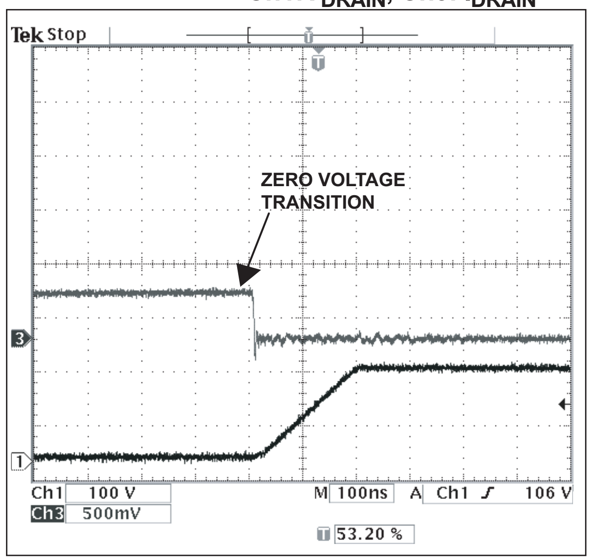


FIGURE 4-5: TYPICAL EFFICIENCY

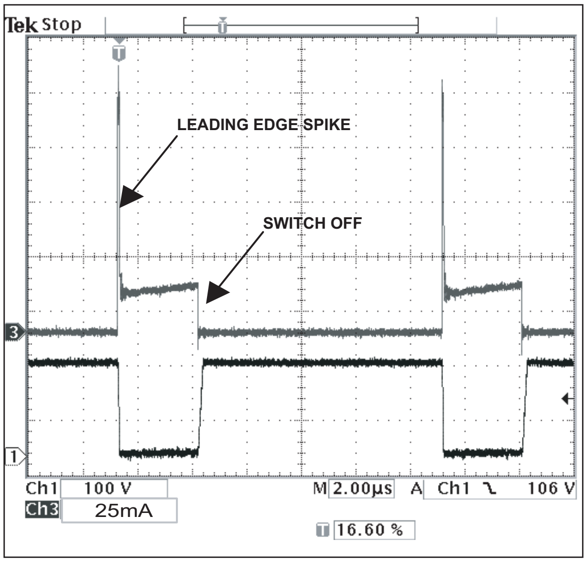


FIGURE 4-6: SWITCH-OFF TRANSITION Ch1:V_{DRAIN}, Ch3: I_{DRAIN}

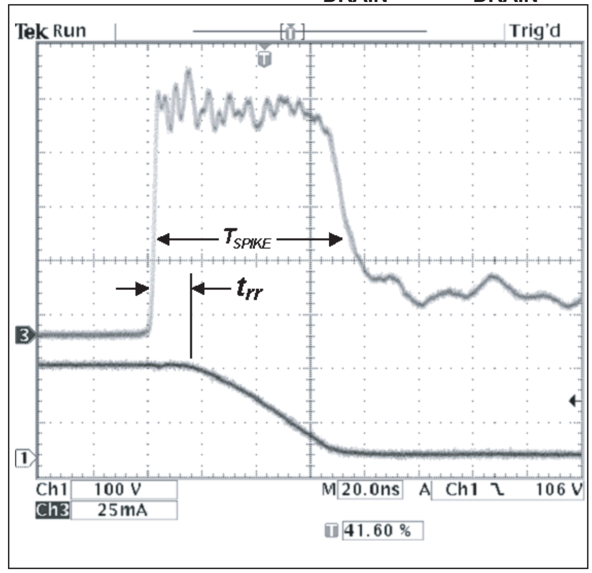
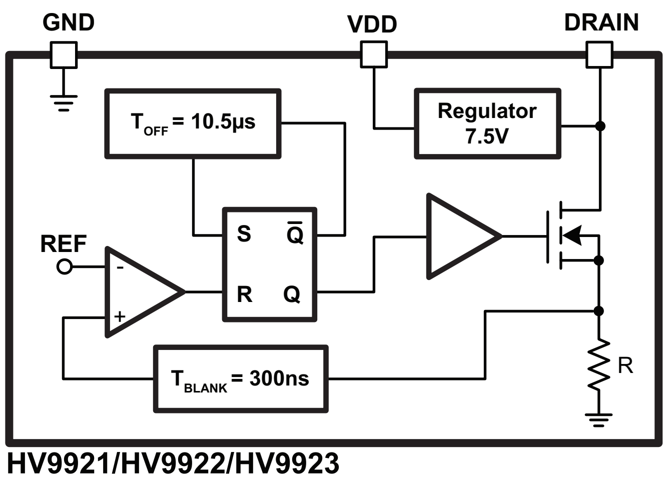


FIGURE 4-7: FUNCTIONAL BLOCK DIAGRAM



5.0 LAYOUT CONSIDERATIONS

For a recommended circuit board layout for the HV9921/22/23, see Figure 5-1.

5.1 Single Point Grounding

Use a single point ground connection from the input filter capacitor to the area of copper connected to the GND pin.

5.2 Bypass Capacitor (C_{DD})

The V_{DD} pin bypass capacitor C_{DD} should be located as near as possible to the V_{DD} and GND pins.

5.3 Switching Loop Areas

The area of the switching loop connecting the input filter capacitor C_{IN}, the diode D1 and the HV9921/22/23 together should be kept as small as possible.

The switching loop area connecting the output filter capacitor C_O, the inductor L1 and the diode D1 together should be kept as small as possible.

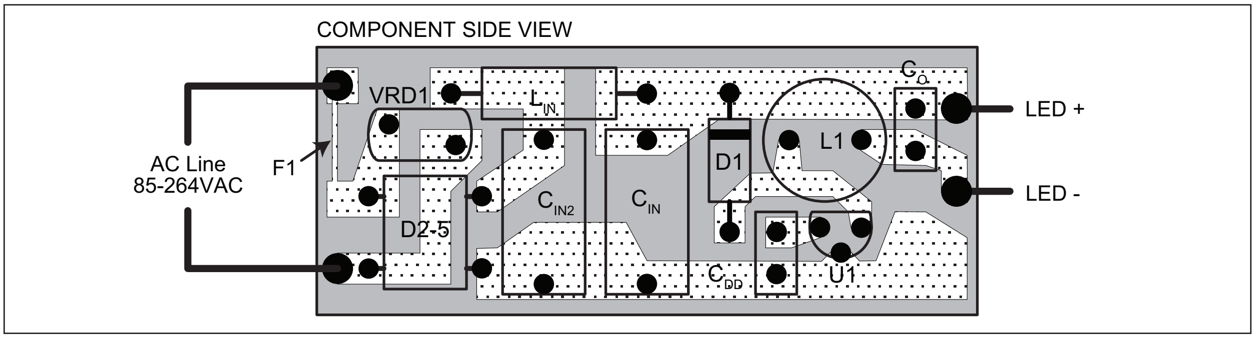
5.4 Thermal Considerations vs. Radiated EMI

The copper area where GND pin is connected acts not only as a single point ground, but also as a heat sink. This area should be maximized for good heat sinking, especially when the SOT-89 package is used. The same applies to the cathode of the free-wheeling diode D1. Both nodes are quiet; therefore, they will not cause radiated RF emission. The switching node copper area connected to the DRAIN pin of the HV9921/22/23, the anode of D1 and the inductor L1 needs to be minimized. A large switching node area can increase high frequency radiated EMI.

5.5 Input Filter Layout Considerations

The input circuits of the EMI filter must not be placed in the direct proximity to the inductor L1 in order to avoid magnetic coupling of its leakage fields. This consideration is especially important when unshielded construction of L1 is used. When an axial input EMI filter inductor L_{IN} is selected, it must be positioned orthogonal with respect to L1. The loop area formed by C_{IN2}, L_{IN} and C_{IN} should be minimized. The input lead wires must be twisted together.

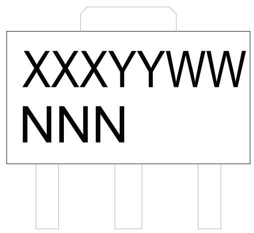
FIGURE 5-1: RECOMMENDED CIRCUIT BOARD LAYOUT WITH HV9921/22/23



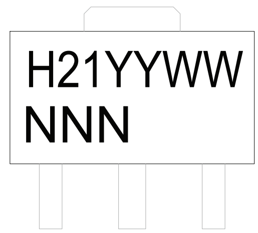
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

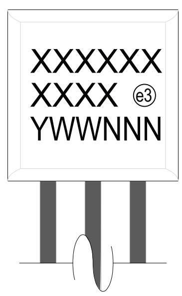
3-lead TO-243AA*
(SOT-89)



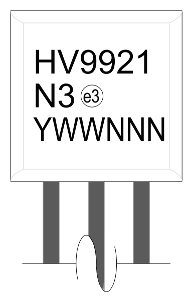
Example



3-lead TO-92

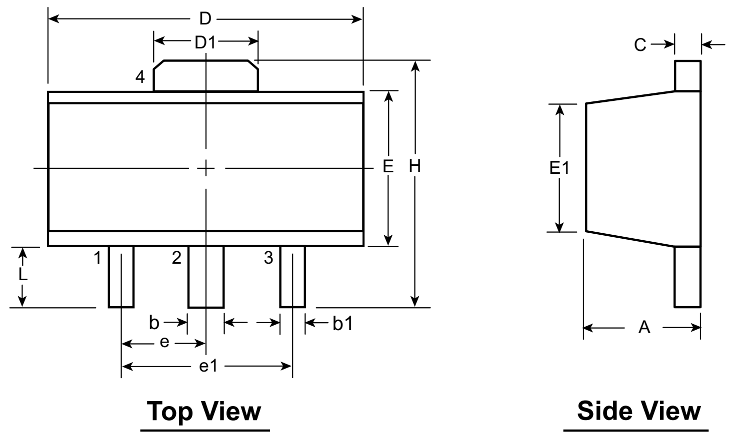


Example



Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.
Note:		In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or may not include the corporate logo.

3-Lead TO-243AA (SOT-89) Package Outline (N8)

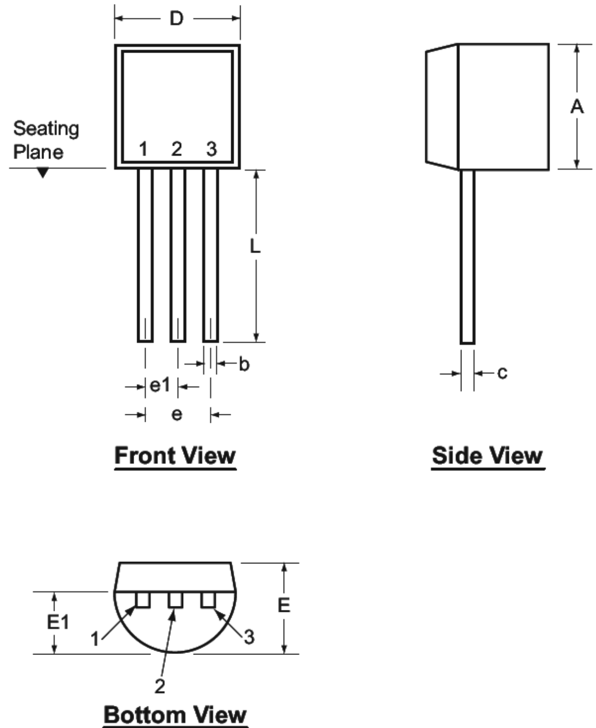


Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00†	1.50 BSC	3.00 BSC	3.94	0.73†
	NOM	-	-	-	-	-	-	-	-			-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.
***†** This dimension differs from the JEDEC drawing*
***Drawings not to scale**.*

3-Lead TO-92 Package Outline (L/LL/N3)



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (October 2014)

- Original Release of this Document.

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PART NO. **XX** - **X** - **X**

Device | **Package Options** | **Environmental** | **Reel**

Device:	HV9921 =	3-Pin Switch-Mode LED Lamp Driver IC, 20 mA output current
	HV9922 =	3-Pin Switch-Mode LED Lamp Driver IC, 50 mA output current
	HV9923 =	3-Pin Switch-Mode LED Lamp Driver IC, 30 mA output current
Package:	N3 =	TO-92
	N8 =	TO-243AA (SOT-89)
Environmental	G =	Lead (Pb)-free/ROHS-compliant package
Reel:	(nothing) =	1000/bag for N3 package, 2000/reel for N8 package

Examples:

a) HV9921N3-G: 20 mA output current, TO-92 package, 1000/bag

b) HV9923N8-G: 30 mA output current, TO-243AA(SOT-89) package, 2000/reel

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