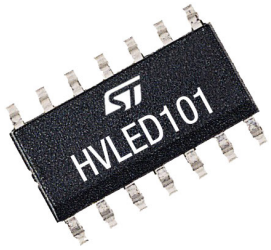
HVLED101

Datasheet

Advanced high power factor flyback controller with valley locking and maximum power control



Product status link
HVLED101

Product summary		
Order code	**Package**	**Packaging**
HVLED101	SOP14	Tube
HVLED101TR		Tape and reel

Features

- Quasi-Resonant (QR) topology
- Primary side regulation of output voltage
- Direct optocoupler connection for secondary side regulated loop
- High power factor and low THD in universal and extended range (PF> 0.9 and THD < 5% @ full load and < 10% @ 1/3 load)
- 800 V fast high-voltage startup
- Extremely low input power at no-load and standby conditions
- Integrated input voltage detection for high power factor capabilty, DC rail detection and protection triggering
- Programmable frequency foldback with valley locking for noise free operation
- Programmable maximum input power limitation for safety standard compliancy
- Programmable brownout and input overvoltage protection
- Latch-free device guarantee by smart Auto Restart Timer (ART)
- Input pin for remote protection with NTC management (threshold hysteresis and linearization)

Application

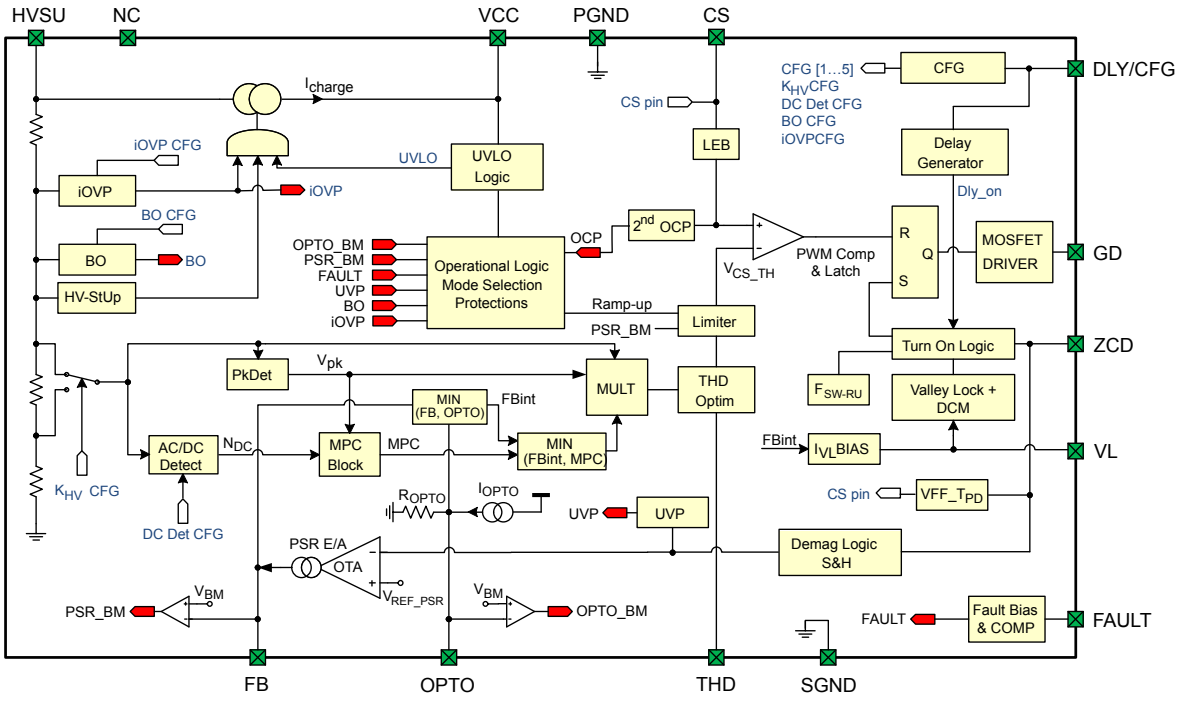
- Single-stage LED drivers with high power factor up to 180 W
- Two-stage LED drivers up to 200 W

Description

The HVLED101 is an enhanced peak current mode controller able to control mainly high power factor (HPF) flyback or buck-boost topologies having an output power up to 180 W. Some other topologies, like buck, boost and SEPIC could also be implemented. Primary Side Regulation of output voltage and Optocoupler control can be applied independently on the chip both exploiting precise regulation and very low standby power during no-load conditions. The innovative ST high-voltage technology allows to directly connect the HVLED101 to the input voltage in order to both start up the device and monitor the input voltage without the need of external components. Integrated valley locking feature guarantees noise free operation during medium and low load operation and maximum power control allows limiting the input power to a level programmable by the user to increase converter safety. Abnormal conditions like open circuit, output short-circuit, input overvoltage or undervoltage, external protection circuitries and circuit failures like open loop and overcurrent of the main switch are effectively controlled. A smart Auto Restart Timer (ART) function is built in to guarantee an automatic application recover, without any loss of reliability.

1 Block diagram

Figure 1. **Block diagram**



2 Typical applications

Figure 2. **HVLED101 typical PSR application**

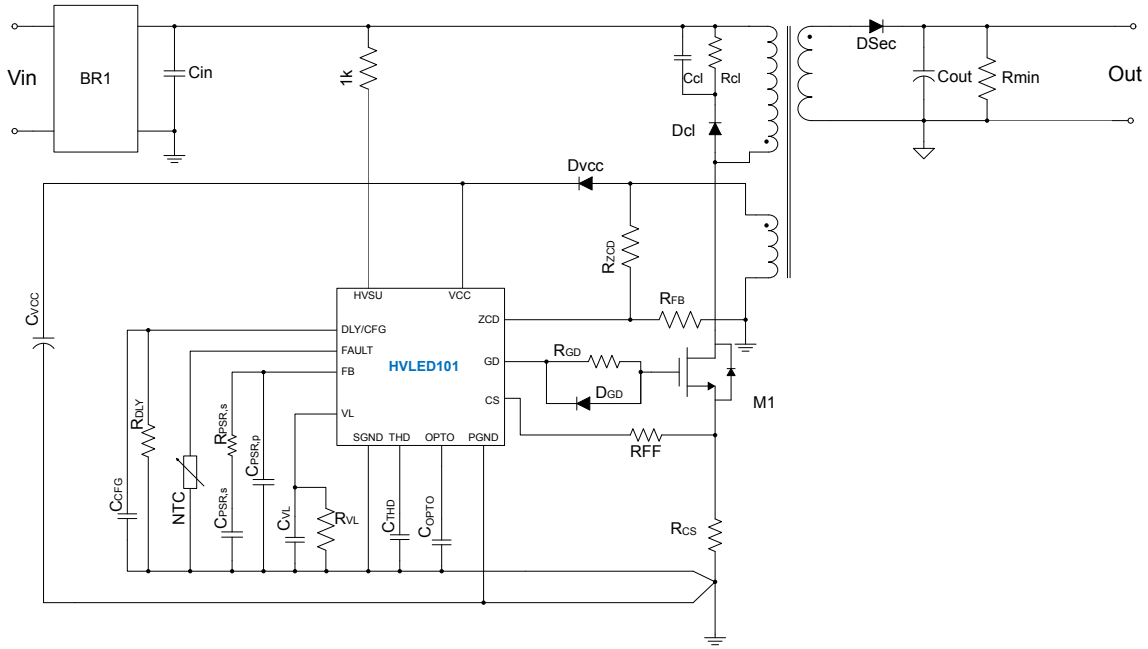
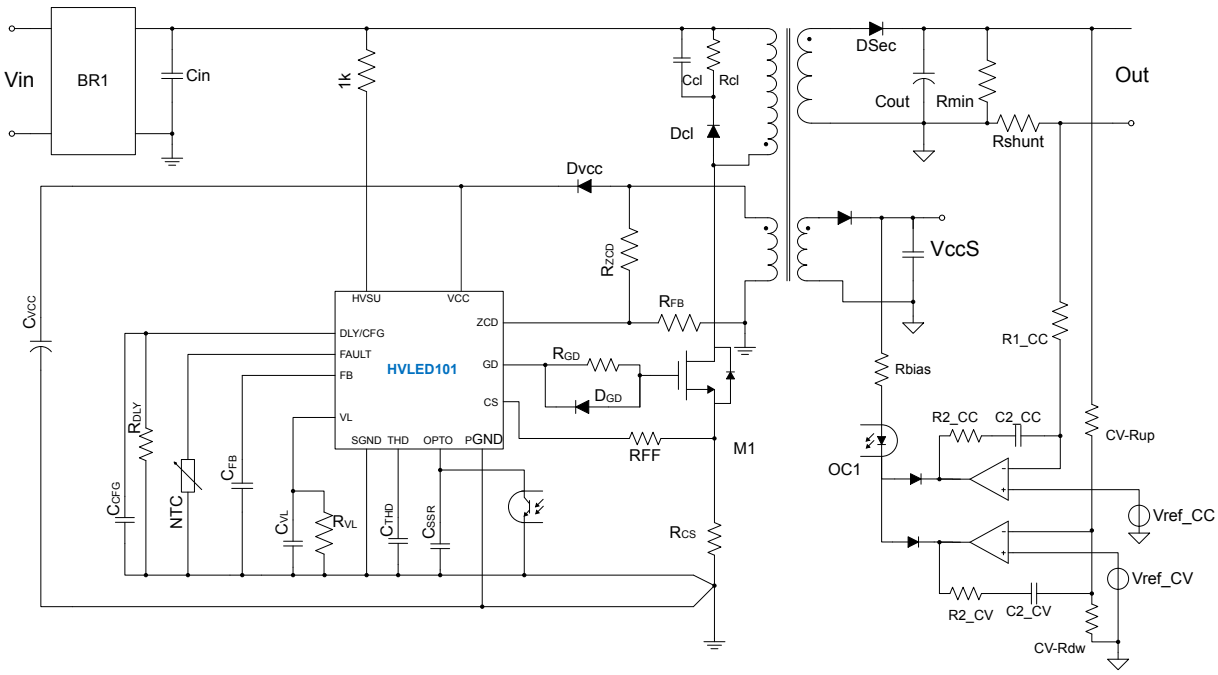


Figure 3. **HVLED101 typical SSR application**



3 Pin Settings

Figure 4. **Device pinout**

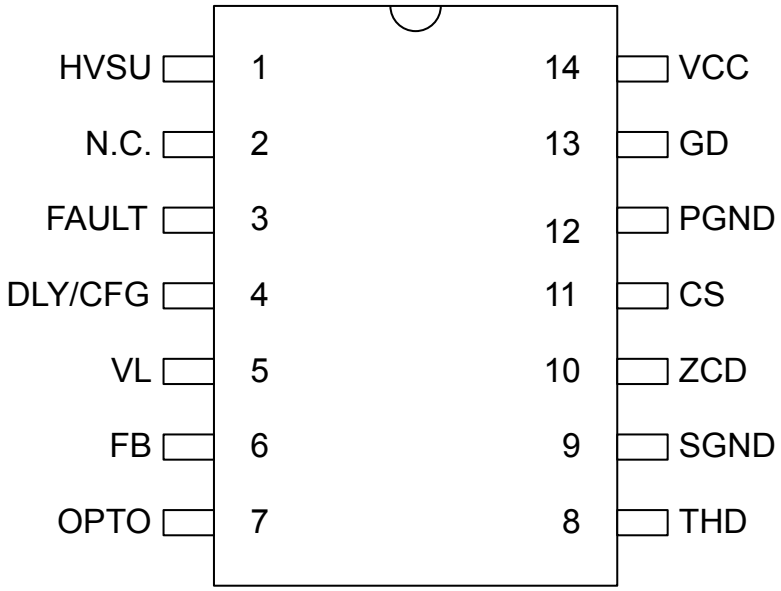


Table 1. **Pin description**

Symbol	Pin	Description
HVSU	1	High-voltage startup and input voltage detection. The pin, able to withstand 800 V, is to be connected to either the DC side of the input rectifier bridge, using a low value resistor (1 kΩ typ), or the AC side of a rectifier bridge with two diodes. It embeds the internal startup unit that quickly charges the capacitor connected between VCC pin and PGND pin during startup and low consumption. During operational mode, this pin measures the input voltage to obtain high power factor and to detect both input overvoltage and undervoltage, according to protection configuration, selected on the DLY/CFG pin.
N.C.	2	Not connected pin for clearance.
FAULT	3	This pin is intended to stop the IC when either the voltage goes below an internal threshold or the pin is left floating. It is suitable to supply an NTC thermistor. The hysteresis of lower disable threshold results in a thermal hysteresis when NTC is connected. When the functionality is unused, connect a 33 kΩ resistor between FAULT pin and SGND.
DLY/CFG	4	The parallel of a resistor and a capacitor is connected between this pin and SGND pin: the value of the resistance sets the delay time between ZCD detection and MOSFET turn-on, while the time constant of the RC network selects the input detection configuration and protection. Recommended values ranges are 22 ÷ 560 kΩ for R and 10 pF ÷ 100 nF for C.
VL	5	The voltage applied to this pin controls valley locking and frequency fold-back operation. It is internally biased with a current that is proportional to the minimum between the voltages that are present at the FB pin and at the OPTO pin (the internal FB_{int} signal). The level of the frequency fold-back depth is set by a resistor connected to SGND. A capacitor between the VL pin and SGND can be used to filter the fluctuations of FB_{int} signal.
FB	6	Output of the primary side regulation error amplifier (OTA). The pin must be connected to the compensation network for Primary Side Regulation. The voltage present at this pin also controls adaptive burst-mode (deep low consumption mode) and is internally connected to the multiplier, together with OPTO pin voltage and MCP voltage in an “OR-ed” structure.

Symbol	Pin	Description
OPTO	7	This pin is intended to be directly connected to the collector of the optocoupler or to the output of the error amplifier of a non-isolated topology: a pull-up current together with gain resistance is embedded in this pin. The OPTO pin voltage is internally connected to the multiplier, together with FB pin voltage and MCP voltage in an “OR-ed” structure. Deep low consumption mode is invoked pulling this pin lower than the V_{BM} threshold that features as burst-mode level when OPTO is used.
THD	8	A ceramic capacitor is placed between this pin and SGND to set the time constant of the THD optimizer unit. It is strongly recommended to use small package ceramic capacitors, placed as close to the above mentioned pins as possible, to avoid any undesired noise injection.
SGND	9	Reference pin for signal’s ground potential.
ZCD	10	Multiple function pin able to detect the zero current instant, to sense the output voltage for primary side regulation (PSR) and to compensate the peak current detection propagation delay (VFF). The delay time between zero current instant detection and MOSFET turn-on is programmed by the resistance between DLY/CFG pin and SGND. An internal starter unit is active to generate the triggering signal when not externally available (for example, at startup). Valley skipping counter is fed by internal ZCD signal processor. Adaptive minimum turn-off time (for example, the blanking after turn-on), larger during UVP condition, is implemented.
CS	11	Input of the current sense comparator for the power regulation. The current sense resistor (R_{CS}, from primary MOSFET source to ground) must be connected to this pin through a series resistance (RFF): this resistor is fed by an internal current, proportional to ZCD pin current during MOSFET on time interval, that creates the offset to compensate for the PWM comparator propagation delay. A leading-edge blanking time avoids false triggering of the MOSFET’s turn-off due to the noise that may be generated after gate driver turn-on.
PGND	12	Reference pin for VCC and gate driver.
GD	13	Gate driver output. The output stage is suitable to directly drive power MOSFETs. An internal pulldown resistor aims to keep the MOSFET off during low power operating modes.
VCC	14	Supply voltage of the IC. Internal UVLO logic prevents the operation at voltages that are insufficient for an efficient gate driving or internal signal processing. Both a bulk capacitor (typically around 22 µF) and a high frequency filter capacitor (100 nF ceramic, mounted as close to the device as possible) should be connected between this pin and PGND.

4 Electrical data

4.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Pin	Parameter	Test condition	Value	Unit
V_{HVSU_MAX}	HVSU	HVSU maximum voltage	I_{HVSU} < 100 µA, V_{CC} = 15 V	800	V
V_{HVSU_neg}	HVSU	HVSU negative voltage		-0.3	V
V_{CC_MAX}	VCC	IC supply voltage		20	V
V_{GD}	GD	Maximum swing voltage		V_{CC} + 0.3	V
V_{CS}	CS	Current sense applied voltage		7	V
V_{ZCD}	ZCD	Max. ZCD voltage		Self-limited	
I_{ZCD_sink}	ZCD	Max. ZCD pin entering current		1	mA
I_{ZCD_source}	ZCD	Max. ZCD pin exiting current		6	mA
V_{NEG}	CS, FB, OPTO, FAULT, VL, DLY/CFG, THD	Maximum negative voltage		-0.3	V
V_{POS}	FB, OPTO, FAULT, VL, DLY/CFG, THD	Maximum positive voltage		3.6	V
V_{GND_D}	SGND, PGND	Maximum voltage difference between PGND and SGND		+/- 0.3	V

Where not otherwise indicated the AMRs are intended applied when $V_{CC} > V_{CCon}$.
When $V_{CC} < V_{CCon}$, the minimum between the indicated value and V_{CC}+0.3 V must be considered.
Stressing the device above the rating listed in the above table may cause permanent damage to the device. Exposure to absolute maximum rated conditions may affect device reliability.

4.2 ESD immunity levels

Table 3. ESD immunity levels

Mode	Pin	Reference Specification	Value	Unit
HBM	All	According to JS001	±1.75	kV
CDM	All	According to JES002	±500	V

4.3 Thermal data

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{th_JA}	Thermal resistance junction to ambient	120	°C/W
T_J	Junction temperature operating range	-40 to 125	°C
T_{stg}	Storage temperature range	-55 to 150	°C

4.4 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Min.	Max.	Unit	Remarks
V_{CC}	V_{CC} supply voltage	V_{CC-OFF}	19	V	After device turn-on
$V_{HV\_op}\_1$	HVSU voltage range CFG1, CFG3, CFG5	0	480	V	Linearity not guaranteed above 480 V
$V_{HV\_op}\_2$	HVSU voltage range CFG2, CFG4	0	760	V	Linearity not guaranteed if V_{PK} is lower than 200 V
V_{FB}	FB pin regulation voltage range	0.3	2.8	V	
V_{OPTO}	OPTO pin regulation voltage range	V_{BM}	2.8	V	
V_{CS_op}	CS pin operative condition	0	1.2	V	
V_{ZCD}	ZCD pin operative voltage	Self-limited	3.3	V	DC condition, I_{source} < 1 mA R_{ZCD} = 22 kΩ to 47 kΩ
I_{ZCD_src}	ZCD pin operative source current	0	3	mA	During on-time
I_{ZCD_snk}	ZCD pin operative sink current	0	1	mA	During off-time
V_{VL}	VL pin operative voltage	0	3.0	V	
V_{FAULT}	FAULT pin operating range	0	3.3	V	

5 Electrical characteristics

(T_J = -40 °C to 125 °C, 25 °C production tested, V_{CC} = 16 V, SGND = PGND = 0 V, unless otherwise specified.)

Table 6. Electrical characteristics

Symbol	Pin/Block	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage							
V_{CC-ON}	VCC	Turn-on threshold	V_{HVSU} > $V_{HV-START}$ [TrackVCC]	13	14	15	V
V_{CC-OFF}	VCC	Low consumption mode activation	Active mode [TrackVCC]	7.4	7.8	8.2	V
V_{CC-LOW}	VCC	V_{CC} for HVSU high current activation				1.5	V
V_{CC-SHD}	VCC	V_{CC} for IC reset	Low consumption	6.5		7.4	V
Supply current							
$I_{CC-START-UP}$	VCC	Startup current	Startup, V_{CC} = 12 V			270	µA
I_{CC}	VCC	Operating supply current	f_{SW} = 25 kHz, C_{GD} = 1 nF		5.4	6	mA
I_{CC-LC}	VCC	Protection VCC supply current	OCP, brownout, or iOVP			510	µA
$I_{CC-OPTO-BM}$	VCC	OPTO burst-mode VCC current	OPTO = 0 V, FAULT active, DLY/CFG active R_{DLY} = 120 kΩ			610	µA
$I_{CC-PSR-BM}$	VCC	PSR burst-mode VCC current	FB = 0 V, OPTO unbiased, FAULT active, DLY/CFG active R_{DLY} = 120 kΩ			500	µA
High-voltage startup generator							
$V_{HV-START}$	HVSU	Start voltage	I_{Vcc} < 100 µA			20	V
I_{CHG-H}	VCC	V_{CC} charging current	V_{HVSU} > $V_{HV-START}$, startup, V_{CC} = 13 V	5			mA
I_{CHG-L}	VCC	V_{CC} charging current during iOVP or at low V_{CC}	V_{HVSU} > $V_{HV-START}$, iOVP on OR V_{CC} < V_{CC-LOW}	1.2			mA
I_{HV-ON}	HVSU	HVSU on-state current	V_{HVSU} > $V_{HV-START}$, startup, V_{CC} = 13 V	5			mA
I_{BLEED}	HVSU	HVSU discharging current during iOVP	V_{HVSU} > $V_{HV-START}$, iOVP on, CFG1, CFG3, V_{CC} < 18 V	1.55			
I_{HV-LKG}	HVSU	HVSU off-state leakage current	V_{HVSU} = 400 V, active mode		17	25	µA
Input voltage sensing							
V_{iOVP}	HVSU	Input overvoltage protection threshold	CFG1, CFG3, or CFG5	530	555	580	V
V_{BO-L}	HVSU	Brownout threshold (instantaneous voltage)	CFG1, CFG4, or CFG5	94	105	116	V
V_{BO-H}	HVSU		CFG3	170	190	210	V
T_{BO}	HVSU	Brownout activation time	CFG1, CFG3, CFG4, or CFG5	500	835	1180	ms
T_{BO-LEB}	HVSU	Blanking time after brownout activation	CFG1, CFG3, CFG4, or CFG5	150	250	350	ms
T_{DBNC}	HVSU	Brownout debounce time	CFG1, CFG3, CFG4, or CFG5	0.78	1.25	1.72	ms

Symbol	Pin/Block	Parameter	Test condition	Min.	Typ.	Max.	Unit
K_{HV-LV}	HVSU	Internal voltage divider ratio	$V_{HVSU-pk}$ < 480V, CFG1, CFG3 or CFG5		4.65		mV/V
K_{HV-HV}	HVSU		$V_{HVSU-pk}$ > 150V, CFG2, or CFG4		2.91		mV/V
$V_{DC-DET-L}$	HVSU	DC voltage detection level	CFG1, CFG2, CFG4, or CFG5	94	105	116	V
$V_{DC-DET-H}$	HVSU		CFG3	170	190	210	V
T_{DC-DET}	HVSU	DC voltage detection time		30	50	70	ms
Feedback input and multiplier							
V_{OS}	FB, OPTO	FB or OPTO offset voltage	Active mode [TrackFB]	0.45	0.5	0.55	V
K_M	FB, OPTO	Multiplier gain	Active mode		0.176		V/V
K_{MPC}	FB, OPTO	Scaling factor for MPC level calculation			270		V^2
V_{BM}	FB, OPTO	Burst-mode threshold	Active mode, falling [TrackFB]		0.6		V
V_{BM_HYST}	FB, OPTO	Burst-mode hysteresis	Low consumption, rising		50		mV
T_{REP}	FB	PSR burst-mode repetition rate	V_{FB} = 0.6 V		0.4		ms
			V_{FB} = 0.3 V	2.6	4	5.4	ms
R_{THD}	THD	THD optimizer internal resistance	On time running		22		kΩ
PSR OTA							
$V_{REF-PSR}$	FB	PSR loop reference	T_{AMB} = 25 °C	2.55	2.6	2.65	V
			Over all temperature range	2.5	2.6	2.7	V
g_m	OTA	Transconductance	ΔI_{FB} = ±10 µA, V_{FB} = 1.65 V	1.3	2.3	3.2	mS
G_{V-dB}	OTA	Voltage gain	Open loop		75		dB
GBWP	OTA	Gain-bandwidth product			360		kHz
I_{FB-SRC}	FB – OTA	FB pin pull-up current (OTA)	Active mode, VZCD, off = 2.0 V, V_{FB} = 1.65 V		2		mA
I_{FB-SNK}	FB – OTA	FB pin pull-down current (OTA)	Active mode, VZCD, off = 3.2 V, V_{FB} = 1.65 V		2		mA
V_{UVP}	FB	Undervoltage protection level	[TRACKZCD]	0.35	0.4	0.45	V
T_{UVP}	FB	Maximum undervoltage protection time		60	100	140	ms
OPTO input							
$V_{OPTO-BIAS}$	OPTO	OPTO biasing voltage	Whole temperature range	2.8			V
$I_{OPTO-BIAS}$	OPTO	OPTO biasing current	V_{OPTO} = 0 V	120	150	180	µA
R_{OPTO}	OPTO	Internal parallel resistor		40	52	65	kΩ

Symbol	Pin/Block	Parameter	Test condition	Min.	Typ.	Max.	Unit
$T_{OPTO-TRIG}$	OPTO	Minimum pulse duration to exit from ramp-up phase				10.5	µs
Current sense input							
V_{CS-MIN}	CS	Current sense minimum level during burst-mode	$V_{FB} < V_{BM}$	25	50	80	mV
V_{CS-RU}	CS	Current sense level during ramp-up	During fixed frequency ramp-up phase	170	200	230	mV
T_{LEB}	CS	Leading edge blanking		230	300	390	ns
V_{OCP2}	CS	Saturation protection threshold (2nd OCP)	During on-time [TrackCS]	1.2	1.3	1.4	V
V_{OCP1}	CS	Cycle-by-cycle current sense limit (1st OCP)	During on-time [TrackCS]	0.837	0.9	0.963	V
T_{OCP}	CS	Max. stop state duration after 2nd OCP	Tpulse = 1 µs, amplitude 2 V	0.72	1.04	1.41	ms
T_{PD}	CS	Propagation to output of current sense detection	On time running, dV/dt = 0.141 V/us		80		ns
K_{FF}	CS, ZCD	Current gain between ZCD source current and CS pin source current	On time running, I_{ZCD} = 0 to 3 mA		75		µA/mA
ZCD input							
$V_{ZCD-TRIG}$	ZCD	ZCD triggering threshold	Negative going edge [TRACKZCD]	0.16	0.2	0.26	V
$V_{ZCD-ARM}$	ZCD	ZCD arming threshold	Positive going edge [TRACKZCD]	0.24	0.3	0.39	V
T_{BLANK}	ZCD	ZCD minimum blanking time	From MOSFET turn-off, with PSR S&H > V_{UVP}	0.97	1.5	2.1	µs
			From MOSFET turn-off, with PSR S&H < V_{UVP}	3.3	5.5	7.7	µs
$T_{DLY-MIN}$	DLY/CFG	ZCD trigger to GD on min. delay	R_{DLY} = 120 kΩ		355		ns
$T_{DLY-MAX}$	DLY/CFG	ZCD trigger to GD on max. delay	R_{DLY} = 270 kΩ		675		ns
$T_{WAIT-MIN}$	ZCD	ZCD waiting time after T_{BLANK} elapse	Starting from ZCD trigger, R_{DLY} = 120 kΩ [track TDLY]		2.2		µs
$T_{WAIT-MAX}$	ZCD		Starting from ZCD trigger, R_{DLY} = 2.7 kΩ [track TDLY]		4.8		µs
$V_{ZCD-CLP-low}$	ZCD	ZCD negative clamping voltage	I_{ZCD} source = 3 mA	-250			mV
$I_{ZCD-Bias}$	ZCD	ZCD pin biasing current	V_{ZCD} = 2.7 V			1	µA
$V_{ZCD-max}$	ZCD	ZCD pin max. positive voltage	I_{ZCD} sink = 1mA	3			V

Symbol	Pin/Block	Parameter	Test condition	Min.	Typ.	Max.	Unit
Timing							
T_{ART}		Auto-restart time		1.5	2.5	3.5	s
F_{SW-RU}		Ramp-up operating frequency		15	25	35	kHz
δ_{MAX-RU}		Max. Duty cycle during ramp-up		40	50	60	%
T_{CF}		Maximum duration of ramp-up phase		120	200	280	ms
FAULT pin characteristics							
$V_{FLT-OFF}$	FAULT	FAULT pin disable threshold	Falling edge [trackFLT]	740	800	860	mV
V_{FLT-ON}	FAULT	FAULT pin enable threshold	Rising edge [trackFLT]	790	850	910	mV
$I_{FLT-BIAS}$	FAULT	FAULT pin biasing current	FAULT = GND	45	50	55	µA
$V_{FLT-OPEN}$	FAULT	FAULT pin open detection voltage	Active mode	2.6	2.7	2.8	V
Gate driver							
V_{GDH}	GD	Output high voltage	I_{GD} source = 5 mA	15.5			V
V_{GDL}	GD	Output low voltage	I_{GD} sink = 5 mA			0.1	V
I_{SRC}	GD	Output source peak current	Max. value [not tested in production]	0.48	0.6		A
I_{SNK}	GD	Output sink peak current	Max. value [not tested in production]	0.83	1.2		A
T_F	GD	Fall time	C_{GD} = 1 nF, from 14.5 V to 1.5 V		15		ns
T_R	GD	Rise time	C_{GD} = 1 nF, from 1.5 V to 14.5 V		30		ns
R_{P-DWN}	GD	Gate driver pull-down resistor			80		kΩ
VL pin characteristics							
$V_{VL-BIAS}$	VL	Saturation voltage	VL = open, V_{FB} = 3V, V_{OPTO} = 2.8V [TrackVL]	2.8			V
$I_{VL-P-UP}$	VL	Pull-up current	V_{VL} = 0 V, V_{FB} = 3 V, V_{OPTO} = 1 V [TrackVL]		10		µA
			V_{VL} = 0 V, V_{FB} = 3 V, V_{OPTO} = 2 V [TrackVL]		20		µA
VL1H	VL	Hysteresis level for VL1			1.9		V
VL1	VL	QR to 2nd valley threshold			1.7		V
VL2H	VL	Hysteresis level for VL2			1.5		V
VL2	VL	2nd to 3rd valley threshold			1.3		V
VL3	VL	3rd to 4th valley threshold			1.2		V
VL4	VL	4th to 5th valley threshold			1.1		V

Symbol	Pin/Block	Parameter	Test condition	Min.	Typ.	Max.	Unit
VL5	VL	5^{th} to 6^{th} valley threshold			1		V
V_{DCM}	VL	Unlocked operation limit			0.86		V
K_{DCM}	VL	DCM characteristic slope			-130		µs / V
$T_{DCM-MAX}$	VL	Max. DCM time with linearity guaranteed	VL = 0.3V		70		µs
DLY/CFG pin characteristics							
$V_{DLY-BIAS}$	DLY/CFG	DLY pin Bias voltage	Active mode [TrackCFG]		1.5		V
K_{DLY}	DLY/CFG	ZCD to GD on gain			2.13		ns/kΩ
V_{CFG-L}	DLY/CFG	Decay hysteresis for CFG selection	[TrackCFG]		0.5		V
Tau_{CFG1}	DLY/CFG	Time constant to set CFG1		30		45	µs
Tau_{CFG2}	DLY/CFG	Time constant to set CFG2		100		140	µs
Tau_{CFG3}	DLY/CFG	Time constant to set CFG3		300		410	µs
Tau_{CFG4}	DLY/CFG	Time constant to set CFG4		860		1200	µs
Tau_{CFG5}	DLY/CFG	Time constant to set CFG5		2050		TBD	µs

6 Application information

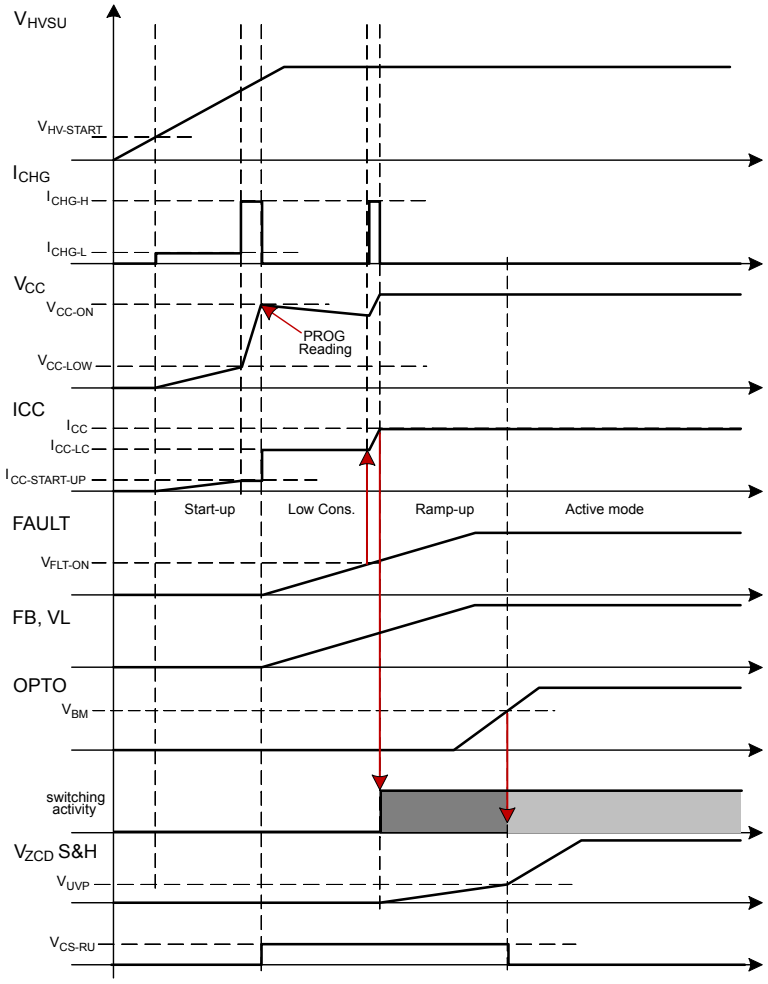
6.1 Typical application

The HVLED101 high power factor flyback controller is suitable to operate either as a single-stage high power factor (HPF) flyback controller or as a DC/DC flyback controller in a two-stage application with front-end PFC converter. The control can be primary side (PSR) or secondary side (SSR). Application schematics of the two control types are reported in Figure 2 and Figure 3.

6.2 Operating modes

The IC presents various operating modes, described in the following sections. Figure 5 shows the operation during initial startup phase.

Figure 5. Initial startup phase



6.2.1 Startup phase

As soon as HVSU pin voltage reaches $V_{HV-START}$, the high-voltage startup unit is turned on to charge the VCC capacitor.

The charging current is limited to I_{CHG-L} until V_{CC} voltage reaches V_{CC-LOW} threshold, and then it is toggled to a higher charging current (I_{CHG-H}) to minimize the startup time.

Once the V_{CC} reaches V_{CC-ON} threshold, the DLY/CFG pin is read to set the configuration of input voltage protections and input voltage range.

Once the protection set-up is fetched, the following pins are pulled up: FB, VL, FAULT and OPTO.

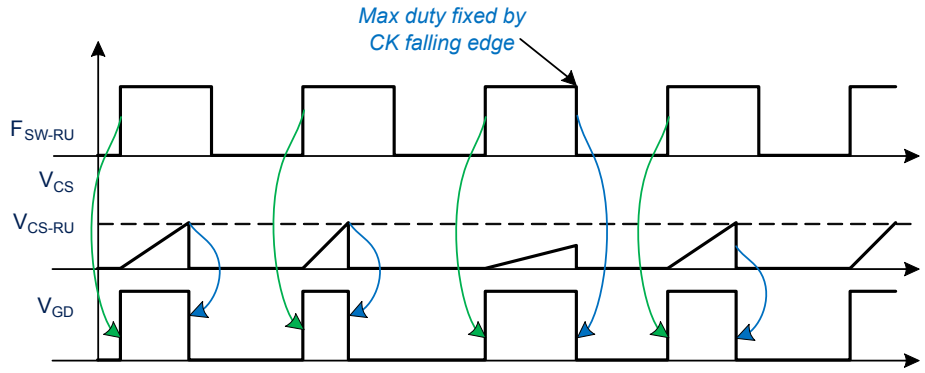
When the voltage on the FAULT pin is higher than V_{FLT-ON} threshold, the HVSU recharges the VCC capacitor and the switching activity starts. The first switching cycles activate the next operating phase: the ramp-up phase.

6.2.2 Ramp-up phase

This operating mode is intended to ensure a safe increase of the output voltage. This goal is achieved transferring an almost constant power to the output by fixing the minimum current sense threshold at V_{CS-RU} and driving the external power MOSFET at constant operating frequency F_{SW-RU}, with the maximum duty cycle fixed at 50%.

The THD optimizer unit is forced to operate with a duty cycle equal to 1 (see relevant section for further details).

Figure 6. Ramp-up waveforms



When both output voltages (read by ZCD sample and hold block) are higher than V_{UVP} threshold and OPTO pin is pulled up for at least $T_{OPTO-TRIG}$, the IC enters active mode.

If the ramp-up exit condition is not satisfied within T_{CF}, the IC shuts down, and automatic restart is attempted after T_{ART}.

During this phase the internal PSR error amplifier is always on as well as the FAULT pin pull-up current.

6.2.3 Active mode

During active mode, the IC provides the GD signal to drive the external power switch according to application signals.

All the parameters are set at their operating range performance and protections are ready to manage undesired events.

The power consumption of the IC in this phase depends on the switching frequency and the characteristics of the adopted switch.

The OPTO disable feature activates a deep low consumption mode, while the FAULT disable mean activates a standard low consumption mode.

The input OVP is active (in CFG 1, 3 and 5) as well as the brownout and output undervoltage protections.

6.2.4 Low consumption mode

In this state, the IC stops switching activity and turns off the major part of internal structures in order to reduce VCC consumption down to I_{CC-LC}.

In this operating mode, the high-voltage startup logic is active to maintain the VCC pin above V_{CC-OFF} (low level) if necessary.

This state is invoked when the following conditions are met:

- overcurrent protection.
- FAULT pin protection.
- the inactive phase of brownout level protection is running.
- input overvoltage protection senses an excessive input voltage at pin HVSU.

6.2.5 Deep low consumption mode

This state is intended to reduce the IC consumption to the minimum level in order to reduce the input power consumption during burst-mode condition (FB or OPTO driven).

When the deep low consumption mode condition is removed, the system evolves to the relevant next state without turning on the high-voltage startup unit.

6.2.6 Auto-restart time and check state

These are auxiliary states. Auto-restart time is intended to maintain the device supplied for a time equal to T_{ART} until a new restart procedure is automatically generated.

If V_{CC} drops below V_{CC-OFF}, the timers are frozen, while if V_{CC} drops below V_{CC-SHD} the internal logic of the device is reset and all automatic procedures are also interrupted.

The check state is a logic state that is invoked after V_{CC-ON} trigger to check the status of all protections and take the proper actions according to protection logic.

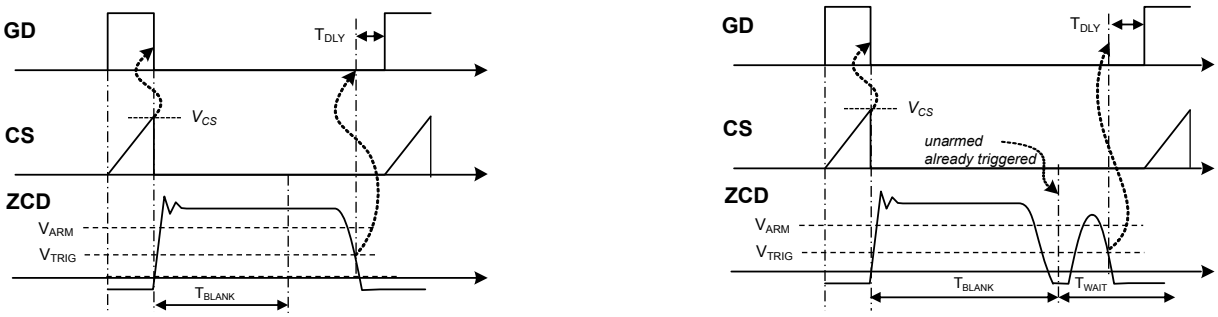
6.3 Control loop

The HVLED101 IC is optimized to operate as high power factor peak current mode quasi-resonant (QR) flyback (Figure 7). In order to realize this operating scheme, it embeds a multiplier that creates the threshold for the PWM comparator that turns off the main switch when the current measured across a shunt resistor, placed between the source of said switch and GND, reaches the above-mentioned threshold.

During QR operation, the turn-on command is given by an internal logic that detects the falling edge subsequent to the transformer demagnetization and applies the delay time programmed by the resistance connected to DLY/CFG pin.

A minimum off-time (T_{BLANK}) is provided to ignore the falling edges that could be associated with spurious oscillations of leakage inductance.

Figure 7. QR operating scheme



The IC operates in quasi-resonant mode, but one or more resonance valley can be skipped to slow down the operating frequency and improve the system efficiency. The VL pin can be used to adjust the valley skipping levels as described in the relevant paragraph.

During fixed frequency operation, the turn-on command is given by an internal logic.

6.3.1 Multiplier and THD optimization

The HVLED101 is primarily intended to deliver power to a load from an AC line. A multiplier is needed to shape the current sense threshold and obtain the desired power factor correction.

The proprietary THD optimizer embedded into HVLED101 minimizes the distortion of the absorbed AC current (THD) and maximizes the Power Factor (PF), independently from the particular set-up of the transformer (turn ratio and primary inductance).

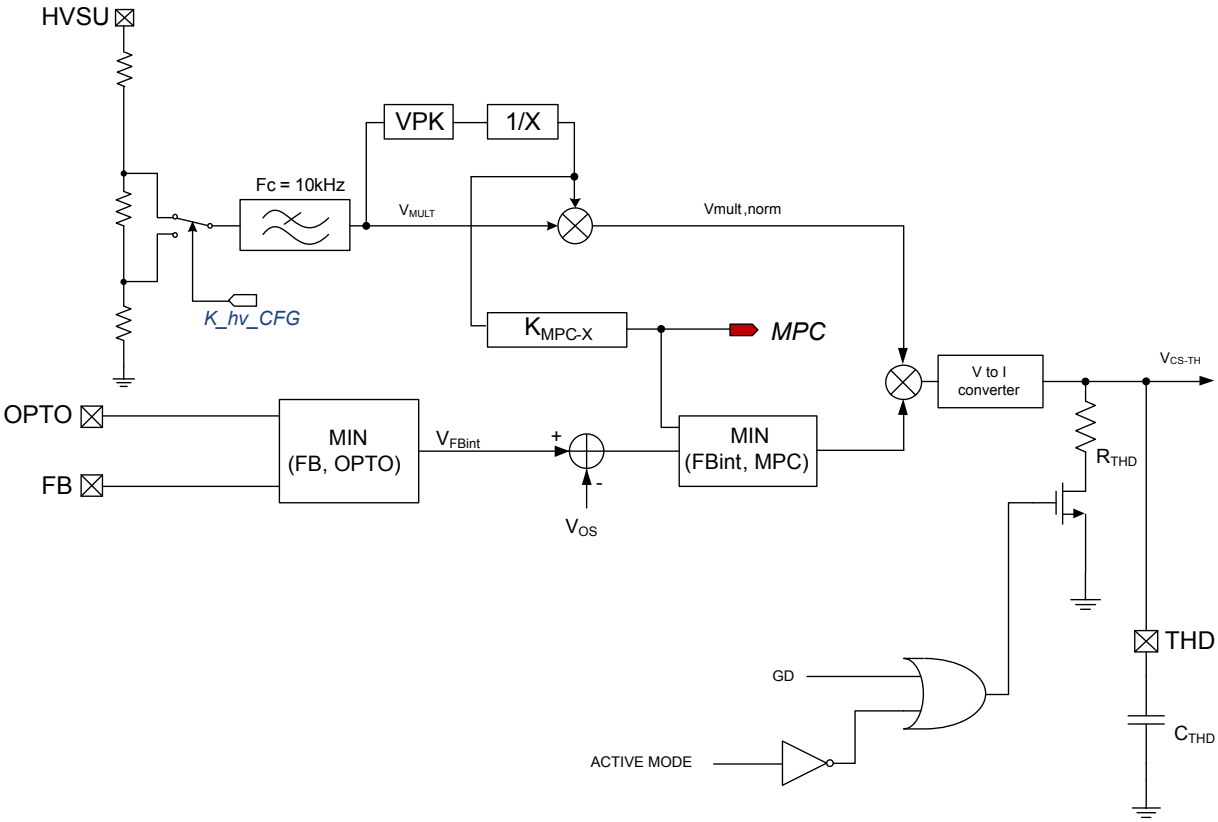
The THD optimization unit is placed between the multiplier output and the current sense threshold limiter and is active during active mode only.

The IC performance is optimized for the use of a transformer that has a reflected voltage (Vout times turn ratio) into a range between 100 V and 250 V.

The current sense threshold is given by the following relationship:

$$V_{CS} = \frac{V_{HVSU}}{V_{HVSU\_pk}} \cdot \frac{K_M}{\delta_{THD}(\theta)} \cdot (V_{FBint} - V_{OS})$$

Figure 8. Multiplier and THD optimizer block diagram



Where K_M is the DC gain of the THD optimizer and $\delta_{THD}(\theta)$ is the duty cycle of the internal optimizer MOSFET.

An external Capacitor, C_{THD}, connected between THD pin and GND is used to filter the switching frequency from V_{CS} threshold. The value of such capacitor must be selected in order to obtain:

$$\tau_{THD} = R_{THD} \cdot C_{THD} = \left(3to5\right) \cdot \frac{1}{F_{SW\_min}}$$

The internal THD switch is normally switched together with GD: if valley skipping operation is running, the THD pin is put in high impedance on in correspondence with the 6th valid falling edge of ZCD signal.

The THD MOSFET activity is described in Table 7.

The minimum value of V_{CS} is set to $V_{CS\text{-}RU}$ during startup or $V_{CS\text{-}MIN}$ when PSR burst-mode is activated, while it is zero during normal operation.

The peak detector of the input voltage divider is intended to operate when the peak amplitude (or DC value) of the input voltage is between 105 V and 480 V (CFG1, CFG2 or CFG5) or between 175 V and 760 V (CFG3 or CFG4).

Table 7. **THD gate activity vs. operating modes**

Operating mode	THD gate activity
Active mode (QR up to 6th valley)	GD_{THD} same as GD activity
Active mode (from 6th valley DCM mode)	GD_{THD} off (THD pin = HiZ)
Ramp-up time	GD_{THD} always on
Burst mode inactive phase (both PSR or OPTO)	GD_{THD} always on
OCP protection period	GD_{THD} always on
iOVP protection period	GD_{THD} always off (THD pin = HiZ)
Brownout protection	GD_{THD} always off (THD pin = HiZ)
Fault protection	GD_{THD} always off (THD pin = HiZ)
Auto restart time (after UVP)	GD_{THD} always off (THD pin = HiZ)

6.3.2 Maximum power control

The THD optimizer block lets the average value of the OPTO or FB value to be proportional to input power and input voltage.

An internal MPC block generates a value that is derived from input voltage and that is connected in OR logic with OPTO and FB.

Such a method allows the topology to absorb from the input source a maximum power that is independent from input voltage and input shape.

At overloading occurrence, the IC does not take any action, but simply limits the delivered power to MPC level.

The value of current sense resistor RCS is defined by this MPC block.

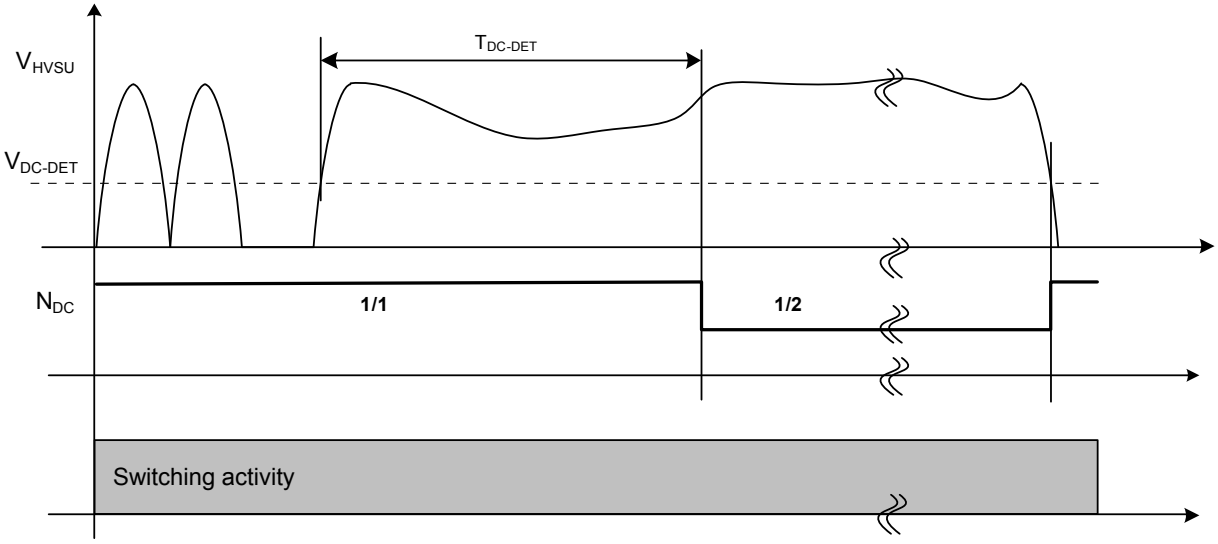
$$R_{CS} = \frac{K_M \cdot K_{MPC}}{4 \cdot N_{DC} \cdot P_{IN\_AVG}}$$

MPC block automatically detects if input voltage is AC or DC: if the input voltage does not drop below $V_{DC\text{-}DET}$ for a time longer than $T_{DC\text{-}DET}$, then it is assumed that a DC voltage is connected and MPC level is adjusted accordingly, putting N_{DC} = ½.

The AC mode is recovered (N_{DC} = 1) at first crossing of said level.

Note that the internal peak detector is always active and triggers the maximum of any fluctuation superimposed to HVSU voltage. If said voltage is a pure DC, the peak detector stores the input voltage itself.

Figure 9. **DC detection waveforms**



6.3.3 Current sense input

The power switch current is read across a shunt resistor placed between the source of the switch and ground.

Said voltage is compared with the value generated by the THD optimizer.

The leading edge blanking (LEB) unit prevents the turn-on spikes from reaching the PWM comparator and avoids false triggering.

When the primary side regulation (PSR) loop serves very light loads, the demagnetization time is very short, and the PSR sampling unit could underestimate the output voltage and could react increasing the real voltage. In order to guarantee a correct sampling of V_{OUT}, a minimum current sense level is activated when PSR burst-mode is active.

The propagation delay of the peak current detection to GD off (T_{PD} + external T_{PROP}) results in a turn-off current that is higher than expected. Said error is proportional to input voltage.

The HVLED101 embeds a propagation delay compensation logic that injects a portion of the current sourced by ZCD pin during on-time into the CS pin. Said current multiplied by the resistance that is placed between CS pin and the shunt resistor develops a voltage offset that compensates the above mentioned error.

$$V_{cs\,.\,OS} = \frac{R_{FF}}{R_{ZCD}} \cdot K_{FF} \cdot \frac{Naux}{Npri} \cdot V_{IN} = \frac{R_{CS} \cdot (T_{PD} + T_{PROP})}{L_P} \cdot V_{IN}$$

Since R_{ZCD} must be fixed at first to have proper biasing of ZCD pin, then R_{FF} can be used to adjust the propagation delay compensation.

6.3.4 Feedback inputs

6.3.4.1 *OPTO*

The OPTO pin is intended to bias and manage the signal coming from the phototransistor collector of a standard optocoupler operating as pull-down current generator.

An internal degeneration resistor facilitates the loop compensation equalizing the ideal current source that bias the pin.

When OPTO pin voltage is lower than burst-mode threshold, the IC stops switching and enters deep low consumption mode: this mechanism can be used also as an alternate entry to disable the IC.

6.3.4.2 *FB*

The FB pin is internally connected to the output of the PSR error amplifier: the PSR loop compensation network must be placed between this pin and GND

When FB pin voltage is lower than PSR burst-mode threshold, the IC starts to generate the PSR burst-mode algorithm, described into the relevant paragraph.

The voltage of the FB pin is internally applied to a “MIN selection” structure together with OPTO pin voltage and MCP internal signal (see “Maximum power control” section).

In order to improve PSR performance, FB is put in high impedance state when input voltage is near zero crossing.

6.3.5 Zero Current Detection (ZCD)

The ZCD pin is intended to realize the zero current detection mechanism according to the state diagram of Figure 10.

6.3.5.1 *ZCD state machine description*

When the MOSFET turns off, the HVLED101 applies a minimum blanking time (T_{BLANK}) in order to reject spurious oscillations.

Said blanking time is longer when V_{OUT} is lower than the undervoltage protection level: in fact, huge oscillations are foreseen in case of output short-circuit.

After minimum blanking time, ZCD logic checks the level of ZCD voltage, if it is higher than arming threshold, then it waits indefinitely for the first falling edge on the ZCD pin below the triggering threshold.

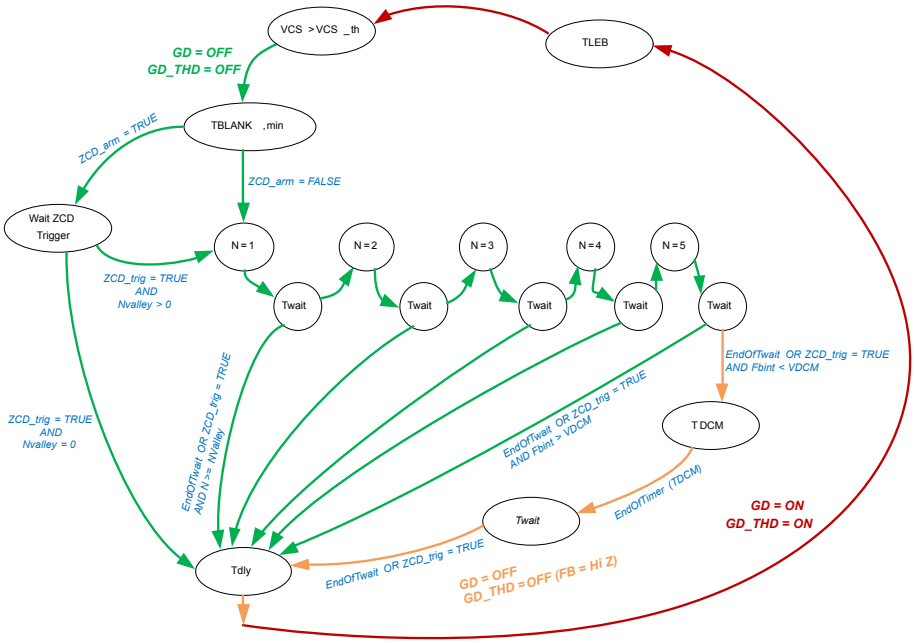
On the contrary, if ZCD level is lower than the arming threshold, a maximum waiting time (T_{WAIT}) is started to prevent latching conditions.

Said waiting time (T_{WAIT}) is proportional to the programmed delay time (T_{DLY}) configured by R_{DLY} resistor on DLY/CFG pin as per the following relationship:

$$T_{WAIT} = 8 \cdot (T_{DLY} - 100ns) + 100ns$$

When the falling edge is detected, the IC can either turn on the MOSFET after the programmed delay time or start counting the number of falling edges (valley) defined by the voltage at VL pin as per valley locking algorithm (see relevant paragraph).

Figure 10. ZCD algorithm diagram



6.3.5.2 *Bottom valley synchronization*

The pin DLY/CFG is used to adjust the delay time that the HVLED101 applies between ZCD trigger signal (falling edge) and MOSFET turn-on.

A delay time can be programmed selecting a proper value of the resistor mounted between DLY/CFG and GND.

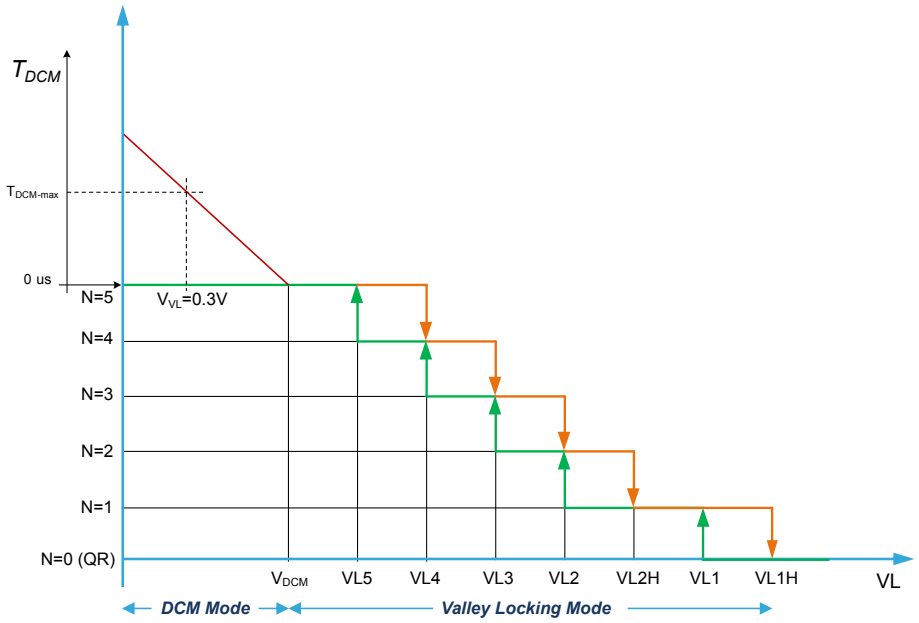
6.3.5.3 *Valley locking and frequency fold-back*

The QR flyback efficiency as well as Power Factor and THD can be improved reducing the operating frequency at light load.

In order to maintain low turn-on losses, the frequency fold-back technique is achieved turning on the MOSFET on the bottom of a resonance valley (valley skip).

In order to avoid random jumping between adjacent valleys (especially at high power), the valley locking scheme is adopted and the number of jumping valleys remains constant until a significant modification of output power or input voltage presents. As a result, input THD is minimized at intermediate load, audible noise is avoided and output variable is smoothly regulated.

Figure 11. **Valley skipping algorithm**



6.4 Primary side regulation feature

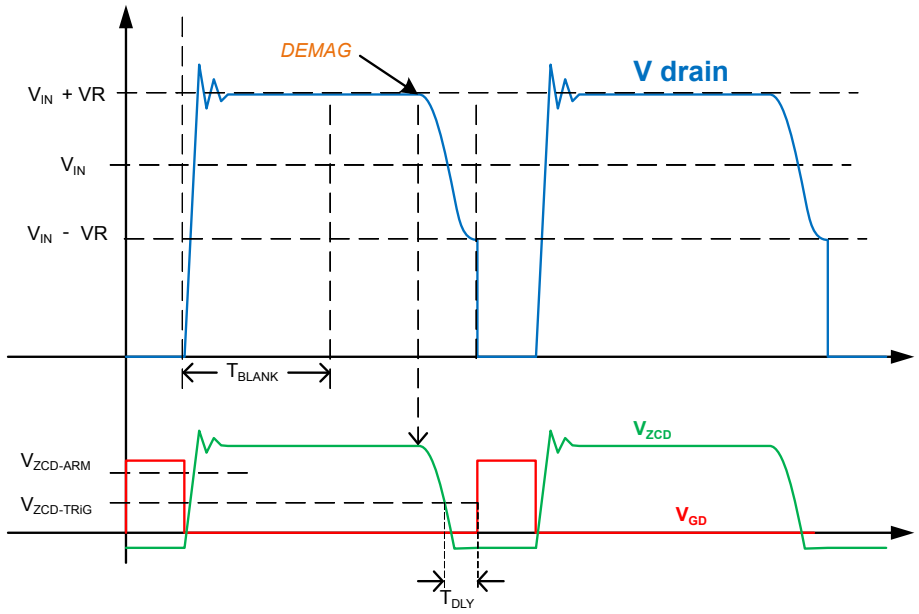
The HVLED101 can regulate the output voltage of a high power factor flyback stage without the need of an error amplifier and relevant optocoupler.

6.4.1 PSR operation

An ST proprietary structure is able to measure the output voltage reading the signal present at the ZCD pin during demagnetization time.

The output voltage measurement is performed in correspondence with the transformer demagnetization instant.

Figure 12. **PSR related signal**



The internal measurement peripheral is active when the switching activity is running and is not frozen by minimum blanking time or frequency fold-back.

When ramp-up mode is running, the PSR unit is functional as well.

The voltage divider connected between the transformer's auxiliary winding and ground sets the output voltage according to the following equation:

$$V_{OUT} = V_{REF.PSR} \cdot \frac{N_{sec}}{N_{aux}} \cdot \left(1 + \frac{R_{ZCD}}{R_{FB}}\right)$$

Near mains zero crossing the converter manages a very low energy amount in each switching cycle. For this reason, ZCD signal amplitude is no longer good information of the output voltage. In order to improve converter performance (THD, PF), in such condition, the FB pin is put in high impedance and is not driven by internal OTA. External compensation network capacitors keep the pin voltage almost constant. The zero crossing condition is detected when the input voltage level goes below a threshold (≈ 70 V).

6.4.2 PSR burst-mode operation

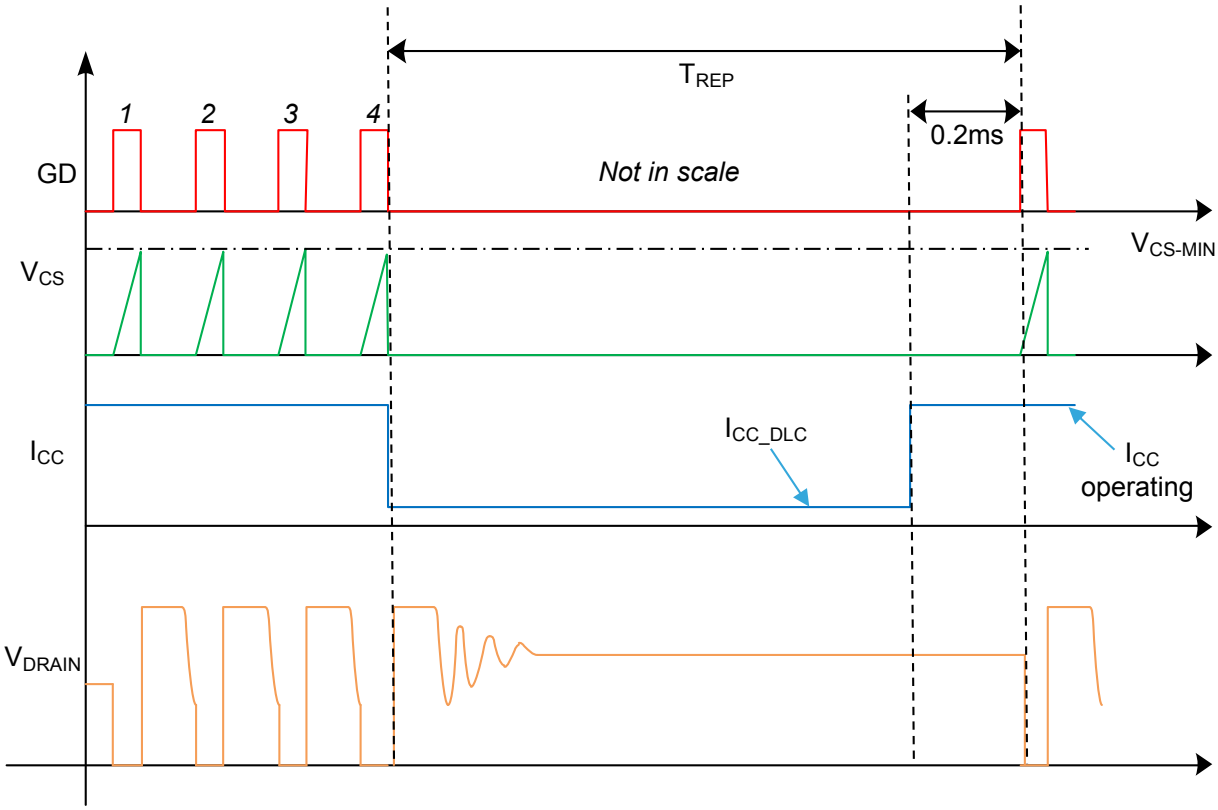
When the output power becomes very small and frequency fold-back is no longer able to reduce the delivered power, the flyback converter must enter burst-mode operation to maintain the output variable regulation.

When the application is regulated by an optocoupler, the secondary side error amplifier sets the repetition rate between active and inactive phase of the burst-mode.

The PSR operation needs to generate some switching activity to refresh the content of the measurement unit.

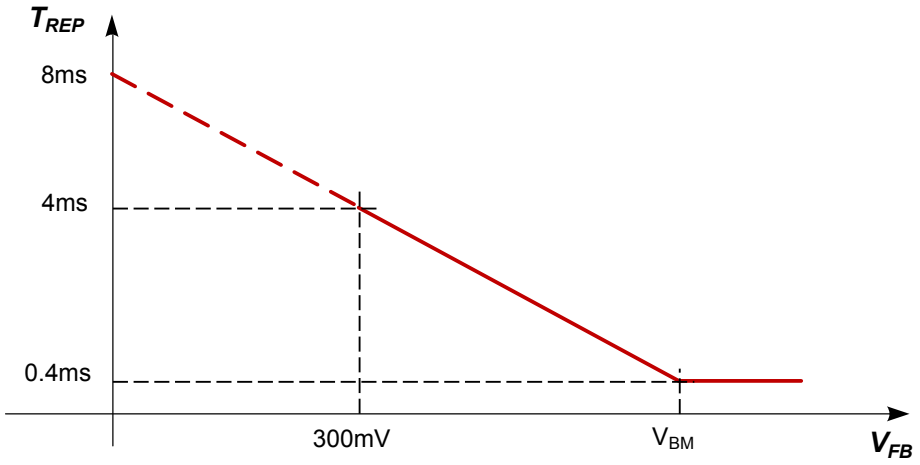
The HVLED101 generates 4 switching cycles following a pure QR scheme (including T_{DLY}) with a repetition time (T_{REP}) that is inversely proportional to the voltage that is present at the FB pin at the end of the 4 switching cycles.

Figure 13. PSR burst-mode waveforms



The following graph represents the relation between FB voltage and T_{REP}.

Figure 14. **PSR burst-mode repetition rate**



During the inactive phase of the burst-mode, the consumption of the HVLED101 is reduced to I_{CC_DLC}.

During the generation of the 4 GD cycles, the current sense threshold is bottom limited to generate a minimum demagnetization time and improve the V_{OUT} measurement's accuracy.

This minimum current sense level represents, in turn, a small minimum power delivered from primary to secondary side: this minimum power delivery has to be dissipated by simple secondary side bleeder resistor (or equivalent structure).

6.5 Gate driver

The gate driver of the HVLED101 is able to drive high and low the gate of an N-channel Silicon MOSFET, with a typical driving strength of 1.2 A/0.6 A (sink/source).

The output of GD pin can reach VCC: care has to be taken to verify that VCC is lower than the absolute maximum rating of the adopted switch.

6.6 IC supply management

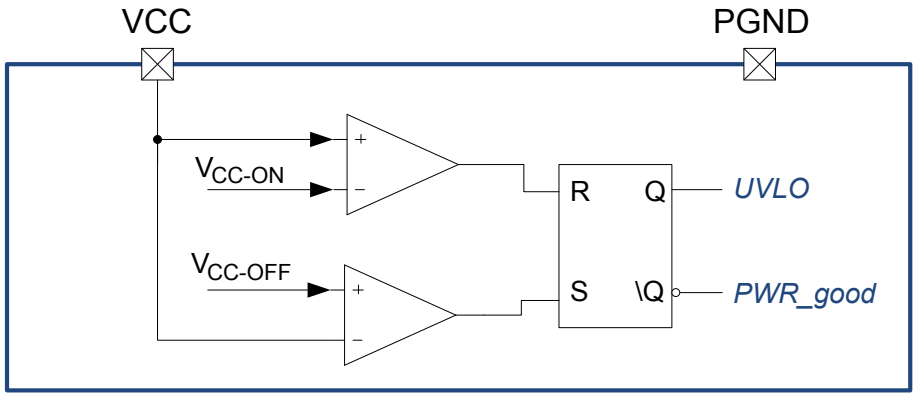
The HVLED101 is supplied applying a DC voltage source between VCC pin and PGND.

This voltage can be easily obtained, during normal operation, by auxiliary winding of flyback transformer, but also other voltage sources can be used.

6.6.1 VCC supply management

The HVLED101 operational scheme is designed to minimize the VCC power consumption, especially during low consumption and deep low consumption modes.

Figure 15. **UVLO and VCC regulation block diagram**



When V_{CC} drops below V_{CC-OFF}, the IC moves to low consumption mode and activates the high-voltage startup to recover a sufficient V_{CC} level (V_{CC-ON}).

6.6.2 High-voltage startup

The high-voltage startup unit is intended to charge the VCC capacitor to a voltage that is at least equal to V_{CC-ON}. This unit is invoked:

- at startup
- during low consumption to maintain the V_{CC} level
- during T_{ART} time to maintain the V_{CC} level
- in case of iOVP to discharge the input capacitor.

Two different charging currents are provided depending on the operating condition as summarized in the table below. The charging current automatically shuts down when V_{CC} reaches approximately 19 V.

Table 8. HVSU activation summary

Operating condition	V_{CC} range	OFF	I_{CHG-H}	I_{CHG-L}
All states if $V_{HVSU} < V_{HV-START}$	Any	X		
Startup (initial phase)	0 V ... V_{CC-LOW}			X
Startup (IC startup)	V_{CC-LOW} ... V_{CC-ON}		X	
Active mode	V_{CC-OFF} ... V_{CC-ON}	X		
Input OVP	V_{CC-OFF} ... V_{CC-AMR}			X
Low consumption mode (LC)	V_{CC-ON} ... V_{CC-OFF} (falling)	X		
VCC recover during LC mode	V_{CC-OFF} ... V_{CC-ON} (rising)		X	
Deep low consumption mode (DLC)	Any	X		

6.7 Parameter selection

Some internal parameters of the device can be programmed selecting the value of the time constant (Tau_{CFGn}) associated with the RC network placed between DLY/CFG and GND.

Once the V_{CC} has risen for the first time above V_{CC-ON}, the DLY/CFG pin is pre-charged up to the $V_{DLY-BIAS}$ and then released.

The DLY/CFG capacitor C_{CFG} is then discharged by R_{DLY} to define a time constant that is internally detected to configure the internal parameters as per the following table.

Table 9. Programming configuration

Tau_{CFGn} (µs)	CFG	iOVP	BrOut	K_{HV}	DC Det.	I_{BLEED} @ iOVP
30 µs ... 45 µs	CFG1	ON	Low	High	Low	ON
100 µs ... 140 µs	CFG2	OFF	OFF	Low	Low	N.A.
300 µs ... 410 µs	CFG3	ON	High	High	High	ON
860 µs ... 1.2 ms	CFG4	OFF	Low	Low	Low	N.A.
> 2.05 ms	CFG5	ON	Low	High	Low	OFF

If the detected time is shorter than 20 µs the IC does not start, while if the time is not detected within an approximate time of 2.05 ms, the IC autonomously proceeds into ramp-up state and sets CFG5. In this phase, the HVSU unit is active to prevent program errors.

The following table summarizes the suggested combination of R_{DLY} and C_{CFG} to obtain both delay time and configuration programming.

Please note that CFG2 has the brownout detection disabled. This is intended to be used mainly for debug purposes because an input voltage lower than 80 V could lead to unpredictable Vout behavior (see PSR operation section).

Table 10. Suggested RDLY-CCFG programming values

T_{DLY} (ns)	R_{DLY} (kΩ) (1%)	C_{DLY} (nF) (5% - >6.3V rated)				
		CFG1	*CFG2*	*CFG3*	*CFG4*	*CFG5*
163.9	30	1.2n	3.9n	12n	33n	82n
183.1	39	1n	2.7n	8.2n	27n	56n
219.3	56	680p	2.2n	6.2n	18n	39n
259.8	75	470p	1.5n	4.7n	12n	33n
355.6	120	270p	1n	2.7n	8.2n	18n
419.5	150	220p	680p	2.2n	6.8n	15n
483.4	180	180p	560p	1.8n	5.6n	12n
568.6	220	150p	470p	1.5n	4.7n	10n
675.1	270	120p	390p	1.2n	3.3n	8.2n
802.9	330	100p	330p	1n	2.7n	6.8n
1101.1	470	82p	220p	680p	2.2n	4.7n
1292.8	560	68p	180p	560p	1.8n	3.9n

The above configurations are intended to be selected in order to fit different application requirements in terms of input voltage. The typical use of the different configurations is shown in the next table.

Table 11. Suggested configuration vs. application input voltage requirements

CFG	Mains voltage range	Typ. Vin range	Note
CFG1	Universal	90 Vac ÷ 305 Vac	
CFG2	Extended	> 80 V ÷ 400 Vac	Only for debug purpose
CFG3	European	180 Vac ÷ 305 Vac	
CFG4	Extended	90 Vac ÷ 400 Vac	
CFG5	Universal	90 Vac ÷ 305 Vac	

6.8 Protections

A comprehensive set of protections is embedded in the HVLED101 in order to facilitate the design of an application with a very high grade of robustness.

6.8.1 Overcurrent protection (2nd OCP)

In case of transformer saturation or secondary side rectifier short-circuit, the primary side current rises quickly to a very high value.

To avoid this current becoming dangerous, a second level OCP protection threshold is provided. It stops the switching activity for a longer duration (T_{OCP}) before recovering the switching activity.

During T_{OCP}, the THD optimizer drives the internal switched resistor always ON (setting δc = 1 in Section 6.3.1).

6.8.2 Input overvoltage protection (iOVP)

The level of this protection is programmed selecting the value of the time constant of the RC network placed between the DLY/CFG pin and GND according to Table 9.

When input voltage surpasses the programmed value, the input overvoltage protection stops the switching activity and activates the discharge current I_{BLEED} (where required).

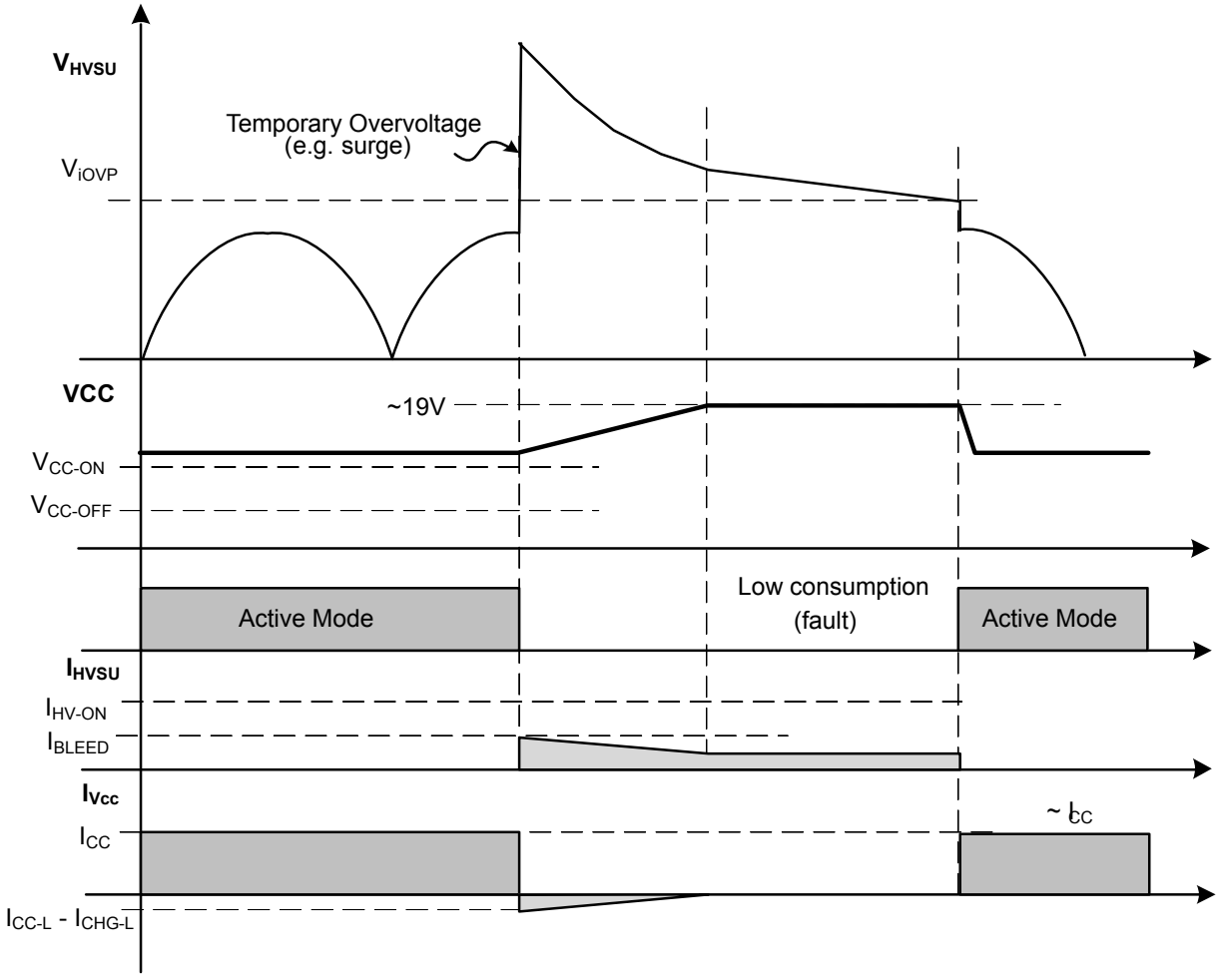
During iOVP, the internal THD optimizer drives the internal switched resistor always OFF (setting δc = 0 in Section 6.3.1) and the THD pin is set in high impedance.

I_{BLEED} current discharges the input capacitor to speed up the recover from surge occurrence.

In case of steady input overvoltage, the VCC pin rises until the I_{BLEED} generator automatically reduces the absorbed current. At this occurrence, the HVSU unit provides the whole current for HVLED101 and the input capacitor is discharged by a current that is almost equal to I_{CC} plus the internal consumption of the HVSU unit.

When HVSU voltage is lower than protection level, the HVSU charges V_{CC} to reach V_{CC-ON} (if required) and active mode is entered.

Figure 16. iOVP waveforms



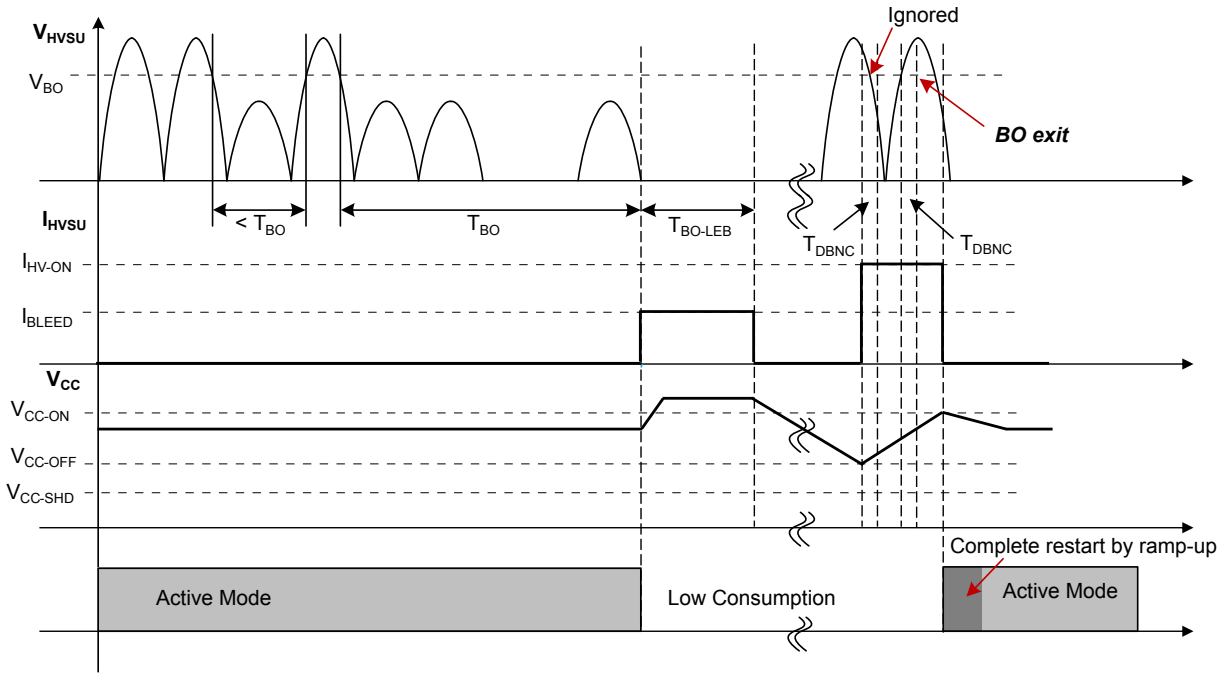
6.8.3 Brownout protection (BO)

In order to avoid operation at insufficient input voltage, the IC moves to low consumption mode if the input voltage is lower than the programmed threshold (Table 9) for at least T_{BO} (500 ms min.). During masking time (T_{BO-LEB}), activated after brownout triggering time, the HVSU comparator is ignored to prevent false restart due to EMI filter resonance oscillations, while I_{BLEED} is turned on to discharge any residual oscillation due to EMI filter operating condition at turn-off instant.

After the end of T_{BO_LEB}, the input voltage is checked to be higher than the threshold only during the charging period of V_{CC}: a small time (T_{DBNC}) is applied after HVSU activation to prevent false reading. To be noted that the value of the resistance that is in series with the HVSU pin, multiplied by I_{CHG-H}, sets the hysteresis for brownout threshold voltage.

During brownout, the internal THD optimizer drives the internal switched resistor always OFF (setting δc = 0 in Section 6.3.1) and the THD pin is set in high impedance.

Figure 17. Brownout protection



6.8.4 Undervoltage protection (UVP)

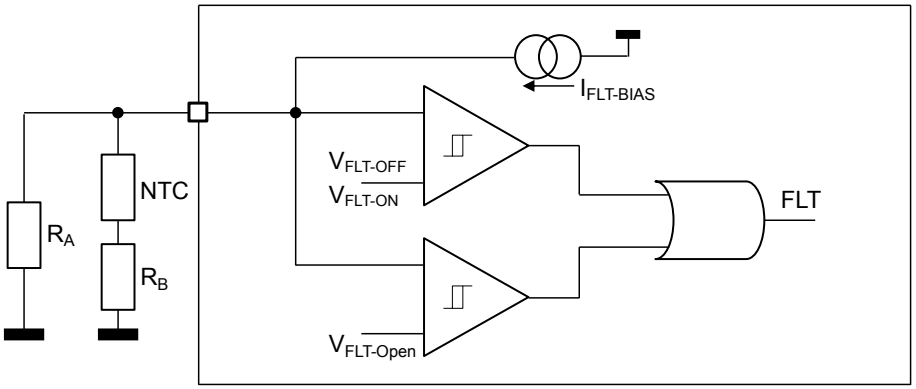
Primary side regulation sample and hold constantly monitors the output voltage. If it steadily falls below the V_{UVP} threshold for at least T_{UVP}, the IC is shut down and ART state is invoked to try a new operating attempt. Note that, during the VCC recycling, the ART timer is frozen during VCC recharging phase (from turn-off to turn-on thresholds); furthermore, as T_{ART} elapses, the HV current generator is activated immediately, without waiting that the VCC turn-off threshold is reached. At operation resuming attempt after ART state, the IC starts from the ramp-up phase.

6.8.5 General fault pin and NTC connection

The HVLED101 embeds one general purpose pin intended to disable the switching activity and move the IC into low consumption if the voltage at this pin falls below a threshold level or is left floating. Also in this case (like for UVP), as the protection is triggered, the ART state is invoked: after T_{ART} elapses, the IC waits for the FAULT condition reset before resuming operation (starting from ramp-up phase).

The FAULT pin is mainly used to manage an NTC thermistor: in fact, the lower threshold has a well-defined hysteresis, the pin sources a precise current to create the desired thermal hysteresis for final application.

Figure 18. **Fault pin block diagram**



The NTC can be linearized using a resistor network consisting of one resistor in series and one in parallel.

The design approach must firstly guarantee that FAULT voltage is greater than $V_{FLT-OPEN}$ if either the temperature is lower than minimum operating value or the NTC is disconnected. Then the value of fault voltage is equal to $V_{FLT-OFF}$ at maximum operating temperature.

The pin is also able to sense the absence of NTC, because the pin left open is internally pulled up above an upper threshold. If NTC is not used, a fixed resistor (22 kΩ to 47 kΩ) should be connected to GND.

During FAULT pin protection, the internal THD optimizer drives the internal switched resistor always OFF (setting δc = 0 in Section 6.3.1) and the THD pin is set in high impedance.

7 Package mechanical data

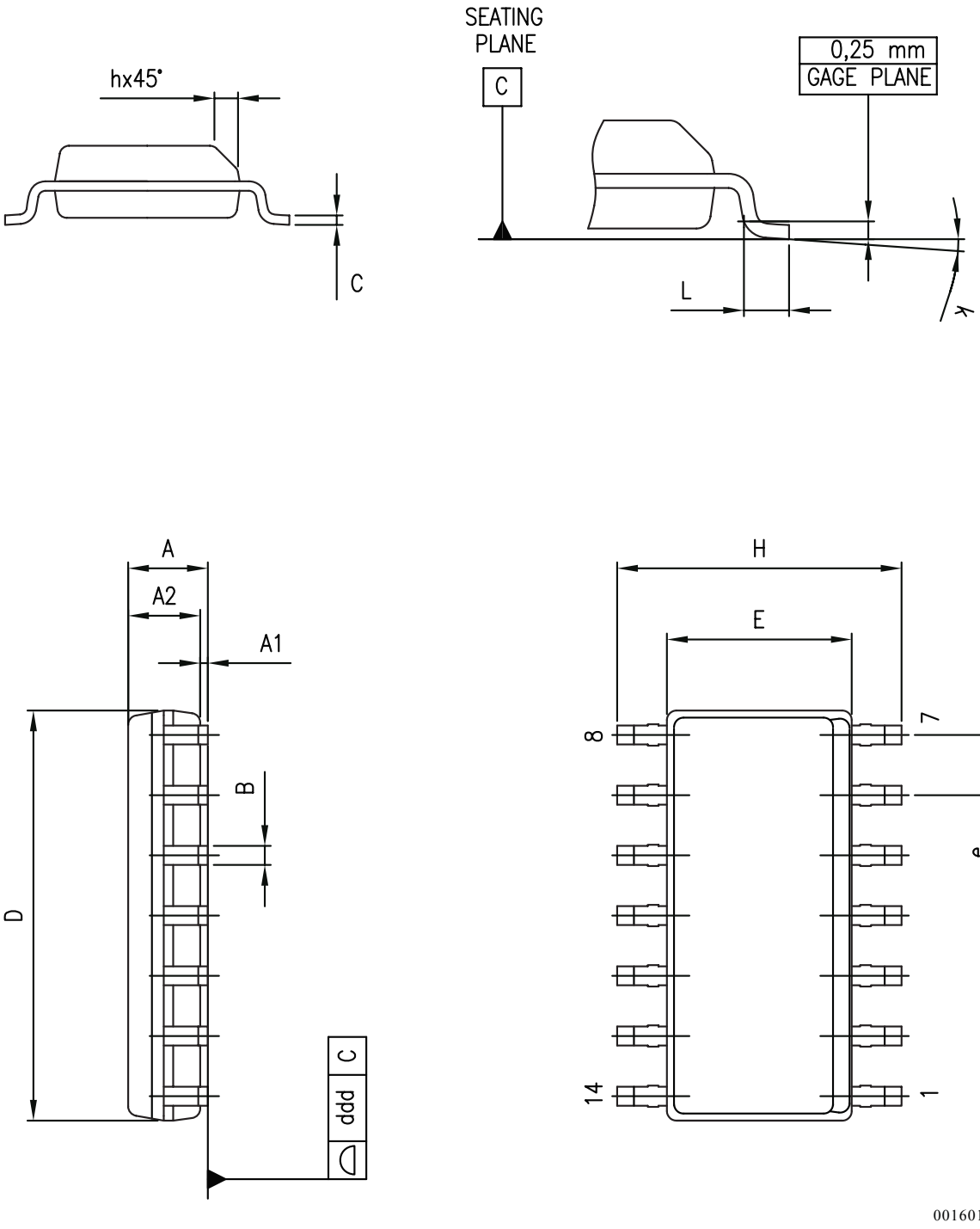
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com.

ECOPACK is an ST trademark.

Table 12. SOP14 mechanical data

Dimensions	mm		
	Min.	Typ.	Max.
A	1.350		1.750
A1	0.100		0.250
A2	1.100		1.650
B	0.330		0.510
C	0.190		0.250
D	8.550		8.750
E	3.800		4.000
e		1.270	
H	5.800		6.200
h	0.250		0.500
L	0.400		1.270
k	0d		8d
ddd			0.100

Figure 19. **Package dimensions**



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8 Ordering information

Table 13. **Ordering information**

Part number	Package	Packaging
HVLED101	SOP14	Tube
HVLED101TR		Tape and reel

Revision history

Table 14. **Document revision history**

Date	Version	Changes
19-Dec-2022	1	Initial release.
21-Dec-2022	2	Updated Table 5

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